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- (71) Applicant: **ATOMERA INCORPORATED** [US/US];  
750 University Avenue, Suite 280, Los Gatos, California  
95032 (US).
- (72) Inventors: **CODY, Nyles Wynn**; 1395 W. Maria Lane,  
Tempe, Arizona 85284 (US). **WEEKS, Keith Doran**;  
2594 West Raintree Way, Chandler, Arizona 85224 (US).  
**VYNE, Robert Michael**; 11415 E Bellflower Ct., Chan-  
dler, Arizona 85249 (US). **STEPHENSON, Robert John**;  
34 Moorfield Road, Duxford Cambridgeshire CB22 4PS  
(GB).

(74) Agent: **REGAN, Christopher F.** et al.; Allen, Dyer, Doppelt + Gilchrist, P.A., 1135 East State Road 434, Suite 3001, Winter Springs, Florida 32708 (US).

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(54) Title: METHOD FOR MAKING A RADIO FREQUENCY SILICON-ON-INSULATOR (RFSOI) WAFER INCLUDING A SUPERLATTICE

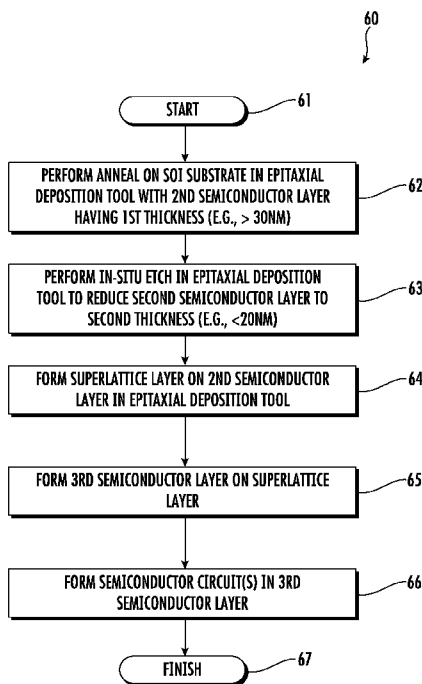


FIG. 5

(57) Abstract: A method for making a semiconductor device may include, in an epitaxial deposition tool, performing an anneal on a semiconductor on insulator (SOI) substrate including a first semiconductor layer, an insulating layer on the first semiconductor layer, and a second semiconductor layer on the insulating layer, the second semiconductor layer having a first thickness. The method may also include, in the epitaxial deposition tool, performing an in-situ etch to reduce the second semiconductor layer to a second thickness less than the first thickness, and forming a superlattice layer on the second semiconductor layer. The superlattice layer may include a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.



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## METHOD FOR MAKING A RADIO FREQUENCY SILICON-ON-INSULATOR (RFSOI) WAFER INCLUDING A SUPERLATTICE

### Technical Field

**[0001]** The present disclosure generally relates to semiconductor devices, and, more particularly, to semiconductor-on-insulator (SOI) wafer and device fabrication.

### Background

**[0002]** Structures and techniques have been proposed to enhance the performance of semiconductor devices, such as by enhancing the mobility of the charge carriers. For example, U.S. Patent Application No. 2003/0057416 to Currie et al. discloses strained material layers of silicon, silicon-germanium, and relaxed silicon and also including impurity-free zones that would otherwise cause performance degradation. The resulting biaxial strain in the upper silicon layer alters the carrier mobilities enabling higher speed and/or lower power devices. Published U.S. Patent Application No. 2003/0034529 to Fitzgerald et al. discloses a CMOS inverter also based upon similar strained silicon technology.

**[0003]** U.S. Patent No. 6,472,685 B2 to Takagi discloses a semiconductor device including a silicon and carbon layer sandwiched between silicon layers so that the conduction band and valence band of the second silicon layer receive a tensile strain. Electrons having a smaller effective mass, and which have been induced by an electric field applied to the gate electrode, are confined in the second silicon layer, thus, an n-channel MOSFET is asserted to have a higher mobility.

**[0004]** U.S. Patent No. 4,937,204 to Ishibashi et al. discloses a superlattice in which a plurality of layers, less than eight monolayers, and containing a fractional or binary or a binary compound semiconductor layer, are alternately and epitaxially grown. The direction of main current flow is perpendicular to the layers of the superlattice.

**[0005]** U.S. Patent No. 5,357,119 to Wang et al. discloses a Si-Ge short period superlattice with higher mobility achieved by reducing alloy scattering in the superlattice. Along these lines, U.S. Patent No. 5,683,934 to Candelaria discloses an

enhanced mobility MOSFET including a channel layer comprising an alloy of silicon and a second material substitutionally present in the silicon lattice at a percentage that places the channel layer under tensile stress.

**[0006]** U.S. Patent No. 5,216,262 to Tsu discloses a quantum well structure comprising two barrier regions and a thin epitaxially grown semiconductor layer sandwiched between the barriers. Each barrier region consists of alternate layers of SiO<sub>2</sub>/Si with a thickness generally in a range of two to six monolayers. A much thicker section of silicon is sandwiched between the barriers.

**[0007]** An article entitled "Phenomena in silicon nanostructure devices" also to Tsu and published online September 6, 2000 by Applied Physics and Materials Science & Processing, pp. 391-402 discloses a semiconductor-atomic superlattice (SAS) of silicon and oxygen. The Si/O superlattice is disclosed as useful in a silicon quantum and light-emitting devices. In particular, a green electroluminescence diode structure was constructed and tested. Current flow in the diode structure is vertical, that is, perpendicular to the layers of the SAS. The disclosed SAS may include semiconductor layers separated by adsorbed species such as oxygen atoms, and CO molecules. The silicon growth beyond the adsorbed monolayer of oxygen is described as epitaxial with a fairly low defect density. One SAS structure included a 1.1 nm thick silicon portion that is about eight atomic layers of silicon, and another structure had twice this thickness of silicon. An article to Luo et al. entitled "Chemical Design of Direct-Gap Light-Emitting Silicon" published in Physical Review Letters, Vol. 89, No. 7 (August 12, 2002) further discusses the light emitting SAS structures of Tsu.

**[0008]** U.S. Pat. No. 7,105,895 to Wang et al. discloses a barrier building block of thin silicon and oxygen, carbon, nitrogen, phosphorous, antimony, arsenic or hydrogen to thereby reduce current flowing vertically through the lattice more than four orders of magnitude. The insulating layer/barrier layer allows for low defect epitaxial silicon to be deposited next to the insulating layer.

**[0009]** Published Great Britain Patent Application 2,347,520 to Mears et al. discloses that principles of Aperiodic Photonic Band-Gap (APBG) structures may be adapted for electronic bandgap engineering. In particular, the application discloses that material parameters, for example, the location of band minima, effective mass, etc., can be tailored to yield new aperiodic materials with desirable band-structure

characteristics. Other parameters, such as electrical conductivity, thermal conductivity and dielectric permittivity or magnetic permeability are disclosed as also possible to be designed into the material.

**[0010]** Furthermore, U.S. Pat. No. 6,376,337 to Wang et al. discloses a method for producing an insulating or barrier layer for semiconductor devices which includes depositing a layer of silicon and at least one additional element on the silicon substrate whereby the deposited layer is substantially free of defects such that epitaxial silicon substantially free of defects can be deposited on the deposited layer. Alternatively, a monolayer of one or more elements, preferably comprising oxygen, is absorbed on a silicon substrate. A plurality of insulating layers sandwiched between epitaxial silicon forms a barrier composite.

**[0011]** Despite the existence of such approaches, further enhancements may be desirable for using advanced semiconductor materials and processing techniques to achieve improved performance in semiconductor devices.

### **Summary**

**[0012]** A method for making a semiconductor device may include, in an epitaxial deposition tool, performing an anneal on a semiconductor on insulator (SOI) substrate including a first semiconductor layer, an insulating layer on the first semiconductor layer, and a second semiconductor layer on the insulating layer, with the second semiconductor layer having a first thickness. The method may also include, in the epitaxial deposition tool, performing an in-situ etch to reduce the second semiconductor layer to a second thickness less than the first thickness, and forming a superlattice layer on the second semiconductor layer. The superlattice layer may include a plurality of stacked groups of layers, with each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.

**[0013]** In an example implementation, the first thickness may be in a range of 30nm to 90nm, and the second thickness may be in a range of 10nm to 20nm. Performing the anneal may comprise annealing the SOI substrate at a temperature greater than 1000°C, and in a hydrogen environment, for example.

**[0014]** Also by way of example, the in-situ etch may comprise performing an

in-situ HCl etch with an HCl gas flow in a range of 100-1000 sccm. In an example implementation, the in-situ etch may be performed at a temperature in a range of 900-1200°C, and at an etch rate in a range of 5-200nm per minute.

**[0015]** In some embodiments, the method may also include epitaxially forming a third semiconductor layer on the superlattice layer, and forming at least one semiconductor circuit in the third semiconductor layer. By way of example, the base semiconductor monolayers may comprise silicon, and the non-semiconductor monolayers may comprise oxygen.

### **Brief Description of the Drawings**

**[0016]** FIG. 1 is a greatly enlarged schematic cross-sectional view of a superlattice for use in a semiconductor device in accordance with an example embodiment.

**[0017]** FIG. 2 is a perspective schematic atomic diagram of a portion of the superlattice shown in FIG. 1.

**[0018]** FIG. 3 is a greatly enlarged schematic cross-sectional view of another embodiment of a superlattice in accordance with an example embodiment.

**[0019]** FIGS. 4A and 4B are a series of schematic cross-sectional diagrams illustrating a conventional approach to SOI wafer formation.

**[0020]** FIG. 5 is a flow diagram illustrating a method for making a semiconductor device including a superlattice in accordance with an example embodiment.

**[0021]** FIGS. 6A and 6B are a series of graphs illustrating RMS roughness vs. temperature for different surface area size ranges associated with example in-situ etch parameters for the method of FIG. 5.

**[0022]** FIG. 7 is a graph of etch rate vs. HCl flow for example in-situ etch parameters for the method of FIG. 5.

**[0023]** FIG. 8 is a graph of etch thickness vs. position for different example HCl gas flow rates which may be used with the method of FIG. 5.

**[0024]** FIG. 9 is a graph of etch thickness vs. position illustrating an example etch step using a susceptor coat in accordance with the method of FIG. 5.

**[0025]** FIG. 10 is a graph of thickness vs. position for an example semiconductor device including a superlattice layer formed using the method of FIG. 5.

### **Detailed Description**

**[0026]** Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings, in which the example embodiments are shown. The embodiments may, however, be implemented in many different forms and should not be construed as limited to the specific examples set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete. Like numbers refer to like elements throughout.

**[0027]** Generally speaking, the present disclosure relates to semiconductor devices having an enhanced semiconductor superlattice therein to provide performance enhancement characteristics. The enhanced semiconductor superlattice may also be referred to as an “MST” layer or “MST technology” in this disclosure.

**[0028]** More particularly, the MST technology relates to advanced semiconductor materials such as the superlattice 25 described further below. In prior work, Applicant theorized that certain superlattices as described herein reduce the effective mass of charge carriers and that this thereby leads to higher charge carrier mobility. See, e.g., U.S. Pat. No. 6,897,472, which is hereby incorporated herein in its entirety by reference.

**[0029]** Further development by Applicant has established that the presence of MST layers may advantageously improve the mobility of free carriers in semiconductor materials, e.g., at interfaces between silicon and insulators like SiO<sub>2</sub> or HfO<sub>2</sub>. Applicant theorizes, without wishing to be bound thereto, that this may occur due to various mechanisms. One mechanism is by reducing the concentration of charged impurities proximate to the interface, by reducing the diffusion of these impurities, and/or by trapping the impurities so they do not reach the interface proximity. Charged impurities cause Coulomb scattering, which reduces mobility. Another mechanism is by improving the quality of the interface. For example, oxygen emitted from an MST film may provide oxygen to a Si-SiO<sub>2</sub> interface, reducing the presence of sub-stoichiometric SiO<sub>x</sub>. Alternately, the trapping of

interstitials by MST layers may reduce the concentration of interstitial silicon proximate to the Si-SiO<sub>2</sub> interface, reducing the tendency to form sub-stoichiometric SiO<sub>x</sub>. Sub-stoichiometric SiO<sub>x</sub> at the Si-SiO<sub>2</sub> interface is known to exhibit inferior insulating properties relative to stoichiometric SiO<sub>2</sub>. Reducing the amount of sub-stoichiometric SiO<sub>x</sub> at the interface more effectively confines free carriers (electrons or holes) in the silicon, and thus improves the mobility of these carriers due to electric fields applied parallel to the interface, as is standard practice in field-effect-transistor (“FET”) structures. Scattering due to the direct influence of the interface is called “surface-roughness scattering”, which may advantageously be reduced by the proximity of MST layers followed by anneals or during thermal oxidation.

**[0030]** In addition to the enhanced mobility characteristics of MST structures, they may also be formed or used in such a manner that they provide piezoelectric, pyroelectric, and/or ferroelectric properties that are advantageous for use in a variety of different types of devices, as will be discussed further below.

**[0031]** Referring now to FIGS. 1 and 2, the materials or structures are in the form of a superlattice 25 whose structure is controlled at the atomic or molecular level and may be formed using known techniques of atomic or molecular layer deposition. The superlattice 25 includes a plurality of layer groups 45a-45n arranged in stacked relation, as perhaps best understood with specific reference to the schematic cross-sectional view of FIG. 1.

**[0032]** Each group of layers 45a-45n of the superlattice 25 illustratively includes a plurality of stacked base semiconductor monolayers 46 defining a respective base semiconductor portion 46a-46n and a non-semiconductor monolayer(s) 50 thereon. The non-semiconductor monolayers 50 are indicated by stippling in FIG. 1 for clarity of illustration.

**[0033]** The non-semiconductor monolayer 50 illustratively includes one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions. By “constrained within a crystal lattice of adjacent base semiconductor portions” it is meant that at least some semiconductor atoms from opposing base semiconductor portions 46a-46n are chemically bound together through the non-semiconductor monolayer 50 therebetween, as seen in FIG. 2. Generally speaking, this configuration is made possible by controlling the amount of non-semiconductor material that is deposited on semiconductor portions 46a-46n

through atomic layer deposition techniques so that not all (i.e., less than full or 100% coverage) of the available semiconductor bonding sites are populated with bonds to non-semiconductor atoms, as will be discussed further below. Thus, as further monolayers 46 of semiconductor material are deposited on or over a non-semiconductor monolayer 50, the newly deposited semiconductor atoms will populate the remaining vacant bonding sites of the semiconductor atoms below the non-semiconductor monolayer.

**[0034]** In other embodiments, more than one such non-semiconductor monolayer may be possible. It should be noted that reference herein to a non-semiconductor or semiconductor monolayer means that the material used for the monolayer would be a non-semiconductor or semiconductor if formed in bulk. That is, a single monolayer of a material, such as silicon, may not necessarily exhibit the same properties that it would if formed in bulk or in a relatively thick layer, as will be appreciated by those skilled in the art.

**[0035]** Applicant theorizes without wishing to be bound thereto that non-semiconductor monolayers 50 and adjacent base semiconductor portions 46a-46n cause the superlattice 25 to have a lower appropriate conductivity effective mass for the charge carriers in the parallel layer direction than would otherwise be present. Considered another way, this parallel direction is orthogonal to the stacking direction. The band modifying layers 50 may also cause the superlattice 25 to have a common energy band structure, while also advantageously functioning as an insulator between layers or regions vertically above and below the superlattice.

**[0036]** Moreover, this superlattice structure may also advantageously act as a barrier to dopant and/or material diffusion between layers vertically above and below the superlattice 25. These properties may thus advantageously allow the superlattice 25 to provide an interface for high-K dielectrics which not only reduces diffusion of the high-K material into the channel region, but which may also advantageously reduce unwanted scattering effects and improve device mobility, as will be appreciated by those skilled in the art.

**[0037]** It is also theorized that semiconductor devices including the superlattice 25 may enjoy a higher charge carrier mobility based upon the lower conductivity effective mass than would otherwise be present. In some embodiments, and as a result of the band engineering achieved by the present invention, the

superlattice 25 may further have a substantially direct energy bandgap that may be particularly advantageous for opto-electronic devices, for example.

**[0038]** The superlattice 25 also illustratively includes a cap layer 52 on an upper layer group 45n. The cap layer 52 may comprise a plurality of base semiconductor monolayers 46. The cap layer 52 may have between 2 to 100 monolayers of the base semiconductor, and, more preferably between 10 to 50 monolayers.

**[0039]** Each base semiconductor portion 46a-46n may comprise a base semiconductor selected from the group consisting of Group IV semiconductors, Group III-V semiconductors, and Group II-VI semiconductors. Of course, the term Group IV semiconductors also includes Group IV-IV semiconductors, as will be appreciated by those skilled in the art. More particularly, the base semiconductor may comprise at least one of silicon and germanium, for example.

**[0040]** Each non-semiconductor monolayer 50 may comprise a non-semiconductor selected from the group consisting of oxygen, nitrogen, fluorine, carbon and carbon-oxygen, for example. The non-semiconductor is also desirably thermally stable through deposition of a next layer to thereby facilitate manufacturing. In other embodiments, the non-semiconductor may be another inorganic or organic element or compound that is compatible with the given semiconductor processing as will be appreciated by those skilled in the art. More particularly, the base semiconductor may comprise at least one of silicon and germanium, for example.

**[0041]** It should be noted that the term monolayer is meant to include a single atomic layer and also a single molecular layer. It is also noted that the non-semiconductor monolayer 50 provided by a single monolayer is also meant to include a monolayer wherein not all of the possible sites are occupied (i.e., there is less than full or 100% coverage). For example, with particular reference to the atomic diagram of FIG. 2, a 4/1 repeating structure is illustrated for silicon as the base semiconductor material, and oxygen as the energy band-modifying material. Only half of the possible sites for oxygen are occupied in the illustrated example.

**[0042]** In other embodiments and/or with different materials this one-half occupation would not necessarily be the case as will be appreciated by those skilled in the art. Indeed it can be seen even in this schematic diagram, that individual

atoms of oxygen in a given monolayer are not precisely aligned along a flat plane as will also be appreciated by those of skill in the art of atomic deposition. By way of example, a preferred occupation range is from about one-eighth to one-half of the possible oxygen sites being full, although other numbers may be used in certain embodiments.

**[0043]** Silicon and oxygen are currently widely used in conventional semiconductor processing, and, hence, manufacturers will be readily able to use these materials as described herein. Atomic or monolayer deposition is also now widely used. Accordingly, semiconductor devices incorporating the superlattice 25 in accordance with the invention may be readily adopted and implemented, as will be appreciated by those skilled in the art.

**[0044]** Referring now additionally to FIG. 3, another embodiment of a superlattice 25' in accordance with the invention having different properties is now described. In this embodiment, a repeating pattern of 3/1/5/1 is illustrated. More particularly, the lowest base semiconductor portion 46a' has three monolayers, and the second lowest base semiconductor portion 46b' has five monolayers. This pattern repeats throughout the superlattice 25'. The non-semiconductor monolayers 50' may each include a single monolayer. For such a superlattice 25' including Si/O, the enhancement of charge carrier mobility is independent of orientation in the plane of the layers. Those other elements of FIG. 3 not specifically mentioned are similar to those discussed above with reference to FIG. 1 and need no further discussion herein.

**[0045]** In some device embodiments, all of the base semiconductor portions of a superlattice may be a same number of monolayers thick. In other embodiments, at least some of the base semiconductor portions may be a different number of monolayers thick. In still other embodiments, all of the base semiconductor portions may be a different number of monolayers thick.

**[0046]** Turning now to FIGS. 4A and 4B, by way of background, typical processes for SOI wafer 30 formation involve thinning the silicon layer 103 on the buried oxide (BOX) layer 102 (which is above a silicon substrate 101) using a single or multiple oxidation steps, followed by HF stripping. Several irregularities may occur in the silicon layer 103 during this process, including the formation of pin holes, etching of the oxide under the pin hole, and undercutting of the BOX layer 102.

These irregularities lead to defects that get incorporated into the subsequent MST film growth. Defects are generated at the edge of the wafer 100 due to the undercutting of the BOX layer 102 and are transported to the surface of the wafer during the HF wafer clean (See FIG. 4B).

**[0047]** Referring additionally to the flow diagram 60 of FIG. 5, an example approach for forming SOI wafers to provide for reduced defects in the fabrication of the above-described MST films is now described. More particularly, to overcome the above-described deficiencies of conventional SOI wafer formation, the present approach allows for annealing and thinning of SOI wafers in the same epitaxial deposition (epi) tool in which the MST film is grown to avoid the formation of pin holes and undercutting of the silicon on the BOX. This may allow for a cleaner process and customizable silicon thickness for different wafers, among other technical advantages.

**[0048]** To maximize the benefits of the MST films for RFSOI devices, it may be desirable to position the MST film around 10-20nm above the BOX layer. However, the above-described limitations of conventional BOX formation generally prevent SOI wafers with a silicon layer this thin on the BOX layer. Beginning at Block 61, and referring to the wafer 100 of FIG. 4A, starting with a silicon thickness of the layer 103 greater than 30nm allows for a high temperature bake or anneal (e.g., greater than 1000°C) in a hydrogen environment to remove the native oxide from the silicon thickness, at Block 62. The method further illustratively includes an in-situ etch (e.g., an HCl etch) in the epi tool to thin the silicon layer to a second thickness (Block 63), followed by MST film deposition, at Block 64. Using this approach, RFSOI substrates with silicon layer 103 thicknesses in the 10-20nm (or otherwise) and desired uniformity may advantageously be achieved. In some embodiments, the completed wafer may be the end product, or further processing may form a third (active) semiconductor layer (e.g., the cap layer 52) on the superlattice 25 (Block 65), and circuitry (e.g., RF circuitry) in the third semiconductor layer (Block 66), as will be appreciated by those skilled in the art. The method of FIG. 5 illustratively concludes at Block 67.

**[0049]** Typical HCl etching of silicon is done at an elevated temperature, e.g., 900 – 1200°C, and using atmospheric conditions. For the present approach, the etch rate may be tuned to controllably target a given silicon thickness, typically on the

order of 10 – 20nm. The starting silicon thickness available on typical SOI wafers is at a minimum of 30nm and up to a few microns in thickness. For this approach, the starting thickness will be 30 – 90nm, and a relatively slow etch rate may be used (e.g., on the order of 5 – 50nm per minute). Additionally, the etching of the silicon preferably maintains a smooth surface so that subsequent devices/circuitry can be manufactured in the silicon. To maintain smooth surfaces, relatively high temperatures and a low HCl gas ratio in hydrogen are used.

**[0050]** More particularly, the foregoing will be further understood with reference to example implementations now described with reference to FIGS. 6A, 6B, and 7-10. Several tests of the above-described silicon smoothing/etching process were performed using an ATM process for different bake temperatures of 900 – 1050°C, and using a relatively low percentage of HCl < 5% in hydrogen. The results are summarized in Table 1 below. Generally speaking, higher temperatures result in a higher etch rate. The test started with two minutes at 900°C and one minute at 1000°C, and the temperature was varied as shown. A ratio of H<sub>2</sub> to HCL was set at 40:1, and the initial tests were run on P- wafers for surface quality evaluation. By way of reference, defect etch is an ATM process at 750°C with fifteen liters HCL and five liters H<sub>2</sub>. Moreover, chamber clean is an ATM process at 1150°C with eighteen liters of HCl and 25-60 liters of H<sub>2</sub>. The results shown in Table 1 demonstrate that higher temperatures give lower haze, and generally lower particle levels (though some fluctuations in particle levels occurred).

Etch Temp	Time	Defects	Haze
900	120	1518	6.41
925	105	6340	0.867
950	90	275	0.5
975	75	194	0.36
1000	60	904	0.268
Reference Wafer		15	0.235

Table 1

**[0051]** Effects of surface roughness vs. etch temperature are shown in plots 70 and 71 of FIGS. 6A-6B for 1x1µm and 10x10µm scan sizes, respectively. The AFM roughness of the 1 liter HCl etch on P- wafers (10µm) was measured, and

~1000°C AFM was found to be better than the rest (1um).

**[0052]** Etch conditions were at a temperature of 1000°C, atmospheric etch, with 40 liters of H<sub>2</sub> and then HCl flows from 100 – 1000 sccm. These conditions provided a thinned silicon surface equal to that of the starting silicon, and a silicon etch rate from about 5 to 200nm/minute. A graph 75 of example silicon etch rates at 1000°C is provided in FIG. 7. However, it should be noted that other conditions may be used in different embodiments.

**[0053]** In the graph 80 of FIG. 8, the results of different etch rates of uniform SOI wafers are shown. The plot line 81 corresponds to a high flow rate of 0.5 liter HCl flow (sccm), and the plot line 82 corresponds to a low flow rate of 0.1 liter HCl flow (sccm), which respectively resulted in 320 angstroms/minute and 40 angstroms/minute etch rates.

**[0054]** In some embodiments, a susceptor coat may be utilized, which allows for more uniform etching of the SOI wafer without removing excessive silicon from the edges of the wafer. The graph 90 of FIG. 9 illustrates a test in which a susceptor coat was used with the above-described etch process. The resulting uniformity is similar to that of the starting SOI wafer.

**[0055]** Once the desired thickness of silicon 103 on the BOX layer 102 is obtained, the MST layer 25 deposition process described above may be run. This puts the MST layer 25 close to the BOX layer 102 of the SOI wafer 100, as seen in the graph 95 of FIG. 10. As noted above, a selectable thickness of silicon (e.g., cap layer 52) may be grown on top of the MST layer 25. The entire process is completed in one epitaxy tool, and the SOI wafer may then be unloaded as an RFSOI-ready wafer already including the MST film. However, in some embodiments further processing may also be performed within the same tool to define additional circuitry on the wafer, if desired.

**[0056]** With respect to technical advantages, thinning of the SOI wafer in the epi tool followed by the growth of the MST layers may result in fewer defects. The thinning of silicon does not undercut the BOX layer, and by using a high temperature bake on the wafer rather than a wet clean, this may result in a cleaner wafer surface. The thinning may also be customized to individual device specifications for respective applications, followed with the deposition of the MST film and cap.

**[0057]** It should be noted that the process examples described above were

run in an epi tool at atmospheric conditions, but the present approach may be implemented in other epi tools at other pressure ranges, e.g., sub-atmospheric conditions in a range of 400-700 Torr or otherwise.

**[0058]** Many modifications and other embodiments of the invention will come to the mind of one skilled in the art having the benefit of the teachings presented in the foregoing descriptions and the associated drawings. Therefore, it is understood that the invention is not to be limited to the specific embodiments disclosed, and that modifications and embodiments are intended to be included within the scope of the appended claims.

## Claims

1. A method for making a semiconductor device comprising:  
in an epitaxial deposition tool,  
performing an anneal on a semiconductor on insulator (SOI) substrate comprising a first semiconductor layer, an insulating layer on the first semiconductor layer, and a second semiconductor layer on the insulating layer, the second semiconductor layer having a first thickness,  
performing an in-situ etch to reduce the second semiconductor layer to a second thickness less than the first thickness, and  
forming a superlattice layer on the second semiconductor layer, the superlattice layer comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base semiconductor monolayers defining a base semiconductor portion, and at least one non-semiconductor monolayer constrained within a crystal lattice of adjacent base semiconductor portions.
2. The method of claim 1 wherein the first thickness is in a range of 30nm to 90nm.
3. The method of claim 1 wherein the second thickness is in a range of 10nm to 20nm.
4. The method of claim 1 wherein performing the anneal comprises annealing the SOI substrate at a temperature greater than 1000°C.
5. The method of claim 1 wherein performing the anneal comprises annealing the SOI substrate in a hydrogen environment.
6. The method of claim 1 wherein performing the in-situ etch comprises performing an in-situ HCl etch.

7. The method of claim 6 wherein performing the in-situ HCl etch comprises introducing an HCl gas flow in a range of 100-1000 sccm.
8. The method of claim 1 wherein performing the in-situ etch comprises performing the in-situ etch at a temperature in a range of 900-1200°C.
9. The method of claim 1 wherein performing the in-situ etch comprises performing the in-situ at an etch rate in a range of 5-200nm per minute.
10. The method of claim 1 further comprising epitaxially forming a third semiconductor layer on the superlattice layer, and forming at least one semiconductor circuit in the third semiconductor layer.
11. The method of claim 1 wherein the base semiconductor monolayers comprise silicon.
12. The method of claim 1 wherein the non-semiconductor monolayers comprise oxygen.
13. A method for making a semiconductor device comprising:
  - in an epitaxial deposition tool,
  - performing an anneal on a semiconductor on insulator (SOI) substrate comprising a first semiconductor layer, an insulating layer on the first semiconductor layer, and a second semiconductor layer on the insulating layer, the second semiconductor layer having a first thickness,
  - performing an in-situ etch to reduce the second semiconductor layer to a second thickness less than the first thickness,
  - forming a superlattice layer on the second semiconductor layer, the superlattice layer comprising a plurality of stacked groups of layers, each group of layers comprising a plurality of stacked base silicon monolayers defining a base silicon portion, and at least one oxygen monolayer constrained within a crystal lattice of adjacent base silicon portions, and

epitaxially forming a third semiconductor layer on the superlattice layer; and forming at least one semiconductor circuit in the third semiconductor layer.

14. The method of claim 13 wherein the first thickness is in a range of 30nm to 90nm.

15. The method of claim 13 wherein the second thickness is in a range of 10nm to 20nm.

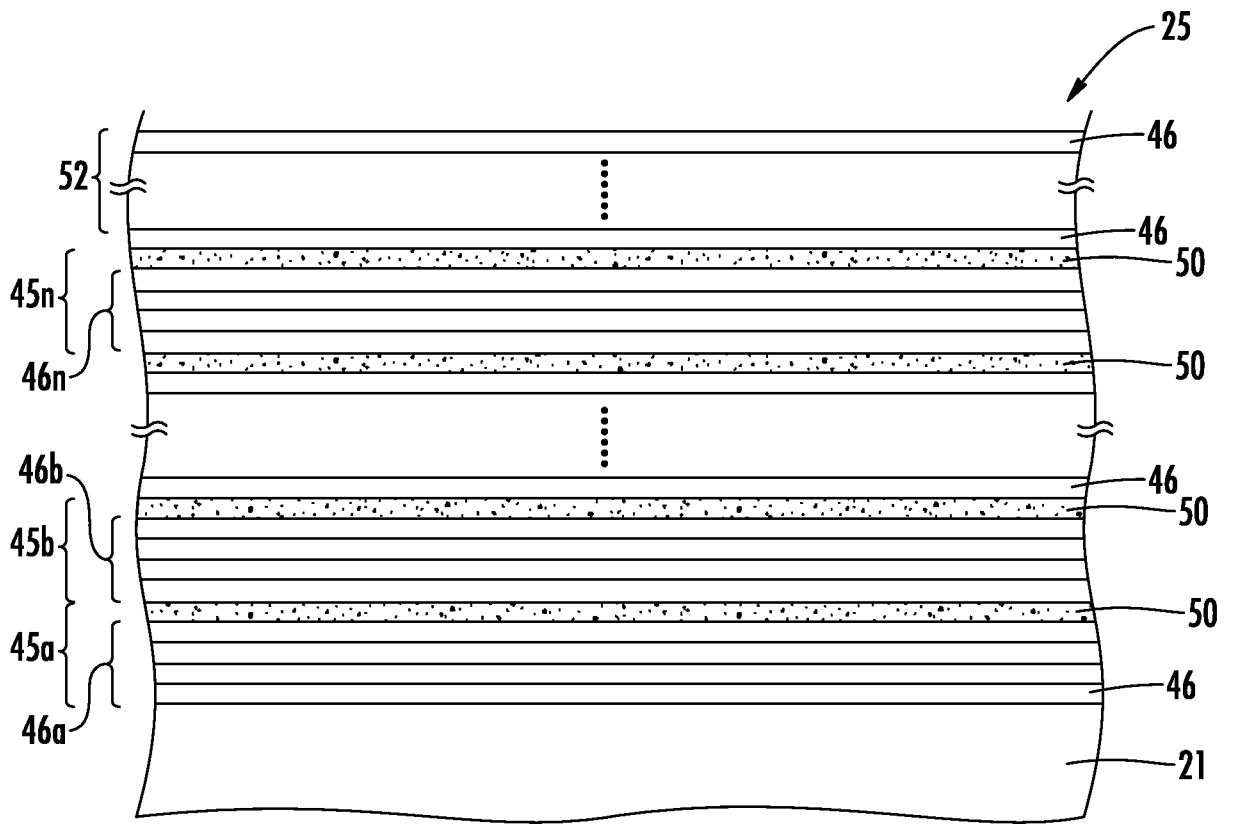
16. The method of claim 13 wherein performing the anneal comprises annealing the SOI substrate at a temperature greater than 1000°C in a hydrogen environment.

17. The method of claim 13 wherein performing the in-situ etch comprises performing an in-situ HCl etch.

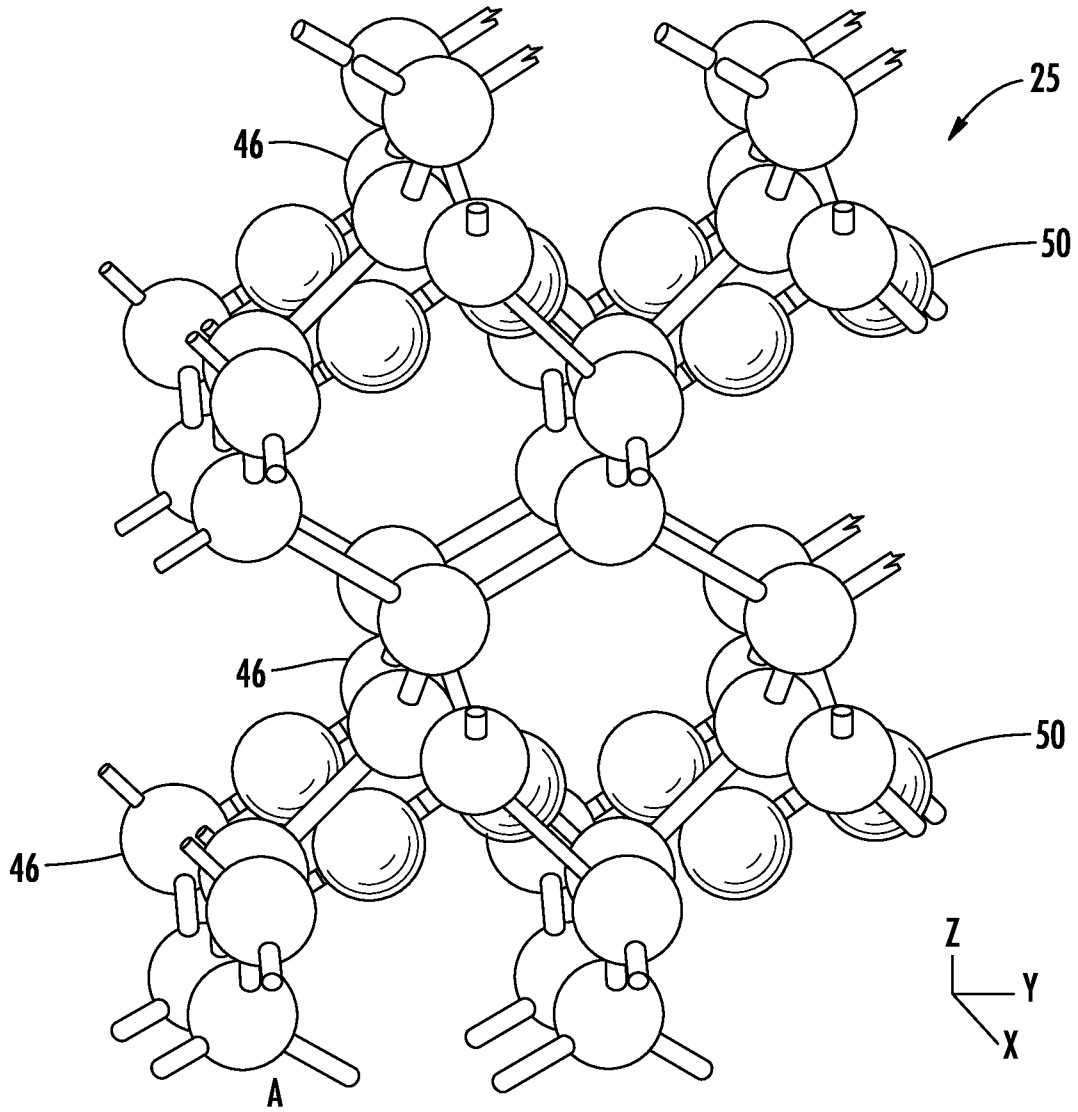
18. The method of claim 17 wherein performing the in-situ HCl etch comprises introducing an HCl gas flow in a range of 100-1000 sccm.

19. The method of claim 13 wherein performing the in-situ etch comprises performing the in-situ etch at a temperature in a range of 900-1200°C and at an etch rate in a range of 5-200nm per minute.

20. The method of claim 13 further comprising forming a susceptor coating on the first semiconductor layer prior to performing the in-situ etch.



**FIG. 1**



**FIG. 2**

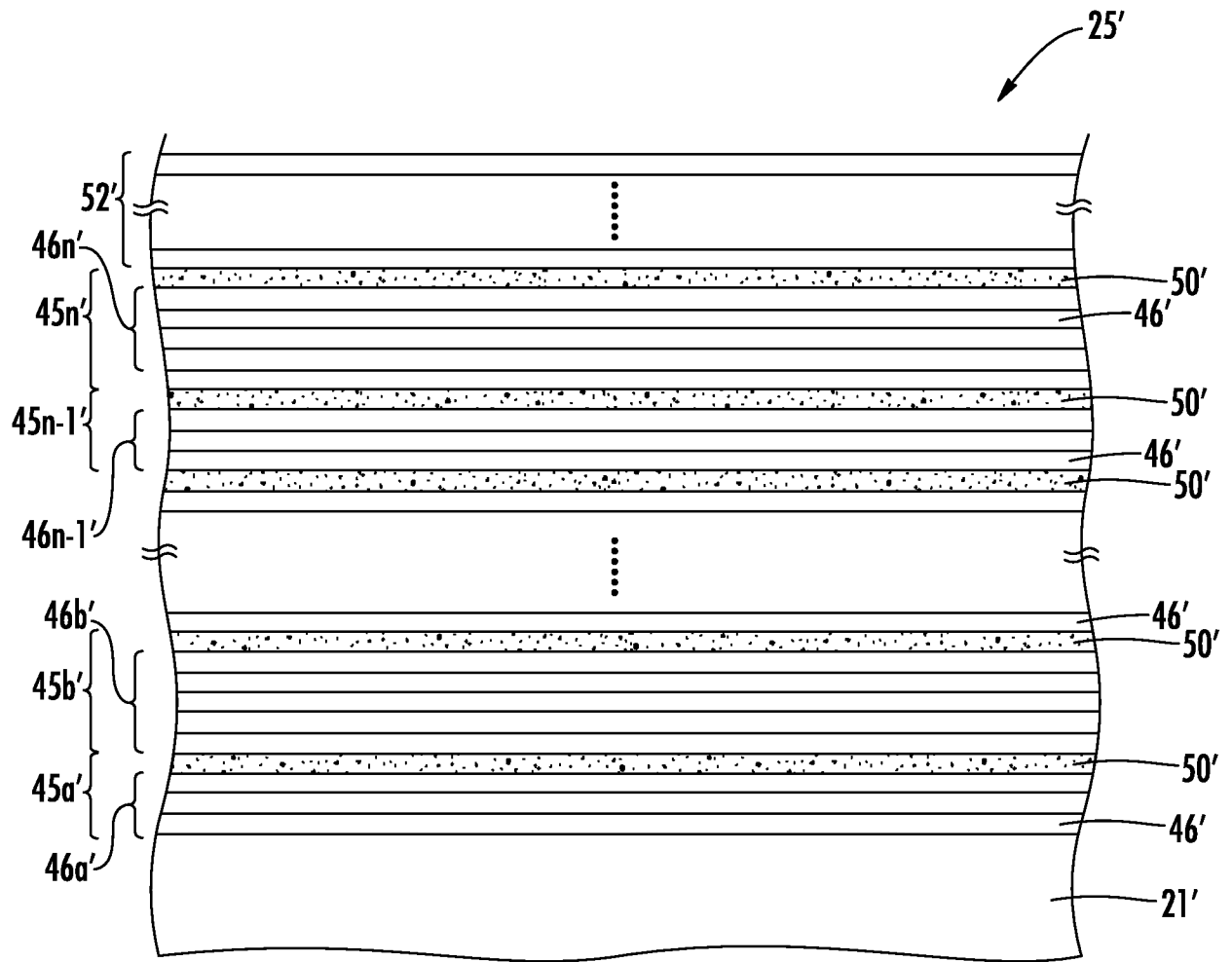
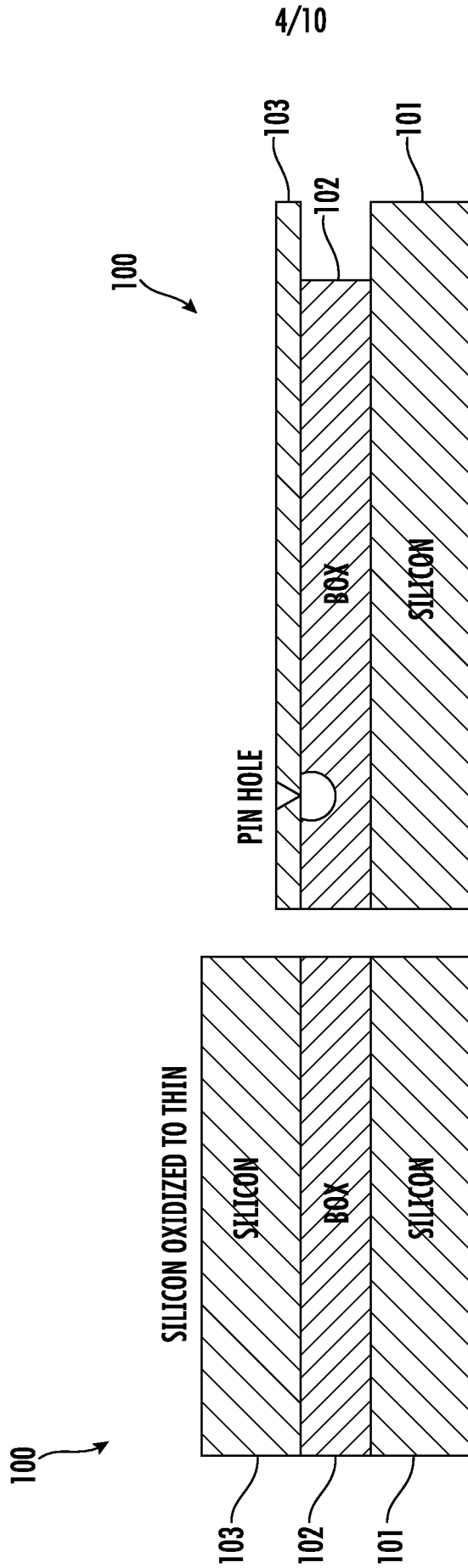


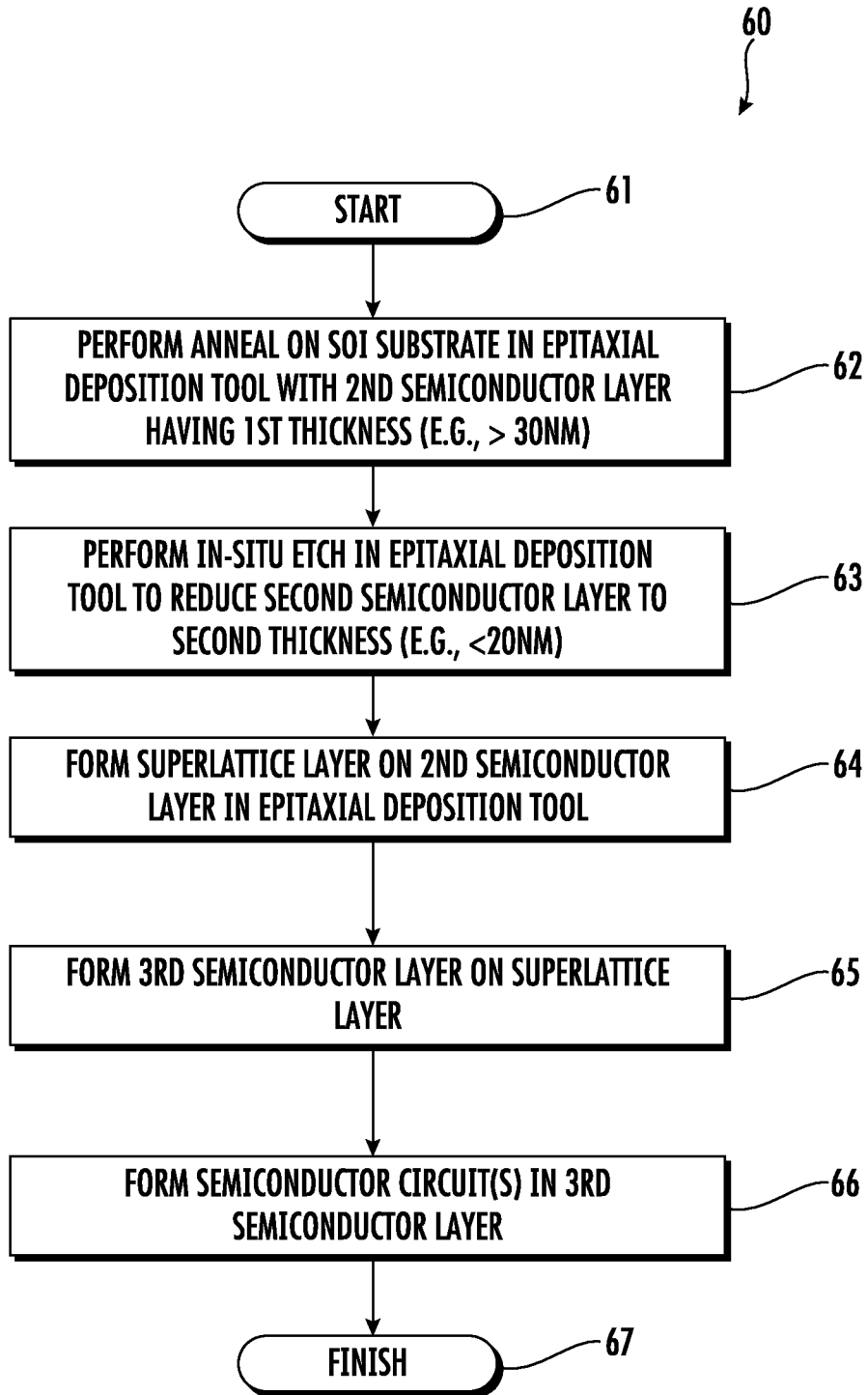
FIG. 3



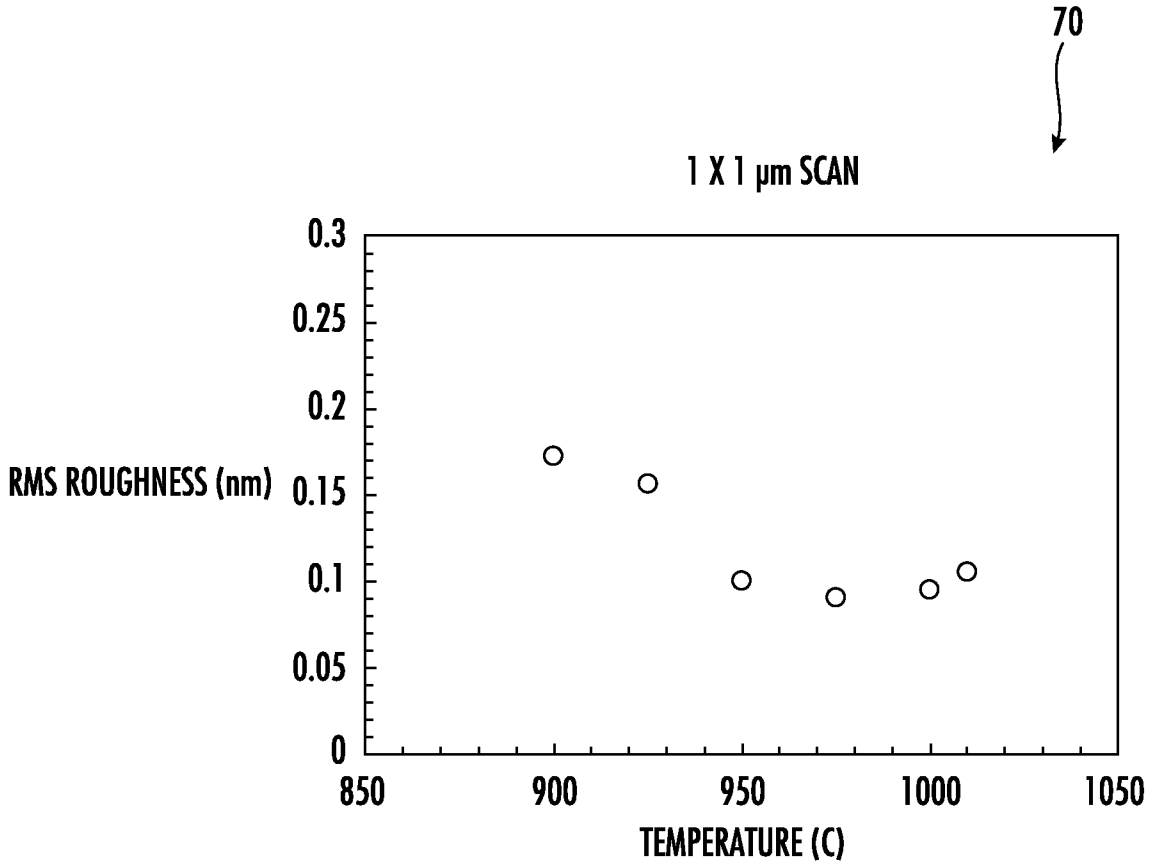
**FIG. 4B**  
**(PRIOR ART)**

**FIG. 4A**  
**(PRIOR ART)**

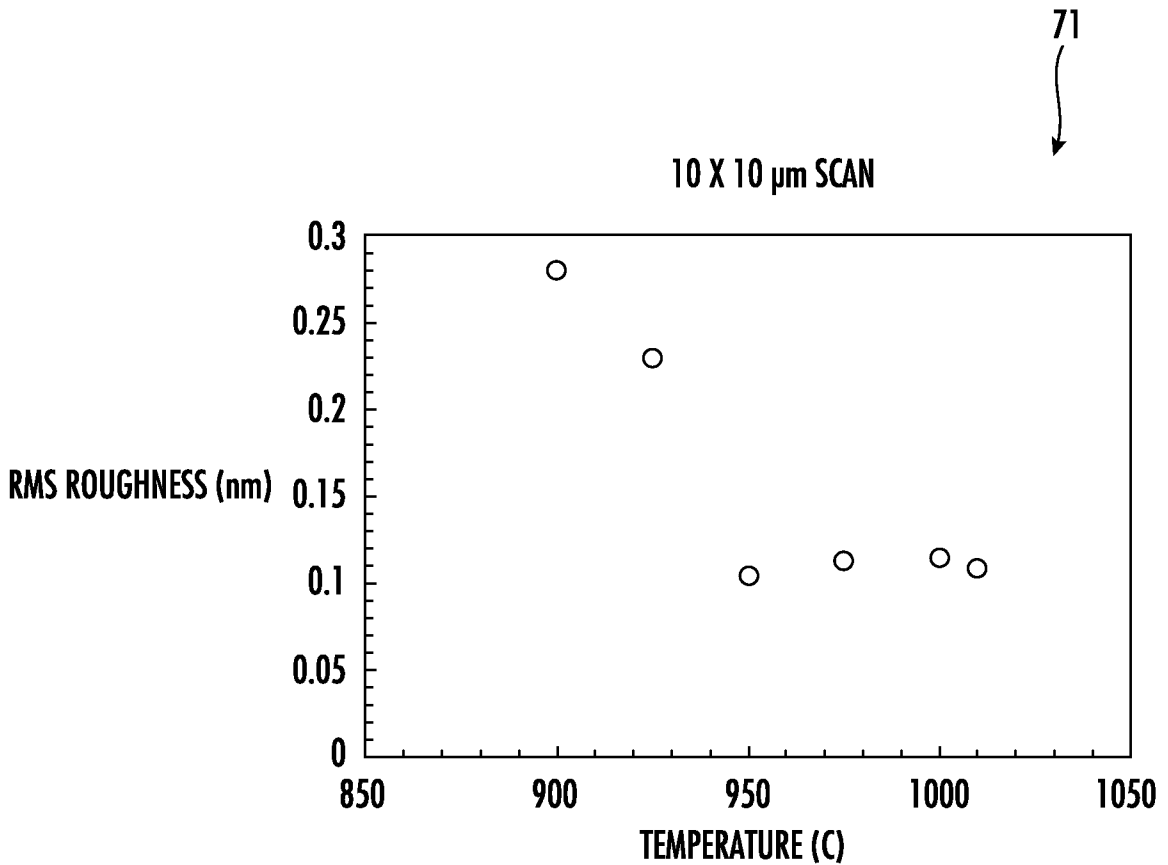
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**FIG. 5**



**FIG. 6A**



**FIG. 6B**

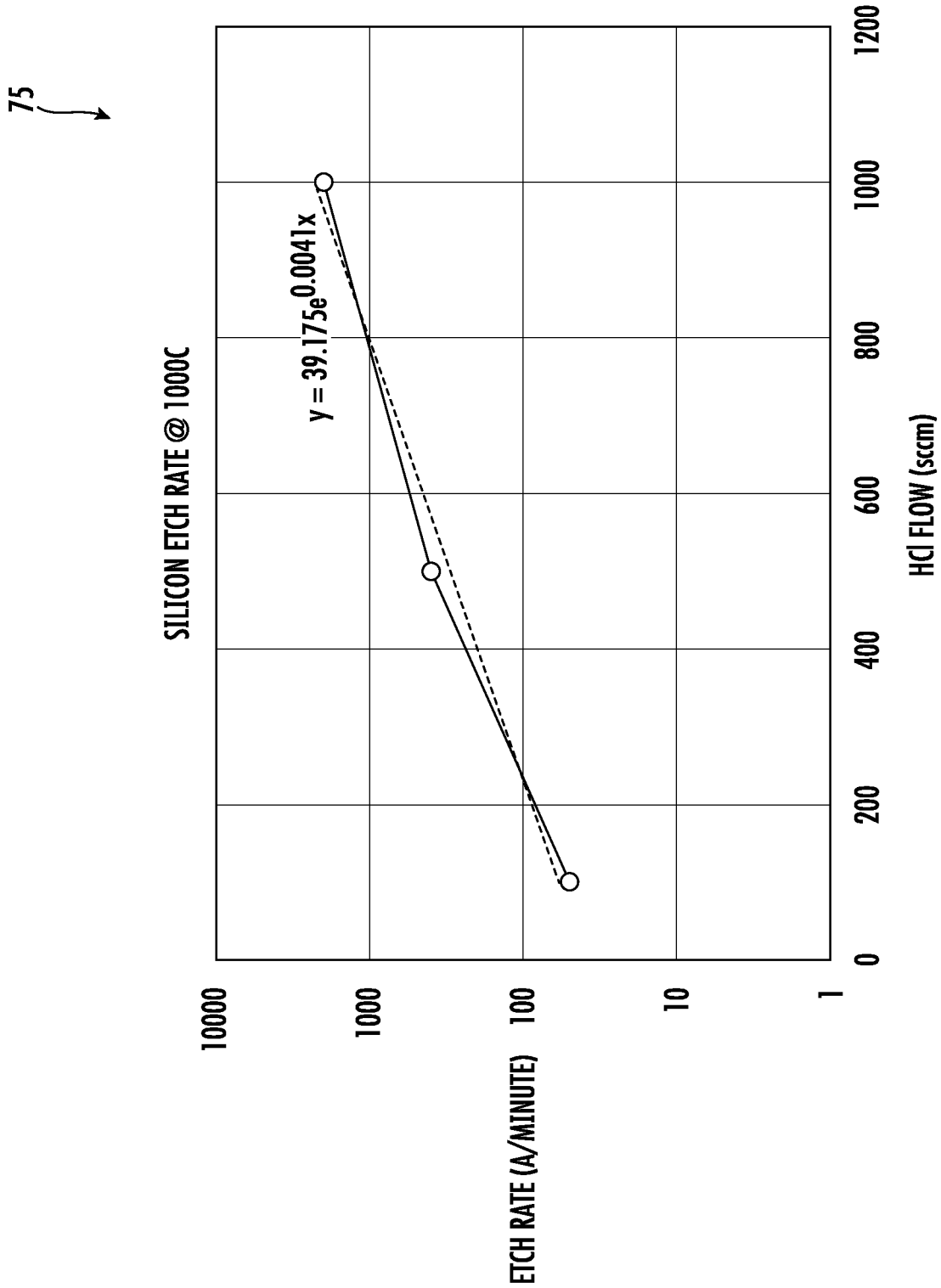


FIG. 7

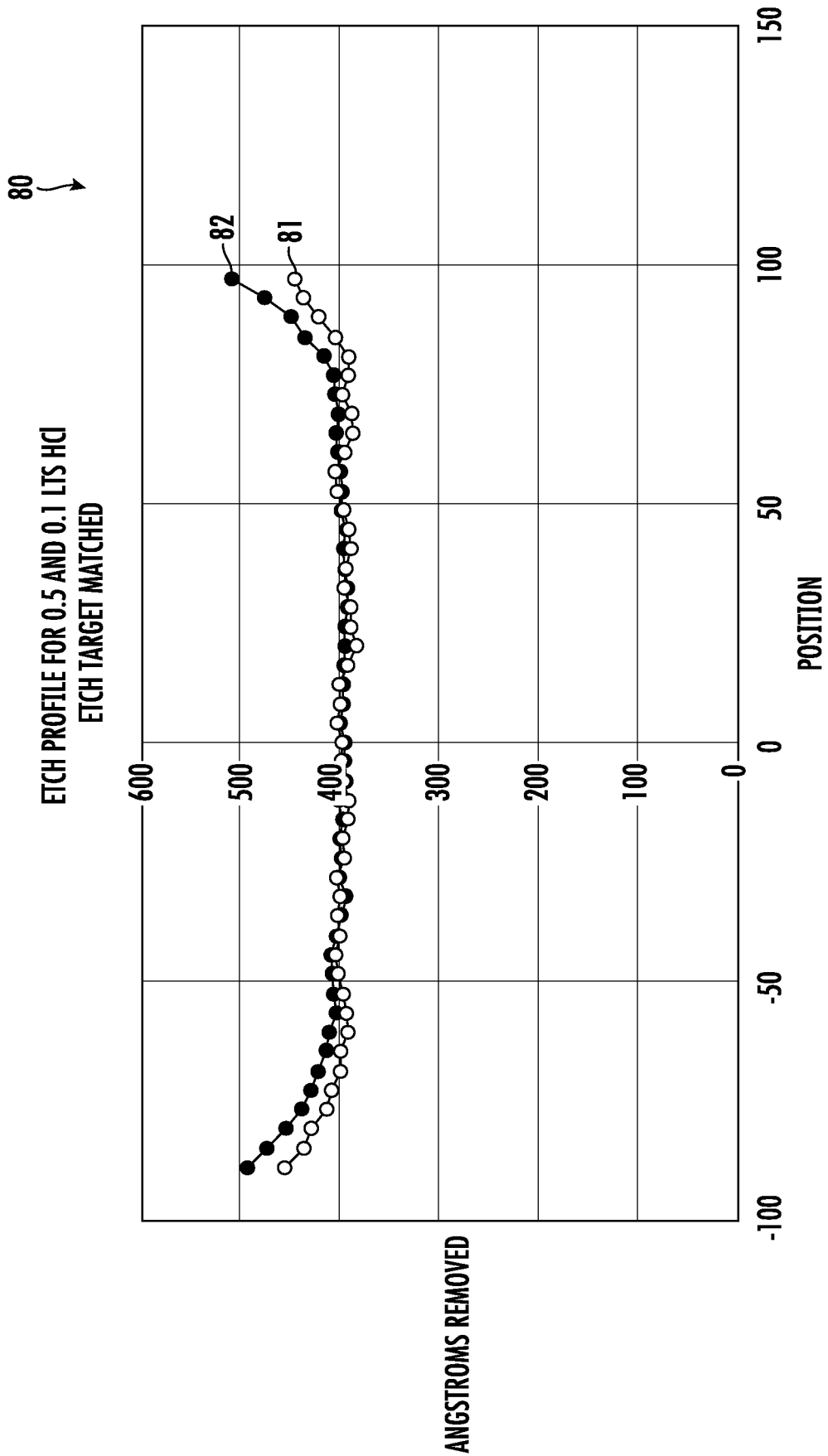


FIG. 8

9/10

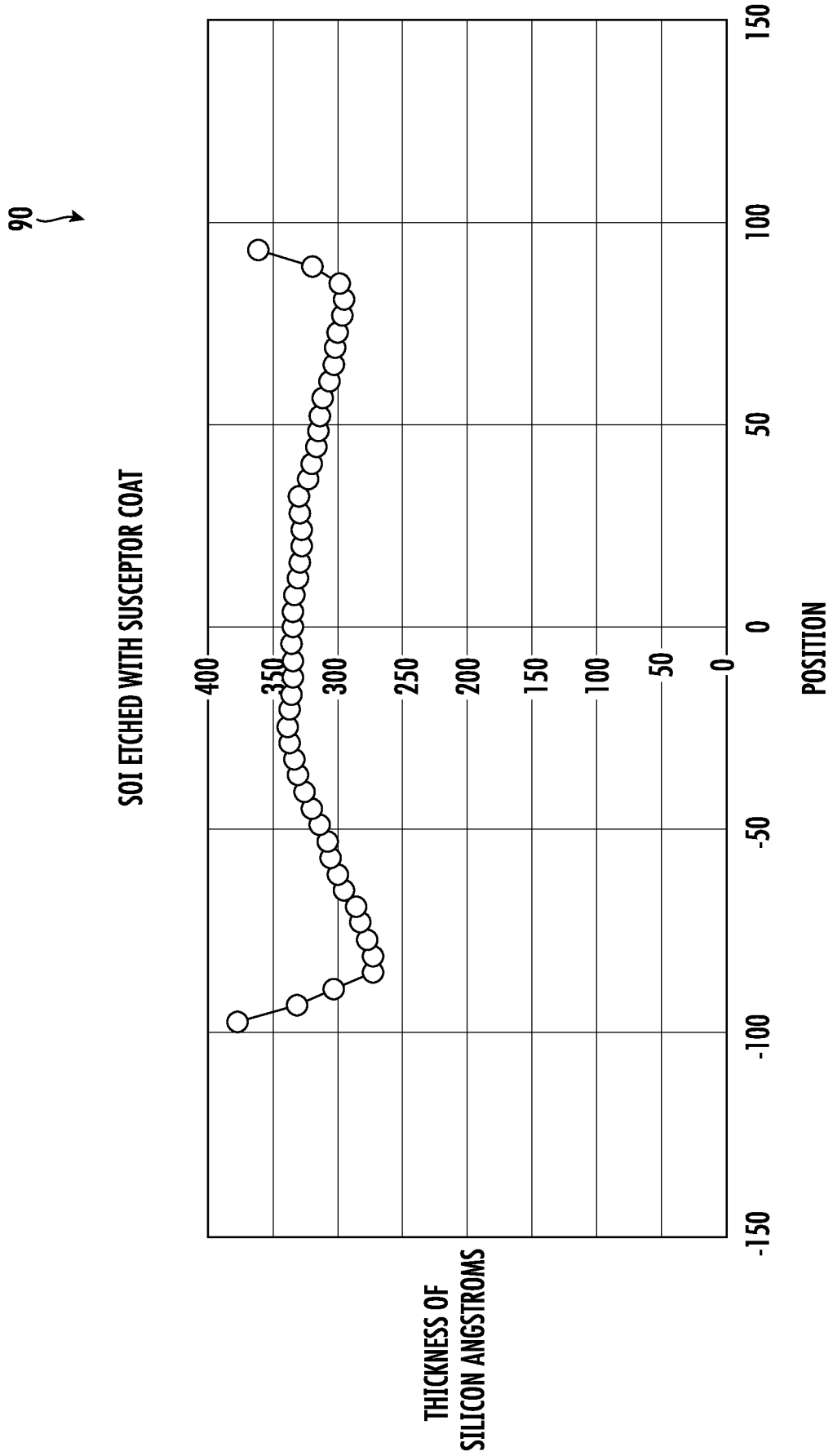


FIG. 9

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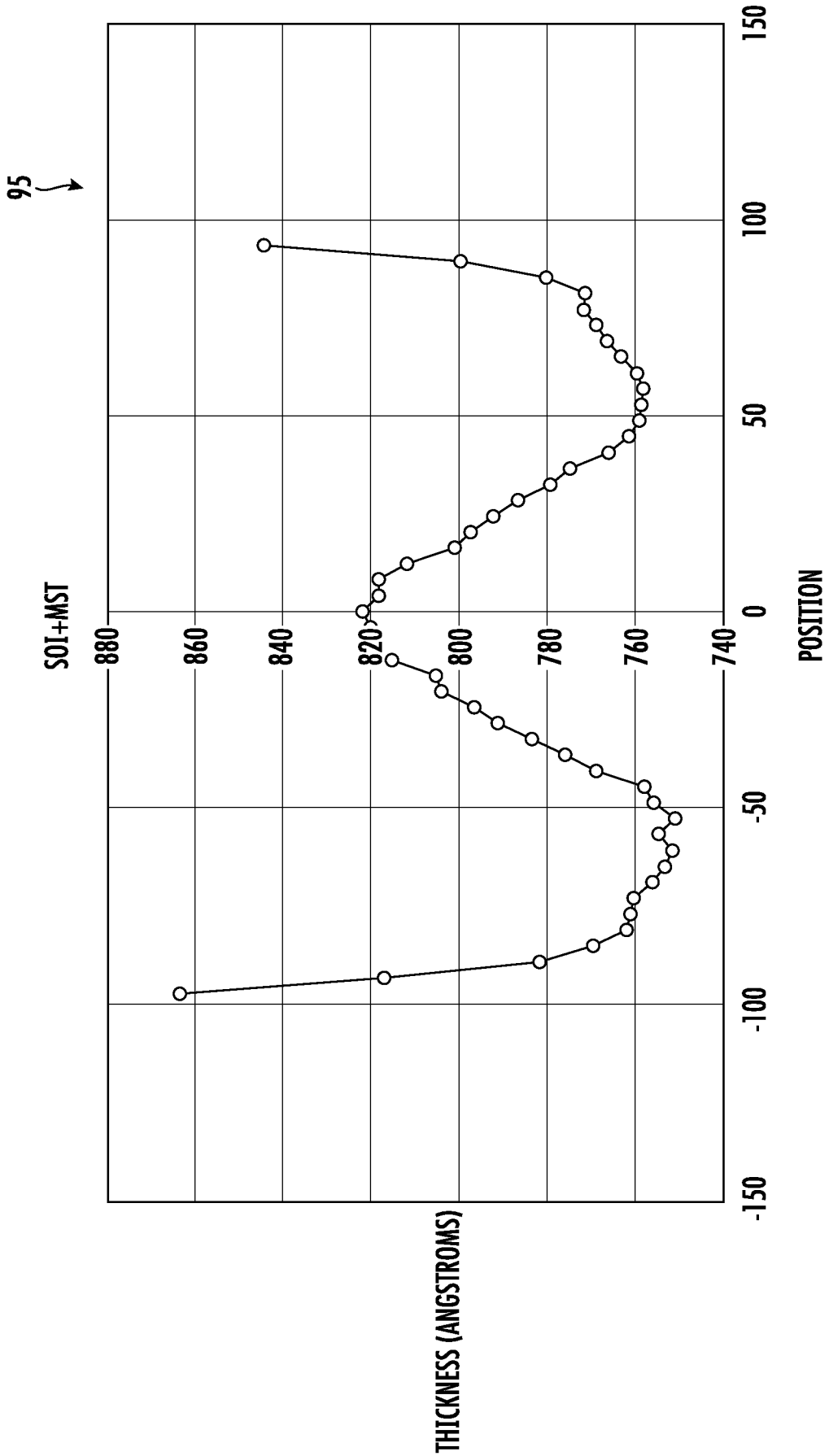


FIG. 10

# INTERNATIONAL SEARCH REPORT

International application No PCT/US2024/019687
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**A. CLASSIFICATION OF SUBJECT MATTER**  
 INV. H01L21/02 H01L21/306  
 ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
**H01L**

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
**EPO-Internal**

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2022/285152 A1 (TAKEUCHI HIDEKI [US] ET AL) 8 September 2022 (2022-09-08) paragraphs [0075] - [0083]; figure 12 -----	1-20
Y	EP 1 936 670 A2 (IMEC INTER UNI MICRO ELECTR [BE]) 25 June 2008 (2008-06-25) paragraphs [0078] - [0088]; figure 1 -----	1-20
A	US 11 075 078 B1 (CODY NYLES WYNN [US] ET AL) 27 July 2021 (2021-07-27) the whole document column 9, lines 7 - 25 -----	1-20

Further documents are listed in the continuation of Box C.       See patent family annex.

\* Special categories of cited documents :

<p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier application or patent but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p>	<p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</p> <p>"&amp;" document member of the same patent family</p>
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Date of the actual completion of the international search  <b>24 June 2024</b>	Date of mailing of the international search report  <b>24/07/2024</b>
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Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Authorized officer  <b>Simeonov, Dobri</b>
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# INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2024/019687

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