(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
30 August 2012 (30.08.2012)

WIPO | PCT

(10) International Publication Number
WO 2012/114060 A1

(51) International Patent Classification:
G09G 3/32 (2006.01)

(21) International Application Number:
PCT/GB2012/000153

(22) International Filing Date:
14 February 2012 (14.02.2012)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
1102949.3 21 February 2011 (21.02.2011) GB

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

(54) **Title**: DRIVE CIRCUITS AND TECHNIQUES

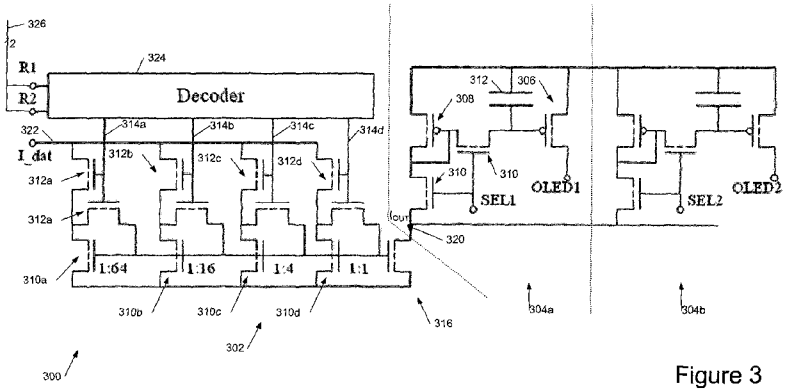

Figure 3

(57) **Abstract**: A pixel driver circuit for an active matrix OLED display comprises: a current programming line to source or sink a programming current for said pixel driver circuit; a range control line to receive a range control signal; a scaling circuit coupled to said current programming line and to said range control line, wherein said scaling circuit is configured to provide a scaled current output dependent on said programming current scaled by said range control signal; and an OLED driver circuit coupled to said scaled current output of said scaling circuit, wherein said OLED driver circuit has a pixel select line and is configured such that activating said pixel select line programs said OLED driver circuit to drive an OLED coupled to said OLED driver circuit with a current dependent on said scaled current output of said scaling circuit.

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DRIVE CIRCUITS AND TECHNIQUES

FIELD OF THE INVENTION

This invention relates to improved pixel drive techniques for organic light emitting diode (OLED) displays.

BACKGROUND TO THE INVENTION

It is known to drive an OLED display using a 'active matrix' arrangement in which individual pixels of a display are activated by an associated thin film transistor. In one drive technique an analogue current is employed to program the drive current of an active matrix OLED pixel so that the current though the pixel, and hence the luminance, is proportional to the programmed level. Thus in a standard current programmed pixel circuit a data line supplies a current which is copied, either on a 1:1 basis or with a fixed scaling, to an output stage.

The standard approach works well for large currents but the required light output from a display pixel does not depend linearly on the grey-scale signal – rather there is a gamma function which relates the grey-scale to the required luminance. For the ITU Rec709 standard used for HDTV (high definition television) this gamma function results in a dynamic range of 1000:1 between the maximum grey level and the minimum non-zero grey level; for the sRGB standard the dynamic range is approximately 200,000:1.

Where the programming current is changed to control the current driven to the OLED this creates a problem as it is difficult to control a current over such a large range to produce a well-matched output both at full scale current (typically of order 1-10 μA) and the minimum grey-level current, typically less than 10nA for Rec709, and potentially less than 50 pA for sRGB.

To take an example, consider an 8 bit, gamma = 2 grey-scale giving 256 gamma = 2 levels, which requires 65536 linear levels. An 8μA full scale current would need a 122pA programming current for the minimum non-zero grey-scale level. As the current becomes smaller the accuracy of the current copy becomes poorer and the programming time becomes longer. The capacitance of the long tracks on an HDTV

panel also makes programming very small currents difficult. The result is that the low grey levels are difficult to achieve, resulting in a short-fall in performance.

Background prior art can be found in JP 2006-128317A; DE 10033933; US 2008/0204378; and WO 2010/061978.

SUMMARY OF THE INVENTION

According to the present invention there is therefore provided a pixel driver circuit for an active matrix OLED display, the circuit comprising: a current programming line to source or sink a programming current for said pixel driver circuit; a range control line to receive a range control signal; a scaling circuit coupled to said current programming line and to said range control line, wherein said scaling circuit is configured to provide a scaled current output dependent on said programming current scaled by said range control signal; and an OLED driver circuit coupled to said scaled current output of said scaling circuit, wherein said OLED driver circuit has a pixel select line and is configured such that activating said pixel select line programs said OLED driver circuit to drive an OLED coupled to said OLED driver circuit with a current dependent on said scaled current output of said scaling circuit.

In embodiments of this pixel driver circuit, adding a range control line substantially extends the practical dynamic range and accuracy of the pixel driver circuit, enabling improved uniformity at low drive levels and more accurate low grey level reproduction.

In embodiments the pixel driver circuitry is relatively complex and may therefore be fabricated on 'chiplets' mounted on the display substrate. In embodiments a chiplet comprises an integrated circuit carrying the drive circuitry for a group of pixels, and having separate connections to each of the pixels for controlling the individual pixels in accordance with the programmed data (there may be a shared input luminance data connection for programming the group of pixels). The chiplets may be distributed over this display substrate and have one or more common serial or parallel input data connections. Each chiplet may be associated with a group of two or more pixels of the display to provide the pixel driver circuitry for the associated pixels. This architecture facilitates sharing of some of the pixel driver circuitry for a group of pixels, as described further below.

In some preferred embodiments of the pixel driver circuit the scaling circuit comprises at least one current mirror and a current mirror ratio select line coupled to the range control line to select an input:output current ratio of the current mirror. Thus, broadly speaking, the range control line (or lines) selects which of a number of scaled current input mirror (or output) stages are used to program the OLED drive current. In embodiments the current mirror ratio select line controls a pair of select transistors to select an input and/or output transistor of the current mirror. For example transistors of different sizes, more particularly channel length and/or width may be selectively connected as an input and/or output transistor and/or selectively connected in parallel with an existing input/output transistor. In embodiments at least two ratio select lines are provided for the current mirror, one to select an input transistor and one to select an output transistor so that a wide range of 'gearing ratios' may be provided between the input and output currents.

In some preferred embodiments the pixel driver circuit comprises two such current mirrors, a first, input-stage current mirror and a second, output-stage current mirror, the input stage current mirror mirroring the current on the current programming line to the output-stage current mirror, and the output-stage current mirror programming the OLED drive current for the OLED driver circuit. The lower ratio of either or both of these current mirrors may be controllable using the range control line (or lines). In embodiments the input-stage current mirror may be common to a group of pixels and a separate output-stage current mirror provided for each OLED pixel. In embodiments the output-stage current mirror is combined with the OLED driver circuit and in this way the pixel select line of the OLED driver circuit may be employed, in effect, to selectively connect an output-stage current mirror to the input-stage current mirror.

In preferred embodiments the range control signal is a multi-bit digital control signal, each bit of this signal controlling application of a current scaling factor to the programming current, to control the OLED drive current (more particularly, the current programming the OLED driver circuit). Conceptually the scaling circuit comprises a variable gain current amplifier with discrete quantised gain settings set by bits of the range control signal. Conveniently a bit of the digital range control signal selects a current mirror ratio by selecting an effective transistor size (channel width:length ratio; the effective dimensions may rise from a combination of transistors connected in parallel). In embodiments the current mirror ratios are powers of 2, but this is not

essential and an arbitrary current ratio may be defined by choosing an arbitrary effective transistor width:length ratio. For example for Rec709 (International Telecommunications Union Recommendation 709) the transfer curve has a piecewise definition with, effectively, a different gamma at low luminance. Thus one current scaling selection may be selected to match the low-luminance response, and another to match the higher luminance response, to facilitate accurate driving.

In embodiments the OLED driver circuit may comprise a 'current copy' circuit in which, during programming, a current on an input data line of the circuit is copied to provide a corresponding output current to drive the OLED pixel. For example the OLED driver circuit may be configured to store a voltage on a capacitor, responsive to activation of the pixel select line to control a driver transistor to drive the OLED with a current substantially equal to the scaled current output of the scaling circuit.

Potentially when switching between ranges, especially at low luminance levels, differences in the response of the pixel driver circuit could give rise to artefacts on the display. Thus in embodiments an OLED display incorporating the pixel driver circuit is combined with a display controller at configured (programmed) to blend the ranges by dithering. In embodiments the ranges of the programming current scaled by the range control signal partially overlap and the controller is configured to select a range such that within a spatial region of the display multiple different ranges are used for driving the OLED pixel currents, when this is possible within the overlapping ranges.

In a related aspect the invention provides a method of providing a current drive to a current–programmed active matrix OLED display, the method comprising: providing a current scaling control line for an active matrix pixel driver circuit of said display; scaling a programming current for a pixel of said OLED display to reduce said programming current by a scale factor, wherein said scaling is performed in said active matrix pixel driver circuit; storing, in said active matrix pixel driver circuit, a drive control voltage for driving said pixel of said OLED display with said scaled programming current; and driving said pixel of said OLED display with said scaled programming current using said stored drive control voltage.

Embodiments of the above described techniques facilitate driving an OLED display pixel with a controllable current of less than 10 nA, and in some applications less than 1 nA or less than 100 pA.

For the avoidance of doubt, 'pixel' as used herein may refer to a pixel that emits only a single colour, or to a pixel comprising a plurality of individually addressable sub-pixels that together enable the pixel to emit a range of colours.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects of the invention will now be further described, by way of example only, with reference to the accompanying Figures in which:

Figures 1a and 1b show, respectively, a luminance-grey-scale transfer curve for Rec. 709/sRGB, and an illustration of a portion of an OLED display including a chiplet integrated circuit;

Figures 2a and 2b show, respectively, an example of a current copy OLED pixel drive circuit, and a conceptual illustration of how an OLED drive current range can be controlled using a controllable current mirror;

Figure 3 shows a first example of a controllable range active matrix pixel driver circuit according to an embodiment of the invention;

Figures 4a and 4b show, respectively, a second example of a controllable range active matrix pixel driver circuit according to an embodiment of the invention, and a group of pixel driver circuits sharing a common input-stage controllable-range current mirror for implementation on a chiplet;

Figure 5 shows a portion of an OLED display incorporating chiplets bearing pixel driver circuits according to an embodiment of the invention; and

Figure 6 shows a combination of an OLED display according to an embodiment of the invention and a controller for the display.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 1a shows a generalised transfer curve relating an input grey-scale data value to a desired pixel luminance. In the example an 8 bit grey-scale value (up to 255) is assumed, but it will be appreciated that this is by way of example only. The non-linearity of the curve is expressed (approximately) by a gamma value, where luminance is proportional to the grey-scale value raised to the power gamma. For example for sRGB gamma is approximately 2.4.

For the Rec. 709 standard the transfer curve 10 comprises a linear portion at grey-scale values near zero and a power law portion with a gamma of 2.4 at higher grey-scale values. The effect of this is that the Rec. 709 standard curve 10a differs from the sRGB curve 10b at low grey-scale values, as illustrated, thus reducing the required dynamic range for HDTV.

We will describe later how embodiments of the invention facilitate obtaining a transfer curve of the type shown in Figure 1a.

In principle the circuits we describe later could be fabricated directly on an active matrix backplane, particularly if only a limited number of ranges is provided, for example, just two ranges. However some preferred implementations of the embodiments of the invention use chiplets for the pixel drive circuitry. In broad terms these comprise small silicon integrated circuits which are stuck onto the glass substrate of a display and connected to OLED pixels and to external connections of the display.

For details reference may be made, for example, to WO 2010/019185: Figure 1b, which is taken from WO 2010/019185, shows a layout view of a group of four pixels (20a, 20b, 20c and 20d) elements of an OLED display device. Each of the four pixels can be arranged to emit a different colour, such as red, green, blue and white (RGBW). Figure 1b represents a portion of a full display where the full display would be constructed of an array of such groups of pixels arranged in many rows and columns. For example, a modern television would be constructed having 1920 rows and 1080 columns of such groups of pixels.

A chiplet 120 is arranged to control the electrical current to pixels 20a, 20b, 20c and 20d. A chiplet is a separately fabricated integrated circuit which is mounted and embedded into the display device. Much like a conventional microchip (or chip) a chiplet is fabricated from a substrate and contains integrated transistors as well as

insulator layers and conductor layers which are deposited and then patterned using photolithographic methods in a semiconductor fabrication facility. These transistors in the chiplet are arranged in a transistor drive circuit to drive the electrical current to pixels of the display. A chiplet is smaller than a traditional microchip and unlike traditional microchips, electrical connections need not be made to a chiplet by wire bonding or flip-chip bonding. Instead, after mounting each chiplet onto the display substrate, deposition and photolithographic patterning of conductive layers and insulator layers continues. Therefore, the connections can be made small, for example through using vias 2 to 15 micrometers in size. The chiplet and connections to the chiplet are small enough to be placed within the area of one or more pixels which, depending on the display size and resolution, may range from approximately 50 micrometers to 500 micrometers in size. Additional details about the chiplet and its fabrication and mounting processes can be found in WO '185.

Each pixel is provided with a lower electrode, such as a lower electrode 161a in pixel 20a. The emitting area of pixel 20a is defined by an opening 163a in an insulator formed over the lower electrode. The device includes multiple conductive elements formed in a first conductive layer which are arranged to facilitate providing electrical signals to the chiplet's transistor drive circuitry to enable the chiplet to control electrical current to the pixels. Chiplet 120 controls current to pixel 20a through a conductor 133a. For example, conductor 133a is connected to chiplet 120 through a via 143a and is also connected to lower electrode 161a through a via 153a. The device also includes a series of signal lines including, power lines, data lines, and select lines which are formed in the first conductive layer and transmit electrical signals from the edge of the display to the chiplets. Power lines are signal lines that provide a source of electrical current to operate the organic electroluminescent elements. Data lines are signal lines which transmit bright information to regulate the brightness of each pixel. Select lines are lines which selectively determine which rows of the display are to receive brightness information from the data lines. As such select lines and data lines are routed in an orthogonal manner.

Power is provided to the chiplet 120 by way of a power line 131. Two vias are provided for connection between the power line and the chiplet 120. A data line 135 is provided in the column direction for communicating a data signal containing brightness information to chiplet 120 for pixel 20a and pixel 20b. Similarly, a data line 136 is provided in the column direction for communicating a data signal containing brightness

information to chiplet 120 for pixel 20b and pixel 20d. In an alternate arrangement the data lines 135 and 136 and the power line 131 can be connected to the chiplet 120 by only a single via for each line. A select line segment 137a is provided in the row direction for communicating a row select signal to chiplet 120 for pixel 20a and pixel 20b. The row select signal is used to indicate a particular row of pixels and is synchronized with the data signal for providing brightness information. Thus the row select signal and the data signals are provided in orthogonal directions. Chiplet 120 communicates the row select signal from select line segment 137a to a select line segment 137b by way of an internal pass-thru connection on the integrated circuit. Select line segment 137b then communicates the row select signal to subsequent chiplets arranged in the same row. Similarly a select line segment 138a is provided in the row direction for communicating a row select signal to chiplet 120 for pixel 20c and pixel 20d. Chiplet 120 communicates the row select signal from select line segment 138a to a select line segment 138b by way of another internal pass-thru connection on the integrated circuit. Select line segments 137a and 137b together serve to form a single select line, which is discontinuous. Connections between the select line segments are provided by the pass-thru connections in the chiplet. While only two segments are shown, the select line can contain a series of many such segments. Select line segments 138a and 138b similarly together serve to form a single discontinuous select line. All of the select lines segments and data lines may be formed from a single metal layer. Communication across the orthogonal array is then achieved by routing either the row select signal, the data signal, or both through the pass-thru connections on the chiplet.

It is also helpful to, facilitate understanding of the operation of embodiments of the invention, to describe an example of an OLED drive circuit. Thus Figure 2 (which is taken from our earlier patent application WO03/038790) shows an example of a "current copying" current-programmed pixel driver circuit. In this circuit the current through an OLED 252 is programmed by setting a drain source current for OLED driver transistor 258 using current generator 266, for example a reference current sink, and copying/memorising the driver transistor gate voltage required for this drain-source current. Thus the brightness of OLED 252 is determined by the current, I_{DAT}, flowing into reference current sink 266, which may be adjustable and set as desired for the pixel being addressed. A switching transistor 264 is connected between drive transistor 258 and OLED 252 to inhibit OLED illumination during the programming phase. In general one current sink 266 is provided for each column data line. To copy

the programming current, switch transistor 268 is "closed" and switch transistor 264 is "opened" so that the programming current flows through drive transistor 258, and switch transistor 270 is also closed to set Vg on drive transistor 270 for the programmed current and to store this Vg value on capacitor 220.

The skilled person will, however, appreciate that there are many other examples of current-programmed pixel drive circuits.

Range-controlled active matrix pixel circuits

Figure 2b illustrates conceptually how an OLED drive current range can be controlled using a controllable current mirror. Thus in the arrangement of Figure 2b, coupling a pair of matched transistors 280, 282 in parallel on the input side of the current mirror configures the mirror to provide an output current which is half the input current. More generally, the OLED drive current I_{OLED} is related to the input, programming current I_{pgm}, and number of input transistors, N_{tr}, by

$$I_{OLED} = \frac{I_{pgm}}{N_{tr}}$$

More generally for *N* input transistors connected in parallel and *M* output transistors connected in parallel,

$$I_{OLED} = I_{pgm} \cdot \frac{M}{N}$$

In an implementation of this approach select transistors are provided to selectively connect the input and/or output transistors in parallel, and hence to control the mirror current ratio and, in a pixel driver circuit, to select a current range.

Although the input and output transistors of the current mirror of Figure 2b are matched, they need not be the same size. In particular, the drain current of a MOSFET is proportional to *W/L* where *W* is the channel width and *L* is the channel length. Thus a wider channel is used to deliver more current and a long thin channel is used to

deliver less current. In the current mirror of Figure 2b, if "input" and "output" label the input and output transistors respectively:

$$I_{OLED} = I_{pgm} \cdot \frac{(W/L)_{output}}{(W/L)_{input}}$$

We will now describe pixel driver circuits which provide a range select input or inputs to change the programming range of a current programmed OLED drive circuit, in particular implemented on a chiplet. The chiplet-based drive circuit is configured to drive a group of OLED pixels, for example 12 pixels. The current programmed chiplet circuit has an input stage which accepts the data current supplied and which then programs a selected one of the, for example 12, output stages using some selection means. The selection means may simply comprise select lines on the OLED drive circuits or a multiplexer may be provided between the input stage and output stages.

In embodiments a small number (one or more) of further control lines, in addition to the data line, are provided to select one from a plurality of different input stages. Each of these input stages may be a mirror transistor, mirror to a common output transistor. In embodiments each of these mirror transistors has a different geometrical scaling to the common output transistor such that each input stage defines a different current scaling for the mirror circuit. The scaled current supplied by the common output transistor is then used to program the selected OLED drive circuit.

Referring now to Figure 3, this shows one example implementation of a controllable range active matrix pixel driver circuit 300 according to an embodiment of the invention. the circuit comprises a first current mirror stage 302 coupled to a plurality of second current mirror stages 304a, b each comprising an OLED drive circuit for driving a respective OLED (not shown).

The first current mirror circuit 302 comprises a set of selectable input transistors 310a-d each of a different size. In the illustrated example the sizes are arranged to reduce the input, programming current by a selectable factor of 1:1, 1:4, 1:16 and 1:64. Each input transistor 310a-d is selected by a corresponding pair of select transistors 312a-d according to a signal on a respective control line 314a-d. The current mirror 302 has an output transistor 316 to provide (source or sink a current I_{OUT} on output line 320. The

input, programming current is provided (by a current source or current sink) on current data line 322, connected to the input transistors 310 by select transistors 312. A decoder 324 receives a control input from a 2 bit range control line 326 and activates one of lines 314a-d in accordance with the range control signal on line 326 to select an input transistor 310a-d, and hence to programme the ratio of the first current mirror 302.

The output current of the first current mirror on line 320 provides an input to each of the OLED drive circuits 304, each of which in the illustrated example comprises a second current mirror. The second current mirror has an input transistor 308 and an output transistor 306, the latter providing a drive current for the OLED. The input transistor 308 is selectively connected to the output 320 for the first current mirror by a pair of select transistors 310 and the operation of the current mirror programmes the voltage onto capacitor 312 which copies the current on line 320 to the OLED driven by the current mirror.

Consider an example in which the input current data line 322 has a full scale current of 8 μA. We assume, in this example, an input range of 1:4, that is 2 μA to 8 μA. The input stage is selected by the range control line 326, more particularly by bits R1 and R2 (which may be provided in parallel or in series). Table 1 below shows the operation of the circuit of Figure 3 for this input current range, showing the scaling and final, OLED drive current range dependent upon the range control signal on the R lines (where, for example, 0 denotes a low voltage and 1 denotes a high voltage).

Input range	**R1, R2**	**scaling**	**Programme range**
2-8μA	0,0	1:1	2-8μA
	0,1	4:1	500nA – 2μA
	1,0	16:1	125nA – 500nA
	1,1	64:1	31nA – 125nA

Table 1

The above example illustrates extending the practical programming range by a factor of 64. Wider ratio ranges may be used to provide an even broader dynamic range. Further, in the lowest programming range, matching at the bottom end is less critical than in the overlap regions.

As a further example, in order to achieve a full 16 bit range of current programming a 7 bit data line may be provided with 2 range lines and a range spacing with a factor of 8. Table 2 below illustrates the operation of this further example:

Input range	R1, R2	scaling	Programme range
0.13 – 16μA (2-16μA ±2%)	00	2:1	63nA – 8μA
	01	16:1	8nA – 1μA
	10	128:1	1 – 125nA
	11	1024:1	122pA – 16nA

Table 2

Referring now to Figure 4a, this shows a second example of an active matrix pixel driver circuit 4 according to an embodiment of the invention. In this example a current mirror 402 has a controllable ratio input portion 404 and a controllable ratio output portion 406, the latter providing an output current on line 420 which is an integer fraction, of the input, programming current on line 422. A 4-bit range control line 414a-d is provided, two bits of the range control signal controlling the input ratio and two bits of the range control signal controlling the output ratio of the current mirror 402. Thus the current mirror comprises a pair of input transistors 410a-b selected by a respective pair of select transistors 412a, b coupled to the respective range control bit lines 414a, b. The output stage comprises two output transistors 416a, b, again each selected by a respective pair of select transistors 418a, b controlled by lines 414c, d. The current output 420 provides a current-programming input to an OLED drive circuit 430, for example of the type shown in Figure 2a.

In embodiments the current mirror 402 provides an output to a plurality of OLED drive circuits 430 each selectable to copy the output current from mirror 402 to an OLED drive current. Optionally, as illustrated in Figure 3, the drive circuit 430 may also incorporate a current mirror. This arrangement is conceptually illustrated in Figure 4b.

In Figure 4 example transistor sizes are shown in terms of channel length and width ratios. Assuming a nominal 1 μA programming, input current, lines S1 to S4 may be controlled to provide a range of ratios and output currents for current mirror 402, as illustrated by table 3 below.

	S1	S2
S3	1:1	2:1
S4	4:1	8:1

	S1	S2
S3	1μA	½ μA
S4	¼ μA	1/8μA

Table 3

One potential difficulty with circuits of the type shown in Figures 3 and 4 is that the matching of the transistor characteristics may become inaccurate at low currents where a transistor may be driven at below its threshold voltage. This may be addressed by arranging for the current ranges to overlap, especially at low current levels, and then randomly picking the scaling factor to effectively blend or dither the current ranges over a spatial region of the display. This function may be implemented in a display controller.

Referring now to Figure 5, this shows, schematically, a portion of an OLED display 500 provided with a chiplet 502 bearing a plurality of OLED drive circuits 430 sharing a common controllable ratio current mirror 402. In the illustrated example luminous data is provided digitally on data line 504 and an analogue-to-digital converter (not shown) is incorporated into the shared current mirror circuit to provide a programming current. A portion of the data online 504 may provide the range control signal. This data may be delivered as serial data, parallel data, or a combination of the two. A block/pixel select control line or lines 506 is also provided. As illustrated the chip at 502 drives 4 pixels, but in embodiments this chiplet may be shared between a larger number of pixels of the display.

Figure 6 shows a combination of the OLED display 500 of Figure 5 and a controller 600 forming an OLED display system. In this system RGB (red, green, blue) data is input from line 602 and controller 600 performs a grey-scale mapping using a grey-scale lookup table 604 to determine a desired pixel luminance according to a transfer curve,

for example of the type shown in Figure 1a. This provides a digital data value defining the luminance and controller 600 then maps this to a programming current and range and this data is output on lines 504 for following the active matrix pixel driver circuits on the chiplets. In the illustrated example a line 606 controls a shift register 608 to control addressing of the chiplets. Optionally the controller 600 may implement overlapping range spatial dithering as previously described, to reduce visual artefacts at low luminance levels.

No doubt many other effective alternatives will occur to the skilled person. It will be understood that the invention is not limited to the described embodiments and encompasses modifications apparent to those skilled in the art lying within the scope of the claims appended hereto.

CLAIMS

1. A pixel driver circuit for an active matrix OLED display, the circuit comprising:

a current programming line to source or sink a programming current for said pixel driver circuit;

a range control line to receive a range control signal;

a scaling circuit coupled to said current programming line and to said range control line, wherein said scaling circuit is configured to provide a scaled current output dependent on said programming current scaled by said range control signal; and

an OLED driver circuit coupled to said scaled current output of said scaling circuit, wherein said OLED driver circuit has a pixel select line and is configured such that activating said pixel select line programs said OLED driver circuit to drive an OLED coupled to said OLED driver circuit with a current dependent on said scaled current output of said scaling circuit.

2. A pixel driver circuit as claimed in claim 1 where said scaling circuit comprises at least a first current mirror having an input coupled to said current programming line, having a current output to control said scaled current output, and having at least one ratio select line coupled to said range control line and select an input:output current ratio of said first current mirror.

3. A pixel driver circuit as claimed in claim 2 wherein said ratio select line is coupled to control at least a pair of select transistors to select an input transistor of said first current mirror.

4. A pixel driver circuit as claimed in claim 2 or 3 wherein said first current mirror has a second ratio select line coupled to control at least a pair of select transistors to select an output transistor of said first current and mirror circuit.

5. A pixel driver circuit as claimed in claim 2, 3 or 4 where said scaling circuit comprises at least one second current mirror having an input to said current output of said first current mirror, and having a current output coupled to said scaled current output.

6. A pixel driver circuit as claimed in claim 5 wherein said second current mirror has at least one ratio select line coupled to said range control line and select an input: output current ratio of said second current mirror.

7. A pixel driver circuit as claimed in claim 5 or 6 comprising a plurality of said OLED driver circuits, and a plurality of said second current mirrors each coupled to a respective said OLED driver circuit, wherein respective said inputs of said second current mirrors are coupled the same said current output of said first current mirror to share said first current mirror, and wherein said pixel driver circuit is controllable to selectively program each said OLED driver circuit from a respective said second current mirror via said shared first current mirror.

8. A pixel driver circuit as claimed in any preceding claim wherein said range control signal comprises a multi-bit digital control signal, and wherein each said bit of said control signal controls application of a current scaling factor to said programming current to provide a current for programming said OLED driver circuit.

9. A pixel driver circuit as claimed in claim 8 wherein a first bit of said digital control signal is configured to control selection of an input current scaling stage of said scaling circuit, and wherein a second bit of said digital control signal is configured to control selection of an output current scaling stage of said scaling circuit.

10. A pixel driver circuit as claimed in any preceding claim wherein ranges of said programming current scaled by said range control signal overlap.

11. A pixel driver circuit as claimed in any preceding claim wherein said OLED driver circuit is configured to store a voltage on a capacitor, responsive to said activation of said pixel select line, to control a driver transistor to drive said OLED with a current substantially equal to a current of said scaled current output of said scaling circuit.

12. An organic light emitting diode (OLED) display comprising a substrate bearing a plurality of OLED pixels and a plurality of said pixel driver circuits to drive said OLED pixels.

13. An OLED display as claimed in claim 12 further comprising a plurality of chiplets mounted on said substrate, wherein each said chiplet is mounted adjacent a group of said pixels and comprises a chiplet substrate bearing pixel driver circuits for said group of pixels.

14. An OLED display as claimed in claim 12 or 13 when dependent on claim 10, in combination with a display controller configured to select a said range such that within a spatial region of said display multiple different said ranges are used for driving OLED pixel currents within said overlapping ranges.

15. A method of providing a current drive to a current–programmed active matrix OLED display, the method comprising:

providing a current scaling control line for an active matrix pixel driver circuit of said display;

scaling a programming current for a pixel of said OLED display to reduce said programming current by a scale factor, wherein said scaling is performed in said active matrix pixel driver circuit;

storing, in said active matrix pixel driver circuit, a drive control voltage for driving said pixel of said OLED display with said scaled programming current; and

driving said pixel of said OLED display with said scaled programming current using said stored drive control voltage.

16. A pixel driver circuit, OLED display, or method, as recited in any preceding claim, wherein said OLED/pixel is driven with a controllable current of less than 10 nA or less than 1 nA.

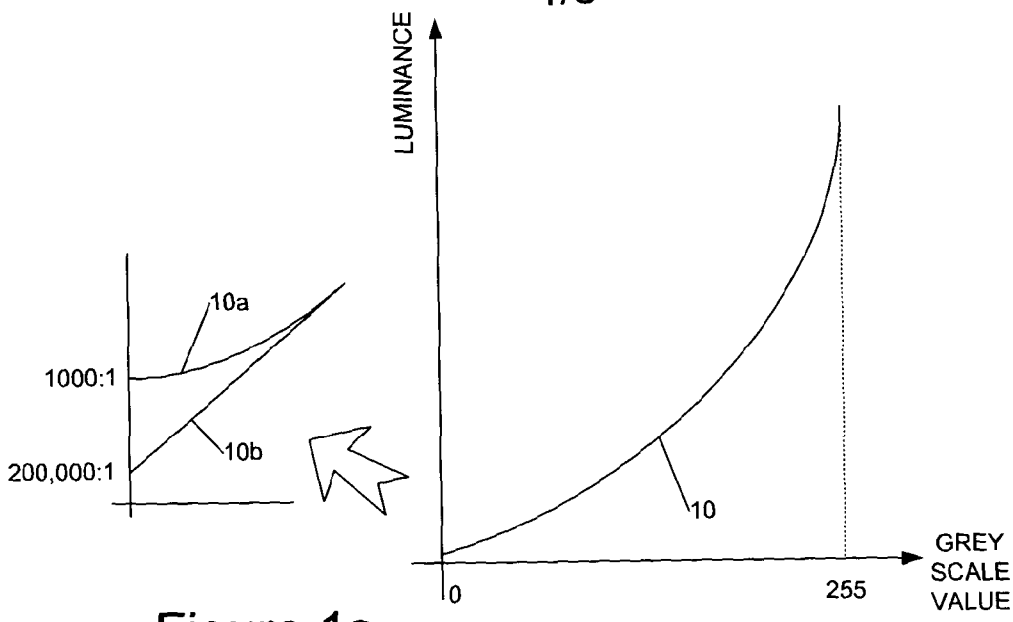

Figure 1a
(PRIOR ART)

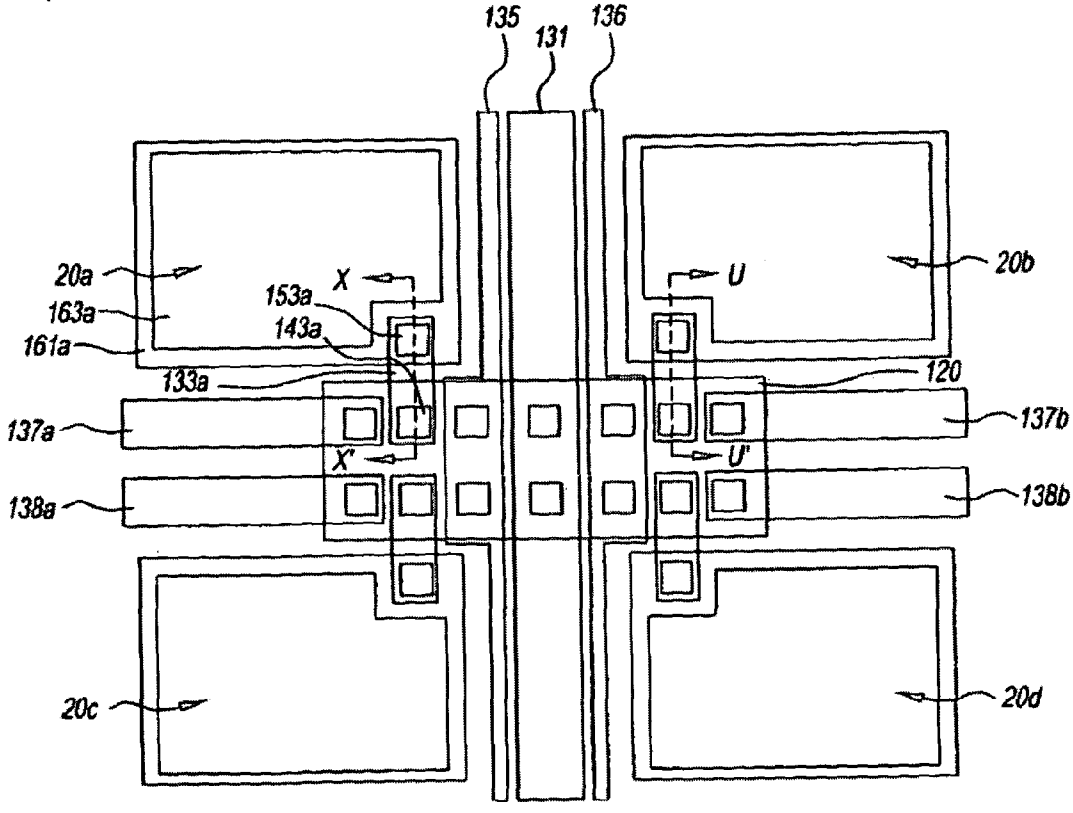

Figure 1b
(PRIOR ART)

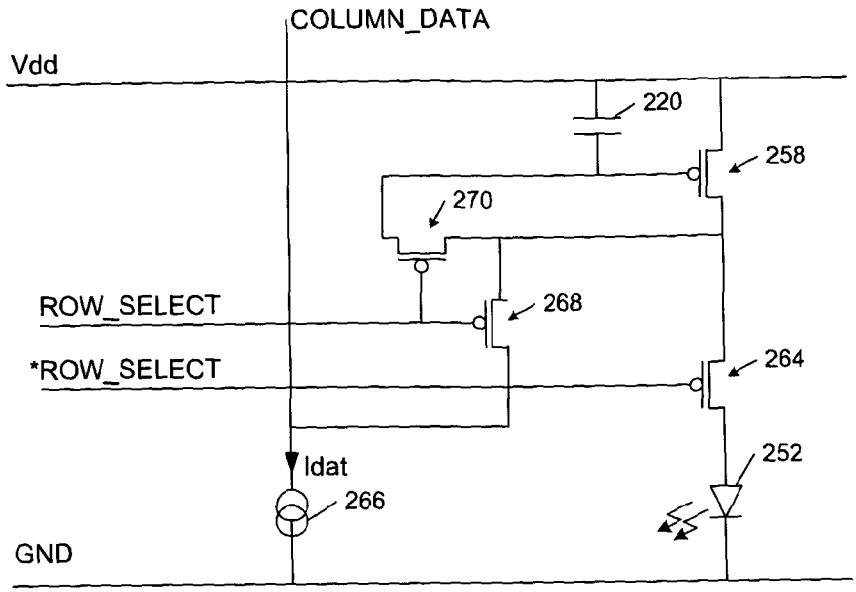

Figure 2a

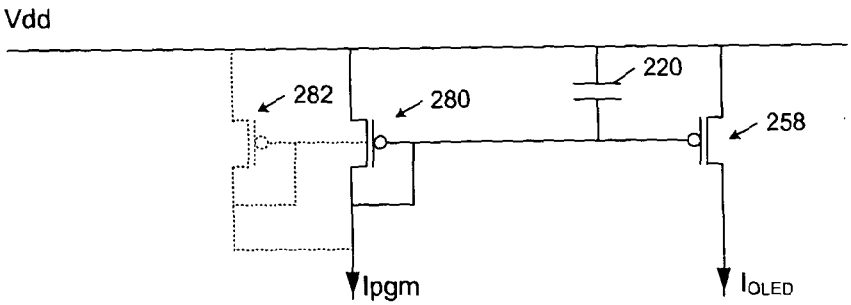

Figure 2b

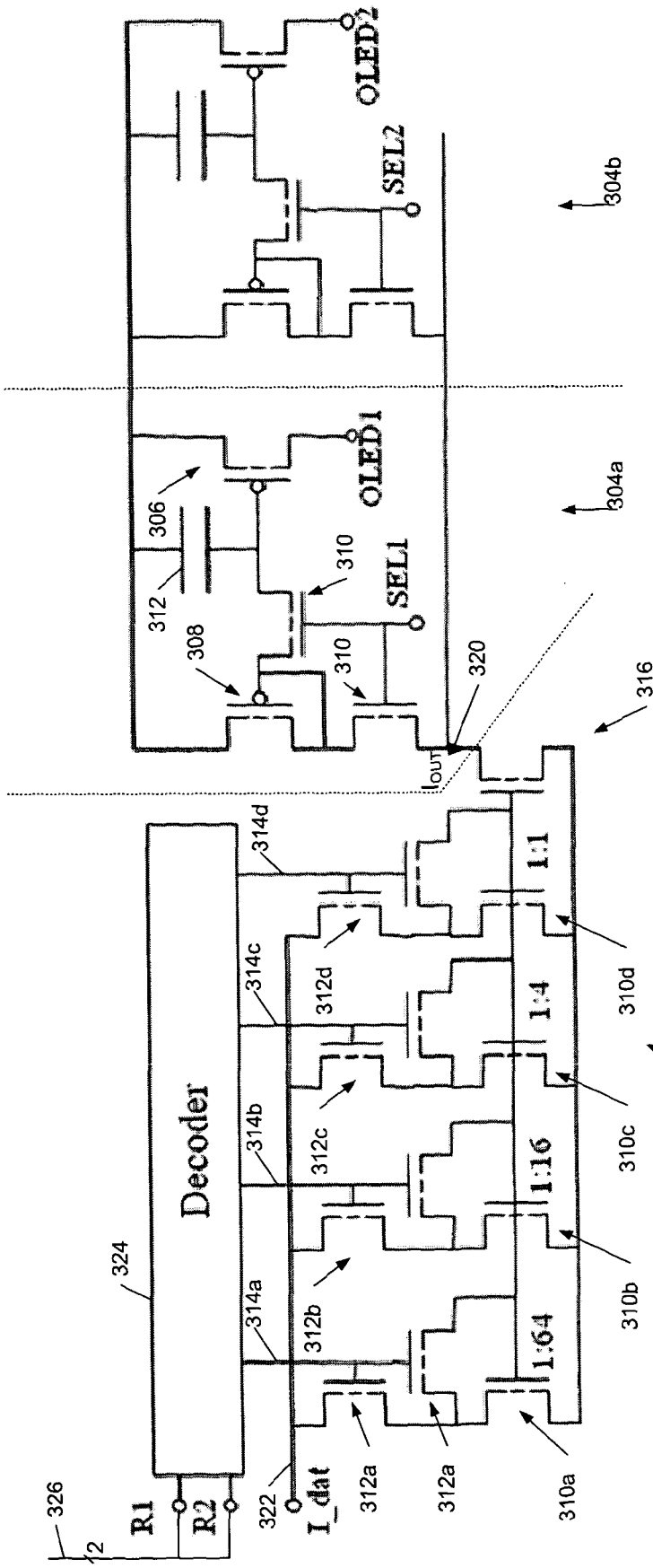
OLED2
SEL2
304b
OLED1
306
310
SEL1
312
308
310
320
316
304a
IOUT
314d
1:1
310d
312d
314c
1:4
302
310c
312c
314b
1:16
310b
324
Decoder
312b
314a
1:64
310a
312a
312a
322
I_dat
326
2
R1
R2
300

Figure 3

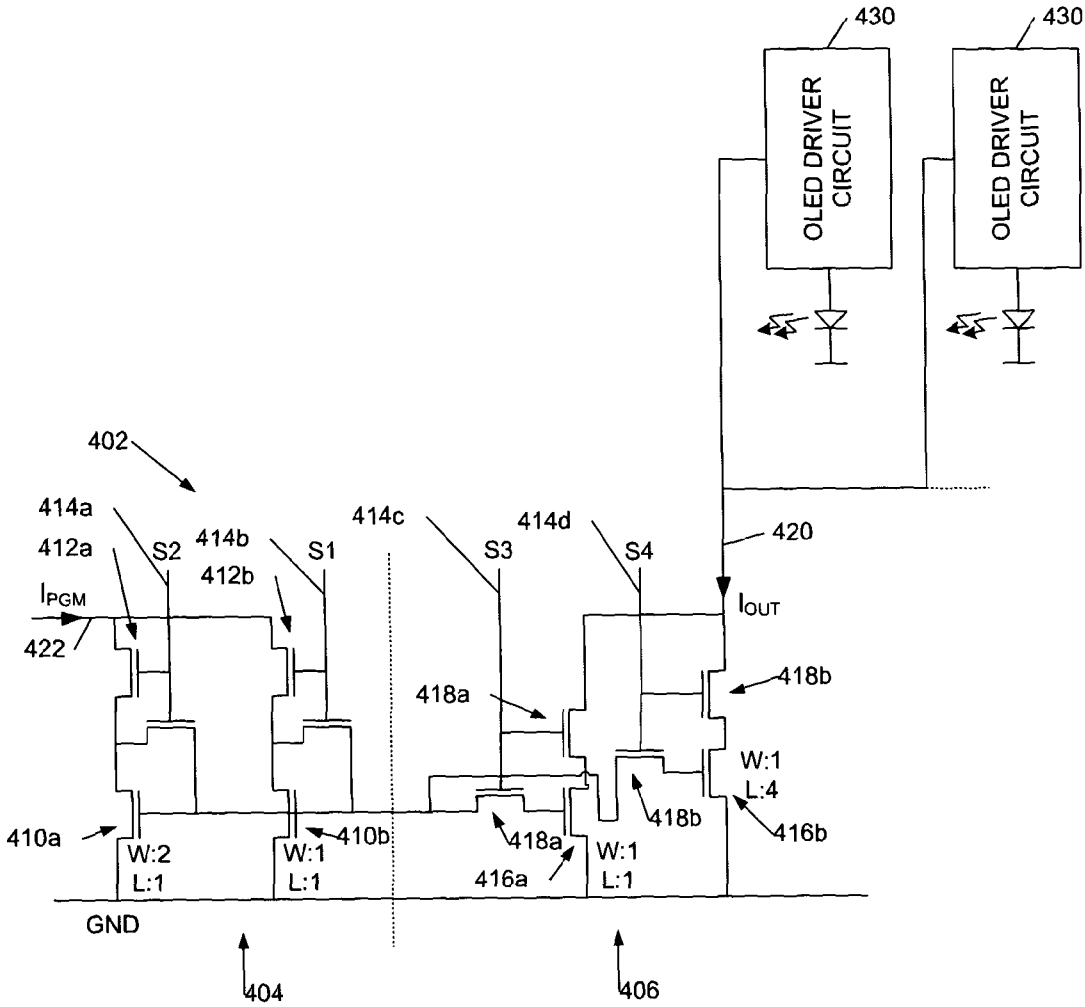

Figure 4a

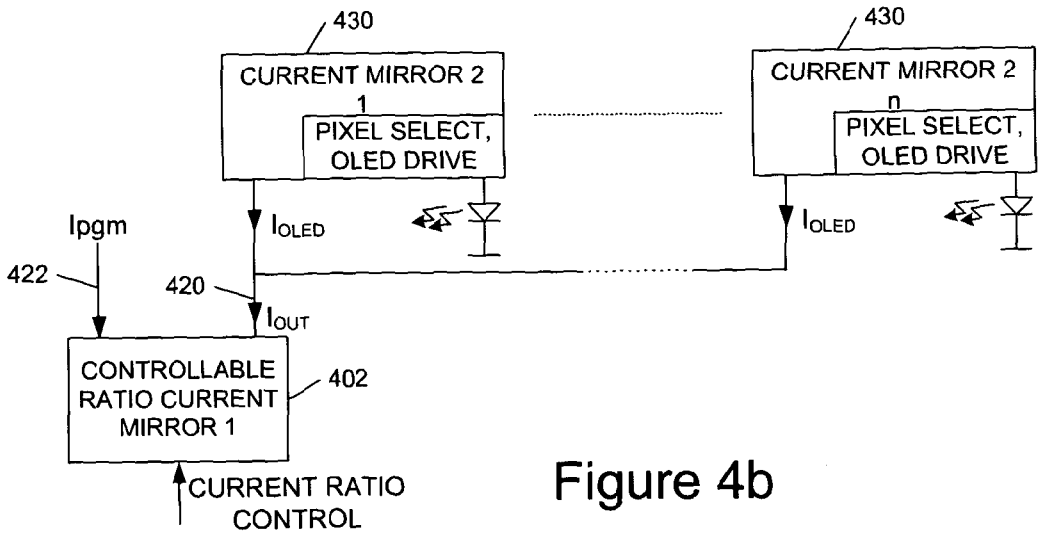

Figure 4b

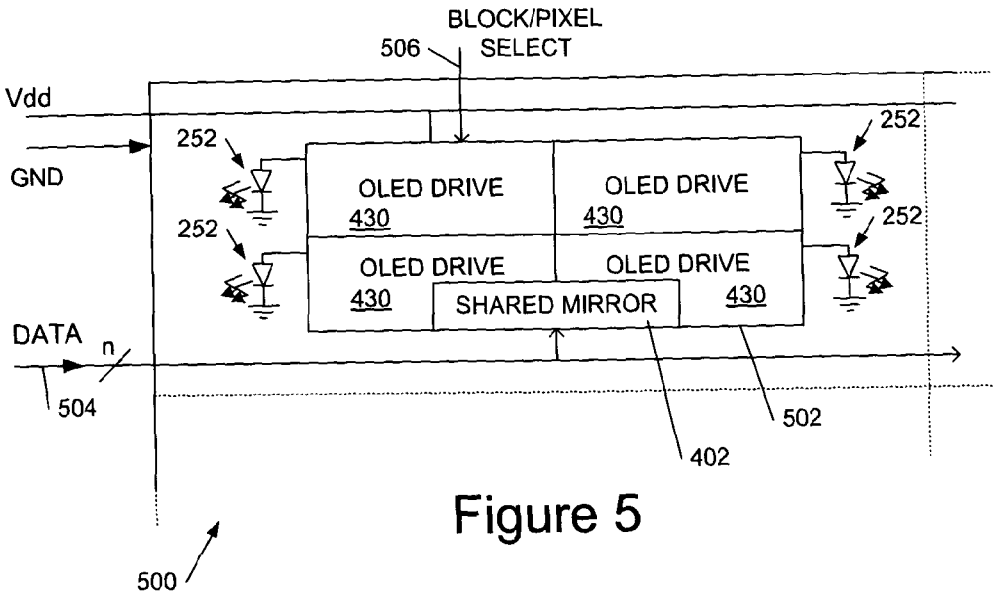

Figure 5

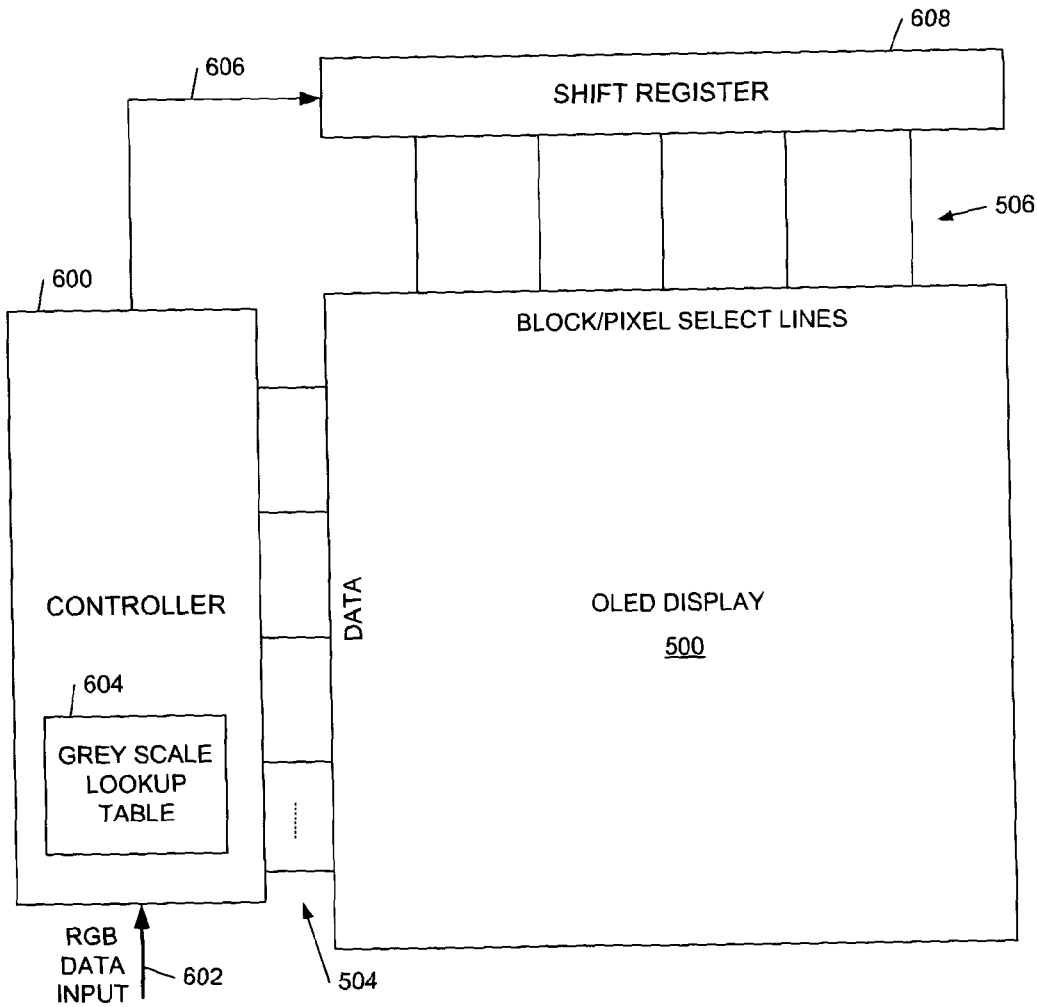

Figure 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/GB2012/000153

A. CLASSIFICATION OF SUBJECT MATTER
INV. G09G3/32
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G09G H03M G05F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2005/017931 A1 (TOYOSHIMA TSUYOSHI [JP] ET AL) 27 January 2005 (2005-01-27) figures 3,4,8,9 paragraphs [0071] - [0079], [0132] - [0136] -----	1-4,8-16
X	US 2005/168490 A1 (TAKAHARA HIROSHI [JP]) 4 August 2005 (2005-08-04) figures 38,63 paragraphs [0411] - [0412], [0902] - [0917] -----	1,2,4-9, 11-13, 15,16
A	US 2003/048669 A1 (ABE KATSUMI [JP]) 13 March 2003 (2003-03-13) figure 27 paragraph [0169] -----	4

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 April 2012	25/04/2012

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Ladiray, Olivier

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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PCT/GB2012/000153

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