(54) Title: HIGH SPEED MEMORY SELF-TIMING CIRCUITRY AND METHODS FOR IMPLEMENTING THE SAME

(57) Abstract

A memory circuit includes a memory core (200) having an array of core cells (202, 203). The array of core cells (202, 203) are coupled to a plurality of wordlines (226) and a plurality of bitline pairs (229). The memory circuit further includes a self-timing path that has a model core cell (203') coupled to a model wordline(222) which is driven by a model wordline driver (206"). The self-timing path also includes a model sense amplifier (204') coupled to the model core cell through a pair of model bitlines (230, /230). The model wordline and the pair of model bitlines are each coupled to a plurality of dummy core cells (202'', 202') to approximate an RC delay of a worst case core cell of the array of core cells (202, 203). Further, the model wordline (222) is a folded wordline, such that the model wordline has a termination at a location that is proximate to the model wordline driver (206').
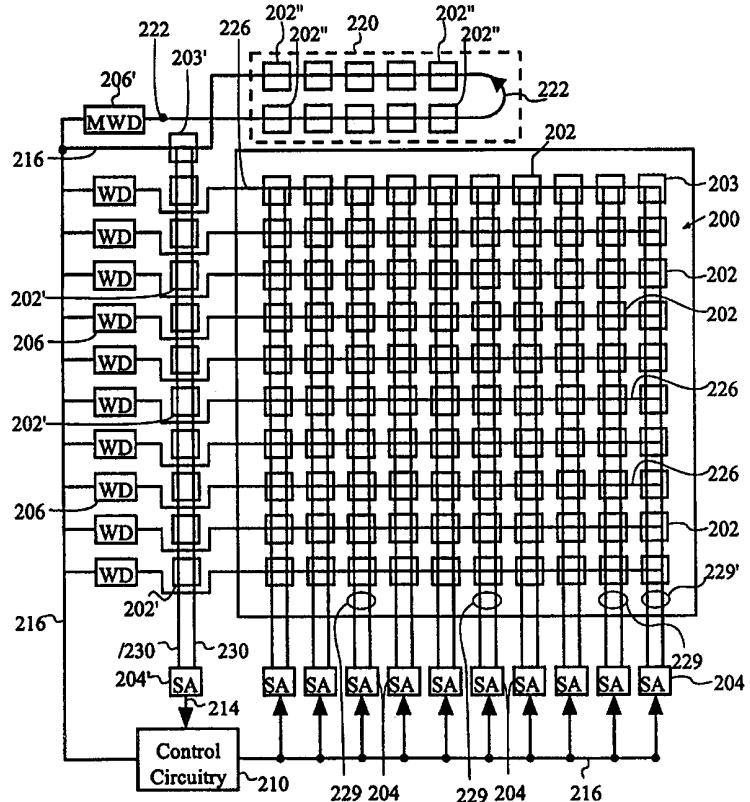
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HIGH SPEED MEMORY SELF-TIMING CIRCUITRY AND METHODS FOR IMPLEMENTING THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to integrated circuits, and more particularly to methods and apparatus for improved memory self-timing circuitry.

2. Description of the Related Art

Semiconductor memory cores are usually laid-out in array format, such that each individual core cell is coupled by a wordline and a pair of differential bitlines. To access data stored in a selected core cell, associated memory accessing circuitry is commonly designed around a memory core. For example, some of the key memory accessing circuitry typically includes addressing circuitry for selecting a core cell, wordline drivers for driving a selected wordline, and sense amplifiers for amplifying the signal read from the selected core cell.

For ease of understanding, Figure 1 shows a block diagram of a memory circuit having a memory core 100 and associated access circuitry. As in conventional memory core designs, a plurality of core cells 102 are laid out in an array format throughout the memory core 100. In this example, a control block circuit 110 is used to control access to selected memory core cells 102 through the use of wordline drivers 106 and sense amplifiers (SA) 104.

In this example, the control block circuit 110 is configured to produce a signal that triggers a selected wordline driver 106 upon a rising edge of the signal 116. When the signal 116 experiences a falling edge (*i.e.,* at a time determined by a conventional self-timing architecture described below), the signal 116 will initiate the sensing of data through one of the selected sense amplifiers 104. As shown, the wordline drivers 106 are connected to each

of the core cells 102 through the use of wordlines that interconnect each of the core cells 102 in a horizontal direction. In a like manner, the sense amplifiers 104 are connected to each of the core cells 102 in the vertical direction, through the use of differential bitlines.

In conventional memory circuitry, designers have used a self-timing architecture that

5   enables a memory circuit to determine when the sense amplifiers 104 should commence sensing data from the core cells 102 in the memory core 100. Self-timing architectures are generally used to approximate a standard delay time (i.e., which is generally the worst case timing delay for a given core) which will be used when an access to any one of the core cells 102 is attempted. The self-timing architecture is generally needed because the actual delay time of a particular core

10   cell 102 will generally be different depending on the location of the particular core cell 102. By way of example, a core cell 103 is located at the furthest location from a given wordline driver 106 and a given sense amplifier 104.

Therefore, an RC delay associated with the wordline that couples the wordline driver 106 to the core cell 103, and the RC delay associated with the bitlines that couple a sense amplifier

15   104 to the core cell 103, will have a combined RC delay that is larger than any other core cell 102 in the memory core 100. For example, the combined RC delay of the wordline and the bitlines that couple to a core cell 101, will be smaller than any other core cell that is laid out in the memory core 100. Therefore, the self-timing architecture which includes a model wordline driver 106', core cells 102', a model core cell 103', a model wordline 112a, model bitlines 112b,

20   sense amplifier 104', and a self-timing return path 114 serves to establish the aforementioned standard delay time.

Accordingly, the self-timing architecture is well suited to estimate when enough bitline differential has been achieved (i.e., due to the worst case model core cell 103') to correctly perform a sense amplification to read the data of a given core cell 102 in the memory core 100.

In operation, the control block circuitry will initiate a select signal 116 to the model wordline driver 106' to access the model core cell 103'. When the model core cell 103' has been accessed, a signal is passed through the model bitlines 112b, through sense amplifier 104' and along the self-timing return path 114, that communicates to the control block circuit 110.

5   A particular problem with conventional self-timing architectures is that memory circuit will be ready to read data once the sense amplifier 104' has received the signal from the model core cell 103'. However, the additional self-timing return path 114 will necessarily add an additional RC delay to the RC delay of the model wordline 112a and the model bitline 112b. This additional RC delay introduced by the self-timing return path 114 will unfortunately slow

10   down a memory accessing operation. As such, the control block circuit 110 will not initiate a ready-to-read signal 116 to a given sense amplifier 104 until the control block circuit 110 receives the signal from the self-timing return path 114. Consequently, in applications where high-speed memory accessing is required, the performance of the entire memory circuit will suffer due to the additional RC delay introduced by the self-timing return path 114.

15   In view of the foregoing, there is a need for self-timed memory circuitry that avoids the introduction of unnecessary RC delays when access to a worst-case model core cell is performed.

SUMMARY OF THE INVENTION

Broadly speaking, the present invention fills these needs by providing methods and apparatuses for self-timing memory circuitry that eliminates unnecessary RC delays and

20   substantially speeds up memory accessing operations. It should be appreciated that the present invention can be implemented in numerous ways, including as a process, an apparatus, a system, a device, or a method. Several embodiments of the present invention are described below.

In one embodiment, a memory circuit is disclosed. The memory circuit includes a memory core having an array of core cells. The array of core cells are coupled to a plurality of wordlines and a plurality of bitline pairs. The memory circuit further includes a self-timing path that has a model core cell that is coupled to a model wordline, and the model wordline is driven by a model wordline driver. The self-timing path also includes a model sense amplifier that is coupled to the model core cell through a pair of model bitlines. The model wordline and the pair of model bitlines are each coupled to a plurality of dummy core cells to approximate an RC delay of a worst case core cell of the array of core cells. Further, the model wordline is a folded wordline, such that the model wordline has a termination at a location that is proximate to the model wordline driver.

In another embodiment, a method for making a memory circuit with a self-timing path is disclosed. The method includes providing a memory core that has an array of core cells. The method further includes integrating a self-timing path of core cells along a model wordline and along a model pair of bitlines. The model wordline is folded such that a model core cell is placed substantially at a beginning point of the model wordline, and an ending point of the model wordline is coupled to the model core cell.

In yet another embodiment, a memory generator for producing a memory circuit that includes a self-timing path is disclosed. The memory circuit has a memory core with an array of core cells. In this embodiment, the memory generator is configured to generate a self-timing path of core cells along a model wordline and along a model pair of bitlines. The model wordline is folded such that a model core cell is placed substantially at a beginning point of the model wordline, and an ending point of the model wordline is coupled to the model core cell.

Other aspects and advantages of the invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

5   The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements.

Figure 1 shows a block diagram of a memory circuit having a memory core and associated access circuitry.

10   Figure 2A shows a memory circuit having a memory core that includes an array of core cells in accordance with one embodiment of the present invention.

Figures 2B and 2C show arrangements for a folded wordline in accordance with alternative embodiments of the present invention.

Figure 3 shows an example of a model core cell in accordance with one embodiment
15   of the present invention.

Figure 4 is an example of a model wordline driver as shown in Figure 2A above in accordance with one embodiment of the present invention.

Figure 5A shows an example of a core cell that lies in the memory core in accordance with one embodiment of the present invention.

20   Figure 5B shows an example of a core cell that is laid out along the model bitlines in accordance with one embodiment of the present invention.

Figure 5C shows an example of a core cell that is laid out along the model wordline in accordance with one embodiment of the present invention.

Figure 6 is an example circuit diagram of a control circuit of Figure 2A in accordance
25   with one embodiment of the present invention.

Figure 7 shows a model path and read timing diagram 700 in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An invention for self-timing memory circuitry that eliminates unnecessary RC delays

5   and substantially speeds up memory accessing operations is disclosed. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be understood, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail in order

10   not to unnecessarily obscure the present invention.

Figure 2A shows a memory circuit having a memory core 200 with an array of core cells 202 in accordance with one embodiment of the present invention. As shown, the core cells 202 are coupled to wordline drivers 206 through wordlines 226 in the horizontal direction, and sense amplifiers 204 through bitlines 229 in the vertical direction. Control

15   circuitry 210 is also shown coupled to each of the wordline drivers 206 and the sense amplifiers 204. In this example, the sense amplifiers 204 are shown as discrete blocks, however, it should be understood that the sense amplifier is typically a circuit that is coupled to each of the bitlines 229 through well known Y-decoder circuitry (not shown).

As is well known, Y-decoders are used for addressing a selected column (i.e.,

20   differential bitlines) within the memory core 200. For example, Y-decoders are generally implemented for reducing memory array aspect ratios by folding (*i.e.,* dividing) long addressable memory columns into several shorter memory columns. Once folded into several columns, the Y-decoder is capable of accessing the addressed data by appropriately performing a suitable multiplexing function.

In this embodiment, an improved self-timing architecture is disclosed to eliminate delays associated with the self-timing return path 114 used in the conventional design of Figure 1. For example, once the RC delays of a wordline 222 and differential bitlines (*i.e.*, 230, /230) are rapidly transferred by a signal 214 to the control circuitry 210 (from a model

5   sense amplifier 204'), a ready to read signal 216 will be immediately transmitted as shown in Figure 2A. The elimination of the RC delay associated with the self-timing return path of conventional designs is primarily facilitated by a folded wordline 220.

Preferably, the folded wordline 220 will include half of a set of core cells 202" stacked over the remaining half. This arrangement therefore provides an efficient path to

10   connect the end of the wordline 222 to the model core cell 203', which is now arranged at the top-leftmost side of the memory core 200. As shown, the model bitlines 230 and /230 are interconnecting a set core cells 202' that lead to the model core cell 203'. In operation, when the control circuitry 210 provides a wordline enable signal with a rising edge of the signal 216 to the model wordline driver 206', the RC delay is computed for only about the path traversed

15   by the wordline 222 and the differential bitlines 230 and /230, that lead to the model sense amplifier 204'.

At that point, the model sense signal 214 is provided to the control circuitry 210. When the control circuitry 210 receives the signal 214, the control circuitry 210 will pass the falling edge of the ready to read signal 216 to the selected sense amplifiers 204. It is

20   important to note that the self-timing architecture of the present invention provides a standard delay to be used by all of the core cells 202 and core cell 203 of the memory core 200. Further, the standard delay is preferably no worse than the RC delay for the worst case scenario of reading the core cell 203.

Figure 2B shows another arrangement for the folded wordline 220' in accordance with

an alternative embodiment of the present invention. As shown, the folded wordline 220' is

arranged at a 90 degree angle compared to the folded wordline 220 of Figure 2A. This

embodiment illustrates that the folded wordline 220' may be arranged in any manner that

5   makes layout more suitable for a particular design, and need not be arranged in one horizontal

orientation. For example, Figure 2C shows yet another orientation for a folded wordline

220''. In this example, the folded wordline 220'' is laid out in an arrangement that would

possibly make laying-out other miscellaneous logic more feasible in a particular integrated

circuit design.

10   It should therefore be understood that the manner in which the folded wordline is

arranged is not important, so long as the folded wordline provides a termination path of the

wordline 222 substantially near the output of the model wordline driver 206'. When this is

properly arranged, no excess RC delay is introduced in the self-timing path. Therefore, only

the representative RC delay of the model wordline 222 and the model bitlines 230 and /230

15   are used by the control circuitry 210 to determine that a ready-to-read signal 216 should be

provided to the given sense amplifiers 204.

Figure 3 shows an example of a model core cell 203' in accordance with one

embodiment of the present invention. In this embodiment, a wordline 226 is shown as a line

that does not interconnect with the model core cell 203', but leads directly into the core cells

20   202 that lie within the memory core 200. However, the model wordline 222 is shown coupled

to a gate of transistors 302 and 304. Also shown is the model bitline 230 which is connected

to a terminal of transistor 304, and the complementary model bitline /230 that is connected

to a terminal of transistor 302. Further, signal 216 is provided by the control circuitry 210 to a

gate of a transistor 306. In general, the model core cell 203' is configured to perform a pull-

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down operation, which is configured to approximate the pull down strength of a core cell 202 that lies within the memory core 200.

In another embodiment, the model core cell 203' may be finely tuned to increase its pull-down drive depending on the depth of a particular memory core 200. For example, the

5   model core cell 203' may be replaced by more than one model core cells to produce increased pull down strength, which may be useful to eliminate any delays that may be introduced by the control circuitry 210 or delays associated with driving larger memory cores.

Figure 4 is an example of a model wordline driver 206' as shown in Figure 2A above in accordance with one embodiment of the present invention. The model wordline driver 206'

10   is shown including a pre-charge circuit 402 that is coupled to the model bitlines 230 and /230, and the signal 216. Also shown is a buffer 404 that receives the signal 216 and outputs a buffered signal onto the model wordline 222. In general, when signal 216 goes HI (*i.e.*, experiences a rising edge), the model wordline driver 206' is triggered to commence an access operation. Further, the buffer 404 is provided with sufficient delay to approximate the delay

15   that will be experienced through a wordline drivers 206 that accesses the memory core 200, as shown in Figure 2A above.

Figure 5A shows an example of a core cell 202 and 203 that lie in the memory core 200 in accordance with one embodiment of the present invention. As shown, the complimentary bitlines 229 and /229 are coupled to drain terminals of a pair of pass gate

20   transistors 502 and 504, respectively. The wordline 226 is shown coupled to the gate of the pass gate transistors 502 and 504. Although one exemplary core cell 202/203 is shown, it should be understood that the embodiments of the present invention are applicable to other core cells and other memory circuits.

Thus, the embodiment of the present invention may be applied to any number of memory circuits, such as ROM memory circuits, RAM memory circuits, SRAM memory circuits, DRAM memory circuits, EPROM memory circuits, EEPROM memory circuits, etc. For more information on memory circuits and core cells, reference may be made to a book

5   entitled "The Art of Electronics, 2nd Edition," by Paul Horowitz and Winfield Hill, pages 812-820 (1996). This book is hereby incorporated by reference.

Figure 5B shows an example of a core cell 202' which is laid out along the model bitline in accordance with one embodiment of the present invention. As shown, bitline 230 is coupled to a drain terminal of a pass gate transistor 502', and bitline /230 is coupled to a drain

10   terminal of a pass gate transistor 504'. In this embodiment, the gate of each of the pass gate transistors 502' and 504' are coupled to ground. Each of the core cells 202' are generally dummy core cells that are used to approximate the RC delay experienced on the bitlines 229' of the memory core 200.

Figure 5C shows an example of a core cell 202'' which is laid out along the model

15   wordline 222 in accordance with one embodiment of the present invention. As shown, a drain terminal of a pass gate transistor 502'' is coupled to Vdd, and a drain terminal of a pass gate transistor 504'' is coupled to Vdd. In this embodiment, the gate of each of the pass gate transistors 502'' and 504'' are coupled to the model wordline 222. Each of the core cells 202'' are also generally dummy core cells that are used to approximate the RC delay

20   experienced on the wordline 226 of the memory core 200.

Figure 6 is an example circuit diagram of the control circuitry 210 of Figure 2A in accordance with one embodiment of the present invention. The control circuitry 210 generally includes a model sense amplifier 204', and SET and RESET latch circuitry 606. The SET and RESET latch circuitry 606 generally includes a transistor 623 that is used for

receiving a reset (/R) signal, a transistor 624 which is used for receiving a SET (S) signal from

a clock (CLK) 602. The SET and RESET latch circuitry 606 also includes a transistor 622

that has its gate coupled to the output of a buffer 603, and the buffer 603 has an input 604

(*i.e.*, which is a delay of CLK 602).

5   Further included in the SET and RESET latch circuitry 606 is a latch 624 and an

inverter 628 that produces the signal 216. Also shown is a reset signal which is

communicated to a gate of a transistor 620 and a gate of a transistor 621. In this example,

bitline 230 is coupled to the model sense amplifier 204', which is shown to be an inverter

circuit. The output of the model sense amplifier 204' is then coupled to an inverter 618.

10   Generally, the reset signal is communicated after a falling edge of the signal 216 is received.

As mentioned above, when signal 216 goes LOW (*i.e.*, a falling edge), the sense amplifier is

provided with a ready-to-read signal. On the other hand, when signal 216 goes HI, a wordline

driver is signaled to access a particular cell.

          Figure 7 shows a model path and read timing diagram 700 in accordance with one

15   embodiment of the present invention. Initially, when a memory clock (CLK) signal

experiences a rising edge 702, the signal 216 is caused to produce a rising edge 704. The

rising edge 704 of signal 216 therefore causes all addressed wordlines (including the model

wordline), to experience a rising edge 706. The rising edge 706 then causes the model bitline

230 to produce a falling edge 708. The falling edge 708 then causes a falling edge 710 in the

20   signal 216. The falling edge 710 also acts to shut down the wordlines and model wordlines,

open up the input latches, and pre-charges the bitline and data buses.

          Further, as mentioned above, when signal 216 experiences the falling edge 710, the

sense amplifier 204 will be directed to begin a read, and therefore, cause the rising edge 712

on the sense line. More specifically, the falling edge 710 also produces a falling edge 709 for

all of the address wordlines (including the model wordline), and a rising edge 711 in the bitline 230. In addition, the rising edge 712 of the sense signal will cause an edge 714 in an output "Q" reflecting the value of the sensed data, in this case a logical "1". It is important to note that the rising edge 712 will occur almost simultaneously when just enough bitline differential 730 has been achieved for the worst case core cell 203.

In fact, because the RC delay of the self-timing return path 114 of the prior art has been eliminated, the time in which the worst case core cell 203 reaches enough bitline differential is substantially the same as when the model core cell 203' has reached enough bitline differential. Advantageously, a memory circuit will be able to perform access operations at very high speeds because unnecessary delays have been eliminated.

Although the foregoing invention has been described in some detail for purposes of clarity of understanding, it will be apparent that certain changes and modifications may be practiced within the scope of the appended claims. It should therefore be understood that the various circuit diagrams may be embodied in any form which may include, for example, any suitable semiconductor substrate, printed circuit board, packaged integrated circuit, or software implementation.

By way of example, hardware description language (HDL) design and synthesis programs, such as, VHDL® hardware description language available from IEEE of New York, New York may be implemented to design the silicon-level layouts. Accordingly, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope and equivalents of the appended claims.

What is claimed is:

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CLAIMS

1.   A memory circuit, comprising:

a memory core having an array of core cells, the array of core cells being coupled to a

5   plurality of wordlines and a plurality of bitline pairs; and

a self-timing path having a model core cell that is coupled to a model wordline that is

driven by a model wordline driver, the self-timing path further including a model sense

amplifier that couples to the model core cell through a pair of model bitlines, the model

wordline and the pair of model bitlines are each coupled to a plurality of dummy core cells to

10   approximate an RC delay of a worst case core cell of the array of core cells; and the model

wordline is a folded wordline such that the model wordline has a termination at a location that

is proximate to the model wordline driver.

2.   A memory circuit as recited in claim 1, wherein the model core cell is coupled

15   to the termination of the model wordline at the location that is proximate to the model

wordline driver.

3.   A memory circuit as recited in claim 2, further comprising:

a control circuit that is configured to activate the self-timing path, the control circuit is

20   coupled to the model sense amplifier that couples to the model core cell through a pair of

model bitlines.

4.   A memory circuit as recited in claim 3, wherein the control circuit is configured to communicate a wordline enable signal to the model wordline driver to activate the self-timing path, such that the model wordline driver performs an access to the model core cell through the folded wordline.

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5.   A memory circuit as recited in claim 4, wherein the control circuit produces a ready to read signal that is communicated to a sense amplifier of the memory core.

6.   A memory circuit as recited in claim 5, wherein the control circuit produces the
10   ready to read signal upon receiving a self-timing path RC delay of the model wordline and the pair of model bitlines is communicated to the control circuit.

7.   A memory circuit as recited in claim 6, wherein the self-timing path RC delay is substantially equal to the RC delay of the worst case core cell.

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8.   A memory circuit as recited in claim 7, wherein the worst case core cell is the furthest one of the array of core cells from a wordline driver and the sense amplifier of the memory core.

20   9.   A memory circuit as recited in claim 1, further including:

a plurality of wordline drivers being coupled to the plurality of wordlines; and

a plurality of sense amplifiers being coupled to the plurality of bitline pairs.

10.   A memory circuit as recited in claim 2, wherein a control circuit is coupled to each of the plurality of wordline drivers and each of the plurality of sense amplifiers that are coupled to the array of core cells.

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11.   A memory circuit as recited in claim 1, wherein the memory circuit is selected from the group consisting of a ROM circuit, a RAM circuit, an SRAM circuit, a DRAM circuit, an EPROM circuit, an EEPROM circuit.

10   12.   A method for making a memory circuit with a self-timing path, comprising the acts of:

providing a memory core having an array of core cells;

integrating a self-timing path of core cells along a model wordline and along a model pair of bitlines, the model wordline is folded such that a model core cell is placed

15   substantially at a beginning point of the model wordline, and an ending point of the model wordline is coupled to the model core cell.

13.   A method for making a memory circuit with a self-timing path as recited in claim 12, further comprising the act of:

20   communicating a ready to read signal to a sense amplifier of the memory core after an RC delay signal indicating that an RC delay along the model wordline and an RC delay along the model pair of bitlines is complete.

14.   A method for making a memory circuit with a self-timing path as recited in claim 13, wherein a falling edge of the ready to read signal triggers the sense amplifier of the memory core.

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15.   A method for making a memory circuit with a self-timing path as recited in claim 14, wherein a rising edge of the ready to read signal triggers a model wordline driver that is coupled to the model wordline at the beginning point of the model wordline.

10   16.   A method for making a memory circuit with a self-timing path as recited in claim 15, wherein the memory circuit is selected from the group consisting of a ROM circuit, a RAM circuit, an SRAM circuit, a DRAM circuit, an EPROM circuit, an EEPROM circuit.

17.   A memory generator for producing a memory circuit that includes a self-timing

15   path, the memory circuit includes a memory core with an array of core cells, comprising:

generating a self-timing path of core cells along a model wordline and along a model pair of bitlines, the model wordline is folded such that a model core cell is placed substantially at a beginning point of the model wordline, and an ending point of the model wordline is coupled to the model core cell.

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18.   A memory generator for producing a memory circuit as recited in claim 17, wherein the model pair of bitlines are arranged along a side of the memory core that is adjacent to a plurality of wordline drivers.

19.   A memory generator for producing a memory circuit as recited in claim 18, wherein a model wordline driver is aligned next to the plurality of wordline drivers, and the model wordline driver is placed next to the model core cell.

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20   A memory generator for producing a memory circuit as recited in claim 19, wherein a control circuit is configured to receive a combined RC delay of the model wordline and the model pair of bitlines without a return path RC delay.

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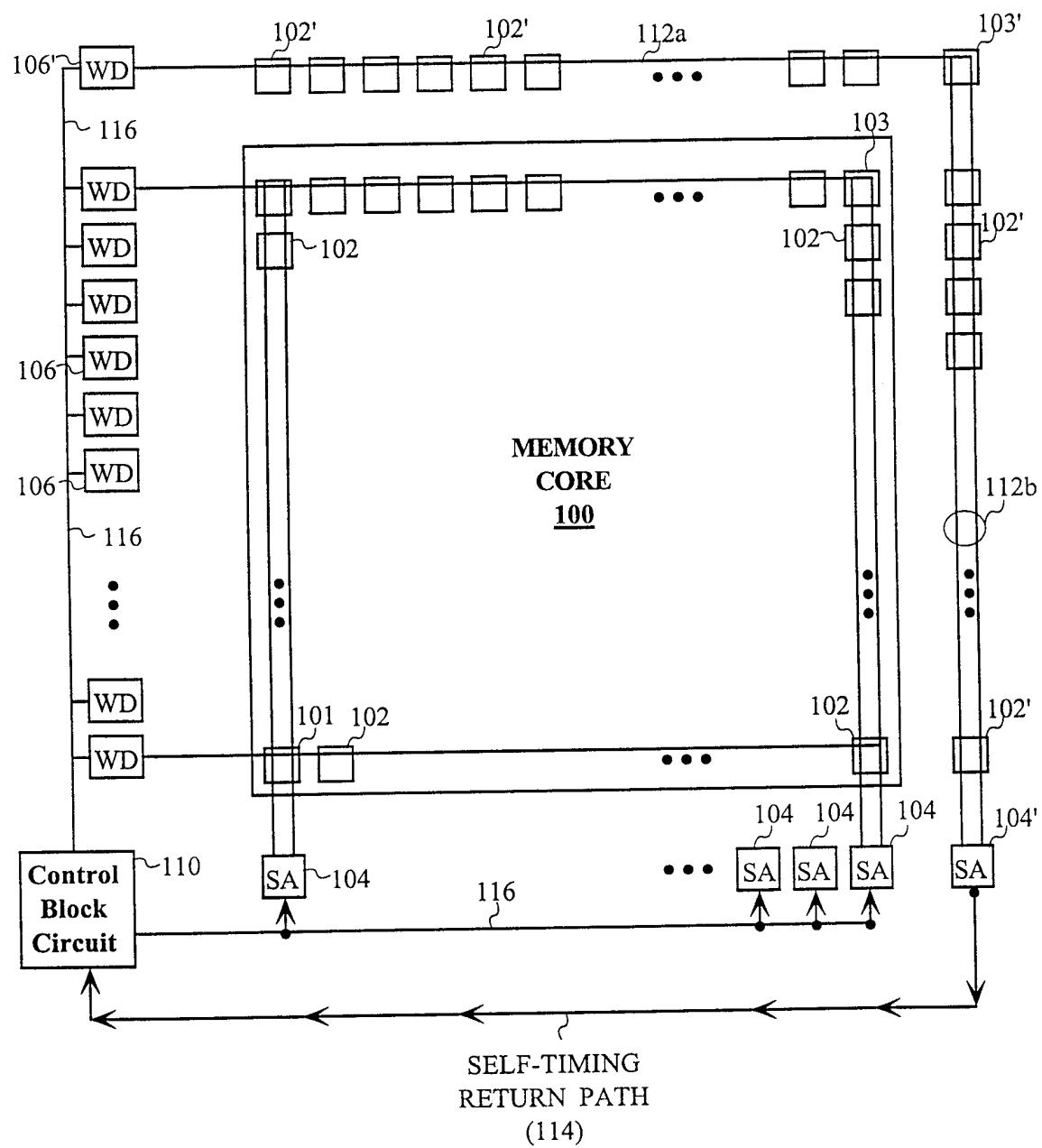
FIG. 1
(prior art)
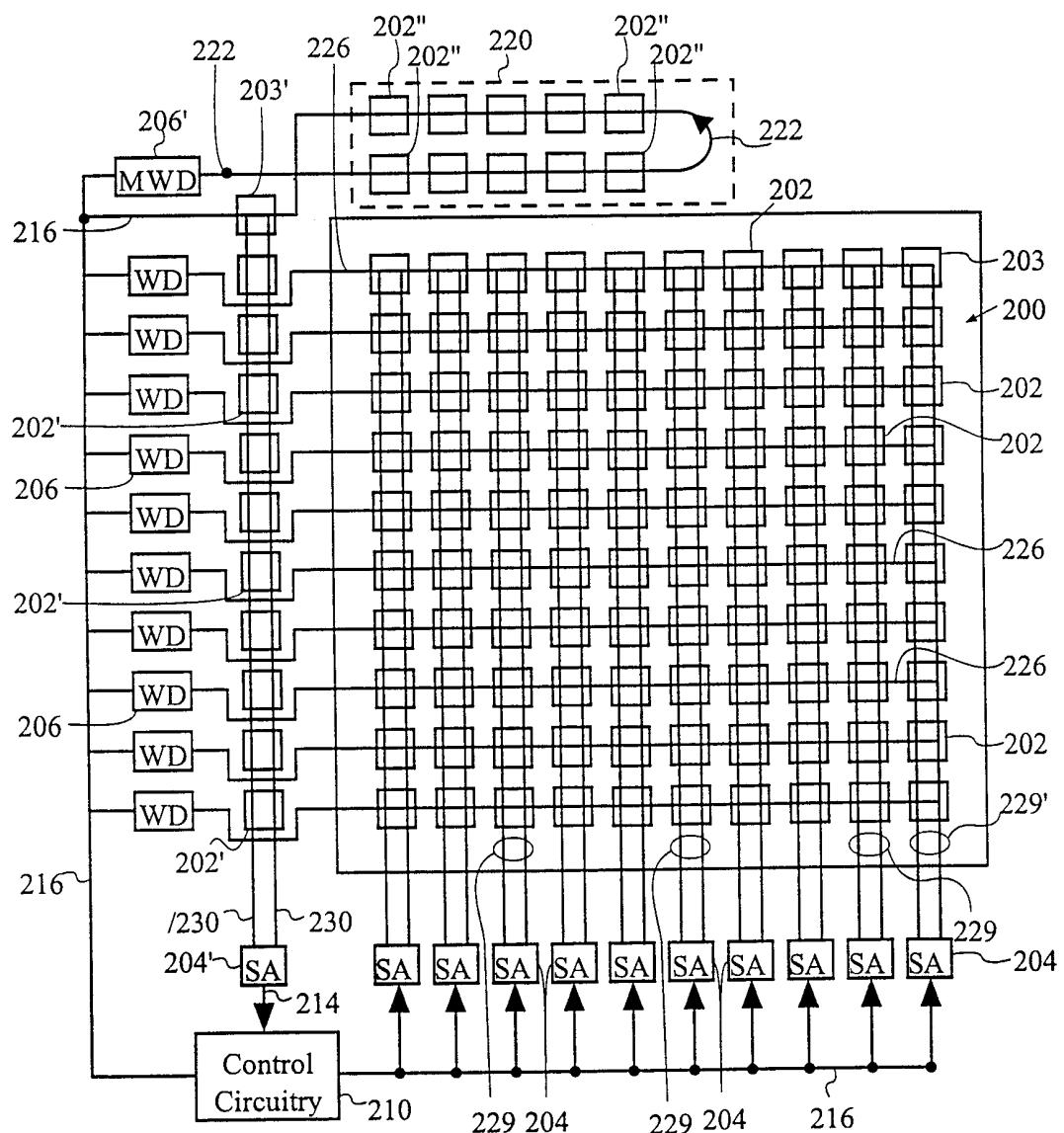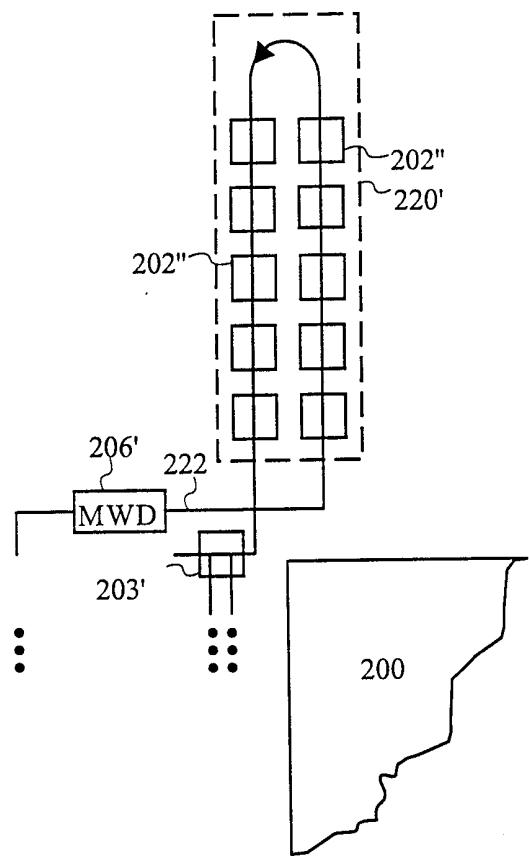
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FIG. 2A

FIG. 2B

FIG. 2C

4/10

203'

230
304

306

216

222

302
/230

226

226

FIG. 3

206'

402

/230

216

230

404

216

222

FIG. 4

202 / 203

229

/229

502

504

226

226

FIG. 5A

7/10

FIG. 5B

202"

Vdd

502"

Vdd

504"

222   222

FIG. 5C

9/10
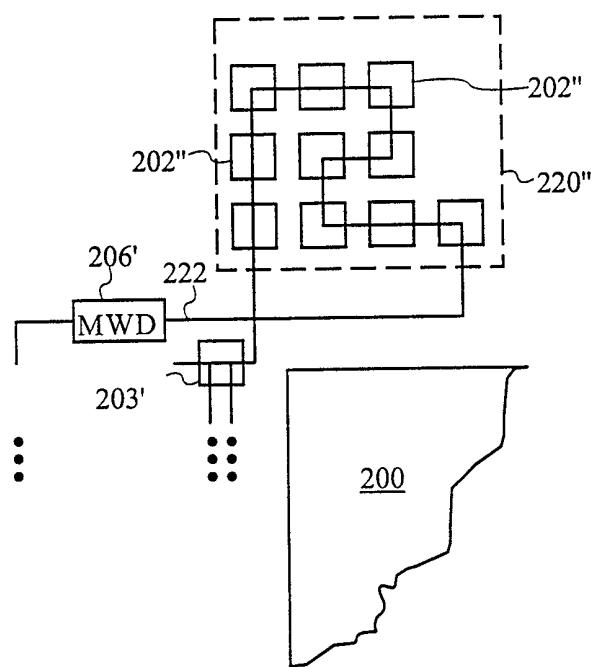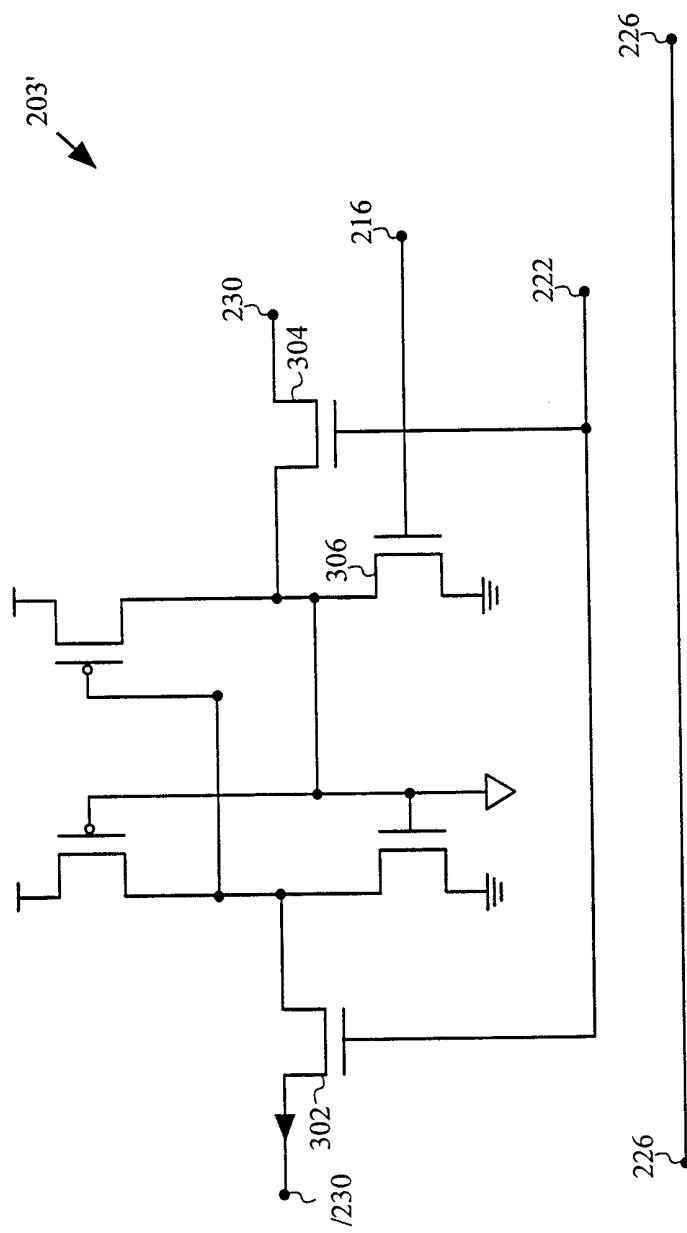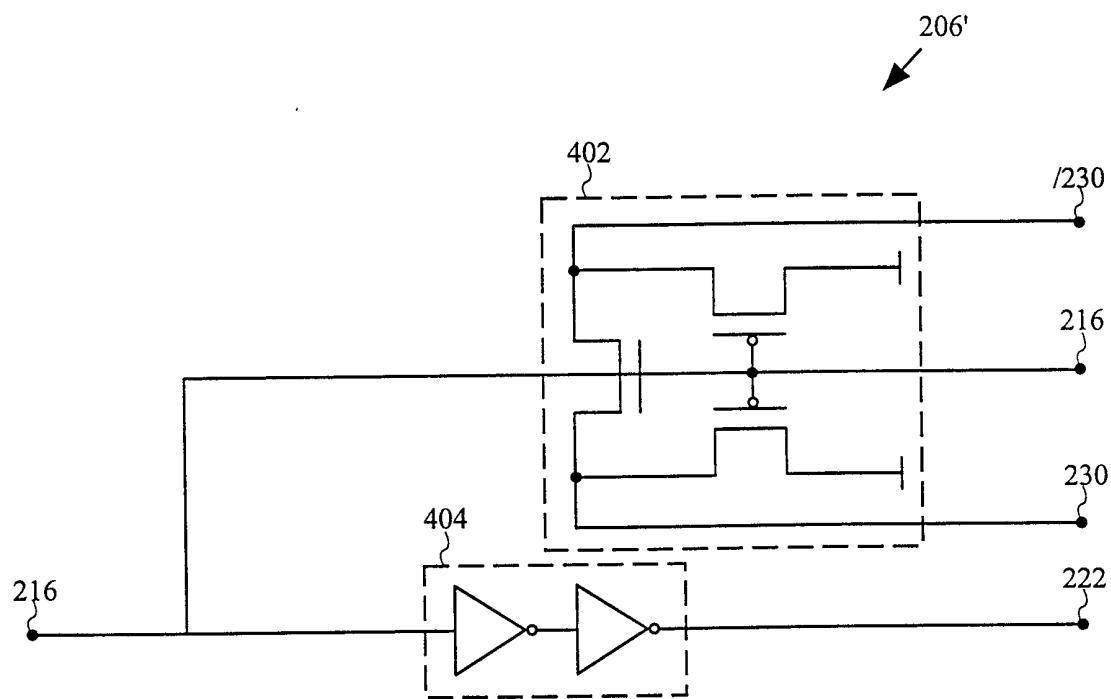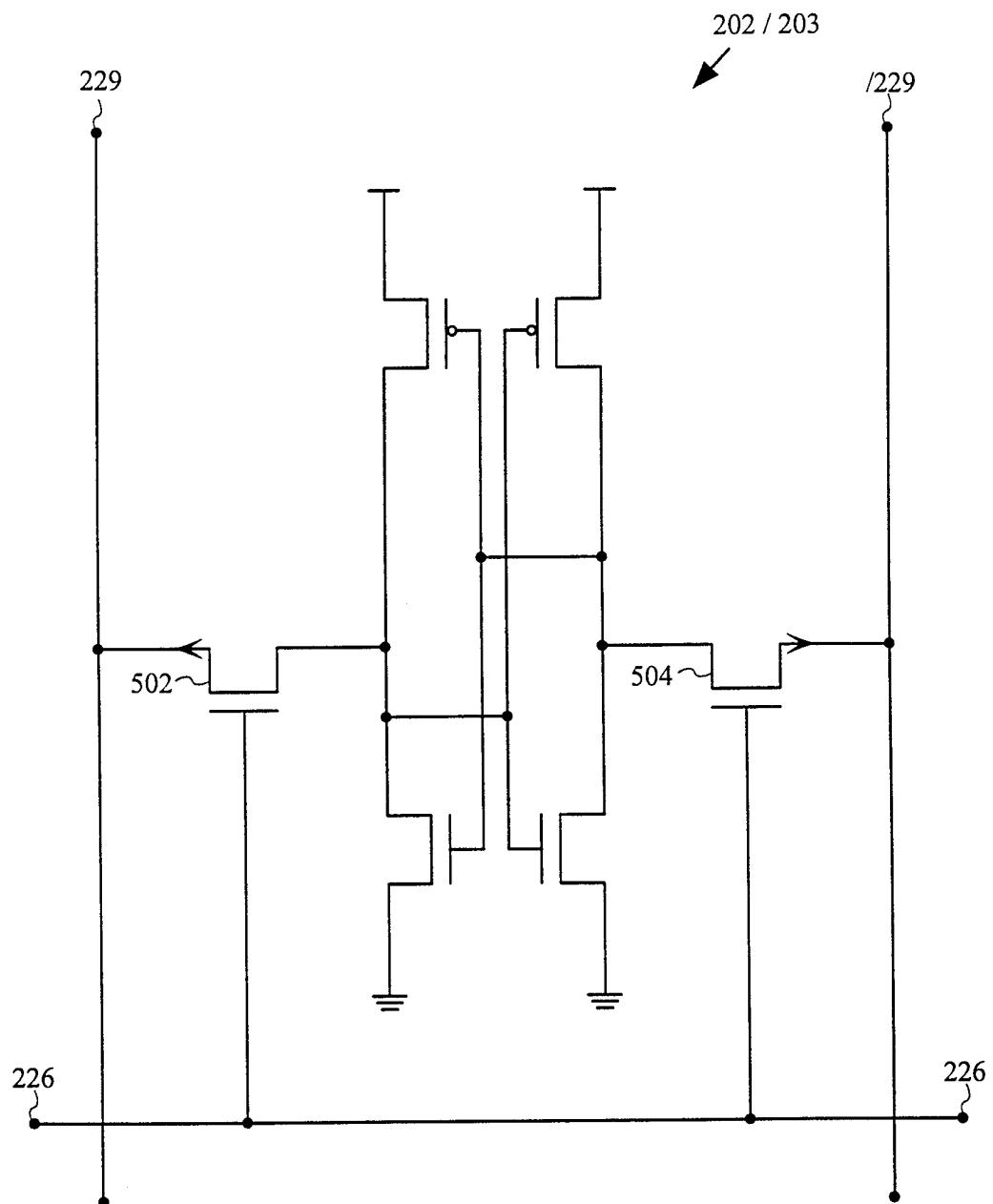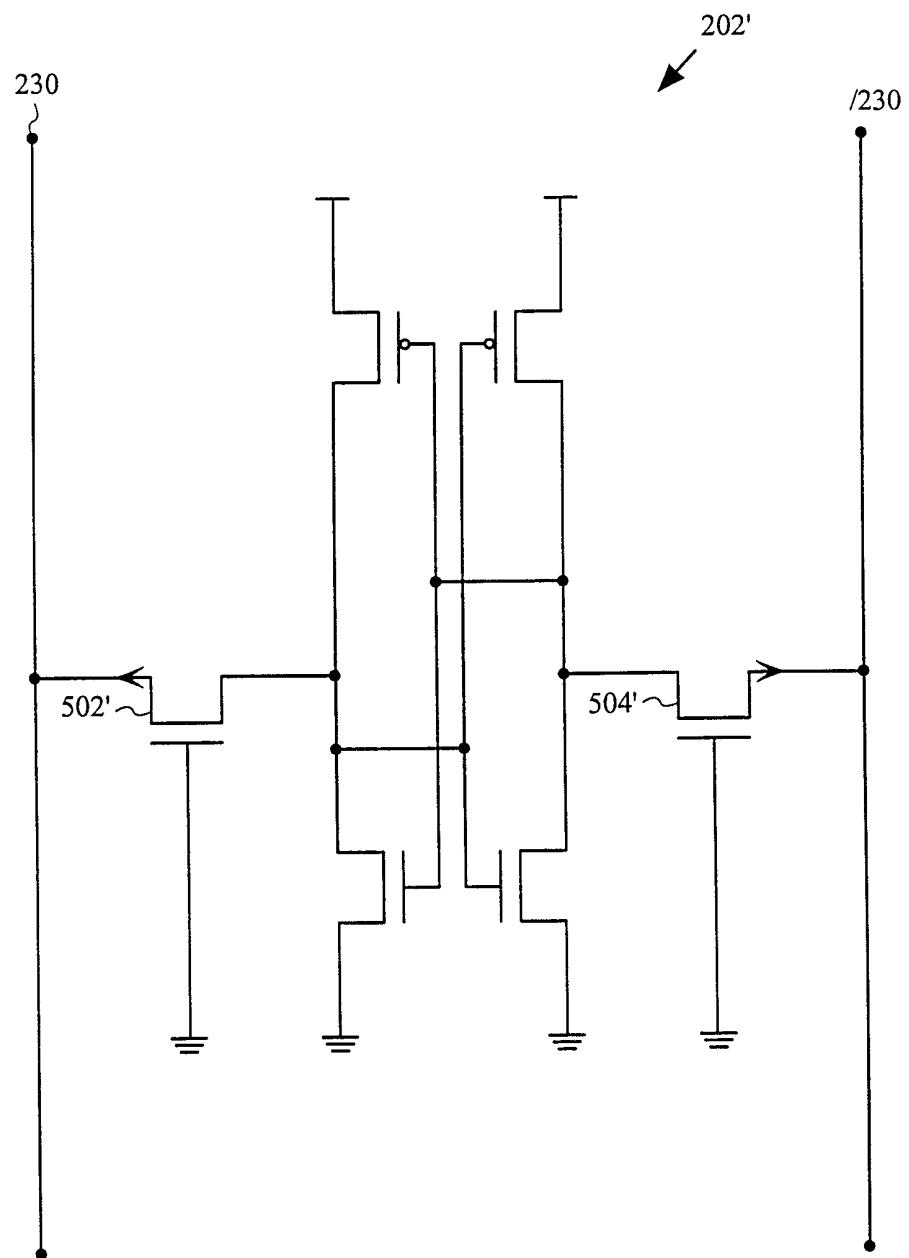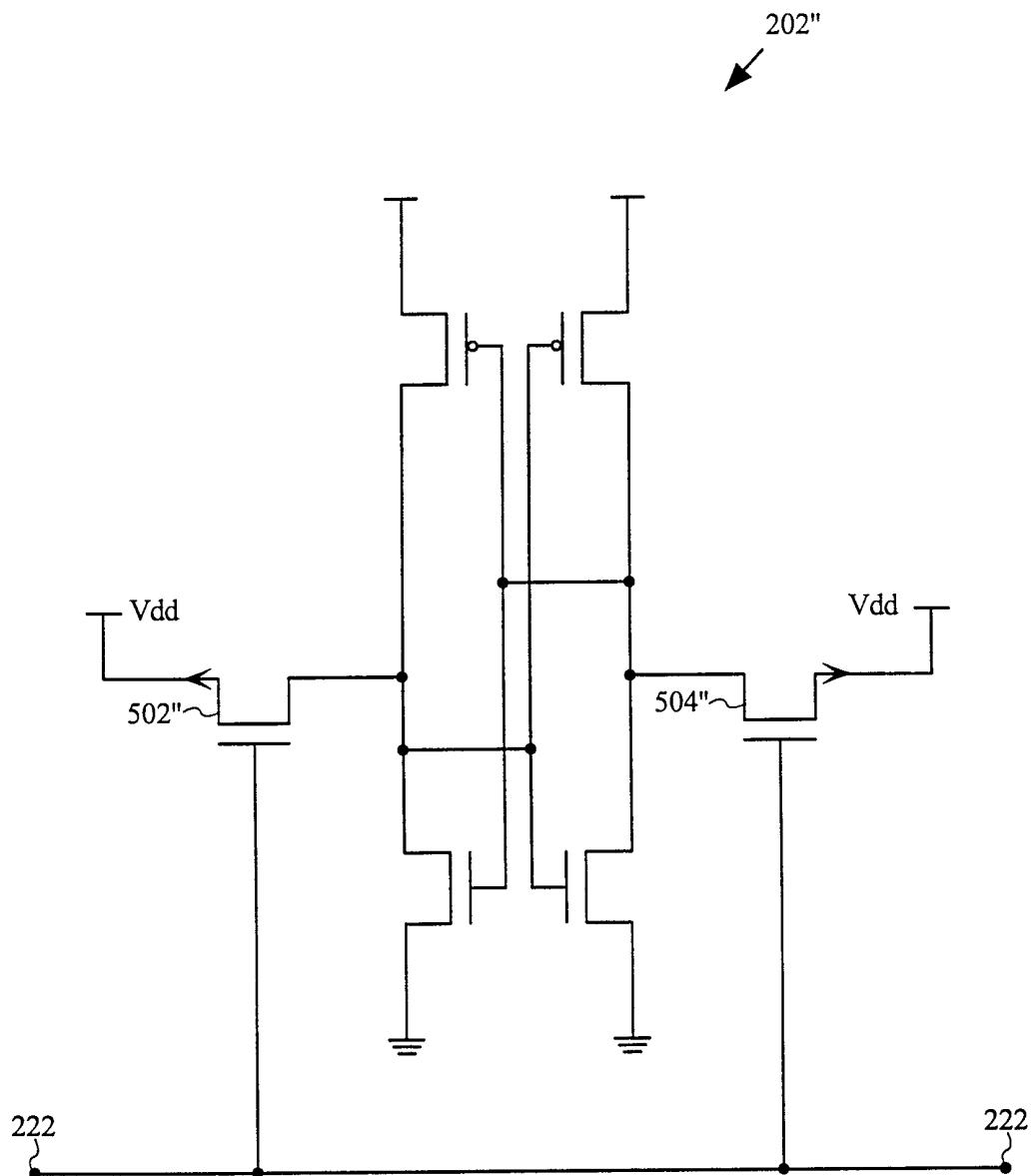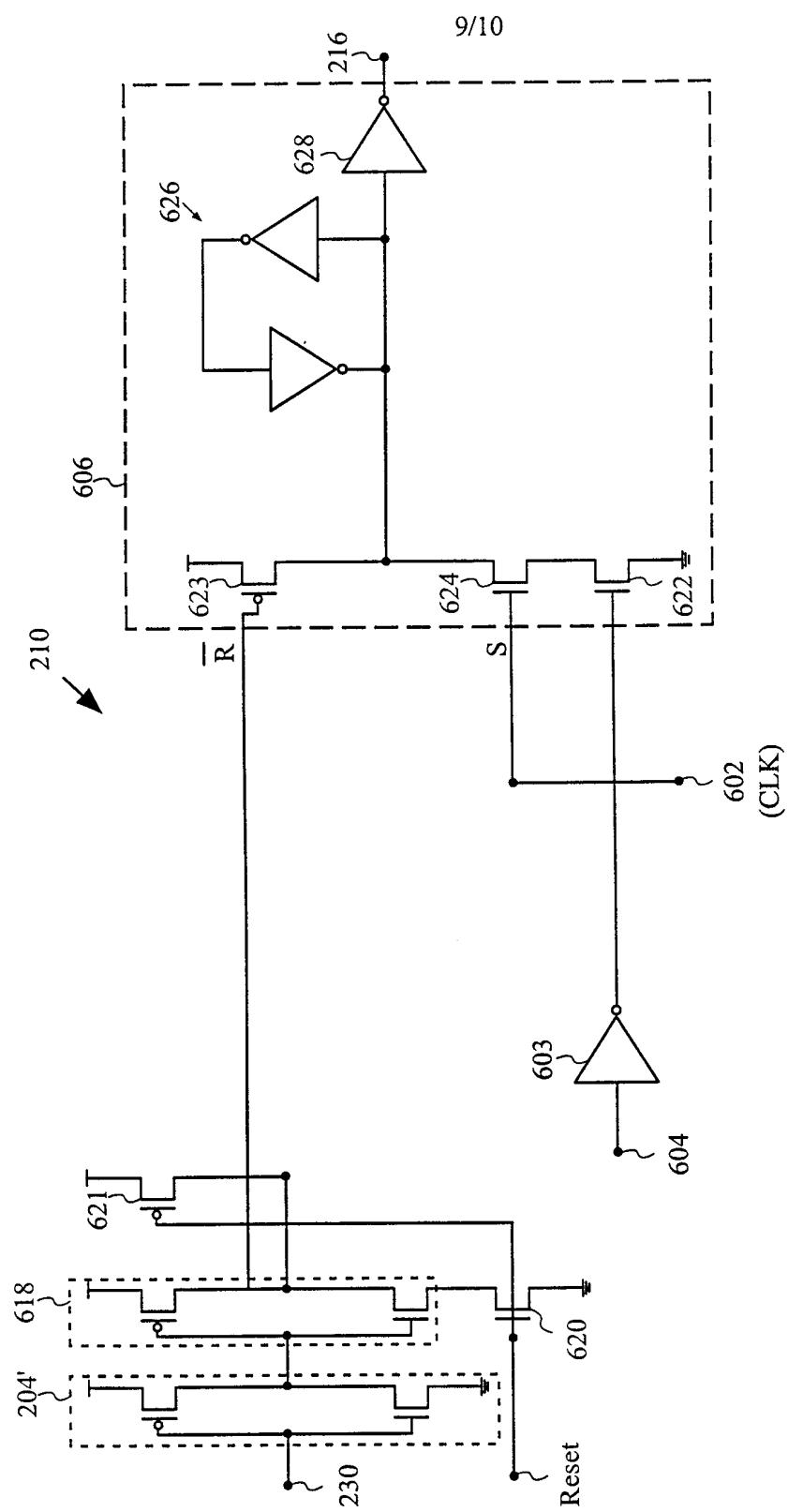
FIG. 6

Model Path and Read Timing
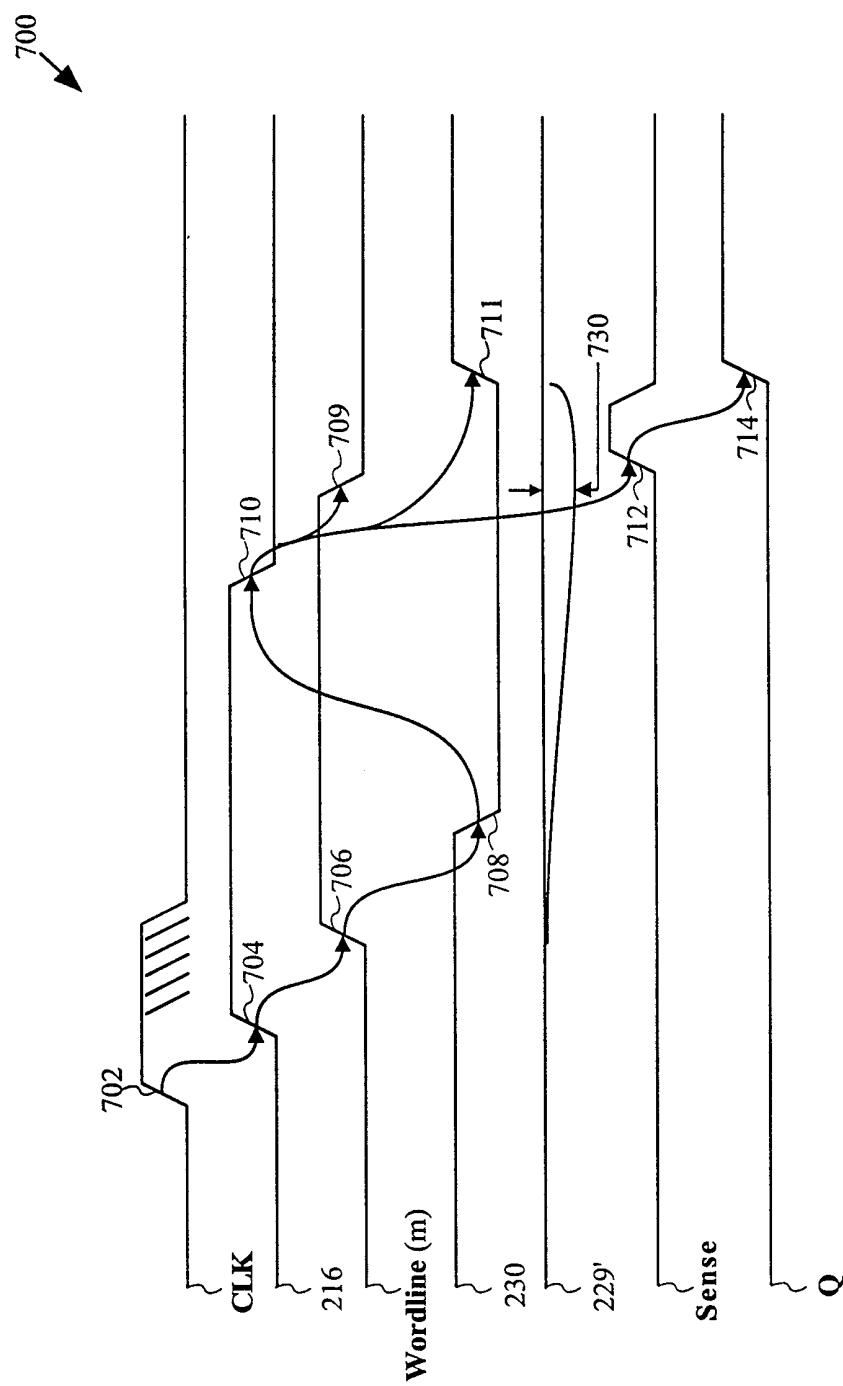

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/21939

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :G11C 7/02
US CL :365/210, 233, 194, 51
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
U.S. : 365/210, 233, 194, 51

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS (memory, storage, self-timing, model cell, delay)

C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5,270,590 A (PASCUCCI) 14 December 1993 (14/12/93), see entire document.	None
A, P	US 5,751,649 A (KORNACHUK ET AL) 12 May 1998 (12/05/98), see entire document.	None
A, E	US 5,844,851 A (PASCUCCI ET AL) 01 December 1998 (01/12/98), see entire document.	None

☐ Further documents are listed in the continuation of Box C.   ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance		
"E"	earlier document published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)		
		"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed	"&"	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 FEBRUARY 1999	3 0 MAR 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	Authorized officer ANDREW Q. TRAN
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Form PCT/ISA/210 (second sheet)(July 1992)*