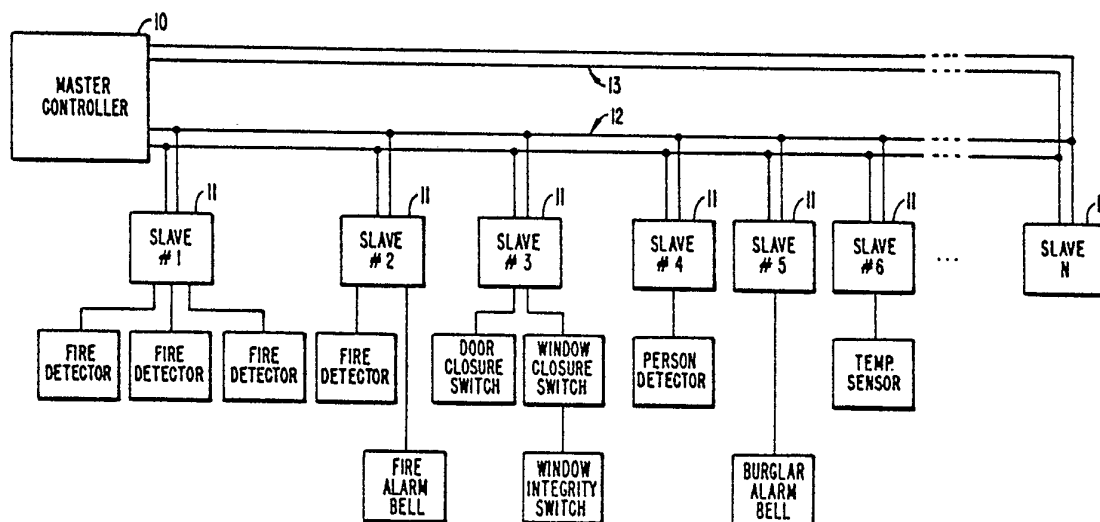




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁴ : G08B 25/00, 26/00, H04Q 9/00	A1	(11) International Publication Number: WO 87/ 03405 (43) International Publication Date: 4 June 1987 (04.06.87)
(21) International Application Number: PCT/US86/02559 (22) International Filing Date: 26 November 1986 (26.11.86) (31) Priority Application Number: 801,979 (32) Priority Date: 26 November 1985 (26.11.85) (33) Priority Country: US (71) Applicant: SENSOR SCAN, INC. [US/US]; 2255 Mor- ello, Pleasant Hill, CA 94523 (US). (72) Inventors: ZINNERT, Alan, Paul ; 319 Manley Road, Ripon, CA 95366 (US). IVASHIN, Victor, S. ; 142 Aoria Drive, Pleasant Hill, CA 94523 (US). (74) Agent: ARONSON, Elliot, B.; Townsend and Town- send, One Market Plaza, 2000 Steuart Tower, San Francisco, CA 94105 (US).		(81) Designated States: AT (European patent), BE (Euro- pean patent), CH (European patent), DE (European patent), FR (European patent), GB (European pa- tent), IT (European patent), JP, LU (European pa- tent), NL (European patent), SE (European patent). Published <i>With international search report.</i>

(54) Title: COMMUNICATIONS TECHNIQUE FOR A SUPERVISORY CONTROL SYSTEM



(57) Abstract

An alarm system with a master controller (10) includes a master processor and a transmitter unit responsive to that processor for providing a voltage signal that includes a data component and an uninterrupted DC voltage power component. The DC power component has a magnitude sufficient to power all of the devices operatively associated with the various slave controllers (11) connected to a twisted pair of wires (12 and 13). The transmitting unit is appropriately connected to communicate the voltage signal to the twisted pair. Each slave controller (11) includes voltage demodulation units for receiving the voltage signal and for deriving therefrom the data component and the uninterrupted DC voltage power component. Each slave controller includes a current modulation device connected to the twisted pair for modulating the current therein and responsive to an on-board slave processor so as to find a data signal for communication to the master controller. The master controller (10) in turn includes a current demodulation device for receiving the modulated current on the twisted pair and providing a data signal to the master processor.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	FR	France	ML	Mali
AU	Australia	GA	Gabon	MR	Mauritania
BB	Barbados	GB	United Kingdom	MW	Malawi
BE	Belgium	HU	Hungary	NL	Netherlands
BG	Bulgaria	IT	Italy	NO	Norway
BJ	Benin	JP	Japan	RO	Romania
BR	Brazil	KP	Democratic People's Republic of Korea	SD	Sudan
CF	Central African Republic	KR	Republic of Korea	SE	Sweden
CG	Congo	LI	Liechtenstein	SN	Senegal
CH	Switzerland	LK	Sri Lanka	SU	Soviet Union
CM	Cameroon	LU	Luxembourg	TD	Chad
DE	Germany, Federal Republic of	MC	Monaco	TG	Togo
DK	Denmark	MG	Madagascar	US	United States of America
FI	Finland				

COMMUNICATIONS TECHNIQUE FOR
A SUPERVISORY CONTROL SYSTEM

5 BACKGROUND OF THE INVENTION

The invention relates to supervisory systems such as used with burglar or fire alarms or with remote sensors for sensing such parameters as humidity or temperature.

10 A supervisory system is a system for monitoring and controlling the operation and function of a number of devices and/or sensors typically at a plurality of remote locations. The system includes a central, master controller, which is in communication with
15 a plurality of slave controllers, at each of the remote locations. Each slave controller will monitor and control one or more devices. For example, in a burglar alarm system a slave controller at a particular location may monitor a number of window and door closure
20 sensors and operate an associated burglar alarm. In a fire alarm system, a slave controller monitors a number of fire or smoke detectors and makes an appropriate response when a detector is tripped. For example, the slave controller can respond by activating a traditional
25 fire alarm bell or it can send a signal to a central station or activate a telephone autodialer for contacting the local fire department.

Systems operating on the same principle are also used to monitor environmental parameters such as
30 temperature and humidity sometimes with associated alarms when the environmental parameters vary beyond tolerable limits.

Known supervisory systems include a two-way communications network between the master controller
35 and the remote, slave controllers. The master controller is able to send signals to the slaves for a variety

of purposes. For example, the master controller may want to shut down the alarm system at a remote location during normal business hours and then automatically
5 power up the alarm system upon an appropriate signal after closing. A master controller may also want to signal a remote slave to activate a relay on a local device under the supervision of the slave. The slaves, on the other hand, generally need to communicate with
10 the master controller to signal alarm conditions or to send monitored parameter readings back to the master for storage and/or interpretation.

The supervisory system also needs a network of power lines from the master controller to the slave
15 to supply power for operating the slaves themselves and/or for powering devices which are connected to the slaves.

Supervisory systems are known which use separate lines for power and for communications. This is
20 wasteful simply because it requires twice as much wire to be strung and at least two independent control networks. It is also wasteful because existing unsupervised alarm systems, which typically run a single twisted pair of wires between the various sensors,
25 alarms, and control devices, cannot readily be converted to a supervised system without rewiring the whole network.

Other supervisory systems are known which use the same lines for both communications and for supply-
30 ing power. Some such systems send low-frequency AC power and high-frequency data signals down the same line. These systems are subject to transmission line losses, which limits the size of the network and the distance between remote slaves which can be serviced by
35 single master controller. In addition, many devices require a DC power source for operation, so that these systems must have additional AC to DC conversion and regulation units.

Other supervisory systems are known which supply DC power over the same lines used for communications. Systems operating on this principle interrupt the power supply, for example, for periods on the order of milliseconds during which a data signal is sent. Such power interrupts can interfere with proper functioning of alarm systems and many devices. These systems must be used with special filtering circuits, which attempt to mask the power interrupts and minimize their effect. Such systems are also limited in the amount of power which they can supply. Special low-power devices, which draw extremely low currents, must be designed and manufactured for use with such systems.

SUMMARY OF THE INVENTION

The present invention provides a supervisory system including a master controller and a plurality of slave controllers, which provides continuous, uninterrupted DC power along a single twisted pair of wires to all the slave controllers and at the same time provides for two-way communications between the master and slaves over the same twisted pair without the interruption of power characteristic of the prior art.

According to the invention, the slave controllers are connected to the master controller by a single twisted pair of wires. The master controller includes a master processor and a transmit means responsive to that processor for providing a voltage signal comprised of the data component and an uninterrupted DC voltage power component. The DC power component has a magnitude sufficient to power all of the devices operatively associated with the various slave controllers connected to the pair of wires. The transmitting means is appropriately connected to communicate the voltage signal to the twisted pair. Each slave controller includes a voltage demodulation means for

receiving the voltage signal and for deriving therefrom the data component and the uninterrupted DC voltage power component. The power component may be used for
5 powering the slave controller itself and/or any devices associated with the slave controller. Thus, the master controller communicates to the slave controllers by sending a voltage-modulated signal along the twisted pair, the modulation varying, for example, between 12
10 volts and 14 volts.

The slave controllers communicate with the master controller by a current modulated signal. Each slave controller includes current modulation means connected to the twisted pair for modulating the current
15 therein and responsive to an on-board slave processor so as to find a data signal for communication to the master controller. The master controller in turn includes current demodulation means for receiving the modulated current on the twisted pair and providing a
20 data signal to the master processor.

Other features and advantages of the present invention will be evident by reference to the following portions of the specification and the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

25 Figure 1 is an overall block diagram showing a particular arrangement of master and slave controllers in a supervisory system of the present invention.

Figure 2 is a functional block diagram of a portion of the master controller showing a means for
30 communicating with the slave controllers according to the invention.

Figure 3 is a functional block diagram of a slave controller.

35 Figure 4 is a block schematic diagram of an embodiment of the master controller showing digital circuitry and analog functional block.

Figure 5 is a schematic of an implementation of analog circuitry for the master controller.

Figure 6 is a schematic diagram of an implementation of analog circuitry for the slave controller.

Figure 7 is a schematic diagram of an alarm bell supervision circuit for use with the analog implementation of Figure 6.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

10 A. System Overview

Figure 1 shows an overall view of an illustrative configuration of a supervisory system. The system includes a master controller 10 and a plurality of slave controllers 11 which are connected in parallel to the master controller by communication line 12. In the present system the line 12 need consist of only a single pair of wires, sometimes referred to as a "twisted pair." In an actual installation in the field it may be convenient to bundle the twisted pair 12 with other lines for other purposes; however, for proper operation of the present invention only a single twisted pair is needed.

As explained more fully below, the line 12 is used both to provide two-way communications between the master and slave controllers and to deliver DC power to the slave controllers for operation of the slaves themselves and of any controlled devices. Thus, when line 12 is referred to as a communications line, "communications" is used in the broad sense to encompass the communication of both power and information, and no limitation to only data communications is intended.

For proper operation of the system a single twisted pair 12 is sufficient to define a communications loop and is all that is needed to define a minimal configuration of the present invention. However, for reasons explained below, a preferred embodiment

also includes a return loop 13 consisting of a second pair of wires.

5 A feature of the present system is its great flexibility in the number of system configurations which can be accommodated. For purposes of illustration, Figure 1 shows one such configuration based upon a room having a fire alarm system, a burglar alarm system, and a system for monitoring the room temperature. A configuration like this might be used, for
10 example, in connection with a high-security air-conditioned room containing a mainframe computer, which for proper operation is to be maintained within fixed temperature limits.

15 As illustrated in Figure 1, the first two slave controllers are dedicated to the fire alarm subsystem. Slave No. 1 communicates with three fire detection units at three separate inputs. Suitable fire detection units for the use with the present system,
20 such as smoke detectors or heat detectors, are commercially available. Slave No. 2 communicates with a fourth fire detection unit and a fire alarm bell, which is activated under command from the master controller
10 when one of the fire detection units has been
25 tripped, as will be explained below. Slave Nos. 3-5 comprise the burglar alarm subsystem. Slave No. 3 is connected to a door closure switch for detecting when the door to the room has been opened. At a parallel input slave No. 3 is connected to a window closure
30 switch for detecting when a window has been opened and in series to a window integrity switch, such as a strip of metallic tape adhered to the window pane, for detecting when the window has been broken. Slave No. 4 is connected to a person detector for determining the
35 unauthorized presence of a person in the room. Suitable person detectors may be provided by motion detectors or infrared detectors and are well known in the security art. Slave No. 5 communicates with a burglar

alarm bell, which is activated upon command from the master controller 10 in response to an alarm condition sensed by one of the burglar detection units.

5 The fire detection units and burglar detection units are provided by binary switches; that is, they are either tripped or they are not tripped. The alarm bells are similarly controlled by binary relays, which are either open or closed. By contrast, slave
10 No. 6 controls a temperature sensor, which is an analog unit monitoring continuous temperature and providing continuous temperature data to slave No. 6. As indicated in Figure 1, the master controller of the present system still has further capacity for supervising
15 other slave controllers located either in the same room as slave controllers Nos. 1-6 or in other remote locations.

Figure 1 is presented only by way of example, and no limitation of the invention to this particular
20 configuration or any particular number of slave controllers is intended. As will be apparent below, the system can be configured in many ways--strictly as a burglar alarm system, as a fire alarm system, as a system for monitoring environmental parameters, or as any
25 combination. In addition, the size of the system can vary over a wide range, for example, to monitor an individual room or to monitor a number of independent offices.

The master controller 10 controls all data
30 communication with the slaves. It provides a source of DC power for the slaves, and serves various other functions such as providing programming capability for tailoring the system for a particular configuration of slaves and devices, for providing alarm indicators, and
35 for sensing for a break in the line 12.

The distinctive communication ability of the present system, whereby the system provides both data communications and a DC power source simultaneously

over the same twisted pair, may be understood by reference to Figure 2. The master controller includes a transmitting means 16 and a receiving means 17, both of which are connected to line 12 at terminals 18 for communications with the slaves.

The transmitting means provides a modulated DC voltage signal at the terminals 18. This signal can be thought of as comprised of an uninterrupted DC voltage component for supplying DC power, on which is superimposed a varying component bearing the data. The uninterrupted DC component has a potential equal to the potential at the node 19. The potential at this point is equal to the potential of the master controller power supply (nominally 12V) reduced by a predetermined voltage drop (about 2V in the illustrated embodiment) across voltage drop circuit 21. Although the master controller supply voltage is indicated as a 12V in Figure 2, this is only a nominal value. In the illustrated embodiment the actual value is closer to 14V, so that the uninterrupted DC component available on line 12 is roughly 12V.

The data component is generated by pulse-modulating the nominal 12V supply for the master controller. The modulation is accomplished by pulse modulator switch 22, which switches the voltage drop circuit in and out upon command from a processor unit (the microprocessor unit 23 seen in Figure 4). A data pulse from the processor unit is applied to power driver 26, which then applies a 24-volt control pulse to the pulse modulator switch 22. DC/DC converter 27, also under control of the processor, provides a 24-volt control source for power driver 26 and voltage drop circuit 21. In this manner, in response to a pulse train from the processor unit along line 21, the transmitting unit 16 supplies a voltage signal to the loop terminals 18 varying nominally between 12 and 14 volts. As will be explained below, at each slave controller

the 12 to 14 volt modulation is demodulated and interpreted as a data signal, and the remaining 12 volts sent out over the line to the slaves is available as a power source.

From time to time the slave controllers will answer messages received from the master controller. In contrast to the voltage-modulated signal transmitted by the master controller, the slave controllers return a current-modulated signal. This signal is received by the receiving unit 17, demodulated, and sent to the master processor unit for interpretation. The receiving unit 17 senses for changes in the current at the loop terminals 18. Current in the loop is applied across the primary side of the toroidal transformer 31. The current change across the primary side is felt as a voltage change across the secondary side. This voltage is applied to a limiter circuit 32 to avoid overdriving the subsequent circuits. From the limiter circuit the signal is applied to integrater and filter circuits which serve as a gain control and wave shaping circuit 33. The integrater and filter shapes the incoming signal approximately into a triangular waveform. The waveform is then applied to a phase lock loop 34, which serves as a frequency sampling circuit generating a pulsed signal which is then sent to the data input of the processor.

Loop short sense circuit 36 senses a loss of voltage if the loop should be shorted out and sends a pulse to the nonmashable interrupt (NMI) part of the master controller processor to stop the data transmission. In the opposite situation of a break in the line 12, the loop return line 13 can be used to communicate with slaves on the other side of the break from the terminals 18. In this situation, the loop return 13 is connected to the transmitting and receiving means 16 and 17 by loop return relay 37, which is energized on command from the master controller processor.

The communication function of the slave controllers is now described broadly with reference to Figure 3. The signal from the master controller is received at a slave controller at the terminals 41. The signal is applied to the receive detector 42 and also to a 5-volt regulator 43. Since 5 volts is substantially less than the minimum value of 10 to 12 volts of any signal coming in from the master controller, the regulator 43 has no difficulty filtering out any pulsation so as to provide a constant source. This source supplies power to the slave controller unit itself. At the terminals 41 a pair of coils 44 filters out the varying data component, if any, from the signal on the line and provides the full uninterrupted DC component at terminals 46 for use as a power source.

The receive detector 43 includes a transformer input 47 coupled to a comparator 48. The fluctuations of the modulated voltage signal off the line are transferred from the primary to the secondary side of the transformer, where they are compared with the reference voltage level of comparator 48, which thereby generates a pulse train in response to the incoming signal. This pulse train is applied to the input of a nonretriggerable monostable multivibrator (one-shot) 49. The leading edge of a pulse will trigger the one-shot 49, which provides a 13 microsecond output pulse for each input pulse. In this manner, any noise or other irregularity of the input signal will not be seen at the output of the one-shot 49. The pulse from one-shot 49 is applied straight into the data input of the on-board microprocessor unit (MPU) 50, which is a receive-timer input for looking at the pulses. The output signal from the nonretriggerable one-shot 49 is also applied to a retriggerable one-shot 51 having an output applied to the interrupt request (IRQ) line of MPU 50. A signal on the IRQ line alerts the MPU that a data signal is coming in so that the MPU will be

prepared to count pulses. As long as a signal is coming in, the retriggerable one-shot 51 is held low, returning to high only at the end of an incoming pulse train.

As will be explained in more detail below, each slave controller has its own address, which is set by the eight-position address select switch 52. The master controller, wishing to send a message to a particular slave controller, will begin its transmission with the address of the target slave controller. The MPU 50 compares the incoming signal with the address specified by the address select 52 to determine if that slave controller has been called. If no match is found, the MPU of that slave controller does not respond.

The slave controllers transmit their messages to the master controller by modulating the current on the line 12 in response to a data signal from the on-board MPU. Specifically, a data signal from the MPU 31 is applied to a transmit driver 53, which functions as an on-off switch. Closure of the switch causes extra current to be drawn off the line 12. When the switch opens, the current returns to normal. The modulated line current is then demodulated at the master controller, as indicated above.

Depending upon the frequency of the output data signal from MPU 51, interference or cross-talk with other slave controllers will sometimes occur. That is, the slave controllers will sometimes "see" each other and try to communicate. To avoid this possibility, a "divide by 2" circuit 54 is inserted between the data output of MPU 50 and the transmit driver 53.

As presently described, whether the transmit driver 53 ends up in a high or low state is dependent upon the final output of the "divide by 2" circuit at the end of a unit of transmission. To assure that the

driver ends up in the off position, a driver hold-off circuit 56 is applied in parallel with the "divide by 2" circuit. The driver hold-off circuit assures that
5 the divider always ends up in the off position, thereby assuring that the transmit driver itself will end up in the off position.

The slave controller includes digital input means 57 providing three input lines for connection to
10 external two-state devices such as door closure switches, which are either in a tripped or untripped state. Digital output means 58 enables the slave to trip an external device such as an alarm bell or a central relay. Analog interface means 59 enables the slave to
15 communicate with an external analog device such as a temperature or humidity sensor.

One of the features of the present system is its great flexibility in the number of configurations it can assume with comparatively small memory available. This flexibility is achieved by programming the
20 dynamical aspects of the system using an object-oriented approach. For a detailed exposition of an object-oriented language, reference is made to SMALLTALK-80, The Language and Its Implementation, by
25 A. Goldberg and D. Robson, Addison-Wesley Publishing Co., Reading, Massachusetts (1983). An exposition of the memory management architecture of the present system may be found by reference to a co-pending application filed contemporaneously herewith entitled "Supervisory Control System With Improved Memory Management"
30 by David Martin and owned by the same owner as the present application.

B. Master Controller

Having described the system generally, a more
35 detailed description is now given of the structure and operation of the master controller. Figures 4A and 4B taken together provide a circuit diagram of the digital circuitry for the operation of the master controller.

The central component of the system is the microprocessor unit (MPU) 23, which interfaces with the master controller memory, peripherals and other subassemblies as will be indicated below. MPU 23 communicates to other parts of the system along 15-byte address bus 61 and 8-byte data bus 62. The passage of data to or from data bus 62 is controlled by transceiver 63. When enabled, the transceiver is in either a transmit mode, along the MPU to transmit data on the bus, or a receive mode, allowing the MPU to receive data from the bus. The mode of transceiver 63 is controlled by gate 64, which responds to an enable signal from the enable port 66 of the MPU and a read/write signal from the read/write port 67 of the MPU. In the present implementation of the master controller the transceiver 63 is provided by a 74HC245 transceiver chip.

The system memory comprises random access memory (RAM) units 68 and 69 together providing 16K bytes of memory, and read-only memory (ROM) units 71 and 72 together providing 16K bytes of read-only memory. In the present implementation the ROMs are provided by 27C64EPROM chips and the RAMs are provided by 6264LP chips. Reading and writing into the RAMs and reading of the ROMs are enabled by the read/write port 67 of the MPU. The data on bus 62 are fed to latch 73, which provides the lower 8 bytes of address along address line 61. The upper seven address bytes are provided from address ports 74 on the MPU. Latch 73 is enable from the address select port 76 on the MPU. Selection of a particular RAM or ROM is controlled by address select switches 77, which also select other subassemblies or functions being addressed by the MPU. Address select switches 77 may be provided by 74HC138 chips. The real time clock 78 controls all real time functions for the system. For example, the real time clock enables an operator or the MPU itself to keep track of the times at which alarm events occur or at

which a false condition arises in the MPU. The real time clock may be provided by a MC146818A chip available from Motorola Corporation. This chip includes a
5 watchdog timer subroutine, which provides a handy safety measure. The watchdog subroutine continually counts down, for example, from 100. When it gets to, say, 10, the MPU resets the chip to 100. If the MPU should lock up, so that it is incapable of resetting the subroutine
10 at 10, the watchdog timer times out and provides a signal for resetting the microprocessor.

Standby block 79 protects the system from unacceptable reductions in power. Lock 79 is responsive to the system nominal 12-volt supply. If the system voltage drops below 7 volts, the standby output
15 communicates a signal to RAMs 68 and 69, real time clock 78, and reset circuit 81. Whenever a standby condition arises, the circuit 81 resets the MPU after the power comes back up. Reset circuit 81 resets not
20 only the MPU itself, it also activates the real time clock reset 82. This circuit assures that the real time clock is not reset before the MPU. Real time clock reset 82 provides a delay so that the clock will reset more than three microseconds after the MPU.

25 A limited amount of programming capability is provided through key pad 83 for adapting the master controller memory to the particular configuration of the system being installed or for modifying the configuration at a later time. Depression of a key on a key
30 pad causes the MPU to fire a tone timer or sonalert to let the user know that the key depression has been received. Key pad 83 communicates with MPU 23 through a conventional key pad encoder 84, which may be provided by a 74C922 chip.

35 To aid in programming the master controller and to provide visual display of data to the user, the master controller includes a 1 by 14 liquid crystal

display (LCD) 86. LCD 86 is coupled to data bus 62 for display of whatever data called for at the key pad 83.

The master controller also includes a plurality of LEDs for alerting the user to various alarm conditions. LEDs 87 may also be used in conjunction with a conventional flasher unit 88 for providing a stronger warning or alert signal.

The function I/O 89 controls the LEDs and other subassemblies in the master controller and at the slave controllers. In particular function I/O 89 controls the power for the transmitting means 16, a trouble scan unit 91 for sensing trouble in burglar and fire alarm bell units, a battery charger for charging backup batteries, and the function I/O 89 also controls the ringing of an alarm bell at a remote location in response to an alarm condition. Function I/O 89 is provided by conventional 74HC374 bus interface chip.

Trouble scan unit 91 is used for verifying the integrity of alarm circuits or other circuits forming part of the system. Trouble scan unit 91 receives a plurality of lines 92, for example, from trouble sense units 93 used for sensing "trouble," that is, a malfunctioning of an alarm bell circuit at a remote location. The lines 92 are in either a high or low state depending upon the condition of the trouble sense unit with which they communicate. Clock 91 notifies the MPU of a trouble condition. For example, if a comparator circuit on a fire bell at a remote location should trigger, this will in turn trigger the appropriate sense input, which will then be communicated to the MPU, which will determine the trouble condition according to which function I/O line was triggered. The MPU will then react accordingly.

Reference is now made to Figures 5A, B, C and D, which taken together show an implementation of the analog circuitry for the master controller. Power control for this circuit comes from the function I/O block

89 in Figure 4B. Control line 94 of Figure 4 corresponds to control line 96 of Figure 5. Power control line 96 feeds power driver 97. The signal along this line will normally be high when the system is in a standby mode. The high signal is fed to transistor 98, which serves as a pull up transistor. When power driver 97 is turned on, a low is sent to transistor 98. This in turn activates both charge pump circuit 99 and transistor 101. Charge pump circuit 99 corresponds to DC/DC converter 27 of Figure 2. It applies 24 volts to transistor 101 and to FET 102. FET 102 and diode string 103 comprise the voltage drop circuit 21 of Figure 2 and FET 104 comprises the pulse modulator switch 22 of Figure 2.

The receiving means of Figure 2 will now be described in more detail with reference to Figures 5A and C. Toroidal transformer 106 has roughly 10 turns on the primary side and 40 turns on the secondary side for a ratio of 1:4. Resistors 107 and 108 provide a half-voltage bias reference for this transformer. Diodes 109 provide a limiter circuit for an essentially square wave that is picked off of the toroidal coil. The diodes 109 limit the peak-to-peak signal to plus or minus 0.6 volts. The signal along line 111 is then applied to integrating and filtering circuitry 112. The first stage 113 provides a passive integrater circuit. Capacitor 114 and choke 116 following the passive integrater prevents too big a signal from entering the second stage, which is an active integrater having characteristics for filtering out high frequencies. The signal coming from the integrating and filtering circuitry 112 is in the form of a triangle wave, which is acceptable to the subsequent phase lock loop. The phase lock loop may be provided by a XR211 chip. It is tuned to 17.5 KHz with a plus or minus 3 KHz lock-in range. The output from the phase lock loop along line

118 is a demodulated data signal, which is applied to the MPU.

The implementation of the slave controllers
5 is much simpler than that of the master controller.
Figures 6A and 6B taken together show a suitable implementation of the slave controller electronics.

While the foregoing provides a full and complete description of an illustrative embodiment of the
10 present invention, various modifications, alternate constructions and equivalents may be employed without departing from the true spirit and scope of the invention. For example, although the present invention arose in the context of fire and burglar alarm systems,
15 it will now be appreciated by those skilled in the art, given the teachings of the present specification, that the principles of the invention may be applied to other supervisory systems as well. Thus, the above description and illustrations are not to be construed as limiting
20 the scope of the invention, which is defined by the appended claims.

WHAT IS CLAIMED IS:

1. Apparatus for use in supervising an alarm system or the like, said system comprising a plurality of slave controllers, each slave controller being in operative association with at least one device to be controlled, and a master controller in communication with said slave controllers, said master controller including a master processor and each slave controller including an associated slave processor for supervising said devices, wherein said apparatus comprises:

a pair of wires connected along their length to said plurality of slave controllers and connected at a first end to said master controller;

voltage means included within said master controller and responsive to said master processor for providing a voltage signal comprised of a data component and an uninterrupted DC voltage power component of a magnitude sufficient to power all said devices in operative association with said slave controllers, said voltage means being connected to said pair of wires for communicating said voltage signal to said slave controllers;

voltage demodulation means included within each said slave controller for receiving said voltage signal and for deriving therefrom said data component and said uninterrupted DC voltage power component;

current modulation included means within each said slave controller and connected to said pair of wires for modulating current therein responsive to the respective slave processor so as to define a data signal for communication to said master controller; and

current demodulation means within said master controller for receiving modulated current on said pair of wires and providing said data signal to said master processor.

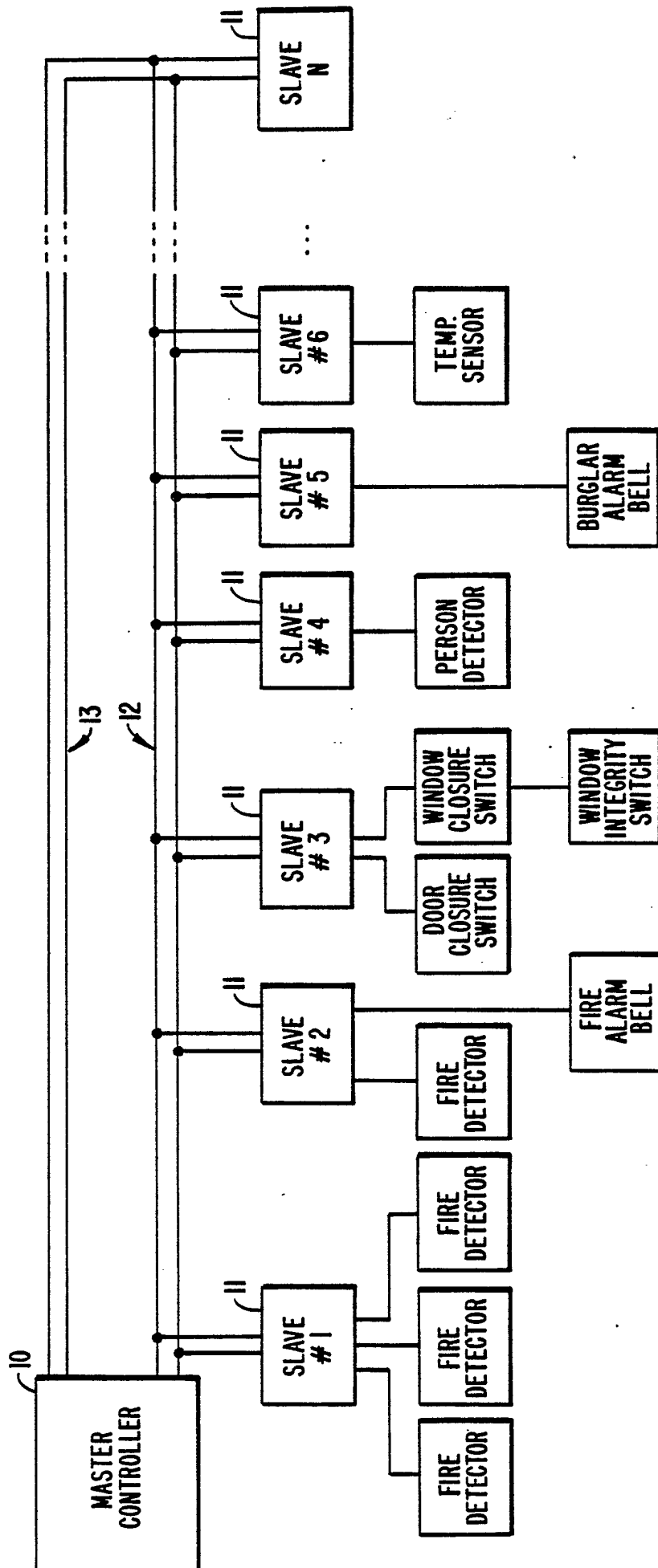


FIG.—1.

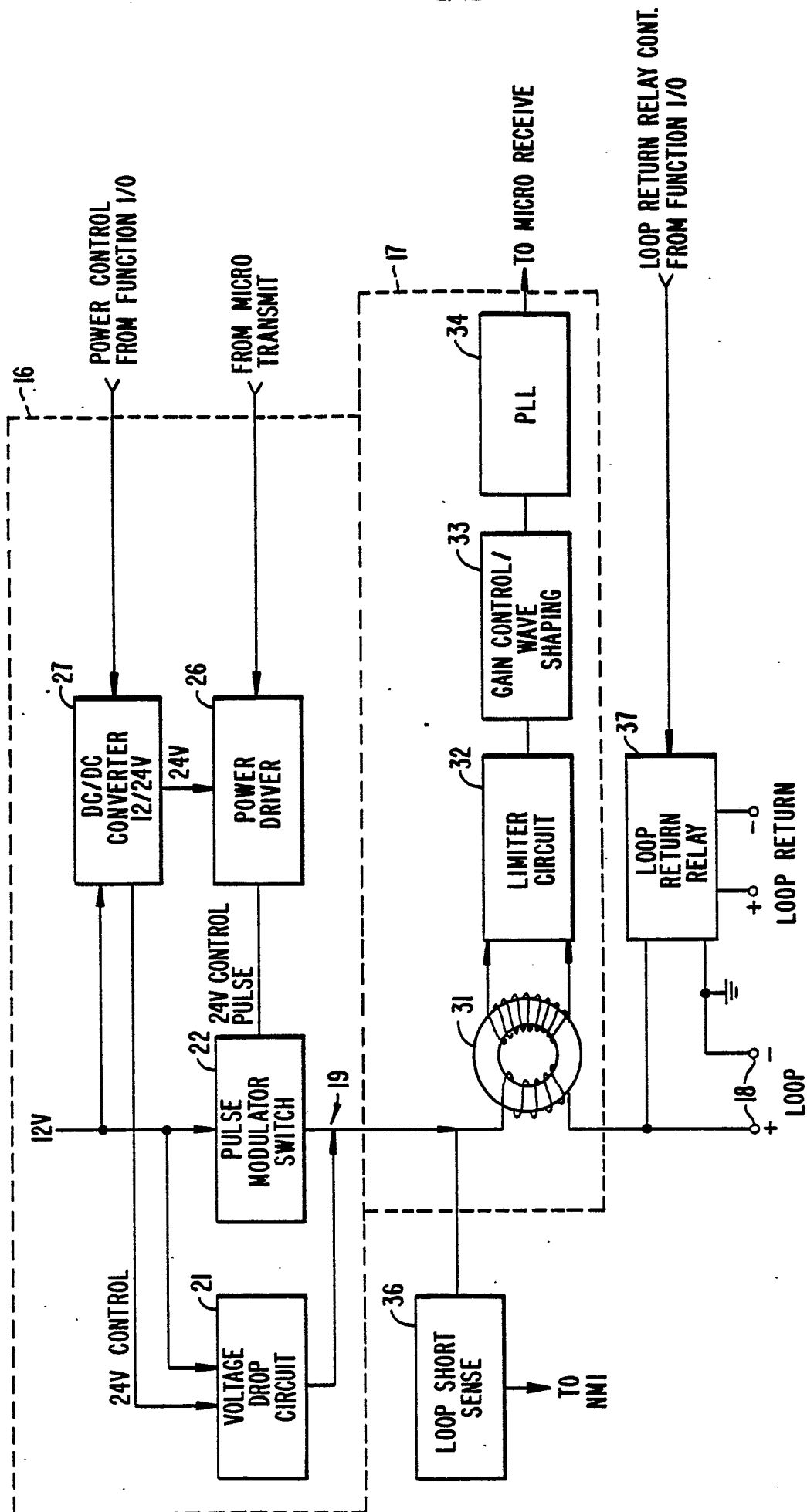


FIG.—2.

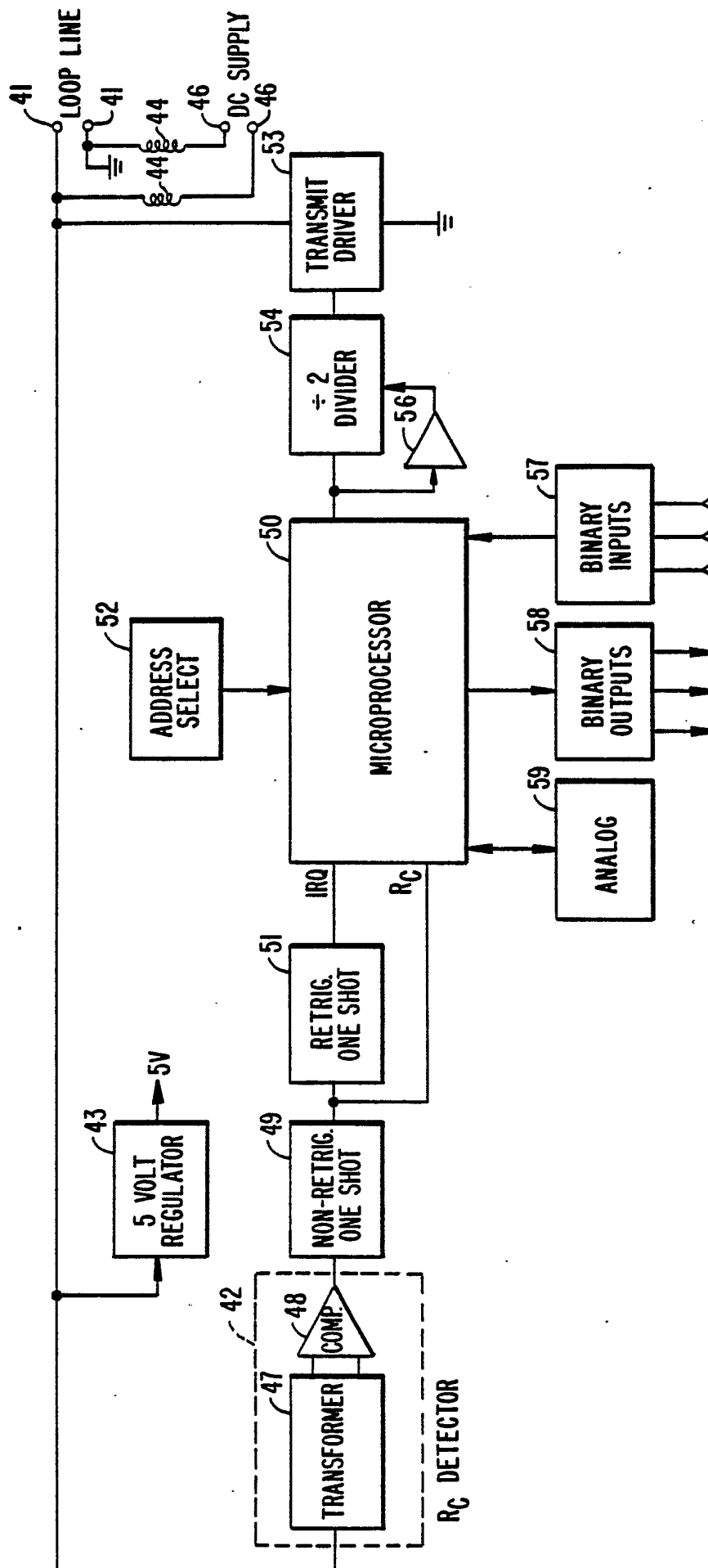


FIG.—3.

4/12

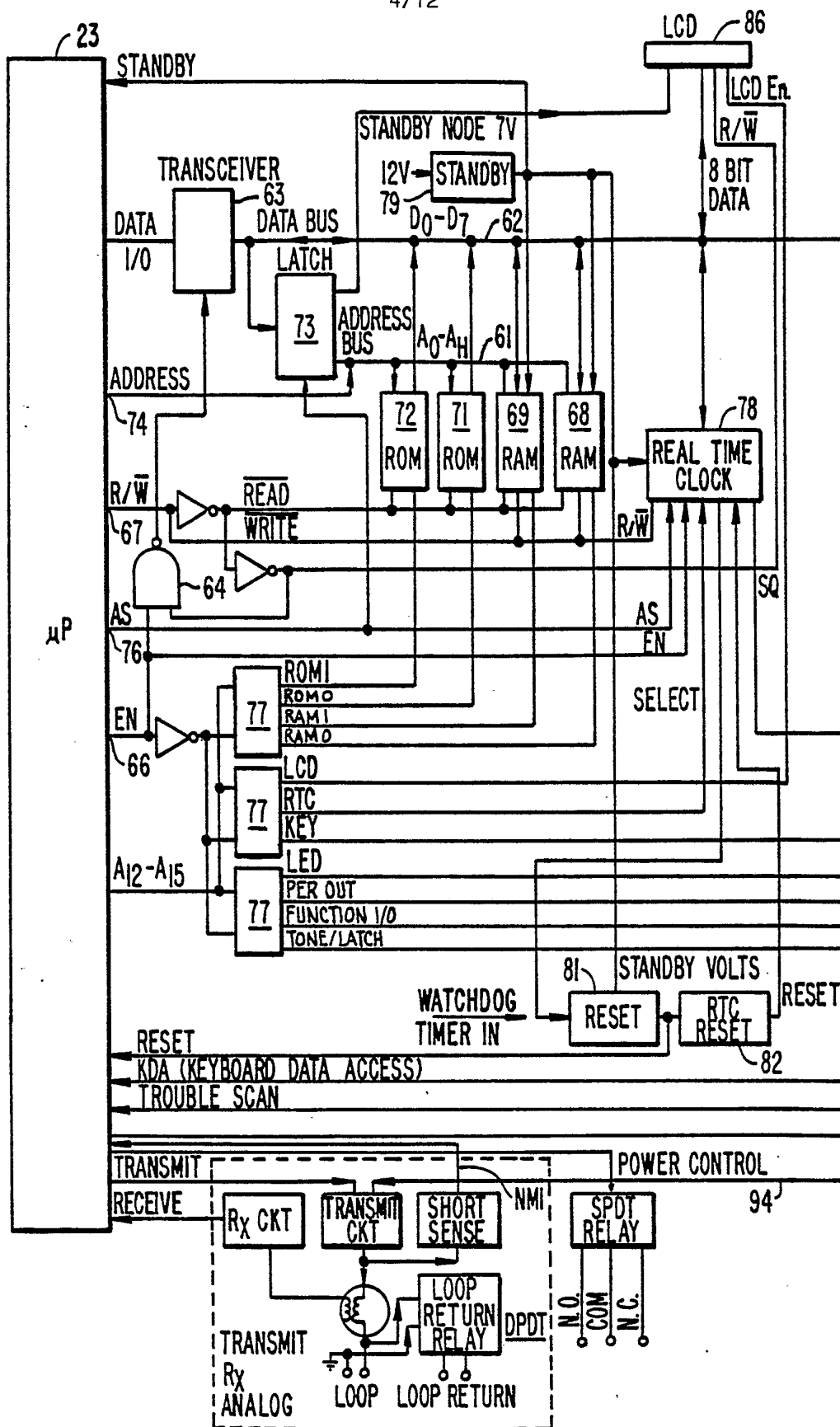


FIG. 4A.

FIG. 4. FIG. 4A. FIG. 4B.

5/12

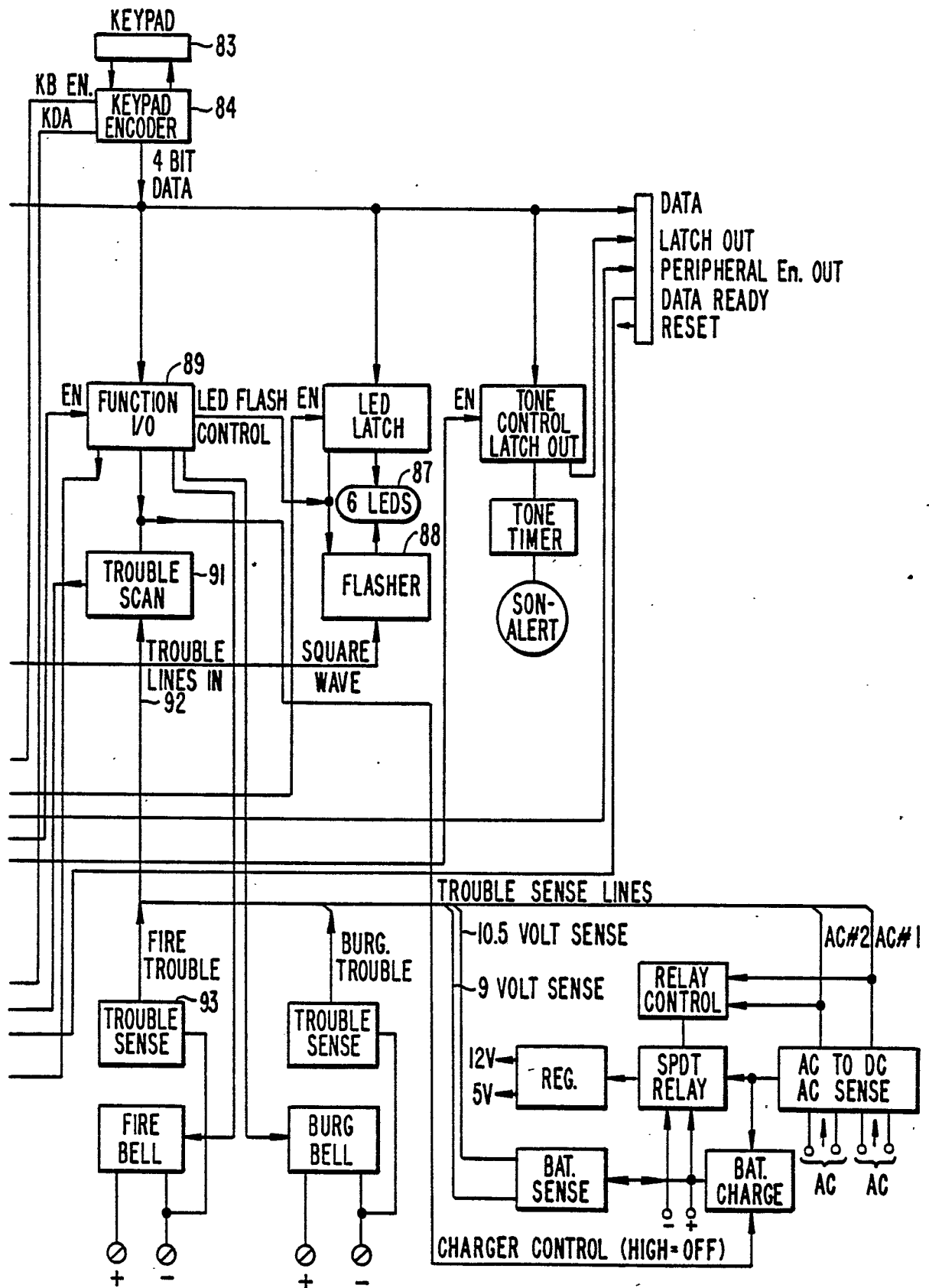


FIG. 4B.

SUBSTITUTE SHEET

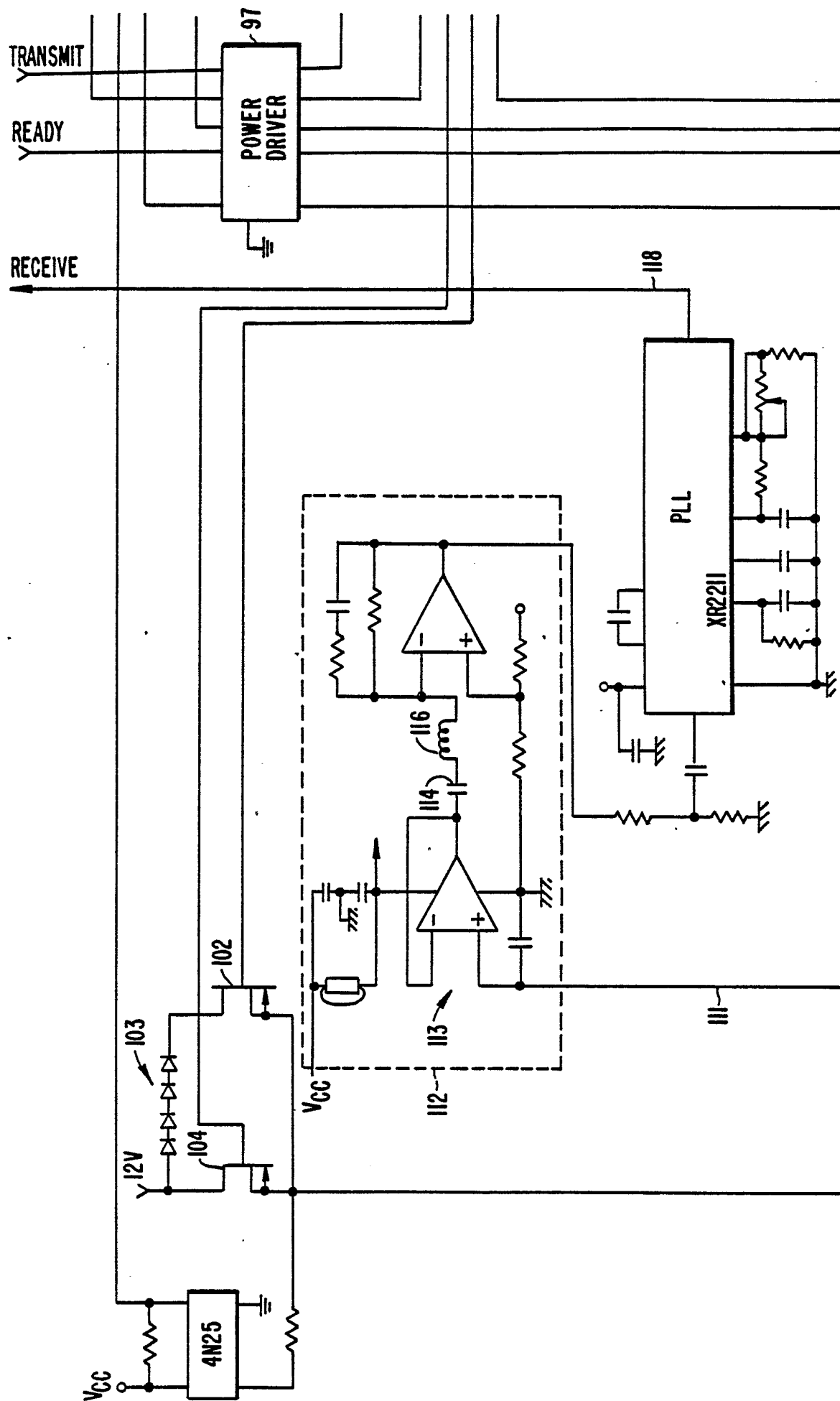


FIG. 5A.

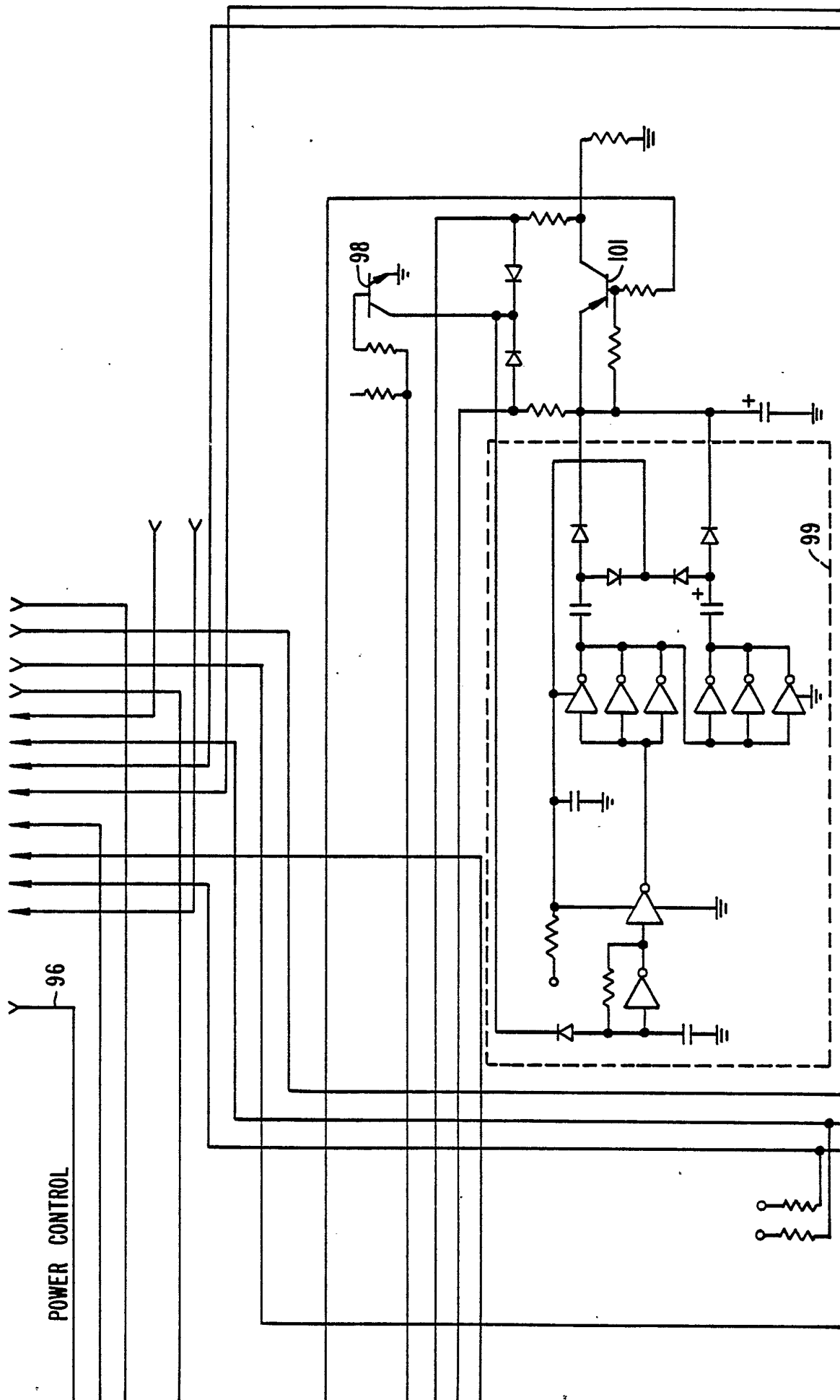


FIG. 5B.

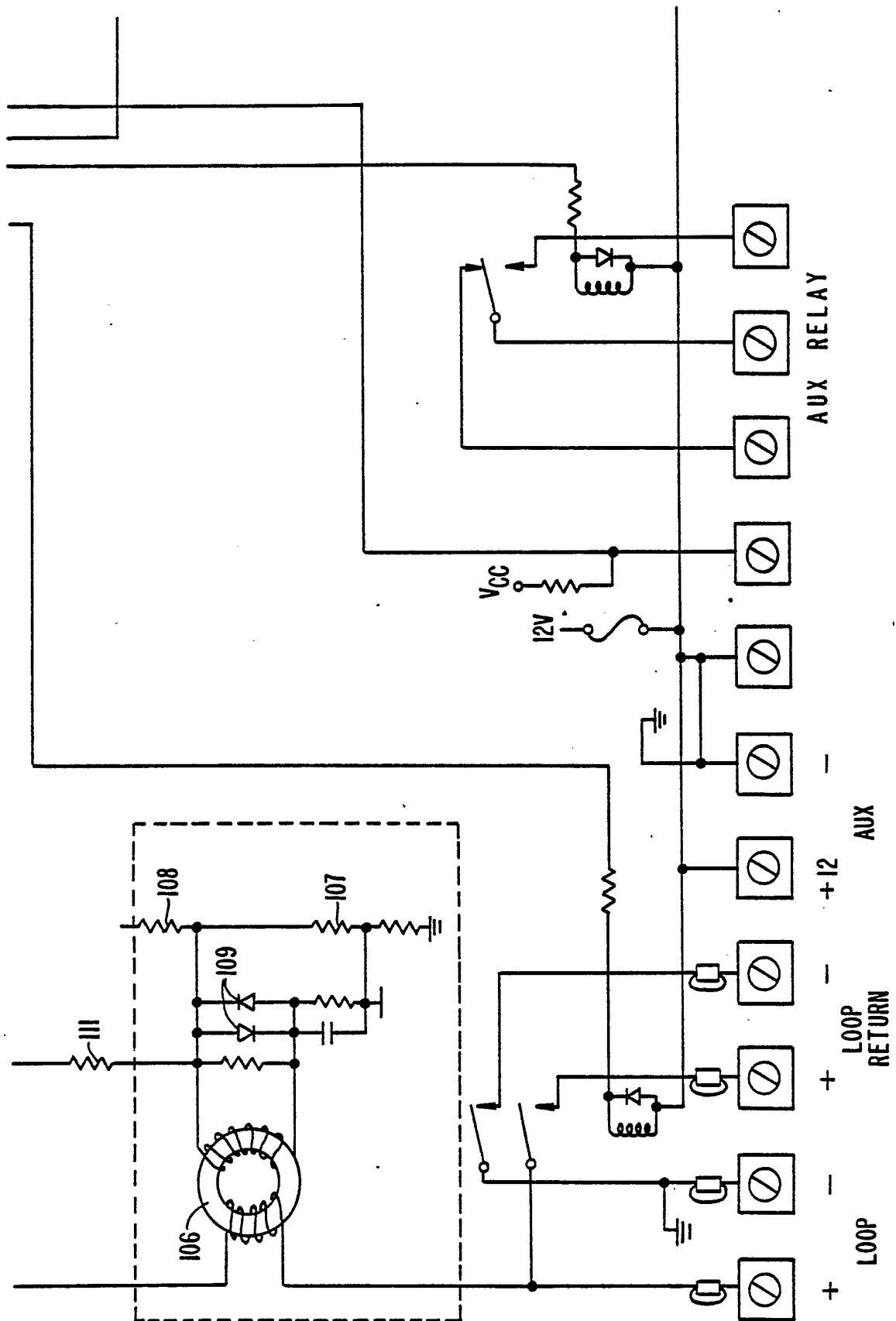


FIG. 5C.

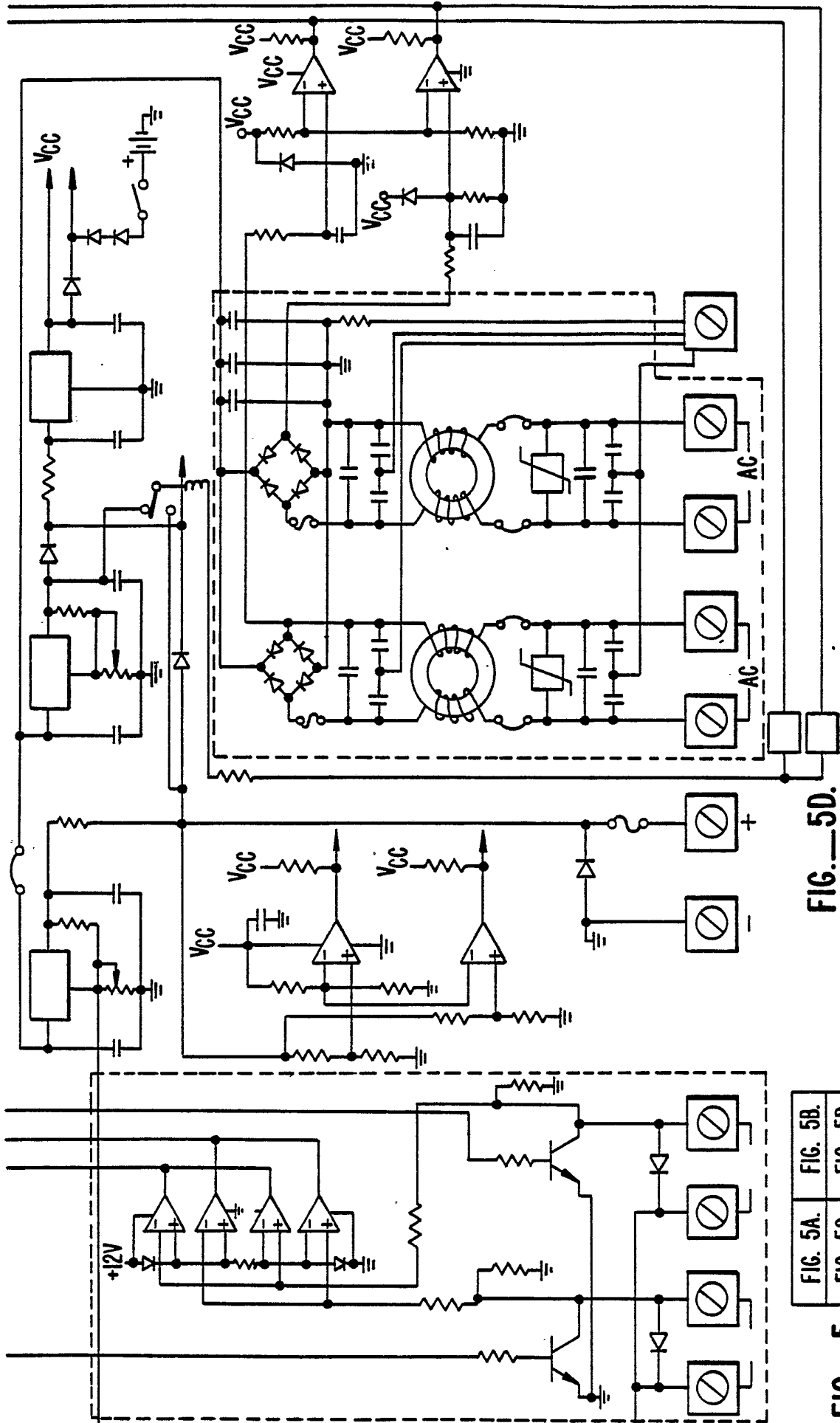


FIG. 5D.

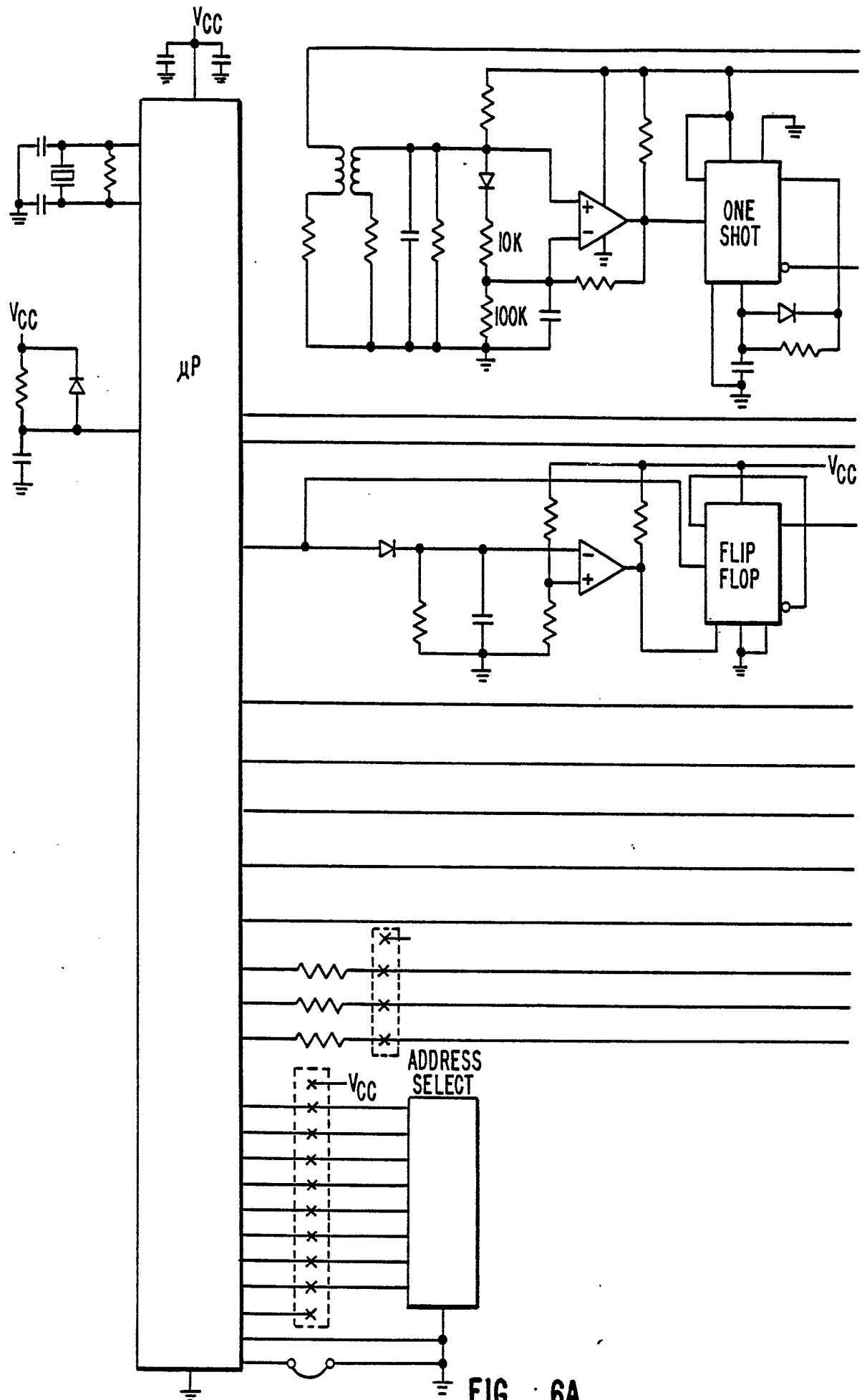


FIG. 6A.

SUBSTITUTE SHEET

11/12

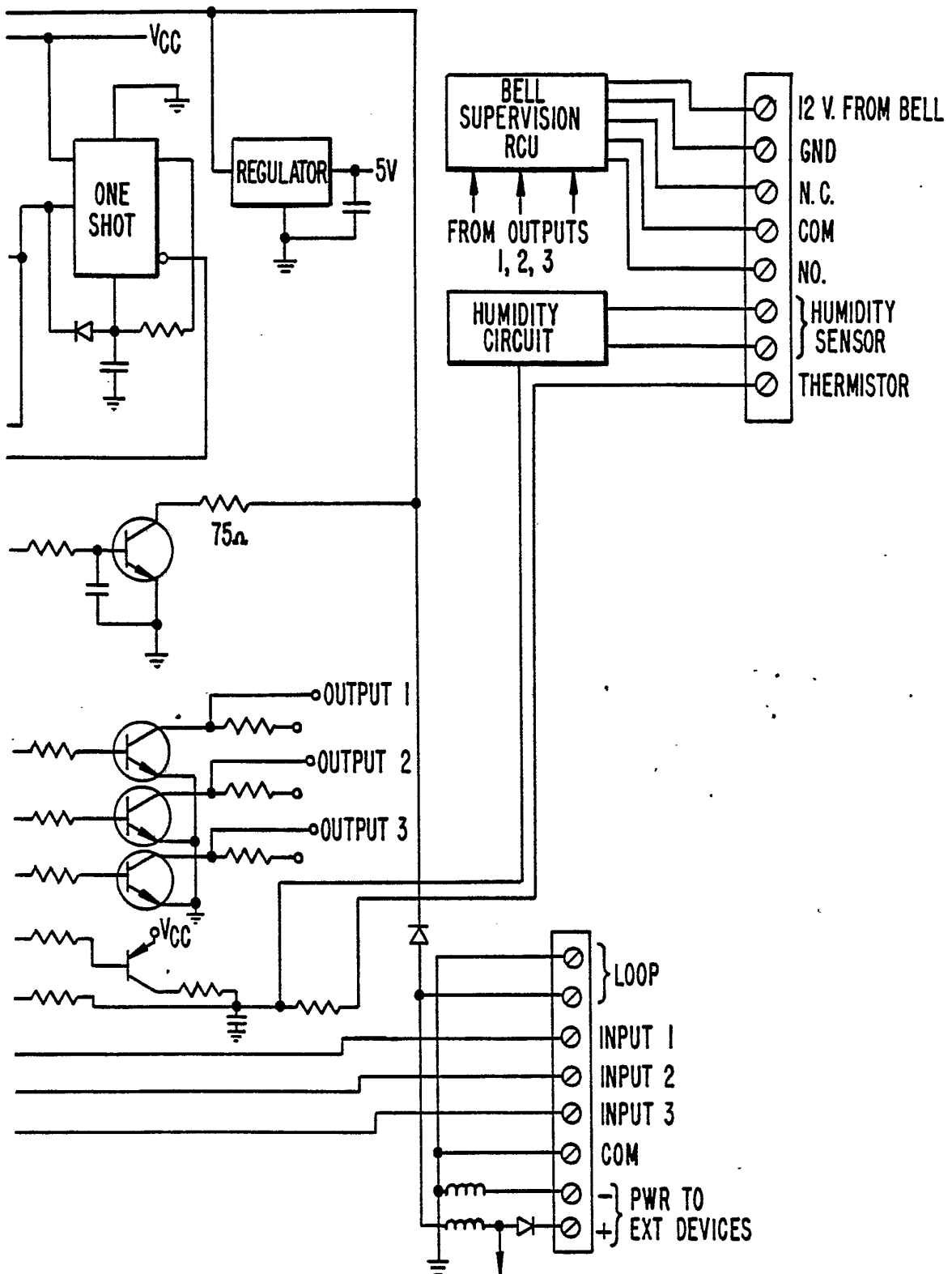


FIG. 6B.

FIG. 6A.	FIG. 6B.
----------	----------

FIG. 6.

SUBSTITUTE SHEET

12/12

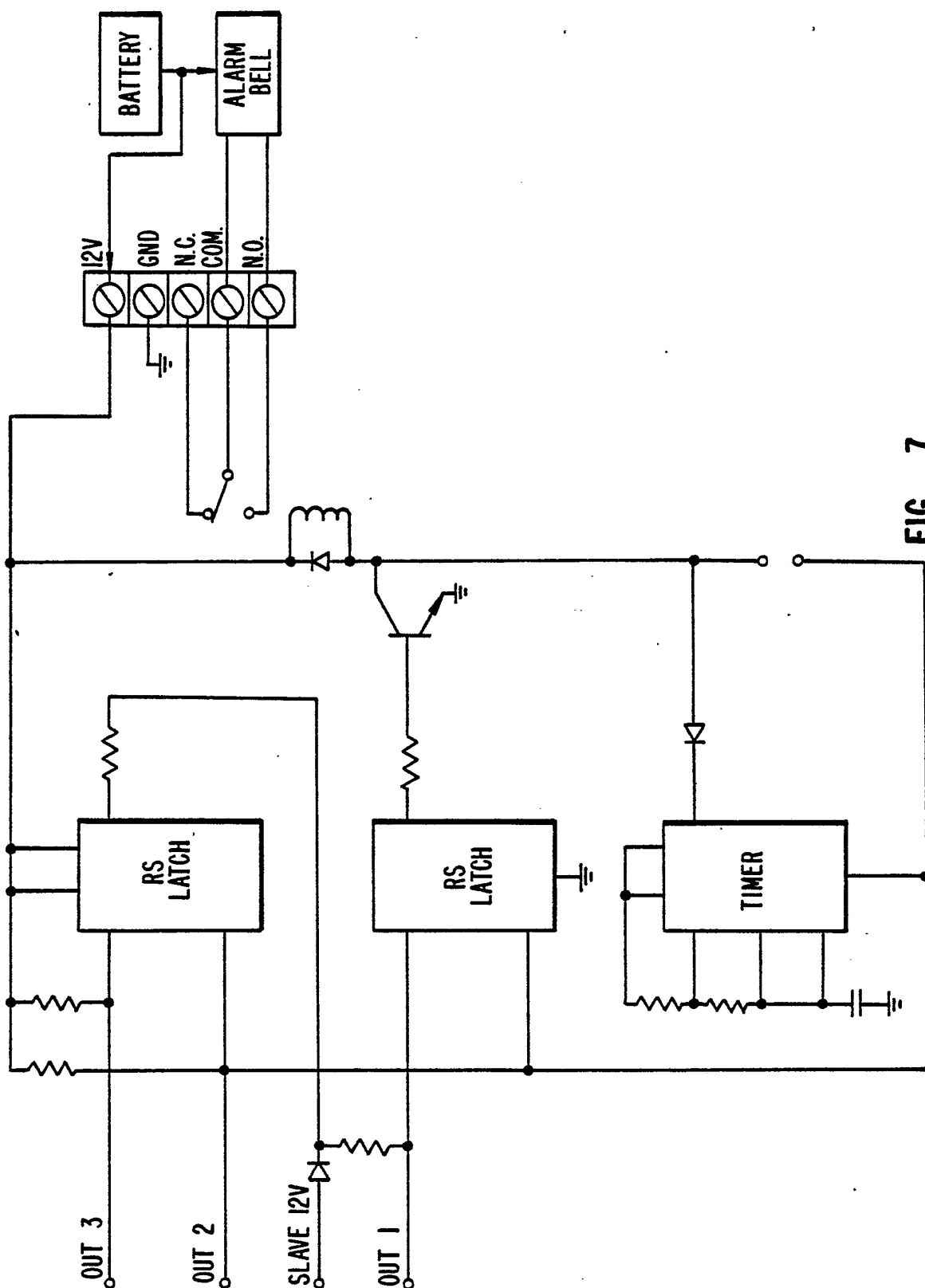


FIG. 7.

INTERNATIONAL SEARCH REPORT

International Application No PCT/US86/02559

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ³		
According to International Patent Classification (IPC) or to both National Classification and IPC		
IPC(4): G08B 25/00, 26/00; H04Q 9/00		
U.S. CL. 340/500, 505, 506, 518, 825.06, 825.07, 825.54		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁴		
Classification System	Classification Symbols	
U.S.	340/500, 505, 506, 518, 825.06-825.13, 825.54, 531, 538	
Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁶		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ¹⁴		
Category *	Citation of Document, ¹⁶ with indication, where appropriate, of the relevant passages ¹⁷	Relevant to Claim No. ¹⁸
Y	US, A, 4,535,401 (Penn) 13 August 1985 See Abstract	1
Y	US, A, 4,139,737 (Shimada et al) 13 February 1979 See column 2, lines 1 to 11	1
A	US, A, 3,927,404 (Cooper) 16 December 1975 See entire document	1
* Special categories of cited documents: ¹⁵ "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family		
IV. CERTIFICATION		
Date of the Actual Completion of the International Search ²		Date of Mailing of this International Search Report ²
30 JANUARY 1987		13 FEB 1987
International Searching Authority ¹		Signature of Authorized Officer ²⁰
ISA/US		Donnie L. Crosland