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Lefferts

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[54] **ARC ELIMINATION CIRCUIT**

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[52] **U.S. Cl.** ..... **307/136,** 317/11 E

[51] **Int. Cl.** **H01h 9/30**

[58] **Field of Search** ..... 317/11 E, 11 R, 33 SC; 307/136, 252 B, 305 R, 305 A

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[57] **ABSTRACT**

A circuit arrangement for eliminating arcs formed across a set of contacts on the opening or closing thereof comprising a thyristor connected across the contacts to be protected. The control electrode of the thyristor is coupled to a control circuit which includes a logic circuit for generating a trigger pulse upon the simultaneous occurrence of a plurality of contact arc-indicative conditions. The control circuit also includes sensing circuits for generating control signals upon the occurrence of preselected arc-indicative conditions, such as preselected contact or load voltages and contact or load transient voltages having a preselected rise time or frequency characteristics.

9 Claims, 6 Drawing Figures

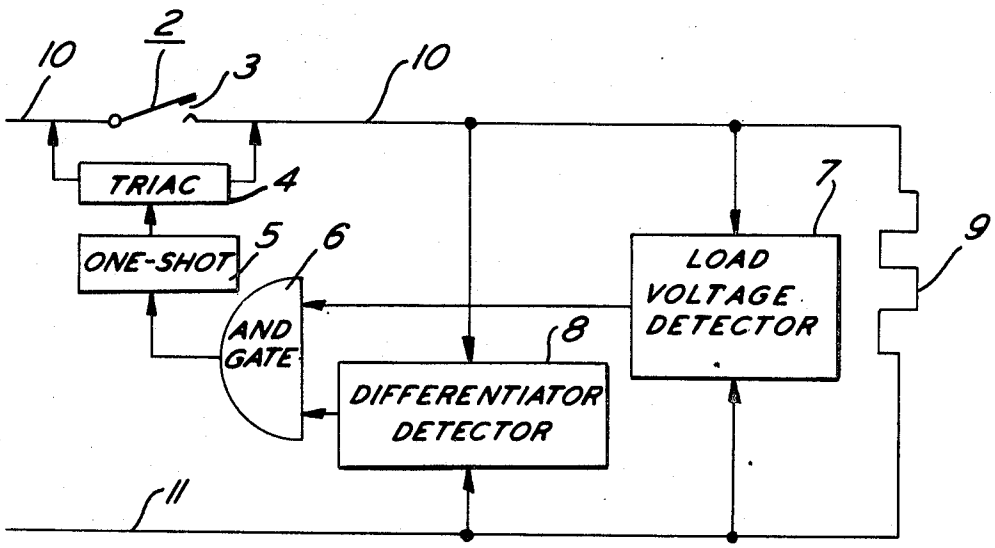
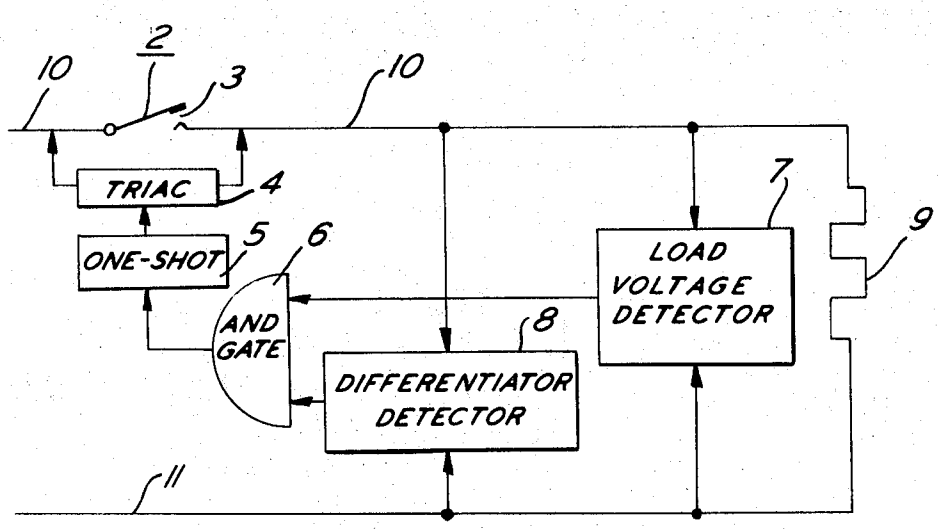
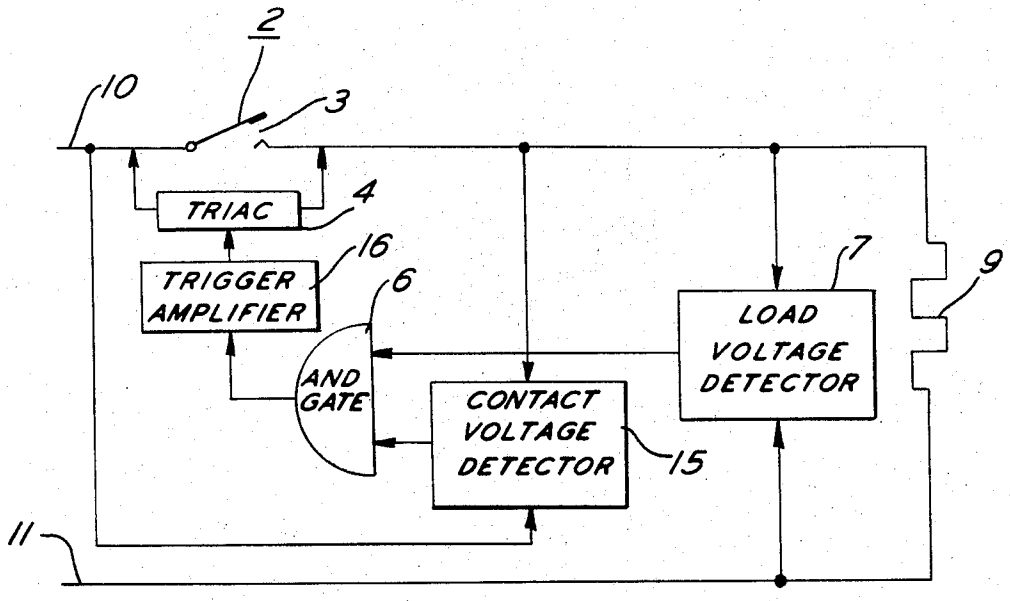


FIG. 1


2
10
3
10
TRIAC
4
7
9
ONE-SHOT
5
6
LOAD VOLTAGE DETECTOR
AND GATE
8
DIFFERENTIATOR DETECTOR
11


2
10
3
TRIAC
4
16
7
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TRIGGER AMPLIFIER
6
LOAD VOLTAGE DETECTOR
AND GATE
CONTACT VOLTAGE DETECTOR
15
11

FIG. 3

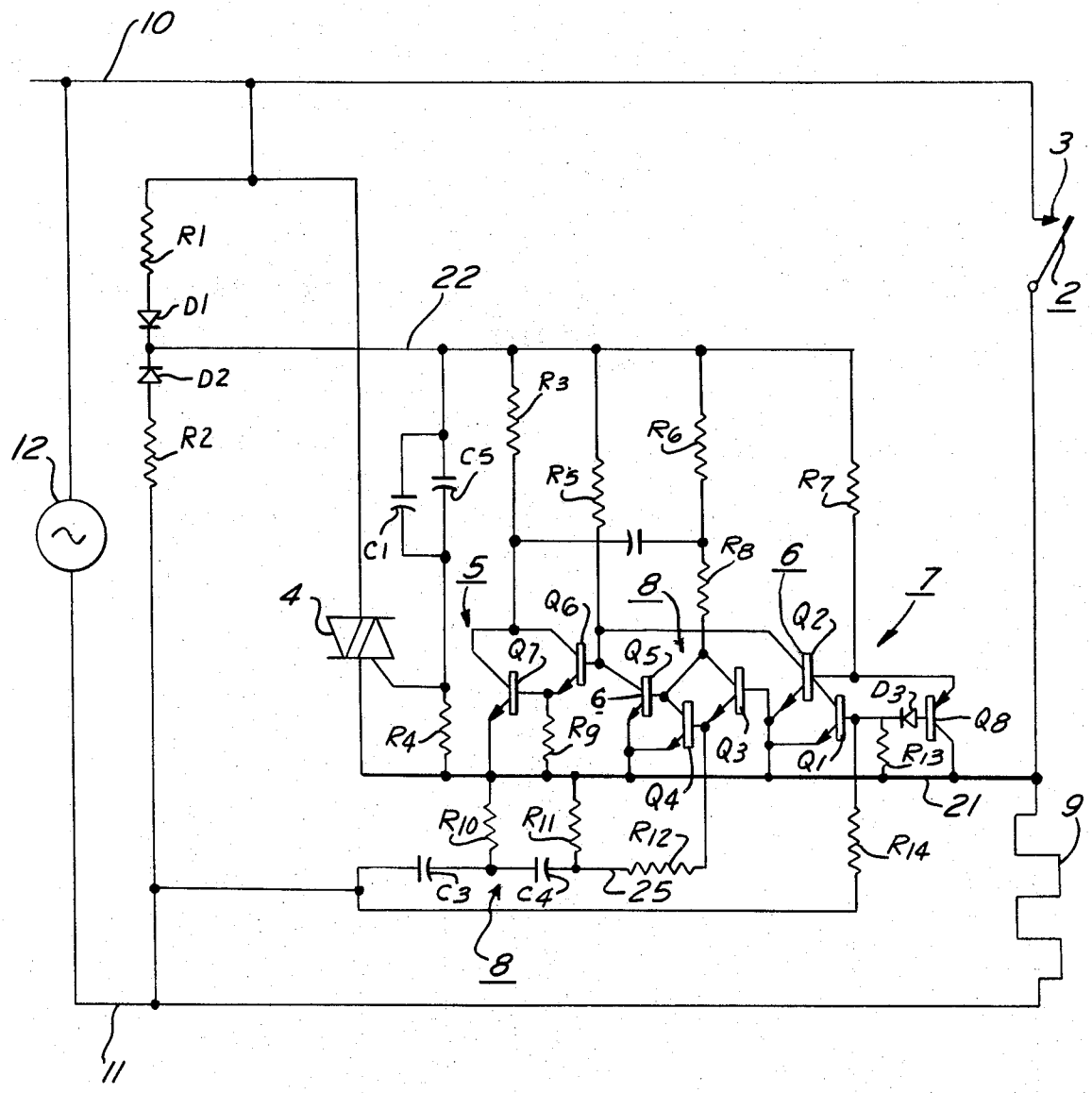
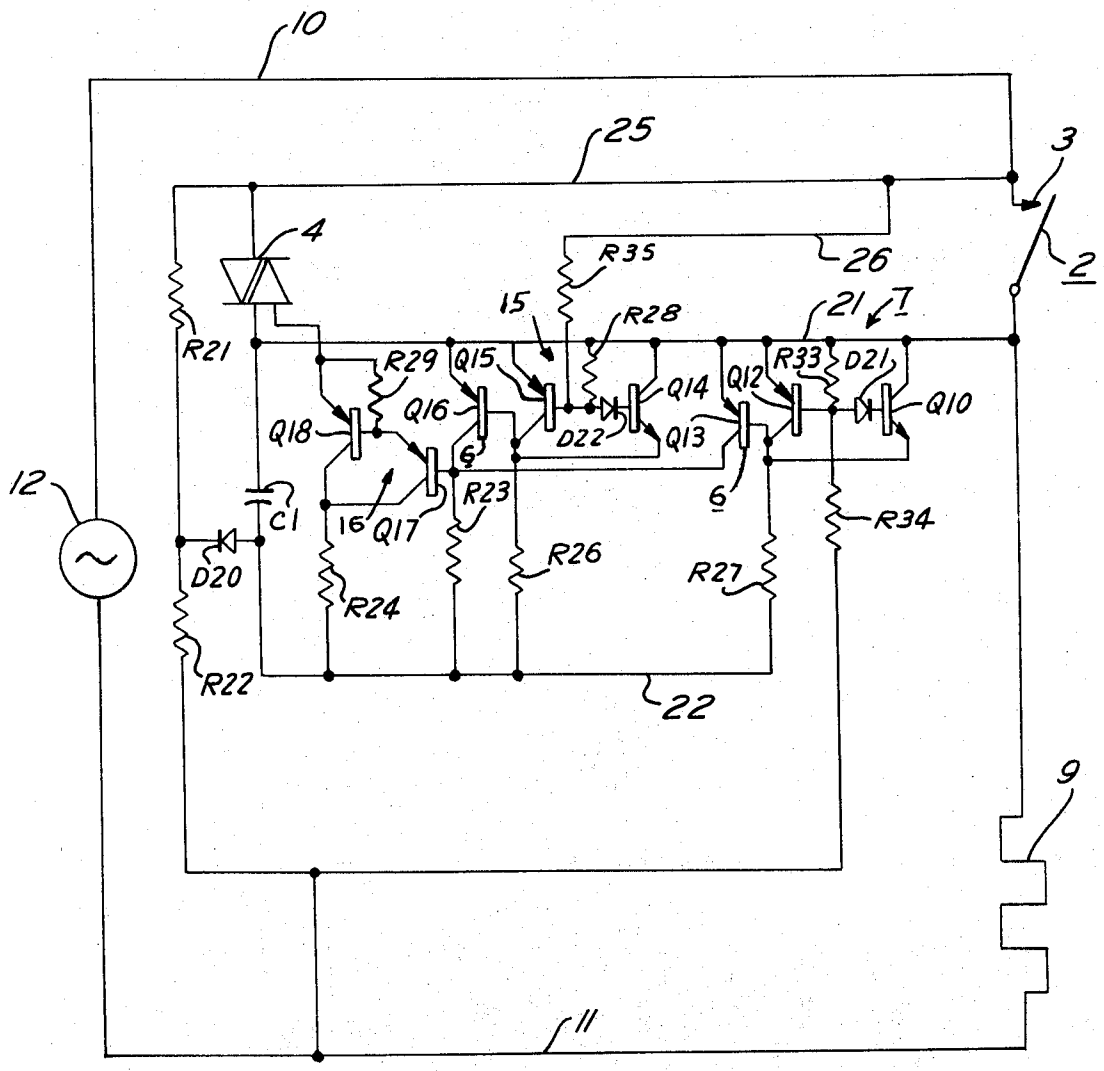

10
3
2
R1
D1
22
D2
R2
12
C5
C1
R3
R5
R6
R7
R8
5
6
7
8
4
Q6
Q7
Q5
Q2
Q1
Q3
Q4
D3
Q8
R4
R9
R13
21
9
R10
R11
R12
R14
C3
C4
25
8
11

FIG. 2


10
25
3
2
4
R35
26
15
R28
21
T
R21
R29
Q15
Q14
Q12
R33
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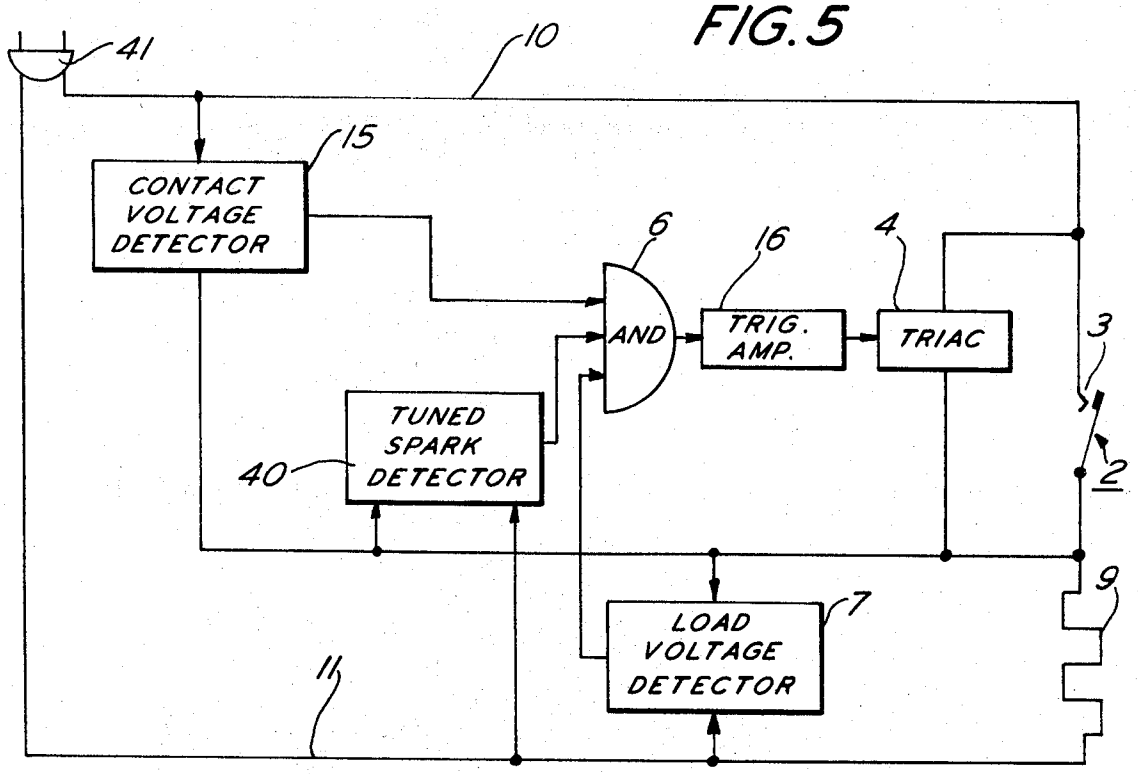
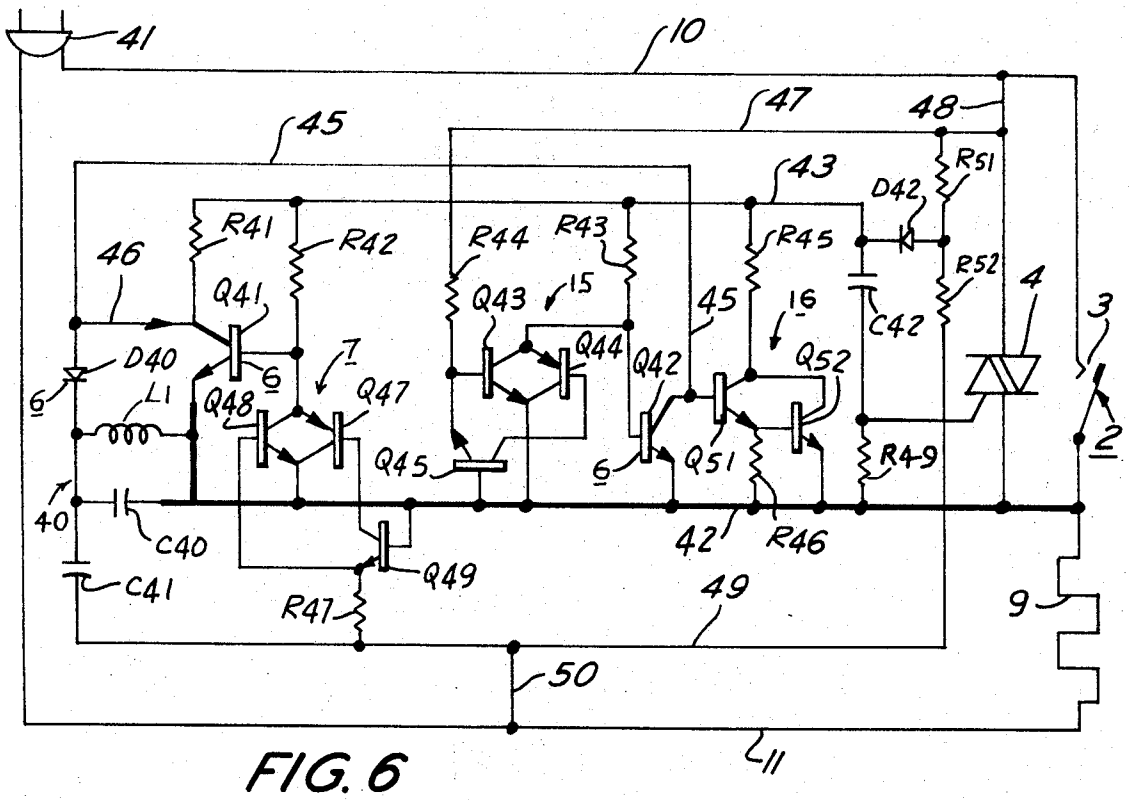
Q10
Q16
Q18
D22
Q13
6
6
12
C1
16
Q17
R23
R34
D20
R26
R27
R24
R22
22
9
11

FIG. 4

FIG. 5


41
10
15
CONTACT VOLTAGE DETECTOR
6
16
4
AND
TRIG. AMP.
TRIAC
3
2
TUNED SPARK DETECTOR
40
9
7
LOAD VOLTAGE DETECTOR
11


41
10
47
48
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43
R51
D42
R41
R42
R44
R43
R45
46
Q41
Q43
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45
16
C42
R52
4
3
D40
6
7
Q44
Q42
Q52
L1
Q48
Q47
Q45
Q51
R49
2
40
C40
42
R46
C41
Q49
R47
49
9
50
11

FIG. 6

ARC ELIMINATION CIRCUIT

BACKGROUND OF THE INVENTION

The present invention relates generally to a circuit arrangement for use in connection with the switching of electrical currents and more particularly to a circuit arrangement for accomplishing this switching without contact arcing or the effects of contact bounce. More specifically, the invention relates to an arc elimination circuit arrangement wherein a thyristor is connected to shunt the switching contacts, the thyristor being operated by a control circuit suitable to turn on the thyristor upon the occurrence of arcing conditions across the switching contacts to thereby prevent or eliminate the formation of an arc.

Generally, electromechanical relays of the type having a coil operative to cause relay contacts to close when energized by a suitable current are employed to control current flow. When the relay contacts open and close, there may be a substantial amount of arcing due to the high electrical field between the contacts, and this arcing causes early contact failure because of the burning produced by the arcing. As a result, the size and expense of relay contacts is much greater than would be required in the absence of such arcing.

Prior art systems have typically employed a bilateral semiconductor connected in shunt across the contacts to be protected. A control circuit is connected to the control terminal of the semiconductor which is triggered on in response to the occurrence or immediately prior to the occurrence of the arcing condition.

These control circuits of the prior art generally respond to the occurrence of some condition associated with the arcing, such as the occurrence of a transient, the closing of a mechanical switch, energization of a relay coil, or some other similar condition. A problem associated with each of these prior art systems is that they are prone to operate erratically when the load being fed by the switch contacts to be protected is inductive or capacitive in nature wherein currents lead or lag the power source.

OBJECTS AND SUMMARY OF THE INVENTION

Accordingly it is an object of the present invention to provide a new and improved control circuit for eliminating contact arcing in control switches.

Another object is to provide a control circuit which can be used in combination with relay contacts to greatly reduce the size and expense of these contacts for a given current rating.

A still further object of the invention is to provide a power control circuit of the type described which is both simple and economical to build.

It is a further object of the invention to provide an arc elimination circuit including a control thyristor, the thyristor being actuated to shunt the contacts being protected only in response to the simultaneous occurrence of a plurality of arc indicative conditions, these conditions being sensed by a control network including a logic network.

Another object is to provide a general purpose arc elimination circuit which will operate satisfactorily with either resistive or highly reactive loads.

In accordance with the above invention, there is provided an arc elimination circuit comprising a thyristor connected in shunt relationship with the contacts to be protected. Coupled to the control electrode of the thyristor is a control circuit for sensing the simultaneous occurrence of a plurality of contact arc indicative conditions and operating said thyristor in response to these conditions. In the preferred embodiment of the invention, the control circuit is responsive to the occurrence of a characteristic transient voltage of a preselected magnitude across the load.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagramatic illustration of the principal components of the control circuits of the invention;

FIG. 2 is a schematic diagram of the control circuits which are shown diagramatically in FIG. 1;

FIG. 3 is a diagramatic illustration of the principal components of the modified control circuit in accordance with the invention;

FIG. 4 is a schematic diagram of the components included in the circuit of FIG. 3;

FIG. 5 is a diagramatic illustration of another embodiment of the invention, and

FIG. 6 is a schematic diagram of a circuit in accordance with the block diagram of FIG. 5.

DETAILED DESCRIPTION OF THE INVENTION

The basic concept of the invention is to provide a general purpose arc elimination circuit which has increased reliability by being responsive to the simultaneous occurrence of a plurality of arc-indicative conditions. The observation which underlies the invention is that the formation of an arc across a set of current carrying contacts is accompanied by a plurality of characteristic arc-indicative conditions across both the contacts themselves and in the associated circuits fed through these contacts.

It has been noted, for example, that an arc is normally preceded by a spark comprising a series of electrical spikes or impulses. These spikes or impulses may be sensed either across the contacts themselves or in the load. The reliability of a circuit which operates only in response to these high frequency spikes is poor, however, since similar signals may be generated by a variety of conditions other than arcing. For this reason, some of the embodiments of the invention include, in addition to a spark detector noted above, a detector which provides an output only after a load voltage of a preselected magnitude exists for a preselected time. In the embodiments of the invention utilizing this feature, an output is provided only after a load voltage of at least 10 volts is present for at least 1 microsecond.

By feeding the outputs of both the spark detector and the load voltage detector to a logic circuit which provides an output only upon the simultaneous occurrence of both these conditions, a substantial improvement in reliability is thereby obtained. The logic circuit controls a trigger circuit which switches a triac connected across the switch contacts, thereby shunting load current around the contacts, and reducing the voltage across the contacts to a value insufficient to sustain an arc.

The above discussed principles of the invention will be understood more thoroughly with reference to the block diagram of FIG. 1 which shows the main components of the preferred embodiment of the invention. In this figure, an a.c. source **12** is shown as being connected to the conductors **10** and **11**. In series across the source **12** is a switch **2** including a set of contacts **3** which are to be protected from the effects of arcing,

and a load 9. Across the contacts 3 is connected a bilateral semiconductor switch or "triac" 4.

The term "triac" is used herein to identify a three electrode a.c. semiconductor switch which is triggered into conduction by a gate signal in a manner somewhat similar to the action of a silicon controlled rectifier, but which differs therefrom in that it can conduct in both directions in response to a positive or negative gate signal. As is well known, the triac, when in its non-conductive or off state presents a high impedance to the flow of current, whereas when triggered to a conductive or on state, it presents a negligible impedance and can be considered in most circuit arrangements to be a short circuit. The triac 4 functions to shunt current around the contacts 3 upon the occurrence of preselected arcing conditions. The remaining components of the system of FIG. 1 of the invention function to control the state of the triac 4 in response to the arc-indicative conditions existing in the circuit.

A load voltage detector 7 senses the voltage across the load 9 and generates a signal when that voltage is a preselected magnitude, regardless of its polarity, as will be explained in greater detail below. The output from the voltage detector circuit 7 comprises a first input to a logic circuit which is illustrated as a coincidence or AND gate 6 in FIG. 1. The second input to the AND gate 6 is generated by a double differentiator and a.c. detector circuit 8 also connected across the load 9. The circuit 8 acts to pass only load voltages having a preselected characteristic, namely fast rise time pulses of either polarity. The voltage pulses passed by the differentiator circuit 8 comprise the second input to the AND gate 6, slow pulses being rejected or prevented from passing regardless of their magnitudes.

Upon the occurrence of the above noted preselected conditions across the load 9 (preselected voltage plus spark) and consequently the presence of suitable signals at both inputs to the AND gate 6, the trigger generating circuit 5 is activated to turn on the triac 4. With the triac 4 in the on condition, arcs formed across the contacts 3 are dissipated through the shunting short circuit of the triac 4.

Referring to FIG. 2, there is shown a schematic diagram of the embodiment of the invention shown diagramatically in FIG. 1 wherein the same reference numbers have been used to designate portions of the circuit noted above with respect to FIG. 1.

For operating the detector circuits of FIG. 2 there is provided a d.c. supply circuit (not shown in FIG. 1) for maintaining a d.c. voltage between the conductors 22 and 21. Conductor 21 is connected to the load side of the switch 2. Connected intermediate lines 22 and 21 is the parallel combination of two filter capacitors C_1 and C_5 in series with the resistor R_4. Conductor 22 is connected to supply line 10 via the diode D_1 and resistor R_1 and is connected to supply line 11 via diode D_2 and resistor R_2. Assuming the switch contacts 3 to be open, capacitors C_1 and C_5 are charged during each positive half cycle of the supply voltage via line 10, R_1, D_1, C_1 and C_5, R_4 and the load to the other side of the supply on line 11, with the conductor 22 becoming positive with respect to the conductor 21. With the switch contacts 3 closed, conductor 21 is at essentially the same potential as supply line 10, and on each negative half cycle of the supply, current flows to charge the capacitors C_1 and C_5 from line 11, via R_2, D_2, C_1 and C_5, resistor R_4 and conductor 21 to the other side of the supply on line 10. It is seen that a d.c. voltage is provided between the lines 21 and 22 regardless of whether the switch contacts 3 are open or closed.

The triac 4 is connected across the switch contacts 3 by having one of its load terminals connected to the supply line 10 and the other load terminal connected to the line 21. The gate electrode of the triac 4 is connected to the junction of the capacitors C_1 and C_5 and the resistor R_4. In the absence of arcing conditions across the contacts 3, the triac 4 is maintained in the non-conductive state by the voltage at the bottom of the capacitors C_1 and C_5 which is approximately the same as that on conductor 21.

The AND gate circuit 6 is comprised of the transistors Q_2 and Q_5 which are biased to be normally in the conductive or on condition. The collectors of the transistors Q_2 and Q_5 are coupled to the positive side of the d.c. supply on conductor 22 through a common load resistor R_5. The emitters of the transistors Q_2 and Q_5 are coupled directly to the negative side of the d.c. supply on conductor 21. The base of transistor Q_5 is coupled to the conductor 22 via the series combination of resistors R_8 and R_6, while the base of the transistor Q_2 is coupled to the conductor 22 via the resistor R_7. As noted above the biasing arrangement for the transistors Q_2 and Q_5 is selected to maintain these transistors in the conductive or on condition in the absence of arcing conditions, when the switch 2 is either closed or open.

The output of the AND gate 6 at the collectors of each of the transistors Q_2 and Q_5 operates the conventional one-shot trigger generating circuit 5 which includes the transistors Q_6 and Q_7. The collectors of Q_6 and Q_7 are coupled to the conductor 22 through a common resistor R_3. The bases of Q_6 and Q_7 are coupled to the conductor 22 through a common resistor R_3. The base of Q_6 comprises the input to the one-shot circuit 5 and is coupled to the output of the AND gate 6 at the collectors of the transistors Q_2 and Q_5. The emitter of transistor Q_6 is coupled to the base of transistor Q_7 and to the conductor 21 via the resistor R_9. The emitter of Q_7 is coupled directly to the negative side of the d.c. supply on conductor 21.

If either or both of the transistors Q_2 or Q_5 is in the on or conducting state, the base of Q_6 is held at approximately the same potential as its emitter due to the voltage drop across resistor R_5. When both the transistors Q_2 and Q_5 are turned off, current through R_5 is diverted through the base emitter circuit transistor Q_6 thereby turning it and transistor Q_7 on. As the transistors Q_6 and Q_7 turn on, a low resistance discharge path is created across the charged capacitors C_1 and C_5, causing a discharge current through the resistor R_4 to trigger the triac 4 on. With the triac triggered on, the contacts 3 of the switch 2 are short circuited.

The AND gate circuit 6 has two inputs, one at the base of the transistor Q_2, the other at the base of transistor Q_5. The first of these inputs is fed by a load voltage detector circuit generally indicated at 7 and comprising the transistors Q_1 and Q_8. The transistors Q_1 and Q_8 are connected such that either one will be conducting when a preselected voltage drop is present across the load 9, regardless of the polarity of that drop. For this purpose the base of the transistor Q_1 is coupled to one side of the load 9 through a resistor R_{14}, and the base of transistor Q_8 is coupled to the same one side of the load 9 through the resistor R_{14} and a diode D_3. The emitter of the transistor Q_1 and the collector of the

transistor Q_8 are coupled directly to the other side of the load. The junction between the diode D_3 and the base of the transistor Q_1 is coupled to the one side of the load via a resistor R_{13}. The collector of the transistor Q_1 and the emitter of the transistor Q_8 are coupled to the positive side of the d.c. supply on line **22** via the resistor R_7.

With the contacts **3** open and no arc-indicative conditions present in the circuit, no voltage will appear across the load **9** and neither of the transistors Q_1 or Q_8 will be turned on. With the switch **2** closed on the positive going half cycle of the a.c. supply **12**, the base of transistor Q_8 will be driven sufficiently negative with respect to the emitter thereof to turn it on. Similarly, on the negative going half cycle of the a.c. supply, the base of transistor Q_1 will be driven sufficiently positive with respect to the emitter thereof to drive it into conduction.

With the contacts **3** physically separated but connected by means of a current carrying arc, sufficient load voltage will be present to trigger either Q_1 or Q_8 depending on the polarity of the a.c. source at that time. With either Q_1 or Q_8 conducting, the voltage drop across the resistor R_7 drives the base of Q_2 (one input to the AND gate **6**) sufficiently negative to turn if off. It is thus seen that when either Q_1 or Q_8 is turned on by the presence of a preselected voltage across the load **9**, which is an arc-indicative condition, one of the two required signals for the operation of the AND gate **6** is generated.

The other input to the AND gate **6** at the base of Q_5 is fed by the transient voltage sensing circuit **8** generally comprising the transistors Q_3 and Q_4, and also including a double differentiator circuit including the capacitor C_3, resistor R_{10}, capacitor C_4, and resistor R_{11}.

The double differentiator circuit comprises the capacitor C_3 and resistor R_{10} connected in series with each other across the load **9** to form a first differentiating circuit. A second differentiating circuit comprising the capacitor C_4 and the resistor R_{11} is connected across the output of the first differentiating circuit, appearing across the resistor R_{10}. Since the load **9** is being fed by a reversible polarity source the output of the differentiating circuit may vary in polarity depending on the polarity of the source **12** at any given instant. For this reason, the output of the double differentiator combination, across resistor R_{11}, is coupled through a voltage dropping resistor R_{12} to a polarity detecting circuit comprising the transistors Q_3 and Q_4 which operate to provide a control signal to one of the inputs to the AND circuit **6** regardless of the polarity of the differentiator output.

In accordance with conventional biasing techniques, the collectors of transistors Q_3 and Q_4 are coupled to the positive side of the d.c. supply on line **22** through the resistors R_6 and R_8. The base of Q_4 is connected to one side of the differentiator output across the resistor R_{11} via the resistor R_{12}, while the emitter thereof is connected to the other side of the differentiator output at conductor **21**. In a similar, but juxtaopposed fashion, the base-emitter circuit of transistor Q_3 is connected across the output of the differentiator circuit by having its base connected to conductor **21** and its emitter connected to the one side of resistor R_{12}.

In the absence of a trigger pulse from the differentiator circuit, both transistors Q_3 and Q_4 are held nonconductive. However, if a transient voltage having a suitably high rate of change appears across the load **9**, a voltage pulse will appear across R_{11} of the double differentiator circuit. The polarity of this pulse will depend, of course, on the polarity of the source supply **12** at that particular time.

If this transient voltage is such that conductor **21** is positive with respect to supply line **11**, transistor Q_4 will be driven into conduction. However, if a high rise time load voltage of opposite polarity is present, the transistor Q_4 will be driven into conduction.

The output of the polarity detection circuits is present at the collectors of the transistors Q_3 and Q_4 and feeds the other input to the AND gate **6** at the base of transistor Q_5.

With both of the transistors Q_3 and Q_4 in their nonconductive states, the voltage at the base of transistor Q_5 (the second input to the AND gate **6**) is insufficient to turn it off. However, when eithe transistor Q_3 or Q_4 is rendered conductive, the current drawn through the resistors R_6 and R_8 pulls the voltage at the base of Q_5 sufficiently negative to turn it off.

As noted previously, if the transistors Q_2 and Q_5 are both turned off a suitable pulse is generated by the one-shot circuit **5** to turn off the triac **4.**

A further embodiment of the invention is illustrated diagramatically in FIG. **3,** wherein like numerals have been used to designate similar components previously described with reference to FIGS. **1** and **2.** Referring to FIG. **3,** it is noted that this embodiment is identical with the one shown in FIG. **1** except that instead of using a transient detector **8** across the load, a contact voltage detector circuit **15** is employed. The contact voltage detector circuit **15** is connected across the contacts **3** and responds to a preselected magnitude of voltage thereacross to generate a control signal which is fed to one input of the logic circuit **6.** In accordance with the previous embodiment, the other control signal to the logic circuit **6** is generated by the load voltage detector **7** which is connected across the load **9.** In addition, in contrast to the circuit of FIGS. **1** and **2** the output of the logic circuit **6** feeds a trigger amplifier circuit **16** which in turn operates the thyristor **4.**

Referring to FIG. **4** there is shown a schematic diagram of the circuit diagramatically illustrated in FIG. **3** wherein like numbers are used to designate similar components. The schematic diagram of FIG. **4** shows a pair of contacts **3** connected in series with a load **9** across a source **12.** A triac **4** is connected across the contacts **3** with its gate terminal coupled to a control circuit which generates a control pulse to fire the triac on the occurrence of preselected conditions.

The control circuit includes an AND gate **6** comprising the transistors Q_{13} and Q_{16} which generates a control pulse to be fed for amplification to a trigger amplifier circuit **16** comprising the transistors Q_{17} and Q_{18}. Referring to the schematic of FIG. **4,** it is seen that the transistors Q_{13} and Q_{16} are normally in the on or conductive state resulting in a current flow through their common load resistor R_{23} which turns of the transistors Q_{17} and Q_{18}. Under these conditions the triac **4** which has its load terminals connected across the contacts **3** is maintained in the off condition.

A d.c. voltage is provided across the capacitor C_{11} for the operation of the detection circuits of FIG. **4.** Capacitor C_{11} is charged from the supply **12** through diode D_{20}, the closed switch **3** and the resistor R_{22} on alternate half cycles of the supply. This charging action

maintains the conductor 21 positive with respect to the conductor 22.

The first input to the AND gate 6 is at the base of transistor Q_{16} and the seconddinput is at the base of transistor Q_{13}. The first input to the AND gate is fed by a load voltage detecting circuit 7 which operates in a fashion similar to that of the voltage detection circuit shown in FIG. 2 and its operation will therefore be only described previously hereinafter as follows: When a preselected voltage drop is present across the load 9, either the transistor Q_{10}, or the transistor Q_{12} will be switched from the off condition to the on condition. More specifically, with line 11 positive with respect to line 21, a current flows from the line 11 through resistors R_{33} and R_{34} to line 21. Hence, a trigger current flows through diode D_{21}, the base-emitter circuit of the transistor Q_{10} and resistor R_{27} to the conductor 22. This trigger current turns on the transistor Q_{10} which drives the base of the transistor Q_{13} sufficiently positive to render it non-conductive. Similarly, when a preselected voltage having a polarity such that line 21 is negative with respect to line 11 appears across the load 9, the transistor Q_{12} will be rendered conductive to turn off the transistor Q_{13}.

The second input to the AND gate 6 at the base of the transistor Q_{16} is generated by the contact voltage sensing circuit 15 generally comprising the transistors Q_{14} and Q_{15} which operates as follows: If a voltage appears across the contacts 3 of a sufficient magnitude and of a plurality such that the line 26 is positive with respect to the line 21, the resistor Q_4 is turned on to render the transistor Q_{16} non-conductive. In an analogous fashion, if the voltage across the contacts 3 is of a preselected magnitude and an opposite polarity to that just described, the transistor Q_{15} will be switched into its conductive state to turn off the transistor Q_{16}.

It is thus seen that two inputs are provided to the AND gate upon the simultaneous occurrence of (a) a preselected voltage magnitude of either polarity across the load 9 and (b) a preselected magnitude of voltage across the contacts 3 of either polarity. With these two inputs simultaneously present at the AND gate, transistors Q_{13} and Q_{16} are cut off, thereby driving the base of transistor Q_{17} positive. The connection between transistors Q_{17} and Q_{18} renders both of these transistors conductive at which time the triac 4 is triggered on to short circuit the contacts of the switch 2 to dissipate the arc formed thereacross.

A still further embodiment of the invention can be seen with reference to the block diagram of FIG. 5 wherein like numbers have been used to identify similar circuits previously described. Referring to FIG. 5, the circuit is generally similar to those of FIGS. 1 and 3 with the exception that the AND gate circuit 6 is provided with three inputs, instead of the previous two described with respect to FIGS. 1–4.

A first input to the AND gate is provided by a tuned circuit 40 which is connected across the load 9 and responds to a preselected high frequency signal across the load to generate a control signal. As stated above, the arc formed across a set of contacts is generally preceded by a "spark," the spark consisting of a short burst of high frequency voltage impulses. The tuned circuit 40 is excited into oscillation upon the occurrence of this spark signal across the load 9. The spark signal can be detected equally well across either the contacts to be protected or the load (as shown in FIG. 4) or at various other points in the circuit.

The second and third inputs to the AND gate are generated by voltage sensing circuits 7 and 15 which generate suitable input signals to the AND gate 6 in the presence of preselected voltages across the load and the contacts. If these preselected voltages across the load and contacts are present concurrently with the control signal from the tuned circuit 40, the AND gate 6 will be activated to turn on the triac 4. However, if either one of the voltages across the contacts or across the load is substantially zero, one of the input signals required for activation of the AND gate 6 will be absent and subsequent shorting of the contacts 3 by the triac 4 will not occur. These voltage sensing circuits improve the reliability of the tuned circuit detector 40 across the load by insuring that the contacts will be shorted out only when a plurality of arc-indicative conditions have been detected. Thus, if the contacts are fully closed, the occurrence of a transient voltage burst in the load due to the nature of the load itself, such as an electric drill, will not activate the triac 4.

Referring to FIG. 6 there is shown a schematic diagram of the circuit diagramatically illustrated in FIG. 5 wherein like numbers have been used to designate similar components previously described. As in the previously described circuit arrangements a switch 2 including a set of contacts 3 is coupled in series with a load 9 across the supply lines 10 and 11, the supply lines being connected to an a.c. source (not shown) via a connector 41. A triac 4 is coupled across the contacts 3 so as to short out these contacts to eliminate arcs upon the occurrence of preselected conditions.

As in the previous circuits, a d.c. voltage for the operation of the sensing circuits is generated between the lines 43 and 42. The d.c. voltage supply circuit includes the voltage divider comprising the resistors R_{51} and R_{52} which are coupled directly across the supply lines 10 and 11. On positive half cycles of the supply, the capacitor C_{42}, resistor R_{49} and the load 9. The d.c. voltage across the lines 43 and 42 is connected to the various sensing circuits to provide the desired biasing of the various components.

The AND gate circuit 6 0f FIG. 6 provides a suitable output voltage on the line 45 only upon the simultaneous occurrence of the three above discussed conditions. The output voltage on line 45 is held highly negative with respect to line 43 in the absence of any one of these arc-indicative conditions. With the voltage at the output of the AND gate 6 on line 45 highly negative, the trigger amplifier circuit 16 comprising the transistors Q_{51} and Q_{52} is held in a non-conductive state. With the trigger amplifier circuit 16 held nonconductive, no trigge pulse is fed to the gate electrode of the triac 4 and it is held in its off condition.

The AND gate 6 generally comprises the diode D_{40} and the transistors Q_{41} and Q_{42}. These components provide three parallel low impedance paths between line 45 and line 42 of the d.c. supply thereby holding line 45 at a highly negative potential, except upon the simultaneous occurrence of particular arc-indicative conditions, at which time these components are switched to their high impedance states, thereby allowing the voltage on line 45 to rise sharply.

The first two low impedance paths comprise the collector emitter circuits of transistors Q_{41} and Q_{42}. Both of the transistors Q_{41} and Q_{42} have their collectors cou-

pled to the positive side of the d.c. supply on line **43** via the common load resistors R_{41}. The emitters of each of the transistors Q_{41} and Q_{42} are connected directly to the negative side of the d.c. supply on line **42.** The bases of the transistors Q_{41} and Q_{42} are each connected to the positive d.c. supply line **43** by resistors R_{42} and R_{43}, respectively. The bases of the transistors Q_{41} and Q_{42} are also connected to voltage sensing circuits **7** and **15** which operate to trigger these transistors from the conducting to the non-conducting condition.

The biasing arrangement for the transistors Q_{41} and Q_{42} maintains them normally in the conductive state. As long as either of the transistors Q_{41} and Q_{42} is conducting, a low impedance path is maintained between the line **45** (output of AND gate) and the negative side of the d.c. supply, thereby holding line **45** highly negative.

The third low impedance path between the line **45** and the line **42** is provided by the diode D_{40} and inductor L_1. The inductor L_1 is part of a tuned circuit, the operation of which will be explained in greater detail hereinafter. During normal operation of the circuit, i.e., in the absence of arcing conditions, the diode D_{40} is forward biased by the voltage drops across transistors Q_{41} and Q_{42} to provide, in combination with the inductor L_1, a third low impedance path from line **45** to line **42.** This last mentioned low impedance path, being in parallel with the other previously mentioned low impedance paths (the collector emitter circuits of transistors Q_{41} and Q_{42}) is also independently capable of holding the line **45** at a highly negative potential.

A first input to the AND gate **6** is generated at the base of transistor Q_{41} and is connected to the output of the load voltage sensing circuit **7** generally comprising the transistors Q_{47}, Q_{48} and Q_{49}, all of these transistors being in the non-conductive state in the absence of a preselected load voltage. Transistors Q_{48} and Q_{49} are of the NPN type, while transistor Q_{47} is of the PNP type. The collector of transistor Q_{48} and the emitter of transistor Q_{47} are connected to the positive side of the d.c. supply on line **43** through the resistor R_{42}. The emitter of transistor Q_{48} and the collector of transistor Q_{47} are coupled directly to the negative side of the supply on line **42** which in turn is connected to one side of the load **9.** The base of transistor Q_{48} is connected to the emitter of transistor Q_{49} and to one side of the load via the resistor R_{47} and conductors **49, 50** and **11.** The base of transistor Q_{47} is connected to the collector of transistor Q_{49}. The base of transistor Q_{49} is connected directly to the negative side of the d.c. supply on line **42** which in turn is coupled to the switch side of the load **9.**

The load voltage detector circuit **7** operates as follows: When the load voltage is of a preselected magnitude and of a polarity such that line **42** is positive with respect to line **11,** current will flow through the base emitter circuit of transistor Q_{49}, turning it on. As the transistor Q_{49} turns on its collector voltage and consequently the voltage at the base of transistor Q_{47} are driven negative to thereby render the transistor Q_{47} conductive. With transistor Q_{47} conducting, base emitter current in transistor Q_{41} is diverted through transistor Q_{47}, thereby rendering transistor Q_{41} non-conductive. With load voltage such that line **42** is negative, transistor Q_{48} is rendered conductive, thereby diverting base current from transistor Q_{41} and turning it off.

A second input to the AND gate circuit **6** is coupled to the base of transistor Q_{42} and acts to switch transistor Q_{42} from its low impedance state to its high impedance state. This second input is provided by a voltage contact detector circuit **15** generally comprising the transistors Q_{43}, Q_{44} and Q_{45}. This contact voltage detector circuit **15** is substantially identical in arrangement and operation to the load voltage circuit **7** of FIG. **6,** and will be described only briefly hereinafter. The contact voltage detector circuit is rendered conductive upon the occurrence of a preselected magnitude of contact voltage of either polarity. For this purpose, transistors Q_{43} and Q_{45} have their base emitter circuits coupled across the switch contacts **3** via the lines **42** on one side, and via resistor R_{44} and conductors **47, 48** and **10** on the other side.

Upon the occurrence of a preselected magnitude of voltage across the contacts **3** having a polarity such that line **42** is positive with respect to line **10,** transistor Q_{45} is rendered conductive which causes transistor Q_{44} to conduct, thereby providing a negative-going voltage pulse at the base of transistor Q_{42} and rendering it non-conductive. In an analagous fashion, if the voltage across the contacts **3** is of a preselected magnitude and a polarity such that the line **10** is positive with respect to the line **42,** a base current flows through transistor Q_{43} to render it conductive, thereby again rapidly decreasing the voltage at the base of transistor Q_{42} and rendering this transistor non-conductive.

Under either of the above noted conditions, one of the previously described low impedance paths comprising the AND gate **6** between line **45** and common line **42** is switched to a high impedance condition.

The third input to the AND gate **6** is provided by the tuned circuit arrangement consisting of the inductor L_1 and capacitor C_{40} which are connected in parallel to each other across the load **9** via the line **42** on one side and the capacitor C_{41} and lines **49, 50** and **11** on the other side.

The tuned circuit detecting circuit **40** operates on the principle that an arc formed between switch contacts is generally accompanied by a spark or burst of high frequency voltage impulses which can be detected across the contacts themselves or at other points in the circuit by connecting the tuned circuit across the load **9,** as shown in FIG. **6.** This voltage burst drives the tuned circuit into oscillation at the resonant frequency of the tuned circuit.

In a sense, the spark acts as an energy source to shock the resonant circuit into oscillation. Part of this oscillation is used to back bias the diode D_{40} thereby changing it from its low impedance state to its high impedance state and, in the presence of the other described conditions, permitting the voltage on line **45** to rise rapidly in the positive direction, thereby rendering the trigger amplifier circuit **16** conductive to trigger the triac **4.**

The frequency to which the combination of capacitor C_{40} and inductor L_1 is tuned can vary within certain limits. An upper limit for this frequency is the duration of the pulse required to trigger the triac **4.** More specifically, the output of the AND gate must be sufficiently long in duration to permit the trigger amplifier **16** to remain conductive long enough to trigger the triac **4.** Preferably, the oscillation of the tuned circuit should be low enough in frequency so that a half wave thereof is approximately two to four times longer than the nec-

essary gate trigger time for the triac 4. Of course, it would be possible to use a pulse stretching circuit in conjunction with a shorter duration AND gate output to provide the necessary triac triggering pulse.

The lower limit for the resonant frequency of the tuned circuit is chosen so that the oscillation of the tuned circuit is very rapid compared to the frequency of the power supply being interrupted by the contacts 3, which is usually 60 cps commercial power.

If the tuned frequency is chose to be too low, the delay between the beginning of the arc and the time at which the triac 4 is made conductive will be too long enough to permit serious damage to the contacts 3. Preferably, the life of any arc should be limited to the small fraction of the duration of a half a cycle of line or power supply frequency. A frequency of between 10 and 30 KHz has been found to operate satisfactorily in this type of circuit.

The capacitor C_{41} serves to provide a high impedance at line frequency between one side of the load and the tuned circuit to thereby isolate it during normal operation of the circuit.

The overall operation of the circuit of FIG. 6 is as follows: With the switch 2 fully open or closed with no arcing conditions present in the circuit, one of the transistors Q_{41} and Q_{42} is conducting, and diode D_{40} is forward biased to provide two low impedance paths from line 45 to line 42. Under these conditions, transistors Q_{51} and Q_{52} of the trigger amplifier and the triac 4 are non-conductive.

In the circuits of the invention, particularly the embodiments of FIGS. 3–6, advantage is taken of the fact that only during an arc condition is there voltage across both the contacts and the load, this being true due to the flow of current to the load through the arc and the simultaneous voltage across the contacts under arcing conditions. Contacts which are completely closed (with contact bounce completed and no arcing thereacross) generally have only an insignificant voltage drop thereacross and a fully open set of contacts causes no voltage drop across the load.

Upon the simultaneous occurrence of three arc-indicative conditions, namely, preselected contact voltage, preselected load voltage and the occurrence of a high frequency spark, each of these low impedance paths are switched to a high impedance state, as explained hereinbefore, thereby providing a positive-going voltage pulse on line 45 to trigger transistors Q_{51} and Q_{52}. As the transistors Q_{51} and Q_{52} turn on, the capacitor C_{42} discharges to develop a negative trigger pulse across the resistor R_{49} to render the triac 4 conductive. When the triac 4 is rendered conductive, the voltage across the contacts 3 is reduced to a value insufficient to sustain an arc.

One skilled in the art will recognize that various combinations of the arc condition sensing means may be employed to achieve the stated purposes and the invention is not limited to the use of any particular combination. The specific embodiments disclosed herein are only illustrative of various combinations within the principle of the invention.

Having described this invention, what I claim is:

1. A circuit for eliminating acrs formed upon the opening or closing of a pair of contacts comprising a thyristor having first and second load electrodes and a control electrode, said load electrodes connected across said contacts, and logic circuit means having first and second inputs and an output, said output coupled to said control electrode, said first input coupled to a load voltage detector circuit, said load voltage detector circuit connected across said load and responsive to a preselected voltage to generate a first control signal, said second input connected to a transient voltage detecting circuit, said detecting circuit being connected across said load and responsive to a voltage having a predetermined rise time characteristic to generate a second control signal, whereby said logic circuit means generates a signal for controlling said thyristor in response to the simultaneous occurrence of said first and second signals.

2. The combination recited in claim 1 wherein said transient voltage detecting circuit comprises a differentiator circuit.

3. The combination recited in claim 1 wherein said thyristor comprises a triac.

4. The combination recited in claim 1 wherein said transient voltage detecting circuit is responsive to preselected transient voltages of opposite polarity.

5. The combination recited in claim 4 wherein said load voltage detector circuit is responsive to preselected load voltages of opposite polarity.

6. The combination recited in claim 2 wherein said differentiator circuit comprises a first differentiating combination connected across said load and a second differentiating circuit combination coupled to the output of said first differentiating combination, and circuit means coupling the output of said second differentiating combination to said second input.

7. A circuit for eliminating arcs formed across contacts upon opening and closing thereof comprising means for generating a plurality of control signals upon the occurrence of preselected arc-indicative conditions in said circuit, logic circuit means responsive to said control signals for generating a control pulse, and a thyristor connected across said contacts and responsive to said control pulse to substantially short circuit said contacts upon the occurrence of said control pulse, said first mentioned means comprises load voltage detecting means for generating a first control signal upon the occurrence of a preselected voltage across said load, and contact voltage detecting means for generating a second control signal upon the occurrence of a preselected voltage across said contacts, said first mentioned means further comprises a tuned circuit detecting means for generating a third control signal upon the occurrence of a transient high frequency voltage burst across said load, and said logic circuit means generates said control pulse upon the simultaneous occurrence of said first, second and third control signals.

8. A circuit for eliminating arcs formed across contacts upon opening and closing thereof comprising means for generating a plurality of control signals upon the occurrence of preselected arc-indicative conditions in said circuit, logic circuit means responsive to said control signals for generating a control pulse, and a thyristor connected across said contacts and responsive to said control pulse to substantially short circuit said contacts upon the occurrence of said control pulse, said first mentioned means includes a transient voltage detecting circuit for generating a first control signal upon the occurrence of a transient voltage across said load having predetermined rise time characteristics and also including load voltage detecting means for generating a second control signal upon the occurrence of a preselected voltage across said load.

9. The combination recited in claim 7 wherein said transient voltage detecting means and said load voltage detecting means are responsive to preselected voltages of either polarity.

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