AU 629548

FORM 1

COMMONWEALTH OF AUSTRALIA

PATENTS ACT 1952

APPLICATION FOR A STANDARD PATENT

I\We,

SONY CORPORATION

of 7-35 KITASHINAGAWA 6-CHOME
SHINAGAWA-KU
TOKYO
JAPAN

hereby apply for the grant of a standard patent for an invention entitled:

APPARATUS FOR DECODING A DIGITAL SIGNAL.

which is described in the accompanying complete specification

Details of basic application(s):

Number of basic application	Name of Convention country in which basic application was filed	Date of basic application
127888/88	JP	25 MAY 88

My/our address for service is care of GRIFFITH HACK & CO., Patent Attorneys, 601 St. Kilda Road, Melbourne 3004, Victoria, Australia.

DATED this 22nd day of May 1989

SONY CORPORATION

GRIFFITH HACK & CO.

TO: The Commissioner of Patents.

GRIFFITH HACK & CO.

601 ST. KILDA ROAD, MELBOURNE,
VICTORIA 3004, AUSTRALIA
TELEPHONE: (03) 529 8600
FAX: 613 529 6296

Australian Patent Declaration Form

Forms 7 and 8

AUSTRALIA

Patents Act 1952

DECLARATION IN SUPPORT OF A CONVENTION OR NON-CONVENTION APPLICATION FOR A PATENT OR PATENT OF ADDITION

Name(s) of Applicant(s)

In support of the application made by SONY CORPORATION

for a patent for an invention entitled

Title

APPARATUS FOR DECODING A DIGITAL SIGNAL

Name(s) and address(es) of person(s) making declaration

I/~~We~~, Shoji Wakayama, General Manager, Patents Div. of c/o SONY CORPORATION, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, Japan

do solemnly and sincerely declare as follows:—

1. I am/we are the applicant(s) for the patent, or authorised by the abovementioned applicant to make this declaration on its behalf.

2. The basic application(s) as defined by Section 141 of the Act was/were made in the following country or countries on the following date(s) by the following applicant(s) namely:-

Country, filing date and name of Applicant for the or each basic application

in JAPAN on May 25, 1988
by SONY CORPORATION
in _____ on _____ 19 ____
by _____

3. The said basic application(s) was/were the first application(s) made in a Convention country in respect of the invention the subject of the application.

4. The actual inventor(s) of the said invention is/are

Name(s) and address(es) of the or each actual inventor

Keiji Kanota, Hajime Inoue and Takahito Seki of all c/o SONY CORPORATION, 7-35, Kitashinagawa 6-chome, Shinagawa-ku, Tokyo, Japan

5. The facts upon which the applicant(s) is/are entitled to make this application are as follows:-

See reverse side of this form for guidance in completing this part

The applicant is the assignee of the actual inventor(s).

DECLARED at Tokyo, Japan this 15 day of May 19 89

SONY CORPORATION

Shoji Wakayama / General Manager, Patents Div.

(12) PATENT ABRIDGMENT (11) Document No. AU-B-35081/89
(19) AUSTRALIAN PATENT OFFICE (10) Acceptance No. 629548

(54) Title
DIGITAL VTR DECODER

International Patent Classification(s)
(51)[4] **H04N 005/93**

(21) Application No. : **35081/89** (22) Application Date : **22.05.89**

(30) Priority Data

(31) Number	(32) Date	(33) Country
63-127888	**25.05.88**	**JP JAPAN**

(43) Publication Date : **30.11.89**

(44) Publication Date of Accepted Application : **08.10.92**

(71) Applicant(s)
SONY CORPORATION

(72) Inventor(s)
KEIJI KANOTA; TAKAHITO SEKI; HAJIME INOUE

(74) Attorney or Agent
GRIFFITH HACK & CO , GPO Box 1285K, MELBOURNE VIC 3001

(56) Prior Art Documents
US 4890161
US 4768108
EP 117719

(57) Claim

1. An apparatus for decoding a transmitted signal comprising:

a) receiver means for receiving said transmitted signal;

b) filter means for limiting the frequency of the output of said receiver means within a predetermined frequency;

c) generator means for generating a clock signal with a frequency equal to a transmitting rate of said signal from the output of said receiver means;

d) converter means for sampling the output of said filter means by said clock signal and converting the same into a binary signal; and

e) process means for processing the output of said converter means to decode said transmitted signal by a

.../2

predetermined method.

2. An apparatus according to claim 1, wherein said predetermined method is class IV partial response method.

5. An apparatus according to any one of the preceding claims, wherein the cut-off frequency of said filter means is a Nyquist frequency of said transmitted signal.

AUSTRALIA

PATENTS ACT 1952

Form 10

629548

COMPLETE SPECIFICATION

(ORIGINAL)

FOR OFFICE USE

Short Title:

Int. Cl:

Application Number:
Lodged:

Complete Specification-Lodged:
Accepted:
Lapsed:
Published:

Priority:

Related Art:

TO BE COMPLETED BY APPLICANT

Name of Applicant:
SONY CORPORATION

Address of Applicant: 7-35 KITASHINAGAWA 6-CHOME
SHINAGAWA-KU
TOKYO
JAPAN

Actual Inventor:

Address for Service: GRIFFITH HACK & CO.,
601 St. Kilda Road,
Melbourne, Victoria 3004,
Australia.

Complete Specification for the invention entitled:
APPARATUS FOR DECODING A DIGITAL SIGNAL

The following statement is a full description of this invention including the best method of performing it known to me:-

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to an apparatus for decoding a digital signal and, more particularly, is directed to an apparatus for decoding a digital signal for use with a digital video tape recorder and so on.

Description of the Prior Art

In order to understand the present invention more clearly, let us first explain the problems inherent in a digital magnetic recording and reproducing apparatus such as a digital video tape recorder and the like.

In the digital magnetic recording and reproducing apparatus, if digital data series (represented in the binary form of "1" or "0") is directly recorded, the following problems 1 to 3 are presented.

1. A maximal frequency of a recorded signal is increased so high that the recorded signal cannot be read.

2. A lot of direct current components and low frequency components frequently appear in the recorded signal so that when a digital signal is recorded and reproduced by utilizing a rotary transformer, a distortion occurs in a reproduced signal. As a result, it is frequently observed that the reproduced information becomes considerably different from the recorded information.

3. When digital data is recorded, data series is generally recorded together with a clock component according to the so-called self-clock system. If digital "1" or "0" is recorded too contiguously, then the error rate in extracting the clock component at the playback side is increased.

In order to solve the above-mentioned problems, the

digital magnetic recording and reproducing apparatus is arranged so as to record and reproduce a digital data signal as follows.

According to this digital magnetic recording and reproducing apparatus, upon recording, a digital input signal is converted to a recording signal having a predetermined frequency characteristic by a channel coding (recording and encoding) circuit. Then, this recording signal is recorded on a magnetic record medium by a recording head. Upon playback, a signal reproduced from the magnetic record medium by a playback head is supplied to and is reproduced by a decoder whose converting characteristic is just opposite to that of the channel coding circuit. The channel coding system might be the Nonreturn to Zero-Inverted (NRZ-I) system, Interleaved NRZ-I (I-NRZ-I) system and Scrambled I-NRZ-I (S-I-NRZ-I) system based on a partial response system (PR system) which makes effective use of intersymbol interference in the digital recording.

According to the NRZ-I system, an NRZ signal of binary code form is converted to an NRZ-I recording signal. The encoder which converts the input signal to the recording signal just before the transmission line might be called a precoder. The NRZ-I system precoder is called a PR (1, -1) encoder because it effects the coding that is the conversion just opposite to the conversion of PR (1, -1) transmission line based on the partial response system. The NRZ-I system has, on the other hand, a disadvantage that when the signal is not inverted, a direct current component frequently increases.

According to the I-NRZ-I system, an NRZ signal is

converted to an I-NRZ-I recording signal. The I-NRZ-I system precoder performs the conversion reverse to that in a PR (1, 0, -1) transmission line based on the class IV partial response and is called a PR (1, 0, -1) encoder or a class IV partial response encoder.

An identifying signal, which results from recording and reproducing the I-NRZ-I recording signal, has frequency characteristics similar to those of the magnetic recording and reproducing systems so that it contains less high frequency components and that it does not contain direct current (DC) components. In addition, the identifying signal cannot be affected by the cross-talk component caused by the increased wavelength of the recording signal and also it cannot be affected by the rotary transformer of the head system.

Although the identifying signal reproduced according to the I-NRZ-I system does not contain direct current components, the recording signal contains direct current components. In order to reduce the direct current component of the recording signal, the S-I-NRZ-I system is proposed. According to the S-I-NRZ-I system, adding the M series signal (represented in the form of binary random number) to the input signal in mod. 2 (or to scramble the input signal by the M series signal), it is possible to reduce the direct current components.

Fig. 1 is a block diagram showing an arrangement of a prior-art digital video tape recorder using the above-mentioned channel coding circuit of the S-I-NRZ-I system.

Referring to Fig. 1, it will be seen that an analog

video signal is supplied to an input terminal 1. This analog video signal is supplied to an analog-to-digital (A/D) converter 2, in which it is converted to a digitized data signal. The digitized data signal is supplied through a bit reduction encoder 3 to an error correction code (ECC) encoder 4, in which it is encoded to have a parity code for the error-correction. The data signal having the parity code is supplied to an M scramble circuit 5 and is thereby converted, for example, to a signal having no direct current (DC) components corresponding to a characteristic of a head-tape system which will be described later. The scramble circuit 5 utilizes a so-called M series signal as a pseudo-random signal and hence is called the M scramble circuit. The signal thus converted is supplied to an adder 6, whereby it is added with a synchronizing (SYNC) code from a terminal 7.

The signal having the synchronizing code added is supplied to an adder 8, and the output signal of the adder 8 is fed through delay elements 9a and 9b back to the adder 8. Each of the delay elements 9a and 9b has a sampling cycle D. The adder 8 and the delay elements 9a and 9b constitute a class IV partial response (PR) (1, 0, -1) precoder shown by a broken line block in Fig. 1, thereby effecting the processing of $[\frac{1}{1 - D^2}]$ according to the class IV partial response system.

The signal from the adder 8 is supplied through a recording amplifier 10 to a recording head 11 and is thereby recorded on a tape 12.

The recorded signal is reproduced from the tape 12 by means of a playback head 13 and a playback amplifier 14.

The electromagnetic transducing system formed of the recording head 11, the tape 12 and the playback head 13 has a characteristic of [1 - D].

The signal from the playback amplifier 14 is supplied through an equalizer 15 to an adder 16, and the signal from the equalizer 15 is supplied through a delay element 17 having a sampling cycle D to the adder 16. The adder 16 and the delay element 17 constitute a class IV partial response (PR) (1, 1) decoder as shown by a broken line block in Fig. 1. Accordingly, when the characteristic [1 - D] of the electromagnetic transducing system formed by the recording head 11, the tape 12 and the playback head 13 is combined with the characteristic [1 + D] of the class IV PR (1, 1) decoder formed of the adder 16 and the delay element 17, there is presented the characteristic $[1 - D^2]$. This characteristic $[1 - D^2]$ is complemetary to the characteristic $[\frac{1}{1 - D^2}]$ of the above-mentioned class IV PR (1, 0, -1) decoder. Accordingly, the following equation is established.

$$\frac{1}{1 - D^2} \times (1 - D) \times (1 + D) = 1$$

Thus, the transmission with transfer function "1" is carried out, and a ternary signal (1, 0, -1) of class IV partial response system is generated.

This ~~ternary~~ ternary signal is supplied to a ~~ternay~~ ternary signal comparator 18 from which there is decoded a signal which is not yet precoded in the recording mode. The thus decoded signal is supplied through an M descrambl. circuit 19 to a time base corrector 20, in which it is timebase-corrected. The signal from the time base corrector 20 is supplied through a bit reduction decoder 22 to a digital-to-analog

(D/A) converter 23, in which it is converted to an analog video signal. This analog video signal is supplied to an output terminal 24.

The signal from the ternary signal comparator 18 is supplied to a synchronizing (SYNC) code detecting circuit 25, and the synchronizing code detected is supplied to a terminal 26.

In the digital circuit system formed of the circuit elements from the A/D converter 2 to the D/A converter 23 of the prior-art digital video tape recorder, a video signal is processed in a digital fashion in the recording system from the A/D converter 2 to the class IV PR (1, 0, -1) precoder formed of the adder 8 and the delay elements 9a and 9b, whereas a video signal is processed in an analog fashion in the reproducing system from the playback head 13 to the ternary comparator 18. A video signal is therefore processed in a digital fashion by a circuit system from the M descramble circuit 19 to the D/A converter 23.

Hence, the equalizer 15, the adder 16 and the delay element forms a decoder system which processes a video signal in an analog fashion. In the analog data processing, it is frequently observed that error occurs in the data signal due to temperature characteristic and aging change.

Further, the delay element 17 forming the class IV partial response (1, 1) decoder is formed of an analog delay line so that the delay time of the delay element 17 cannot be varied without difficulty. As a result, when transmission rate is changed upon cue or review playback mode, it is difficult to vary the sampling frequency in accordance with the transmission rate varied.

In order to solve the above-mentioned problems, it is proposed that the output signal from the playback amplifier 14 is converted in the form of analog to digital signal and the circuit elements from the equalizer 15 to the ternary signal comparator 18 perform the processing in a digital fashion. The digital processing generally requires a sampling frequency twice as high as the transmission rate of a transmission signal from a sampling theorem standpoint. The digital video tape recorder or the like, in particular, requires a very high sampling frequency, which cannot be realized in practice.

OBJECTS AND SUMMARY OF THE INVENTION

It is an object of the present invention to provide an apparatus for decoding a transmitted signal which is less susceptible to the above-mentioned defects of the prior art.

More specifically, it is an object of the present invention to provide an apparatus for decoding a signal in which the signal can be digitally processed at an earlier stage.

According to the present invention, there is provided an apparatus for decoding a transmitted signal comprising:

a) receiver means for receiving said transmitted signal;

b) filter means for limiting the frequency of the output of said receiver means within a predetermined frequency;

c) generator means for generating a clock signal with a frequency equal to a transmitting rate of said signal from the output of said receiver means;

d) converter means for sampling the output of said filter means by said clock signal and converting the same into a binary signal; and

e) process means for processing the output of said converter means to decode said transmitted signal by a predetermined method.

According to the present invention, a transmitted signal can be digitally processed by an equalizer or the like, whereby influences such as temperature characteristic_____

and aging change can be reduced, and a digital signal can be reproduced satisfactorily.

The above, and other objects, ~~features~~ and advantages of the present invention will be apparent from the following detailed description of a preferred embodiment of the invention when read in conjunction with the accompanying drawings, wherein like reference numerals identify the same or similar elements.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing an example of a prior-art digital video tape recorder;

Fig. 2 is a diagram of the frequency spectrum of a reproduced signal used to explain the present invention; and

Fig. 3 is a block diagram of an embodiment of an apparatus for decoding a digital signal according to the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

An embodiment of an apparatus for decoding a digital signal according to the present invention will hereinafter be described with reference to Figs. 2 and 3.

When the class IV partial response system is employed as the recording and reproducing system, the frequency spectrum of a reproduced signal is represented as shown in Fig. 2, in which $\frac{1}{2T}$ is an Nyquist frequency and $\frac{1}{T}$ a transmission rate.

Referring to Fig. 3 which shows an embodiment of the present invention, there is shown a tape 31 on which a video signal is recorded according to the class IV partial response system. The recorded signal is reproduced from the tape 31 by means of a playback head 32 and a playback

amplifier 33.

The signal from the playback amplifier 33 is supplied to a low-pass filter 34 whose cut-off frequency corresponds to the Nyquist frequency of the recorded signal. The signal from the low-pass filter 34 is supplied to an analog-to-digital (A/D) converter 35, in which it is converted to a digital signal. The signal from the playback amplifier 33 is also supplied through a multiply-by-2 circuit 36 to a phase-locked loop circuit 37 which generates a clock signal with the frequency fs equal to the transmission rate. This clock signal is supplied to a terminal 38 as well as to the A/D converter 35. Hence, the A/D converter 35 generates a digitized signal of, for example, 8 bits in response to the clock signal.

The apparatus of the present invention utilizes the class IV partial response system so that even when the sampling is effected by the clock signal with the frequency fs equal to the transmission rate, then a problem of so-called aliasing noise or the like can be avoided.

The digitized signal from the A/D converter 35 is supplied to serially-connected data latch circuits 39a to 39c. The clock signal is supplied to the serially-connected data latch circuits 39a to 39c so that the data latch circuits 39a to 39c generate signals each delayed by the sampling cycle D (transmission rate). These signals are weighted by predetermined weight ratios by weighting circuits 40a to 40c, and are then added together by an adder 41.

The circuit arrangement formed from the latch circuit 39a to the adder 41 constitutes a transversal filter. Thus,

a desired equalizer characteristic can be presented by freely determining the coefficients of the weighting circuits 40a to 40c.

The signal from the adder 41 is supplied to an adder 42 and is also supplied to a data latch circuit 43. The clock signal is supplied to the data latch circuit 43, and the output signal of the latch circuit 43 is supplied to the adder 42, whereby the adder 42 and the latch circuit 43 constitute a class IV partial response (PR) (1, 1) decoder as shown by a broken line block in Fig. 3, thereby performing the decoding expressed as [1 + D].

The signal from the adder 42 is supplied to a digital ternary signal comparator 44, and the compared output signal of one bit is fed to a terminal 45.

The signal developed at the terminal 45 is supplied to the afore-noted M descramble circuit 19 (see Fig. 1) which reproduces (or descrambles) a video signal.

As described above, according to the above embodiment of the present invention, since the video signal can be digitally processed by the equalizer and so on at the first stage of the apparatus, influences due to temperature characteristic, aging change and the like can be reduced. Hence, the apparatus of the invention can reproduce the digital signal satisfactorily.

Since in the above embodiment the data latch circuit is employed as the delay element, the analog delay line can be removed, which provides an increased accuracy from a design standpoint and also a decreased cost from a manufacturing-process standpoint. Further, the circuit elements of the apparatus can cope with the cue playback

mode and the review playback mode with ease.

Furthermore, the circuit elements of the apparatus of the invention can be fabricated as an integrated circuit (IC) and can be logically designed, which provides a highly-effective circuit and also a high performance.

In addition, in the above-mentioned circuit arrangement of the present invention, the output signal of the adder 42 is converted to the analog signal by a D/A converter 46, and the analog signal is supplied through a low-pass filter 47 to a terminal 48, whereby an analog eye pattern can be monitored.

It should be understood that the above description is presented by way of example on a single preferred embodiment of the invention and it will be apparent that many modifications and variations could be effected by one skilled in the art without departing from the spirit and scope of the novel concepts of the invention so that the scope of the invention should be determined only by the appended claims.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. An apparatus for decoding a transmitted signal comprising:

a) receiver means for receiving said transmitted signal;

b) filter means for limiting the frequency of the output of said receiver means within a predetermined frequency;

c) generator means for generating a clock signal with a frequency equal to a transmitting rate of said signal from the output of said receiver means;

d) converter means for sampling the output of said filter means by said clock signal and converting the same into a binary signal; and

e) process means for processing the output of said converter means to decode said transmitted signal by a predetermined method.

2. An apparatus according to claim 1, wherein said predetermined method is class IV partial response method.

3. An apparatus according to claim 1 or 2, wherein said receiver means is a magnetic head and said signal is transmitted through a magnetic medium by recording.

4. An apparatus according to any one of the preceding claims, wherein said signal is precoded in a recording process in accordance with said class IV partial response method.

5. An apparatus according to any one of the preceding claims, wherein the cut-off frequency of said filter means is a Nyquist frequency of said transmitted signal.

6. An apparatus according to any one of the preceding claims, wherein said process means has an equalizer.

7. An apparatus according to claim 6, wherein said equalizer is a transversal filter.

8. An apparatus for decoding a transmitted signal, substantially as herein described with reference to and as illustrated in Figure 3 of the accompanying drawings.

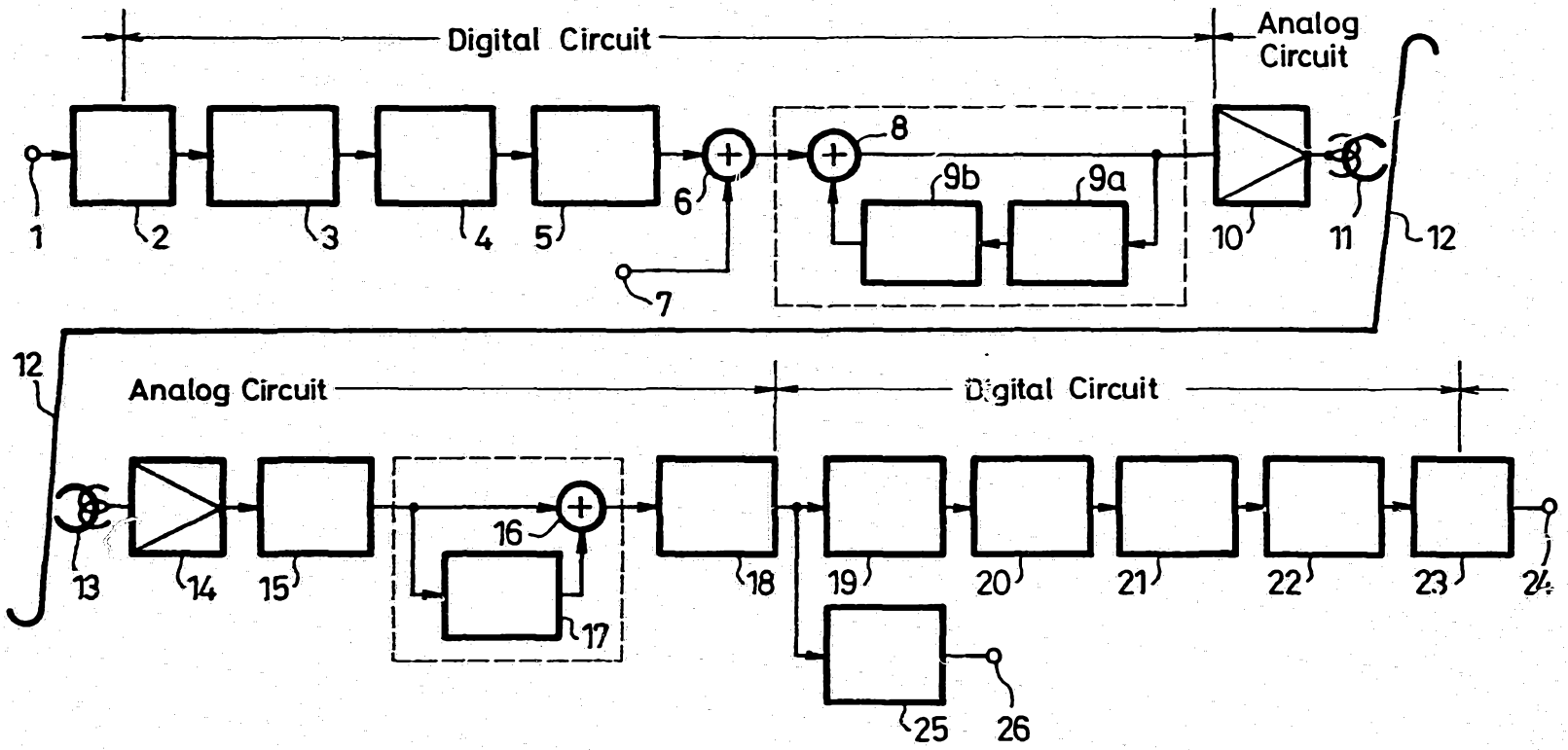
Dated this 11th day of August 1992.

SONY CORPORATION
By Its Patent Attorneys:

GRIFFITH HACK & CO.
Fellows Institute of Patent
Attorneys of Australia.

22 569 35081

FIG. 1



35081/84

FIG. 2

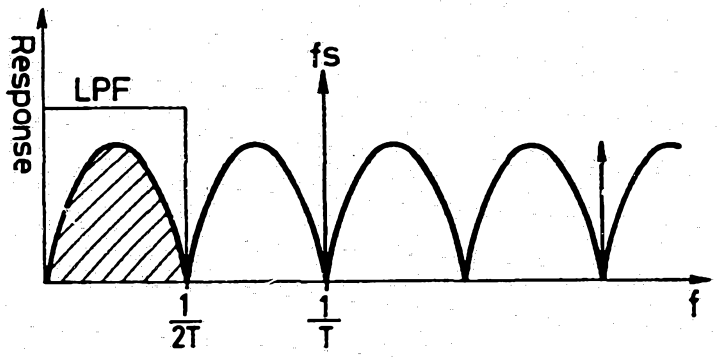
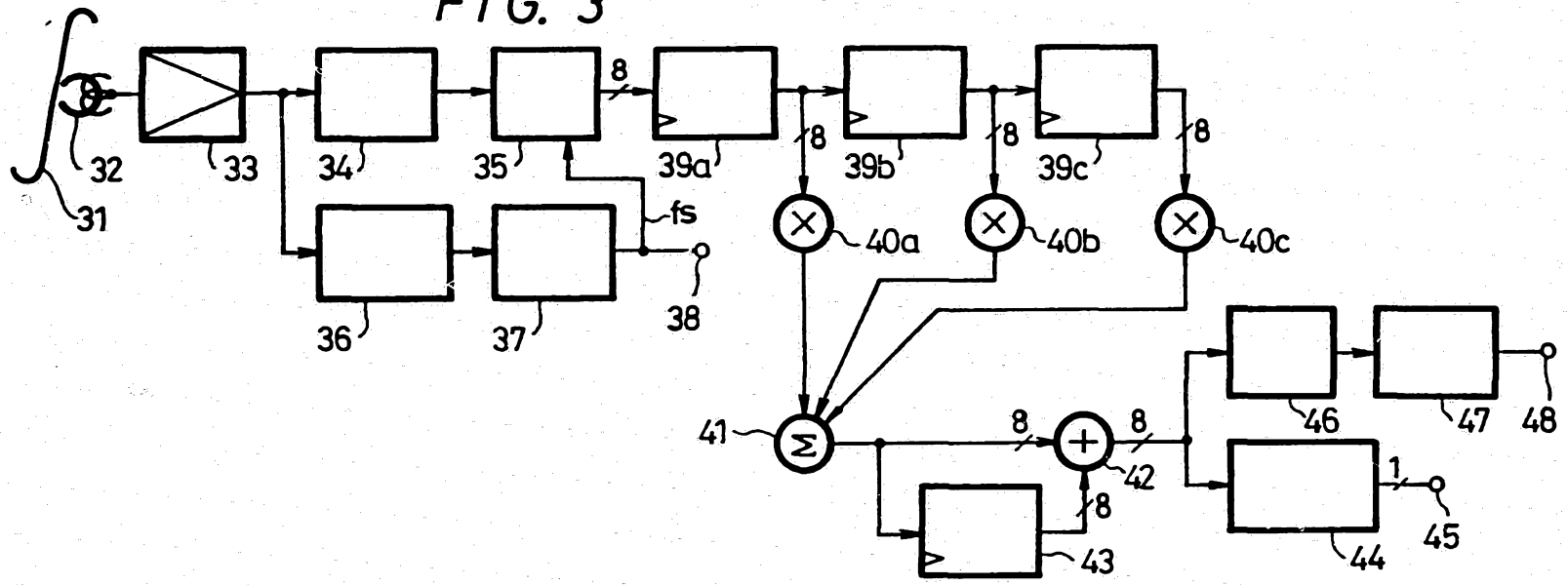

Response
LPF
fs
1/2T
1/T
f

FIG. 3


31
32
33
34
35
8
39a
39b
39c
fs
36
37
38
40a
40b
40c
41
42
43
44
45
46
47
48
1