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(54) **PROGRAMMABLE TEMPERATURE COEFFICIENT ANALOG SECOND-ORDER CURVATURE COMPENSATED VOLTAGE REFERENCE AND TRIM TECHNIQUES FOR VOLTAGE REFERENCE CIRCUITS**

ANALOGE KRÜMMUNGSKOMPENSIERTE SPANNUNGSREFERENZ ZWEITER ORDNUNG MIT PROGRAMMIERBAREM TEMPERATURKOEFFIZIENT UND TRIMMUNGSVERFAHREN FÜR SPANNUNGSREFERENZSCHALTUNGEN

TECHNIQUES DE RÉFÉRENCE ET DE COMPENSATION DE TENSION À COMPENSATION DE COURBURE ANALOGIQUE DE SECOND ORDRE À COEFFICIENT DE TEMPÉRATURE PROGRAMMABLE POUR CIRCUITS DE RÉFÉRENCE DE TENSION

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Description

TECHNICAL FIELD

[0001] Examples of the present disclosure generally relate to electronic circuits and, in particular, to a programmable temperature coefficient analog second-order curvature compensated voltage reference and to trim techniques for voltage reference circuits.

BACKGROUND

[0002] Precision voltage references are important blocks in integrated circuits (ICs), such as System-on-Chip (SoC) ICs. Voltage references are required for various purposes, such as for analog-to-digital converters (ADCs), power management, and the like. Generation of a voltage that is dependent on temperature is also useful in some applications, such as to compensate for temperature effects on circuits. Thus, different circuits in an IC require voltage references having different temperature coefficients (e.g., an ADC uses a temperature-independent voltage reference whereas other circuits, such as switches, require a temperature-dependent voltage reference). Further, circuits for generating voltage references typically use bipolar junction transistors (BJTs). BJTs, however, are parasitic devices in the complementary metal oxide semiconductor (CMOS) process used to fabricate ICs. BJT performance degrades as the CMOS technology scales, which is driven by digital logic. Accordingly, it is desirable to provide a voltage reference circuit that can generate flexible temperature coefficient voltages while compensating for second-order curvature introduced by BJTs.

[0003] US 2006/111865 A1 describes an on-chip temperature sensor for a semiconductor device. The sensor arrangement includes a first current generator producing a first current that is proportional to absolute temperature of the semiconductor device and a second current generator producing a second current that is inversely proportional to absolute temperature of the semiconductor device.

[0004] US 6 265 857 B1 discloses a constant current source circuit which provides current that compensates for changes in performance resulting from changes of temperature. Within the circuit, variable amounts of current having a negative temperature coefficient are mixed with variable amounts of current having a positive temperature coefficient.

[0005] In US 2010/301832 A1 systems and methods for generating a curvature-compensated bandgap voltage reference are described. A curvature-compensated bandgap reference voltage is achieved by injecting a temperature-dependent current at different points in a bandgap reference voltage circuit.

SUMMARY

[0006] Techniques for providing a programmable temperature coefficient analog second-order curvature compensated voltage reference are described. This is performed by providing a voltage reference circuit according to claim 1 and a method of generating a voltage reference according to claim 9. Other aspects of the invention are defined in the dependent claims.

[0007] These and other aspects may be understood with reference to the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] So that the manner in which the above recited features can be understood in detail, a more particular description, briefly summarized above, may be had by reference to example implementations, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical example implementations and are therefore not to be considered limiting of its scope.

Fig. 1 is a block diagram depicting an integrated circuit (IC) according to an example.

Fig. 2 is a block diagram depicting a voltage reference circuit according to an example.

Fig. 3 is a schematic diagram depicting a reference circuit according to an example.

Fig. 4 is a schematic diagram depicting a resistor ladder according to example.

Fig. 5A is a schematic diagram depicting a zero temperature coefficient (Tempco) circuit according to an example.

Fig. 5B is a schematic diagram depicting a curvature correction circuit according to an example.

Fig. 5C is a schematic diagram depicting another portion of the zero Tempco circuit of Fig. 5A according to an example.

Fig. 6 is a graph illustrating the dependence of reference voltage on temperature.

Fig. 7 is a schematic diagram depicting a negative Tempco circuit according to an example.

Fig. 8 is a schematic diagram depicting a positive Tempco circuit according to an example.

Fig. 9 is a flow diagram depicting a method of generating a voltage reference according to an example.

Fig. 10 is a block diagram depicting a test system according to an example.

Fig. 11 is a flow diagram depicting a method of setting trim codes in a voltage reference circuit according to an example.

Fig. 12A is a graph 800 depicting flat trim codes versus output voltage at different temperatures according to an example.

Fig. 12B is a graph 801 depicting ref trim codes versus output voltage at a particular temperature according to an example.

Fig. 13 is a flow diagram depicting a method of setting trim codes in a voltage reference circuit according to another example.

Fig. 14A is a graph depicting measurements of a reference trim code at two different temperatures according to an example.

Fig. 14B is a graph depicting a lookup of the flat trim code according to an example.

Fig. 15 is a block diagram depicting a programmable IC in which the voltage reference circuit described herein can be used according to an example.

Fig. 16 illustrates a field programmable gate array (FPGA) implementation of the programmable IC of Fig. 15.

[0009] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

DETAILED DESCRIPTION

[0010] Various features are described hereinafter with reference to the figures. It should be noted that the figures may or may not be drawn to scale and that the elements of similar structures or functions are represented by like reference numerals throughout the figures. It should be noted that the figures are only intended to facilitate the description of the features. They are not intended as an exhaustive description of the claimed invention or as a limitation on the scope of the claimed invention. In addition, an illustrated example need not have all the aspects or advantages shown.

[0011] Fig. 1 is a block diagram depicting an integrated circuit (IC) 100 according to an example. The IC 100 includes a voltage reference circuit 200, a control circuit 114, and circuits 102. The voltage reference circuit 200 is coupled between a supply node 110, which supplies a voltage Vcc, and a ground node 112, which supplies a ground voltage (e.g., 0 volts). The voltage Vcc may be provided by a voltage supply (not shown) either within the IC 100 or external to the IC 100. The voltage reference circuit 200 is coupled to one or more of the circuits 102 by one or more nodes 104, each of which supplies a zero temperature coefficient (Tempco) voltage. The voltage reference circuit 200 is coupled to one or more of the circuits 102 by one or more nodes 106, each of which supplies a negative Tempco voltage. The voltage reference circuit 200 is coupled to one or more of the circuits 102 by one or more nodes 108, each of which supplies a positive Tempco voltage. Thus, the voltage reference circuit 200 generates zero Tempco voltage(s), negative Tempco voltage(s), and positive Tempco voltage(s). The control circuit 114 supplies control signals to the voltage reference circuit 200 for trimming voltages and/or currents as described in detail below.

[0012] Fig. 2 is a block diagram depicting the voltage reference circuit 200 according to an example. The voltage reference circuit 200 includes a reference circuit 202, a zero Tempco circuit 204, a negative Tempco circuit 206, and a positive Tempco circuit 208. A node 210 couples one output of the reference circuit 202 to each of the Tempco circuits 204...208. A node 212 couples another output of the reference circuit 202 to each of the Tempco circuits 204...208. The nodes 210 and 212 supply control voltages to the Tempco circuits 204...208. The reference circuit 202 generates a proportional-to-temperature current (referred to as Iptat) and a complementary-to-temperature current (referred to as Ictat), as described further below. The control voltages on the nodes 210 and 212 control current sources in the Tempco circuits 204...208 to mirror the currents Iptat and Ictat, respectively. The zero Tempco circuit 204 converts a zero Tempco current Iztat (Iztat = Iptat + Ictat) into one or more zero Tempco voltages at the nodes 104. The negative Tempco circuit 206 converts the current Iztat into one or more negative Tempco voltages at the nodes 106. The positive Tempco circuit 208 converts the current Iztat into one or more positive Tempco voltages at the nodes 108.

[0013] Fig. 3 is a schematic diagram depicting the reference circuit 202 according to an example. The reference circuit 202 includes p-channel field effect transistors (FETs) 302, 304, and 306, such as p-type metal oxide semiconductor FETs (MOSFETs). A p-channel FET is a FET that uses holes as the majority carrier to carry its channel current. The reference circuit 202 further includes an operational amplifier 308, an operational amplifier 316, a multiplexer 320, a resistor 310, a resistor ladder 318, a bipolar junction transistor (BJT) 312, and a BJT 314. The BJTs 312 and 314 are PNP transistors.

[0014] A source of the FET 302 is coupled to the node 110 that supplies Vcc. A drain of the FET 302 is coupled to a node 324. A gate of the FET 302 is coupled to the node 210 that supplies a control voltage V_P. A source of the FET 304 is coupled to the node 110. A drain of the FET 304 is coupled to a node 326. A gate of the FET 304 is coupled to the node 210. A source of the FET 306 is coupled to the node 110. A gate of the FET 306 is coupled to the node 212 that supplies a control voltage Vc. A drain of the FET 306 is coupled to a node 330. The resistor ladder 318, having a total resistance R2, is coupled between the node 330 and the ground node 112.

[0015] Fig. 4 is a schematic diagram depicting a resistor ladder 400 according to example. The resistor ladder 400 can be used as the resistor ladder 318 or any other resistor ladder described herein. The resistor ladder 400 includes a resistor string 408, e.g., resistors $408_1...408_K$, where K is an integer greater than one. The resistors $408_1...408_K$ are coupled in series between a node 410 and a node 412. The resistor ladder 400 further includes a multiplexer 402. Inputs of the multiplexer 402 are respectively coupled to a plurality of taps, e.g., taps $404_1...404_J$, where J is an integer greater than one. Each tap $404_1...404_J$ is coupled to a respective node of the resistor string 408, where the resistor string 408 includes one or more resistors between each pair of nodes. The multiplexer 402 includes a control input 414 for receiving

a signal Ctrl that selects one of the taps 404. The signal Ctrl is a digital signal having ceiling[$\log_2(J)$] bits. The multiplexer 402 includes an output coupled to a node 406. The resistor ladder 400 provides an effective resistance R between the node 406 and the node 412 (shown in phantom for purposes of illustration), which depends on the code value of the Ctrl signal.

[0016] Returning to Fig. 3, a node 328 is coupled to a selected tap of the resistor ladder 318 based on the value of a Flat Trim code. This effectively splits the resistor ladder 318 into a resistance 318_1 between the node 330 and the node 328, and a resistance 318_2 between the node 328 and the ground node 112. The resistance 318_1 has a value R2', and the resistance 318_2 has a value R2".

[0017] An inverting input of the operational amplifier 308 is coupled to the node 324. A non-inverting input of the operational amplifier 308 is coupled to the node 326. An output of the operational amplifier 308 is coupled to the node 210. An inverting input of the operational amplifier 316 is coupled to the node 324. A non-inverting input of the operational amplifier 316 is coupled to a node 328. An output of the operational amplifier 316 is coupled to the node 212.

[0018] The resistor 310, having a resistance R1, is coupled between the node 326 and an emitter of the BJT 314. Each of a base and a collector of the BJT 314 is coupled to the ground node 112. Thus, the BJT 314 is a diode-connected BJT having an anode coupled to the resistor 310 and a cathode coupled to the ground node 112. An emitter of the BJT 312 is coupled to the node 324. Each of a base and a collector of the BJT 312 is coupled to the ground node 112. Thus, the BJT 312 is a diode-connected BJT having an anode coupled to the node 324 and a cathode coupled to the ground node 112. The BJT 314 has N times the emitter area as the BJT 312, where N is an integer greater than one.

[0019] In operation, the operational amplifier 308 is self-biasing and sets the control voltage V_P to turn on the FETs 302 and 304. The operational amplifier 308 applies negative feedback so that the voltage at the node 324 equals the voltage at the node 326. The voltage at the node 324 is a voltage V_{EB1}, which is the voltage between the emitter and base of the BJT 312. The voltage V_{EB1} is complementary to temperature (i.e., has a negative Tempco). The voltage at the emitter of the BJT 314 is V_{EB2}, which is the voltage between the emitter and base of the BJT 314. The voltage V_{EB2} is complementary to temperature. The voltage across the resistor 310, between the node 326 and the emitter of the BJT 314, is $\Delta V_{BE} = V_{EB1} - V_{EB2} = V_{BE2} - V_{BE1}$. The differential voltage ΔV_{BE} can be mathematically expressed as $\Delta V_{BE} = n*V_T*\ln(N)$, where V_T is the thermal temperature, n is the ideality factor, N is the ratio of emitter area between the BJT 314 and the BJT 312, and ln denotes the natural logarithm function. For purposes of example herein, the ideality factor n is assumed to be one and is omitted from subsequent expressions. The thermal voltage $V_T = KT/q$, where T is the temperature in Kelvin, K is the Boltzmann constant, and q is the electron charge in coulombs. As such, ΔV_{BE} is proportional to temperature (i.e., has a positive Tempco). ΔV_{BE} is also dependent on the ratio of collector current, which is related to the base current by the beta factor (i.e., beta = Ic/Ib, where Ic is the collector current and Ib is the base current). The current Iptat can be mathematically expressed as Iptat = ΔV_{BE}/R1, which is also proportional to temperature. The voltage V_P at the node 210 controls current sources in the Tempco circuits to mirror the current Iptat.

[0020] The operational amplifier 316 applies negative feedback through adjustment of the control voltage Vc to equalize the voltage at node 328 and the voltage at node 324 (e.g., V_{EB1}). Thus, the current Ictat (going from the node 330 into the resistor ladder 318) can be mathematically expressed as Ictat = V_{EB}/R2". Since V_{EB1} is complementary to temperature, then Ictat is also complementary to temperature. The voltage Vc at the node 212 controls current sources in the Tempco circuits to mirror the current Ictat. The current Ictat can be trimmed by varying the Flat Trim code. The flat trim balances the temperature coefficient by adjusting Ictat relative to Iptat so that Ictat + Iptat = Iztat is approximately constant over a range of temperature. Note that while the slope of Iptat with respect to temperature is constant, the slope of Ictat with respect to temperature is non-linear. Thus, Iztat varies from the desired constant value over a range of temperature. This first-order error is corrected, as described further below.

[0021] Fig. 5A is a schematic diagram depicting the zero Tempco circuit 204 according to an example. The zero Tempco circuit 204 includes p-channel FETs 502, 504, 506, and 508 (e.g., p-type MOSFETs). The zero Tempco circuit 204 further includes a curvature correction circuit 510, a resistor ladder 512, and a resistor ladder 554.

[0022] A source of the FET 502 is coupled to the node 110 that supplies Vcc. A drain of the FET 502 is coupled to a node 530. A gate of the FET 502 is coupled to the node 212 that supplies the control voltage Vc. A source of the FET 504 is coupled to the node 110 that supplies Vcc. A drain of the FET 504 is coupled to a node 530. A gate of the FET 504 is coupled to the node 210 that supplies the control voltage V_P. A source of the FET 506 is coupled to the node 110. A drain of the FET 506 is coupled to a node 532. A gate of the FET 506 is coupled to the node 212 that supplies the control voltage Vc. A source of the FET 508 is coupled to the node 110 that supplies Vcc. A drain of the FET 508 is coupled to the node 532. A gate of the FET 508 is coupled to the node 210 that supplies the control voltage V_P. The FETs 502 and 504 form a current source 514_1 that mirrors Ictat and Iptat. The FETs 506 and 508 form a current source 514_2 that mirrors Ictat and Iptat.

[0023] The resistor ladder 512, having a resistance R_{LOAD1}, is coupled between the node 530 and the ground node 112. A node 556 is coupled to a selected tap of the resistor ladder 512 based on the value of the Ref1 Trim

code. Selection of the tap results in a resistance 512_1 coupled between the node 530 an the node 556, and a resistance 512_2 coupled between the node 556 and the ground node 112. The resistance 512_1 has a value R_{LOAD1}', and the resistance 512_2 has a value R_{LOAD1}". The curvature correction circuit 510 is coupled to the node 556 to supply a current Icor, as described further below.

[0024] The resistor ladder 554, having a resistance R_{LOAD2}, is coupled between the node 532 and the ground node 112. A node 558 is coupled to a selected tap of the resistor ladder 554 based on the value of the Ref2 Trim code. Selection of the tap results in a resistance 554_1 coupled between the node 532 and the node 558, and a resistance 554_2 coupled between the node 558 and the ground node 112. The resistance 554_1 has a value R_{LOAD2}', and the resistance 554_2 has a value R_{LOAD2}".

[0025] In operation, the control voltage Vc controls the FETs 502 and 506 to supply the current Ictat. The control voltage V_P controls the FETs 504 and 508 to supply the current Iptat. The currents Ictat and Iptat feed the node 530. The control circuit 114 sets the Ref1 Trim to control values of R_{LOAD1}' and R_{LOAD1}". The curvature correction circuit 510 supplies a current Icor to the resistor ladder 512 such that, in steady state condition, the sum of the currents Iztat and Icor conducts through the resistance R_{LOAD1}".

[0026] The node 556 supplies a voltage that is proportional to Iztat+Icor, which is referred to as V_{ref1}. The voltage V_{ref1} has a zero Tempco.

[0027] The currents Ictat and Iptat feed the node 532. In steady state condition, the current Iztat conducts through the resistor ladder 554. The control circuit 114 controls sets Ref2 Trim to control values for R_{LOAD2}' and R_{LOAD2}". The node 558 supplies a voltage, V_{ref2}, which is proportional to Iztat. The voltage V_{ref2} has a zero Tempco. The voltage output by the LPF 538 is proportional to Iztat. The operational amplifier 540, the resistor 544, the resistor 546, and the resistor 552 are configured as a non-inverting amplifier that applies a configured amount of gain to the voltage output by the LPF 538. The gain is determined by the resistance values of the resistors 544, 546, and 552. The node 542 supplies a zero Tempco voltage V_{ref2}. The resistors 544, 548, and 552 form a voltage divider that supplies a fraction of V_{ref2} at the node 550 (e.g., half of the voltage to generate $Vref_2/2$).

[0028] The Ref1 Trim and Ref2 Trim codes set a direct current (DC) level of the corresponding pre-gain voltages at the nodes 556 and 558, respectively. Gain circuits can be used to amplifier or attenuate the pre-gain voltages. Voltage dividers can then provide one or more fractions of the post-gain reference voltage.

[0029] In the example, the zero Tempco circuit 204 includes two current sources 514 for mirroring Ictat and Iptat to generate three zero Tempco voltages. In other examples, the zero Tempco circuit 204 can include less or more than two current sources 514 for generating any number of zero Tempco voltages. In an example, one or both of the gain circuits 516 can be omitted. Alternatively, another current source 514 can feed another resistor ladder that supplies a pre-gain output voltage.

[0030] Fig. 5B is a schematic diagram depicting the curvature correction circuit 510 according to an example. The curvature correction circuit 510 includes p-channel FETs 564, 566, and 568 (e.g., p-type MOSFETs). The curvature correction circuit 510 further includes PNP BJTs 570 and 572, as well as a trans-conductance circuit 578.

[0031] Sources of the FETs 564, 566, and 568 are coupled to the node 110 that supplies Vcc. A drain of the FET 564 is coupled to the node 574, and a gate of the FET 564 is coupled to the node 212 that supplies the control voltage Vc. Drains of the FETs 566 and 568 are coupled to the node 5576. A gate of the FET 566 is coupled to the node 212 that supplies the control voltage Vc. A gate of the FET 568 is coupled to the node 210 that supplies the control voltage V_P. The width of the FETs 566 and 568 are half that of the FET 564. The FET 564 supplies a mirror of the current Ictat, the FET 566 supplies a mirror of the current Ictat/2, and the FET 568 supplies a mirror of the current Iptat/2.

[0032] An emitter of the BJT 570 is coupled to the node 574 to provide the voltage V_{EB3}. An emitter of the BJT 572 is coupled to the node 576 to provide the voltage V_{EB4}. Bases and collectors of the BJTs 570 and 572 are coupled to the ground node 112. Thus, the BJTs 570 and 572 are diode-connected BJTs coupled between the node 574 and the ground node 112, and between the node 576 and the ground node 112, respectively. The BJT 572 has N' times the emitter area as the BJT 570, where N' is an integer greater than one.

[0033] Inputs of the trans-conductance circuit 578 are coupled to the nodes 574 and 576. An output of the trans-conductance circuit 578 is coupled to the node 556 and supplies the current Icor.

[0034] In operation, the current Ictat varies non-linearly with temperature. That is, the derivative of Ictat with respect to temperature is not constant. As such, any voltage generated from Iztat will vary over temperature. Fig. 6 is a graph 600 illustrating the dependence of V_{ref1} on temperature. The graph 600 includes an axis 602 representing temperature, and an axis 606 representing the voltage V_{ref1} in volts. As shown by a curve 610, the voltage V_{ref1} has a convex bow with respect to temperature. That is, V_{ref1} increases with increasing temperature until reaching a maximum value and then decreases with further increases in temperature.

[0035] Returning to Fig. 5B, the curvature correction circuit 510 applies second-order correction to Iztat to mitigate the temperature dependence of V_{ref1} due to first-order error in Ictat. In particular, the differential voltage $AV_{BE2} = V_{BE4} - V_{BE3} = V_T*\ln((N'*Iztat/2)/I_{S4}) - V_T*\ln(Ictat/I_{S3})$, where I_{S4} and I_{S3} are the reverse saturation currents of the BJTs 570 and 572, respectively. If the reverse saturation currents are approximately equal, the expres-

sion reduces to $AV_{BE2} = V_T^*(\ln(N'^*Iztat/2) - \ln(Ictat))$. The graph 600 in Fig. 6 includes an axis 604 representing AV_{BE2} in volts. As shown by a curve 608, the voltage AV_{BE2} has a concave bow with respect to temperature. That is, AV_{BE2} decreases with increasing temperature until reaching a minimum value and then increases with further increases in temperature. The trans-conductance circuit 578 converts the differential voltage ΔV_{BE2} into the current Icor, which has the same concave curvature over temperature. The trans-conductance circuit 578 injects the current Icor into the node 556. As temperature varies, the current Ictat + Icor is substantially constant due to the second-order curvature correction.

[0036] Fig. 5C is a schematic diagram depicting another portion 204A of the zero Tempco circuit 204 according to an example. The portion 204A of the zero Tempco circuit 204 includes p-channel FETs 580 and 582, as well as a resistor ladder 586. A source of the FET 580 is coupled to the node 110 that supplies Vcc. A drain of the FET 580 is coupled to a node 584. A gate of the FET 580 is coupled to the node 212 that supplies the control voltage Vc. A source of the FET 582 is coupled to the node 110 that supplies Vcc. A drain of the FET 582 is coupled to the node 584. A gate of the FET 582 is coupled to the node 210 that supplies the control voltage V_P. The FETs 580 and 582 form a current source 514_3 that mirrors Ictat and Iptat.

[0037] The resistor ladder 586, having a resistance R_{LOAD3}, is coupled between the node 584 and the ground node 112. A node 588 is coupled to a selected tap of the resistor ladder 586 based on the value of the Ref3 Trim code. Selection of the tap results in a resistance 586_1 coupled between the node 584 and the node 588, and a resistance 586_2 coupled between the node 588 and the ground node 112. The resistance 586_1 has a value R_{LOAD3}', and the resistance 586_2 has a value R_{LOAD3}". The node 588 supplies a voltage Vref3 that is a pre-gain zero Tempco voltage.

[0038] Fig. 7 is a schematic diagram depicting the negative Tempco circuit 206 according to the invention. The negative Tempco circuit 206 includes six p-channel FETs 702...712 and resistor ladders 718, 720, 728, and 730. Sources of the FETs 702...712 are coupled to the node 110 that supplies Vcc. Drains of the FETs 702 and 704 are coupled to a node 714. A drain of the FET 706 is coupled to a node 724. Drains of the FETs 708 and 710 are coupled to a node 716. A drain of the FET 712 is coupled to a node 736. Gates of the FETs 702 and 708 are coupled to the node 210 that supplies the control voltage V_P. Gates of the FETs 704, 706, 710, and 712 are coupled to the node 212 that supplies the control voltage Vc. The FETs 702, 704, and 706 form a first current source 715_1, and the FETs 708, 710, and 712 form a second current source 715_2.

[0039] The resistor ladder 718, having a resistance R3, is coupled between the node 714 and a node 726. The resistor ladder 720, having a resistance R4, is coupled between the node 726 and the ground node 112. The resistor ladders 718 and 720 are coupled in series between the node 714 and the ground node 112. A selected tap of the resistor ladder 718, as determined by the code Neg1 Trim generated by the control circuit 114, is coupled to a node 722. The resistor ladder 718 is effectively split between a resistance 718_1 and a resistance 718_2, where the resistance 718_1 has a value R3' and the resistance 718_2 has a value R3". A selected tap of the resistor ladder 720, as determined by the code Neg1 Slope Trim generated by the control circuit 114, is coupled to the node 724. The resistor ladder 720 is effectively split between a resistance 720_1 and a resistance 720_2, where the resistance 720_1 has a value R4' and the resistance 720_2 has a value R4".

[0040] The resistor ladder 728, having a resistance R5, is coupled between the node 716 and a node 734. The resistor ladder 730, having a resistance R6, is coupled between the node 734 and the ground node 112. The resistor ladders 728 and 730 are coupled in series between the node 716 and the ground node 112. A selected tap of the resistor ladder 728, as determined by the code Neg2 Trim generated by the control circuit 114, is coupled to a node 732. The resistor ladder 728 is effectively split between a resistance 728_1 and a resistance 728_2, where the resistance 728_1 has a value R5' and the resistance 728_2 has a value R5". A selected tap of the resistor ladder 730, as determined by the code Neg2 Slope Trim generated by the control circuit 114, is coupled to the node 736. The resistor ladder 730 is effectively split between a resistance 730_1 and a resistance 730_2, where the resistance 730_1 has a value R6' and the resistance 730_2 has a value R6".

[0041] In operation, the FETs 702 and 704 supply a current Iztat (i.e., Ictat+Iptat) through the series combination of the resistor ladder 718 and the resistor ladder 720. The FET 706 supplies a mirror of Ictat through the resistance 720_2. The voltage at the node 722 is V_{neg1} = Iztat*(R3+R4) + Ictat*R4". The voltage V_{neg1} has a zero Temoco component Iztat*(R3+R4) and a negative Tempco component Ictat*R4". Thus, the voltage V_{neg1} has a negative Tempco. The control circuit 114 sets the code Neg1 Slope Trim to control the slope of the negative Tempco for the voltage V_{neg1}. The control circuit 114 sets the code Neg1 Trim to control the DC level of the voltage V_{neg1} given the code used for Neg1 Slope Trim.

[0042] The FETs 708 and 710 supply a current Iztat (i.e., Ictat+Iptat) through the series combination of the resistor ladder 728 and the resistor ladder 730. The FET 712 supplies a mirror of Ictat through the resistance 730_2. The voltage at the node 732 is V_{neg2} = Iztat*(R5+R6) + Ictat*R6". The voltage V_{neg2} has a zero Temoco component Iztat*(R5+R6) and a negative Tempco component Ictat*R6". Thus, the voltage V_{neg2} has a negative Tempco. The control circuit 114 sets the code Neg2 Slope Trim to control the slope of the negative Tempco for the voltage V_{neg2}. The control circuit 114 sets the code Neg2 Trim to control the DC level of the voltage V_{neg2} given the code used for Neg2 Slope Trim. The voltage V_{neg2}

is set independent of the voltage V_{neg1}.

[0043] Although two current sources 715 and two pairs of resistor ladders are shown, the negative Tempco circuit 206 can include any number of current sources 715, each coupled to a pair of resistor ladders as shown in Fig. 7. In this manner, the negative Tempco circuit can supply any number of complementary-to-temperature voltages. In addition, although gain circuits are omitted from Fig. 7, in some examples, one or both of the pre-gain voltage outputs can be coupled to a gain circuit, similar to the configuration shown in Fig. 5A.

[0044] Fig. 8 is a schematic diagram depicting the positive Tempco circuit 208 according to an example. The positive Tempco circuit 208 includes p-channel FETs 802 and 804, a resistor ladder 824, switches 808 and 810, and digital-to-analog (DAC) current sources 816 and 820. Sources of the FETs 802 and 804 are coupled to the node 110 that supplies the voltage Vcc. Drains of the FETs 802 and 804 are coupled to a node 806. A gate of the FET 802 is coupled to the node 212 that supplies the control voltage Vc. A gate of the FET 804 is coupled to the node 210 that supplies the control voltage V_P. The FETs 802 and 804 form a current source 815 that supplies Iztat = Ictat + Iptat.

[0045] The resistor ladder 824, having a resistance R7, is coupled between the node 806 and the ground node 112. A selected tap of the resistor ladder 824, as controlled by the Blk Trim code set by the control circuit 114, is coupled to a node 826. The resistor ladder 824 is effectively split into a resistance 824_1 and a resistance 824_2, having values R7' and R7", respectively. The resistance 824_1 is coupled between the node 806 and the node 826. The resistance 824_2 is coupled between the node 826 and the ground node 112. The node 826 supplies a voltage V_{BLK}.

[0046] One terminal of the switch 808 is coupled to the node 210 that supplies the control voltage V_P. Another terminal of the switch 808 is coupled to a node 812. A reference voltage input of the current DAC 816 is coupled to the node 812. The current DAC 816 includes a digital control input coupled to a bus 818 that supplies a digital signal Blk_p. A current output of the current DAC 816 is coupled to the node 806. A supply voltage input of the current DAC 816 is coupled to the node 110 that supplies the voltage Vcc.

[0047] One terminal of the switch 810 is coupled to the node 212 that supplies the control voltage Vc. Another terminal of the switch 810 is coupled to a node 814. A reference voltage input of the current DAC 820 is coupled to the node 814. The current DAC 820 includes a digital control input coupled to a bus 822 that supplies a digital signal Blk_c. A current output of the current DAC 820 is coupled to the ground node 112. A supply voltage input of the current DAC 820 is coupled to the node 806.

[0048] In operation, the voltage V_{BLK} = Iztat*R7" + Idac*R7". The current Idac, which flows into the node 806, depends on the state of the switches 808 and 810. If both switches 808 and 810 are open, the current Idac is zero. If the switch 808 is closed and the switch 810 is open, the current DAC 816 receives the voltage V_P. The current DAC 816 provides a ratio of the current Iptat based on the code supplied by the digital signal Blk_p. The current DAC 816 outputs a current Idac_p. The current Idac equals the current Idac_p supplied by the current DAC 816. In such case, the voltage V_{BLK} includes a zero Tempco component Iztat*R7" and a positive Tempco component Idac_p*R7".

[0049] If the switch 810 is closed and the switch 808 is open, the current DAC 820 receives the voltage Vc. The current DAC 820 sinks a ratio of the current Ictat based on the code supplied by the digital signal Blk_C. The current DAC 820 sinks a current Idac_c. The current Idac equals the -Idac_c supplied by the current DAC 820. In such case, the voltage V_{BLK} includes a zero Tempco component Iztat*R7" and a positive Tempco component -Idac_c*R7".

[0050] If both switches 808 and 810 are closed, the current Idac = Idac_p - Idac_c. In such case, the voltage V_{BLK} includes a zero Tempco component Iztat*R7" and a positive Tempco component (Idac_p-Idac_c)*R7".

[0051] In some examples, the control circuit 114 generates control signals Blk Ptat and Blk Ctat to open and close the switches 808 and 810 in an alternating sequence. The control circuit 114 controls the magnitude of the oscillation using the digital signals Blk_p and Blk_c. The control circuit 114 controls the DC level of the voltage V_{BLK} using the Blk Trim code. While a single current source 815 and load (resistor ladder 824 and current DACs 816, 820) are shown, it is to be understood that the positive Tempco circuit 208 can include more than one current source 815 and associated load to generate more than one positive Tempco voltage. In some examples, the pre-gain voltage V_{BLK} can be coupled to a gain circuit to provide a positive Tempco voltage with gain.

[0052] Fig. 9 is a flow diagram depicting a method 900 of generating a voltage reference according to an example. The method 900 begins at block 902, where the reference circuit 202 generates Iptat and the control voltage Vp. At block 904, the reference circuit 202 generates Ictat and the control voltage Vc. At block 906, one or more current sources generate a sum current of Iptat and Ictat in response to the control voltages Vp and Vc. For example, at block 908, the zero Tempco circuit 204 generates a zero Tempco voltage from the sum current. At block 910, the negative Tempco circuit 206 generates a negative Tempco voltage from the sum current. At block 912, the positive Tempco circuit 208 generates a positive Tempco voltage from the sum current.

[0053] Fig. 10 is a block diagram depicting a test system 1000 according to an example. The test system 1000 includes automatic test equipment (ATE) 1002 and a wafer 1004 having a plurality of ICs 1100. The ATE 1002 includes a central processing unit (CPU) 1008, a memory 1012, input/output (IO) circuits 1010, and support circuits 1006. The CPU 1008 can be any type of general-purpose processor, such as an x86-based processor,

ARM®-based processor, or the like. The CPU 1008 can include one or more cores and associated circuitry (e.g., cache memories, memory management units (MMUs), interrupt controllers, etc.). The CPU 1008 is configured to execute program code that perform one or more operations described herein and which can be stored in the memory 1012. The support circuits 1006 include various devices that cooperate with the CPU 608. For example, the support circuits 1006 can include a chipset (e.g., a north bridge, south bridge, platform host controller, etc.), voltage regulators, firmware (e.g., a BIOS), and the like. In some examples, the CPU 1008 can be a System-in-Package (SiP), System-on-Chip (SoC), or the like, which absorbs all or a substantial portion of the functionality of the chipset (e.g., north bridge, south bridge, etc.). The IO circuits 1010 include various circuits configured for communication with the ICs 1100.

[0054] The memory 1012 is a device allowing information, such as executable instructions and data, to be stored and retrieved. The memory 1012 can include, for example, one or more random access memory (RAM) modules, such as double-data rate (DDR) dynamic RAM (DRAM). The ATE 1002 can include various other devices, including local storage devices (e.g., one or more hard disks, flash memory modules, solid state disks, and optical disks) and/or a storage interface that enables the test system 1000 to communicate with one or more network data storage systems.

[0055] Fig. 11 is a flow diagram depicting a method 1100 of setting trim codes in a voltage reference circuit according to an example. The method 1100 can be performed by the ATE 1002 for setting the Flat Trim in the reference circuit 202, and the Ref_x Trim (e.g., Ref1 Trim, Ref2 Trim, etc.) in the circuit 500A, for each IC 100 on the wafer 604.

[0056] The method 1100 begins at step 1102, where the wafer 1004 is disposed in a 0 degree Celsius (0C) environment and the ATE 1002 sequences through trim codes for the Flat Trim and measures Vref1. The ATE 1002 obtains a plurality of Vref1 values for a corresponding plurality of trim codes of the Flat Trim. At step 704, the ATE 1002 fits the Vref1 values obtained at step 1102 to a polynomial curve having one or more coefficients (e.g., three coefficients). The ATE 1002 stores the values of the coefficients in the IC 100 (e.g., in the control circuit 114 using, for example, an electronic fuse (e-fuse) or the like type memory element). Fig. 12A is a graph 1200 depicting flat trim codes versus output voltage at different temperatures according to an example. In the graph 1200, the horizontal axis represents flat trim code and the vertical axis represents output voltage. A curve 1202 represents the polynomial curve determined at 1104 (where T1 = 0 C).

[0057] At step 1106, the wafer 1004 is disposed in a 100 degree Celsius (100C) environment and the ATE 1002 sequences through trim codes for the Flat Trim and measures Vref1. The ATE 1002 obtains a plurality of Vref1 values for a corresponding plurality of trim codes of the Flat Trim. At step 1108, the ATE 1002 fits the Vref1 values obtained at step 1106 to a polynomial curve having the same order as that used in step 1104. In the graph 1200, a curve 1204 represents the polynomial curve determined at step 1108.

[0058] At step 1110, the ATE 1002 determines an intersection between the Vref1 curve at 0C and the Vref1 curve at 100C. The ATE 1002 can generate the Vref1 curve at 0C by obtaining the coefficients stored by the control circuit 114 in the IC 100. The ATE 1002 generates the Vref1 curve at 100C in step 1108. At step 712, the ATE 1002 determines a trim setting for the Flat Trim corresponding to the intersection between the Vref1 curve at 0C and the Vref1 curve at 100C. As shown in the graph 1200, the intersection of the curve 1202 and 1204 results in the determined flat trim code value. At step 1114, the ATE 1002 sets the Flat Trim to the determined trim code at step 1112 and adjusts the Ref1 Trim to set a desired voltage of Vref1 (e.g., 1V). Fig. 12B is a graph 1201 depicting ref trim codes versus output voltage at a particular temperature (T = T2) according to an example. In the graph 1201, the horizontal axis represents ref trim code and the vertical axis represents output voltage. A curve 1206 represents ref trim code versus output voltage and an output voltage of 1V results in the determined ref trim code value.

[0059] Fig. 13 is a flow diagram depicting a method 1300 of setting trim codes in a voltage reference circuit according to an example. The method 1300 can be performed by the ATE 1002 for setting the Flat Trim in the reference circuit 202, and the Ref_x Trim (e.g., Ref1 Trim, Ref2 Trim, etc.) in the circuit 500A, for each IC 100 on the wafer 1004.

[0060] The method 1300 begins at step 902, where the ATE 1002 selects an approximate trim code for the Flat Trim. The approximate trim code for the Flat Trim can be set based on simulations of the voltage reference circuit. At step 1304, the wafer 1004 is disposed in a 0C environment and the ATE 1002 selects a trim code for the Ref1 Trim that sets Vref1 to a desired value (e.g., 1 V). The ATE 1002 can adjust the Ref1 Trim and measure Vref1 until Vref1 obtains the desired value. At step 1306, the ATE 1002 stores the selected trim code for Ref1 Trim in the IC 100 (e.g., in the control circuit 114 using, for example, an electronic fuse (e-fuse) or the like type memory element). At step 1308, the wafer 1004 is disposed in a 100C environment and the ATE 1002 selects a trim code for the Ref1 Trim that sets Vref1 to the desired value (e.g., 1 V). At step 1310, the ATE 1002 determines the slope of the Ref1 Trim code over temperature. For example, the ATE 1002 can compute the difference between the Ref1 Trim code values at 0C and at 100C. Fig. 14A is a graph 1400 depicting measurements of the Ref1 Trim Code at two different temperatures according to an example. In the graph 1400, the horizontal axis represents temperature and the vertical axis represents Ref1 Trim Code value. At temperature T1, code1 is obtained. At temperature T2, code2 is obtained. If the temperature

coefficient was zero, the same code would be obtained at both temperatures. The ATE 1002 determines the slope of curve 1002 at step 1310. At step 912, the ATE 1002 obtains a trim code value for the Flat Trim from a lookup table based on the Ref1 Trim code slope determined at step 1310. The lookup table can include a plurality of trim code values for the Flat Trim for a corresponding plurality of Ref1 Trim code slope values. Fig. 14B is a graph 1001 depicting a lookup of the flat trim code given a slope of Ref1 Trim according to an example. In the graph 1401, the horizontal axis represents flat trim code and the vertical axis represents the slope of the curve 1402 shown in Fig. 10A. The temperature coefficient determined in step 1310 from the curve 1402 is corrected by changing the flat trim code setting based on a curve 1404.

[0061] Fig. 15 is a block diagram depicting a programmable IC 1 according to an example in which the voltage reference circuit 200 described herein can be used. The programmable IC 1 includes programmable logic 3, configuration logic 25, and configuration memory 26. The programmable IC 1 can be coupled to external circuits, such as nonvolatile memory 27, DRAM 28, and other circuits 29. The programmable logic 3 includes logic cells 30, support circuits 31, and programmable interconnect 32. The logic cells 30 include circuits that can be configured to implement general logic functions of a plurality of inputs. The support circuits 31 include dedicated circuits, such as transceivers, input/output blocks, digital signal processors, memories, and the like. The logic cells and the support circuits 31 can be interconnected using the programmable interconnect 32. Information for programming the logic cells 30, for setting parameters of the support circuits 31, and for programming the programmable interconnect 32 is stored in the configuration memory 26 by the configuration logic 25. The configuration logic 25 can obtain the configuration data from the nonvolatile memory 27 or any other source (e.g., the DRAM 28 or from the other circuits 29). In some examples, the programmable IC 1 includes a processing system 2. The processing system 2 can include microprocessor(s), memory, support circuits, IO circuits, and the like.

[0062] Fig. 16 illustrates a field programmable gate array (FPGA) implementation of the programmable IC 1 that includes a large number of different programmable tiles including transceivers 37, configurable logic blocks ("CLBs") 33, random access memory blocks ("BRAMs") 34, input/output blocks ("IOBs") 36, configuration and clocking logic ("CONFIG/CLOCKS") 42, digital signal processing blocks ("DSPs") 35, specialized input/output blocks ("I/O") 41 (e.g., configuration ports and clock ports), and other programmable logic 39 such as digital clock managers, analog-to-digital converters, system monitoring logic, and so forth. The FPGA can also include PCIe interfaces 40, analog-to-digital converters (ADC) 38, and the like.

[0063] In some FPGAs, each programmable tile can include at least one programmable interconnect element ("INT") 43 having connections to input and output terminals 48 of a programmable logic element within the same tile, as shown by examples included at the top of Fig. 11. Each programmable interconnect element 43 can also include connections to interconnect segments 49 of adjacent programmable interconnect element(s) in the same tile or other tile(s). Each programmable interconnect element 43 can also include connections to interconnect segments 50 of general routing resources between logic blocks (not shown). The general routing resources can include routing channels between logic blocks (not shown) comprising tracks of interconnect segments (e.g., interconnect segments 50) and switch blocks (not shown) for connecting interconnect segments. The interconnect segments of the general routing resources (e.g., interconnect segments 50) can span one or more logic blocks. The programmable interconnect elements 43 taken together with the general routing resources implement a programmable interconnect structure ("programmable interconnect") for the illustrated FPGA.

[0064] In an example implementation, a CLB 33 can include a configurable logic element ("CLE") 44 that can be programmed to implement user logic plus a single programmable interconnect element ("INT") 43. A BRAM 34 can include a BRAM logic element ("BRL") 45 in addition to one or more programmable interconnect elements. Typically, the number of interconnect elements included in a tile depends on the height of the tile. In the pictured example, a BRAM tile has the same height as five CLBs, but other numbers (e.g., four) can also be used. A DSP tile 35 can include a DSP logic element ("DSPL") 46 in addition to an appropriate number of programmable interconnect elements. An IOB 36 can include, for example, two instances of an input/output logic element ("IOL") 47 in addition to one instance of the programmable interconnect element 43. As will be clear to those of skill in the art, the actual I/O pads connected, for example, to the I/O logic element 47 typically are not confined to the area of the input/output logic element 47.

[0065] In the pictured example, a horizontal area near the center of the die (shown in Fig. 16) is used for configuration, clock, and other control logic. Vertical columns 51 extending from this horizontal area or column are used to distribute the clocks and configuration signals across the breadth of the FPGA.

[0066] Some FPGAs utilizing the architecture illustrated in Fig. 11 include additional logic blocks that disrupt the regular columnar structure making up a large part of the FPGA. The additional logic blocks can be programmable blocks and/or dedicated logic.

[0067] Note that Fig. 16 is intended to illustrate only an exemplary FPGA architecture. For example, the numbers of logic blocks in a row, the relative width of the rows, the number and order of rows, the types of logic blocks included in the rows, the relative sizes of the logic blocks, and the interconnect/logic implementations included at the top of Fig. 11 are purely exemplary. For

example, in an actual FPGA more than one adjacent row of CLBs is typically included wherever the CLBs appear, to facilitate the efficient implementation of user logic, but the number of adjacent CLB rows varies with the overall size of the FPGA.

[0068] A number of non-limited examples are provided below.

[0069] In one example, a voltage reference circuit according to claim 1 is provided.

[0070] Some such voltage reference circuit may further include: a third current source coupled to a third load circuit, the third current source generating the sum current of the proportional-to-temperature current and the complementary-to-temperature current in response to the first and second control voltages, the third load circuit generating a positive Tempco voltage from the sum current and at least one of the complementary-to-temperature current and the proportional-to-temperature current.

[0071] In some such voltage reference circuit, the third current source may include a first field effect transistor (FET) and a second FET having a first common source and a first common drain, a gate of the first FET coupled to receive the first control voltage and a gate of the second FET coupled to receive the second control voltage.

[0072] In some such voltage reference circuit, the third load circuit may include: a first current digital-to-analog converter (DAC), switchably coupled to receive the first control voltage, and configured to supply a first positive temperature coefficient (Tempco) current; a second current DAC, switchably coupled to receive the second control voltage, and configured to supply a second positive Tempco current; and a resistor ladder coupled between the first common drain and a ground node, the resistor ladder converting the sum current plus one or both of the first positive Tempco current and the second positive Tempco current into the positive Tempco voltage.

[0073] In some such voltage reference circuit, the first current source may include a first field effect transistor (FET) and a second FET having a first common source and a first common drain, a gate of the first FET coupled to receive the first control voltage and a gate of the second FET coupled to receive the second control voltage, and wherein the first load circuit may include a resistor ladder coupled between the first common drain and a ground node, the resistor ladder converting the sum current into the zero Tempco voltage.

[0074] Some such voltage reference circuit may include: a curvature compensation circuit configured to inject a correction current into the resistor ladder to combine with the sum current, the curvature compensation circuit comprising: a third FET and a fourth FET having a second common source and a second common drain, a gate of the third FET coupled to receive the first control voltage and a gate of the third FET coupled to receive the second control voltage; a fifth FET having a gate coupled to receive the second control voltage; a first diode-connected bipolar junction transistor (BJT) coupled between a drain of the fifth FET and the ground node; a second diode-connected bipolar junction transistor (BJT) coupled between the second common drain and the ground node; and a trans-conductance circuit configured to convert a voltage between the drain of the fifth FET and the second common drain to the correction current.

[0075] In some such voltage reference circuit, the second current source may include: a first field effect transistor (FET) and a second FET having a first common source and a first common drain, a gate of the first FET coupled to receive the first control voltage and a gate of the second FET coupled to receive the second control voltage; and a third FET having a gate coupled to the second control voltage; and wherein the second load circuit may include: a first resistor ladder and a second resistor ladder coupled in series between the first common drain and a ground node, the first and second resistor ladders receiving the sum current from the first common drain, a portion of the second resistor ladder receiving the complementary-to-temperature current from a drain of the third FET.

[0076] In some such voltage reference circuit, the reference circuit may include: a first field effect transistor (FET) and a second FET having a first common source and a first common gate; a first diode-connected bipolar junction transistor (BJT) coupled between a drain of the first FET and a ground node; a first resistor and a second diode-connected BJT coupled in series between a drain of the second FET and the ground node; a first operational amplifier having a non-inverting input coupled to the drain of the second FET, an inverting input coupled to the drain of the first FET, and an output coupled to the first common gate; a third FET having a source coupled to the common source; a resistor ladder coupled between a drain of the third FET and the ground node; and a second operational amplifier having an inverting input coupled to the drain of the first FET, a non-inverting input coupled to the resistor ladder, and an output coupled to a gate of the third FET.

[0077] In another example, a method of generating a voltage reference according to claim 9 is provided. Some such method may further include: generating the sum current of the proportional-to-temperature current and the complementary-to-temperature current in a third current source response to the first and second control voltages; and generating a positive Tempco voltage from the sum current and at least one of the complementary-to-temperature current and the proportional-to-temperature current in a third load circuit coupled to the third current source. In some such method, the step of generating the positive Tempco voltage may include: supplying a first positive Tempco current from a first current digital-to-analog converter (DAC) switchably coupled to receive the first control voltage;

supplying a second positive Tempco current from a second current DAC switchably coupled to receive the second control voltage; and

converting the sum current plus one or both of the

first positive Tempco current and the second positive Tempco current into the positive Tempco voltage in a resistor ladder circuit.

[0078] Some such method may further include: injecting a correction current into the first load circuit to combine with the sum current.

[0079] While the foregoing is directed to specific examples, other and further examples may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

Claims

1. A voltage reference circuit (200), comprising:

a reference circuit (202) comprising a first circuit configured to generate a proportional-to-temperature current (Iptat) and corresponding first control voltage (Vp) and a second circuit configured to generate a complementary-to-temperature current (Ictat) and corresponding second control voltage (Vc);
a first load circuit; and
a first current source (514_1-514_3) coupled to the first load circuit, the first current source (514_1-514_3) generating a sum current of the proportional-to-temperature current (Iptat) and the complementary-to-temperature current (Ictat) in response to the first and second control voltages, the first load circuit generating a zero temperature coefficient, Tempco, voltage from the sum current; the voltage reference circuit **characterised in that** it further comprises:

a second load circuit; and
a second current source (715_2) coupled to the second load circuit, the second current source (715_2) generating another sum current of the proportional-to-temperature current (Iptat) and the complementary-to-temperature current (Ictat) in response to the first and second control voltages, the second load circuit generating a negative Tempco voltage from the other sum current and the complementary-to-temperature current (Ictat), wherein the second load circuit comprises a first resistor ladder (728) and a second resistor ladder (730) coupled in series between the second current source (715_2) and a ground node (112), the first and second resistor ladders (728, 730) receiving the other sum current, a portion of the second resistor ladder (730) receiving the complementary-to-temperature current (Ictat), the first resistor ladder (728) configured to control the level of the negative Tempco voltage and the second resistor ladder (730) configured to control the slope of the negative Tempco voltage.

2. The voltage reference circuit (200) of claim 1, further comprising:
a third current source coupled to a third load circuit, the third current source generating the sum current of the proportional-to-temperature current (Iptat) and the complementary-to-temperature current (Ictat) in response to the first and second control voltages, the third load circuit generating a positive Tempco voltage from the sum current and at least one of the complementary-to-temperature current (Ictat) and the proportional-to-temperature current (Iptat).

3. The voltage reference circuit (200) of claim 2, wherein the third current source comprises a first field effect transistor, FET, and a second FET having a first common source and a first common drain, a gate of the first FET coupled to receive the first control voltage (Vp) and a gate of the second FET coupled to receive the second control voltage (Vc).

4. The voltage reference circuit (200) of claim 3, wherein the third load circuit comprises:

a first current digital-to-analog converter, DAC, switchably coupled to receive the first control voltage (Vp), and configured to supply a first positive temperature coefficient, Tempco, current;
a second current DAC, switchably coupled to receive the second control voltage (Vc), and configured to supply a second positive Tempco current; and
a resistor ladder coupled between the first common drain and a ground node (112), the resistor ladder converting the sum current plus one or both of the first positive Tempco current and the second positive Tempco current into the positive Tempco voltage.

5. The voltage reference circuit (200) of claim 1, wherein the first current source (514_1) comprises a first field effect transistor, FET, (502) and a second FET (504) having a first common source and a first common drain, a gate of the first FET (502) coupled to receive the first control voltage (Vp) and a gate of the second FET (504) coupled to receive the second control voltage (Vc), and wherein the first load circuit comprises a third resistor ladder (512) coupled between the first common drain and a ground node (112), the third resistor ladder converting the sum current into the zero Tempco voltage.

6. The voltage reference circuit (200) of claim 5, further comprising:

a curvature compensation circuit (510) configured to inject a correction current (Icor) into the third resistor ladder to combine with the sum current, the curvature compensation circuit (510) comprising:

a third FET (568) and a fourth FET (566) having a second common source and a second common drain, a gate of the third FET (568) coupled to receive the first control voltage (Vp) and a gate of the fourth FET (566) coupled to receive the second control voltage (Vc);
a fifth FET (564) having a gate coupled to receive the second control voltage (Vc);
a first diode-connected bipolar junction transistor, BJT, (570) coupled between a drain of the fifth FET (564) and the ground node (112);
a second diode-connected bipolar junction transistor, BJT, (572) coupled between the second common drain and the ground node (112); and
a trans-conductance circuit (578) configured to convert a voltage between the drain of the fifth FET (564) and the second common drain to the correction current (Icor).

7. The voltage reference circuit (200) of claim 1, wherein the second current source (715_2) comprises:

a first field effect transistor, FET, and a second FET having a first common source and a first common drain, a gate of the first FET coupled to receive the first control voltage and a gate of the second FET coupled to receive the second control voltage; and
a third FET having a gate coupled to the second control voltage.

8. The voltage reference circuit (200) of claim 1, wherein the reference circuit (202) comprises:

a first field effect transistor, FET, (302) and a second FET (304) having a first common source and a first common gate;
a first diode-connected bipolar junction transistor, BJT, (312) coupled between a drain of the first FET (302) and a ground node (112);
a first resistor (310) and a second diode-connected BJT (314) coupled in series between a drain of the second FET (304) and the ground node (112);
a first operational amplifier (308) having a non-inverting input coupled to the drain of the second FET (304), an inverting input coupled to the drain of the first FET (302), and an output coupled to the first common gate;
a third FET (306) having a source coupled to the common source;
a resistor ladder (318) coupled between a drain of the third FET (306) and the ground node (112); and
a second operational amplifier (316) having an inverting input coupled to the drain of the first FET (302), a non-inverting input coupled to the resistor ladder (318), and an output coupled to a gate of the third FET (306).

9. A method of generating a voltage reference, comprising:

generating a proportional-to-temperature current (Iptat) and corresponding first control voltage in a first circuit of a reference circuit (202);
generating a complementary-to-temperature current (Ictat) and corresponding second control voltage in a second circuit of the reference circuit (202);
generating a sum current of the proportional-to-temperature current (Iptat) and the complementary-to-temperature current (Ictat) in a first current source (514_1-514_3) in response to the first and second control voltages and
generating a zero temperature coefficient, Tempco, voltage from the sum current in a first load circuit coupled to the first current source ;**characterised in that** the method further comprises:

generating another sum current of the proportional-to-temperature current (Iptat) and the complementary-to-temperature current (Ictat) in a second current source (715_2) in response to the first and second control voltages; and
generating a negative Tempco voltage from the other sum current and the complementary-to-temperature current (Ictat) in a second load circuit coupled to the second current source (715_2), wherein the second load circuit comprises a first resistor ladder and a second resistor ladder coupled in series between the second current source (715_2) and a ground node (112), the first and second resistor ladders receiving the other sum current, a portion of the second resistor ladder receiving the complementary-to-temperature current (Ictat), the first resistor ladder configured to control the level of the negative Tempco voltage and the second resistor ladder configured to control the slope of the negative Tempco voltage.

10. The method of claim 9, further comprising:

generating the sum current of the proportional-to-temperature current (Iptat) and the complementary-to-temperature current (Ictat) in a third current source response to the first and second

control voltages; and
generating a positive Tempco voltage from the sum current and at least one of the complementary-to-temperature current (Ictat) and the proportional-to-temperature current (Iptat) in a third load circuit coupled to the third current source.

11. The method of claim 10, wherein the step of generating the positive Tempco voltage comprises:

supplying a first positive Tempco current from a first current digital-to-analog converter (DAC) switchably coupled to receive the first control voltage;
supplying a second positive Tempco current from a second current DAC switchably coupled to receive the second control voltage; and
converting the sum current plus one or both of the first positive Tempco current and the second positive Tempco current into the positive Tempco voltage in a resistor ladder circuit.

12. The method of claim 9, further comprising:
injecting a correction current into the first load circuit to combine with the sum current.

Patentansprüche

1. Spannungsreferenzschaltung (200), umfassend:

eine Referenzschaltung (202) umfassend eine erste Schaltung, die dazu konfiguriert ist, einen zur Temperatur proportionalen Strom (Iptat) und eine entsprechende erste Steuerspannung (Vp) zu erzeugen, und eine zweite Schaltung, die dazu konfiguriert ist, einen zur Temperatur komplementären Strom (Ictat) und eine entsprechende zweite Steuerspannung (Vc) zu erzeugen;
eine erste Lastschaltung; und
eine erste Stromquelle (514_1-514_3), die mit der ersten Lastschaltung gekoppelt ist, wobei die erste Stromquelle (514_1-514_3) einen Summenstrom des zur Temperatur proportionalen Stroms (Iptat) und des zur Temperatur komplementären Stroms (Ictat) als Reaktion auf die erste und die zweite Steuerspannung erzeugt, wobei die erste Lastschaltung eine Spannung mit einem Temperaturkoeffizienten von Null, Tempco, aus dem Summenstrom erzeugt; wobei die Spannungsreferenzschaltung **dadurch gekennzeichnet ist, dass** sie ferner umfasst:

eine zweite Lastschaltung; und
eine zweite Stromquelle (715_2), die mit der zweiten Lastschaltung gekoppelt ist, wobei die zweite Stromquelle (715_2) einen anderen Summenstroms des zur Temperatur proportionalen Stroms (Iptat) und des zur Temperatur komplementären Stroms (Ictat) als Reaktion auf die erste und zweite Steuerspannung erzeugt, wobei die zweite Lastschaltung eine negative Tempco-Spannung aus dem anderen Summenstrom und dem zur Temperatur komplementären Strom (Ictat) erzeugt, wobei die zweite Lastschaltung eine erste Widerstandsleiter (728) und eine zwischen der zweiten Stromquelle (715_2) und einen Erdungsknoten (112) in Reihe gekoppelte zweite Widerstandsleiter (730) umfasst, wobei die erste und zweite Widerstandsleiter (728, 730) den anderen Summenstrom empfängt, wobei ein Abschnitt der zweiten Widerstandsleiter (730) den zur Temperatur komplementären Strom (Ictat) empfängt, wobei die erste Widerstandsleiter (728) zum Steuern des Pegels der negativen Tempco-Spannung konfiguriert ist und die zweite Widerstandsleiter (730) dazu konfiguriert ist, die Steigung der negativen Tempco-Spannung zu steuern.

2. Spannungsreferenzschaltung (200) nach Anspruch 1, ferner umfassend:
eine dritte Stromquelle, die mit einer dritten Lastschaltung gekoppelt ist, wobei die dritte Stromquelle den Summenstrom des zur Temperatur proportionalen Stroms (Iptat) und des zur Temperatur komplementären Stroms (Ictat) als Reaktion auf die erste und die zweite Steuerspannung erzeugt, wobei die dritte Lastschaltung eine positive Tempco-Spannung aus dem Summenstrom und mindestens einem von dem zur Temperatur komplementären Strom (Ictat) und dem zur Temperatur proportionalen Strom (Iptat) erzeugt.

3. Spannungsreferenzschaltung (200) nach Anspruch 2, wobei die dritte Stromquelle einen ersten Feldeffekttransistor, FET, und einen zweiten FET mit einer ersten gemeinsamen Source und einem ersten gemeinsamen Drain, ein Gate des ersten FET, das gekoppelt ist, um die erste Steuerspannung (Vp) zu empfangen, und ein Gate des zweiten FET, das gekoppelt ist, um die zweite Steuerspannung (Vc) zu empfangen, umfasst.

4. Spannungsreferenzschaltung (200) nach Anspruch 3, wobei die dritte Lastschaltung umfasst:

einen ersten Digital-Analog-Wandler, DAC, der schaltbar gekoppelt ist, um die erste Steuerspannung (Vp) zu empfangen, und dazu konfiguriert ist, einen ersten Strom mit positivem Temperaturkoeffizienten, Tempco, zu liefern;

einen zweiten Strom-DAC, der schaltbar gekoppelt ist, um die zweite Steuerspannung (Vc) zu empfangen, und dazu konfiguriert ist, einen zweiten positiven Tempco-Strom zu liefern; und eine Widerstandsleiter, die zwischen dem ersten gemeinsamen Drain und einem Erdungsknoten (112) gekoppelt ist, wobei die Widerstandsleiter den Summenstrom plus einem oder beiden von dem ersten positiven Tempco-Strom und dem zweiten positiven Tempco-Strom in die positive Tempco-Spannung umwandelt.

5. Spannungsreferenzschaltung (200) nach Anspruch 1, wobei die erste Stromquelle (514_1) einen ersten Feldeffekttransistor, FET, (502) und einen zweiten FET (504) mit einer ersten gemeinsamen Source und einem ersten gemeinsamen Drain umfasst, wobei ein Gate des ersten FET (502) zum Empfangen der ersten Steuerspannung (Vp) gekoppelt ist und ein Gate des zweiten FET (504) zum Empfangen der zweiten Steuerspannung (Vc) gekoppelt ist, und wobei die erste Lastschaltung eine dritte Widerstandsleiter (512) umfasst, die zwischen dem ersten gemeinsamen Drain und einem Erdungsknoten (112) gekoppelt ist, wobei die dritte Widerstandsleiter den Summenstrom in die Tempco-Nullspannung umwandelt.

6. Spannungsreferenzschaltung (200) nach Anspruch 5, ferner umfassend:

eine Krümmungskompensationsschaltung (510), die dazu konfiguriert ist, einen Korrekturstrom (Icor) an die dritte Widerstandsleiter zum Kombinieren mit dem Summenstrom anzulegen, wobei die Krümmungskompensationsschaltung (510) umfasst:
einen dritten FET (568) und einen vierten FET (566) mit einer zweiten gemeinsamen Source und einem zweiten gemeinsamen Drain, wobei ein Gate des dritten FET (568) zum Empfangen der ersten Steuerspannung (Vp) gekoppelt ist und ein Gate des vierten FET (566) zum Empfangen der zweiten Steuerspannung (Vc) gekoppelt ist;
einen fünften FET (564) mit einem Gate, das zum Empfangen der zweiten Steuerspannung (Vc) gekoppelt ist;
einen ersten diodengeschalteten bipolaren Flächentransistor, BJT, (570) der zwischen einem Drain des fünften FET (564) und dem Erdungsknoten (112) gekoppelt ist;
einen zweiten diodengeschalteten bipolaren Flächentransistor, BJT, (572) der zwischen dem zweiten gemeinsamen Drain und dem Erdungsknoten (112) gekoppelt ist; und
eine Transkonduktanzschaltung (578), die zum Umwandeln einer Spannung zwischen dem Drain des fünften FET (564) und dem zweiten gemeinsame Drain zum Korrekturstrom (Icor) konfiguriert ist.

7. Spannungsreferenzschaltung (200) nach Anspruch 1, wobei die zweite Stromquelle (715_2) umfasst:

einen ersten Feldeffekttransistor, FET und einen zweiten FET mit einer ersten gemeinsamen Source und einem ersten gemeinsamen Drain,
ein Gate des ersten FET, das gekoppelt ist, um die erste Steuerspannung zu empfangen, und
ein Gate des zweiten FET, das gekoppelt ist, um die zweite Steuerspannung zu empfangen; und
einen dritten FET mit einem Gate, das mit der zweiten Steuerspannung gekoppelt ist.

8. Spannungsreferenzschaltung (200) nach Anspruch 1, wobei die Referenzschaltung (202) umfasst:

einen ersten Feldeffekttransistor, FET, (302) und einen zweiten FET (304) mit einer ersten gemeinsamen Source und einem ersten gemeinsamen Gate;
einen ersten diodengeschalteten bipolaren Flächentransistor, BJT, (312), der zwischen einem Drain des ersten FET (302) und einem Erdungsknoten (112) gekoppelt ist;
einen ersten Widerstand (310) und einen zweiten diodengeschalteten BJT (314), der zwischen einem Drain des zweiten FET (304) und dem Erdungsknoten (112) in Reihe gekoppelt ist;
einen ersten Operationsverstärker (308) mit einem nicht invertierenden Eingang, der mit dem Drain des zweiten FET (304) gekoppelt ist, einen invertierenden Eingang, der mit dem Drain des ersten FET (302) gekoppelt ist, und einen Ausgang, der mit dem ersten gemeinsamen Gate gekoppelt ist;
einen dritten FET (306) mit einer Source, die mit der gemeinsamen Source gekoppelt ist;
eine Widerstandsleiter (318), die zwischen einem Drain des dritten FET (306) und dem Erdungsknoten (112) gekoppelt ist; und
einen zweiten Operationsverstärker (316) mit einem invertierenden Eingang, der mit dem Drain des ersten FET (302) gekoppelt ist, einen nicht invertierenden Eingang, der mit der Widerstandsleiter (318) gekoppelt ist, und einen Ausgang, der mit einem Gate des dritten FET (306) gekoppelt ist.

9. Verfahren zum Erzeugen einer Spannungsreferenz, umfassend:

Erzeugen eines zur Temperatur proportionalen

Stroms (Iptat) und einer entsprechenden ersten Steuerspannung in einer ersten Schaltung einer Referenzschaltung (202);
Erzeugen eines zur Temperatur komplementären Stroms (Ictat) und einer entsprechenden zweiten Steuerspannung in einer zweiten Schaltung der Referenzschaltung (202);
Erzeugen eines Summenstroms des zur Temperatur proportionalen Stroms (Iptat) und des zur Temperatur komplementären Stroms (Ictat) in einer ersten Stromquelle (514_1-514_3) als Reaktion auf die erste und die zweite Steuerspannung und
Erzeugen einer Spannung mit einem Temperaturkoeffizienten von Null, Tempco, aus dem Summenstrom in einer ersten Lastschaltung, die mit der ersten Stromquelle gekoppelt ist; **dadurch gekennzeichnet, dass** das Verfahren ferner umfasst:

Erzeugen eines anderen Summenstroms des zur Temperatur proportionalen Stroms (Iptat) und des zur Temperatur komplementären Stroms (Ictat) in einer zweiten Stromquelle (715_2) als Reaktion auf die erste und die zweite Steuerspannung; und
Erzeugen einer negativen Tempco-Spannung von dem anderen Summenstrom und dem zur Temperatur komplementären Strom (Ictat) in einer zweiten Lastschaltung, die mit der zweiten Stromquelle gekoppelt ist (715_2), wobei die zweite Lastschaltung eine erste Widerstandsleiter und eine zweite Widerstandsleiter umfasst, die zwischen der zweiten Stromquelle (715_2) und einem Erdungsknoten (112) in Reihe gekoppelt sind, wobei der erste und der zweite Widerstandsleiter den anderen Summenstrom empfängt, wobei ein Abschnitt der zweiten Widerstandsleiter den zur Temperatur komplementären Strom (Ictat) empfängt, wobei die erste Widerstandsleiter dazu konfiguriert ist, den Pegel der negativen Tempco-Spannung zu steuern, und die zweite Widerstandsleiter dazu konfiguriert ist, die Steigung der negativen Tempco-Spannung zu steuern.

10. Verfahren nach Anspruch 9, ferner umfassend:

Erzeugen des Summenstroms des zur Temperatur proportionalen Stroms (Iptat) und des zur Temperatur komplementären Stroms (Ictat) in einer dritten Stromquellenreaktion auf die erste und die zweite Steuerspannung; und
Erzeugen einer positiven Tempco-Spannung aus dem Summenstrom und mindestens einem des zur Temperatur komplementären Stroms (Ictat) und des zur Temperatur proportionalen Stroms (Iptat) in einer dritten Lastschaltung, die mit der dritten Stromquelle gekoppelt ist.

11. Verfahren nach Anspruch 10, wobei der Schritt des Erzeugens der positiven Tempco-Spannung umfasst:

Liefern eines ersten positiven Tempco-Stroms von einem ersten Strom-Digital-Analog-Wandler (DAC), der schaltbar gekoppelt ist, um die erste Steuerspannung zu empfangen;
Liefern eines zweiten positiven Tempco-Stroms von einem zweiten Strom-DAC, der schaltbar gekoppelt ist, um die zweite Steuerspannung zu empfangen; und
Umwandeln des Summenstroms plus eines oder beider von dem ersten positiven Tempco-Strom und dem zweiten positiven Tempco-Strom in die positive Tempco-Spannung in einer Widerstandsleiterschaltung.

12. Verfahren nach Anspruch 9, ferner umfassend:
Anlegen eines Korrekturstroms an die erste Lastschaltung zum Kombinieren mit dem Summenstrom.

Revendications

1. Circuit de référence de tension (200), comprenant :

un circuit de référence (202) comprenant un premier circuit configuré pour générer un courant proportionnel à la température (Iptat) et une première tension de commande (Vp) correspondante et un second circuit configuré pour générer un courant complémentaire à la température (Ictat) et une seconde tension de commande (Vc) correspondante ;
un premier circuit de charge ; et
une première source de courant (514_1-514_3) couplée au premier circuit de charge, la première source de courant (514_1-514_3) générant un courant somme du courant proportionnel à la température (Iptat) et du courant complémentaire à la température (Ictat) en réponse aux première et seconde tensions de commande, le premier circuit de charge générant une tension à coefficient de température, Tempco, nul à partir du courant somme ;
le circuit de référence de tension étant **caractérisé en ce qu'**il comprend en outre :

un deuxième circuit de charge ; et
une deuxième source de courant (715_2) couplée au deuxième circuit de charge, la deuxième source de courant (715_2) générant un autre courant somme du courant

proportionnel à la température (Iptat) et du courant complémentaire à la température (Ictat) en réponse aux première et seconde tensions de commande, le deuxième circuit de charge générant une tension à Tempco négatif à partir de l'autre courant somme et du courant complémentaire à la température (Ictat), le deuxième circuit de charge comprenant une première échelle de résistance (728) et une deuxième échelle de résistance (730) couplées en série entre la deuxième source de courant (715_2) et un nœud de masse (112), les première et deuxième échelles de résistance (728, 730) recevant l'autre courant somme, une partie de la deuxième échelle de résistance (730) recevant le courant complémentaire à la température (Ictat), la première échelle de résistance (728) étant configurée pour commander le niveau de la tension à Tempco négatif et la deuxième échelle de résistance (730) étant configurée pour commander la pente de la tension à Tempco négatif.

2. Circuit de référence de tension (200) selon la revendication 1, comprenant en outre :
une troisième source de courant couplée à un troisième circuit de charge, la troisième source de courant générant le courant somme du courant proportionnel à la température (Iptat) et du courant complémentaire à la température (Ictat) en réponse aux première et seconde tensions de commande, le troisième circuit de charge générant une tension à Tempco positif à partir du courant somme et du courant complémentaire à la température (Ictat) et/ou du courant proportionnel à la température (Iptat).

3. Circuit de référence de tension (200) selon la revendication 2, la troisième source de courant comprenant un premier transistor à effet de champ, FET, et un deuxième FET ayant une première source commune et un premier drain commun, une grille du premier FET couplée pour recevoir la première tension de commande (Vp) et une grille du deuxième FET couplée pour recevoir la seconde tension de commande (Vc).

4. Circuit de référence de tension (200) selon la revendication 3, le troisième circuit de charge comprenant :

un premier convertisseur numérique-analogique, DAC, de courant couplé de manière commutable pour recevoir la première tension de commande (Vp), et configuré pour fournir un premier courant à coefficient de température, Tempco, positif ;
un second DAC de courant, couplé de manière commutable pour recevoir la seconde tension de commande (Vc), et configuré pour fournir un second courant à Tempco positif ; et
une échelle de résistance couplée entre le premier drain commun et un nœud de masse (112), l'échelle de résistance convertissant le courant somme plus un ou les deux du premier courant à Tempco positif et du second courant à Tempco positif en tension à Tempco positif.

5. Circuit de référence de tension (200) selon la revendication 1, la première source de courant (514_1) comprenant un premier transistor à effet de champ, FET, (502) et un deuxième FET (504) ayant une première source commune et un premier drain commun, une grille du premier FET (502) couplée pour recevoir la première tension de commande (Vp) et une grille du deuxième FET (504) couplée pour recevoir la seconde tension de commande (Vc), et le premier circuit de charge comprenant une troisième échelle de résistance (512) couplée entre le premier drain commun et un nœud de masse (112), la troisième échelle de résistance convertissant le courant somme en tension à Tempco nul.

6. Circuit de référence de tension (200) selon la revendication 5, comprenant en outre :
un circuit de compensation de courbure (510) configuré pour injecter un courant de correction (Icor) dans la troisième échelle de résistance à combiner avec le courant somme, le circuit de compensation de courbure (510) comprenant :

un troisième FET (568) et un quatrième FET (566) ayant une seconde source commune et un second drain commun, une grille du troisième FET (568) couplée pour recevoir la première tension de commande (Vp) et une grille du quatrième FET (566) couplée pour recevoir la seconde tension de commande (Vc) ;
un cinquième FET (564) ayant une grille couplée pour recevoir la seconde tension de commande (Vc) ;
un premier transistor à jonctions bipolaires, BJT, connecté en diode (570) couplé entre un drain du cinquième FET (564) et le nœud de masse (112) ;
un second transistor à jonctions bipolaires, BJT, connecté en diode (572) couplé entre le second drain commun et le nœud de masse (112) ; et
un circuit de transconductance (578) configuré pour convertir une tension entre le drain du cinquième FET (564) et le second drain commun en courant de correction (Icor).

7. Circuit de référence de tension (200) selon la revendication 1, la deuxième source de courant (715_2) comprenant :

un premier transistor à effet de champ, FET, et un deuxième FET ayant une première source commune et un premier drain commun, une grille du premier FET couplée pour recevoir la première tension de commande et une grille du deuxième FET couplée pour recevoir la seconde tension de commande ; et
un troisième FET ayant une grille couplée à la seconde tension de commande.

8. Circuit de référence de tension (200) selon la revendication 1, le circuit de référence (202) comprenant :

un premier transistor à effet de champ, FET, (302) et un deuxième FET (304) ayant une première source commune et une première grille commune ;
un premier transistor à jonctions bipolaires, BJT, connecté en diode (312) couplé entre un drain du premier FET (302) et un nœud de masse (112) ;
une première résistance (310) et un second BJT connecté en diode (314) couplés en série entre un drain du deuxième FET (304) et le nœud de masse (112) ;
un premier amplificateur opérationnel (308) ayant une entrée non inverseuse couplée au drain du deuxième FET (304), une entrée inverseuse couplée au drain du premier FET (302), et une sortie couplée à la première grille commune ;
un troisième FET (306) ayant une source couplée à la source commune ;
une échelle de résistance (318) couplée entre un drain du troisième FET (306) et le nœud de masse (112) ; et
un second amplificateur opérationnel (316) ayant une entrée inverseuse couplée au drain du premier FET (302), une entrée non inverseuse couplée à l'échelle de résistance (318) et une sortie couplée à une grille du troisième FET (306).

9. Procédé de génération d'une référence de tension, comprenant :

la génération d'un courant proportionnel à la température (Iptat) et d'une première tension de commande correspondante dans un premier circuit d'un circuit de référence (202) ;
la génération d'un courant complémentaire à la température (Ictat) et une seconde tension de commande correspondante dans un second circuit du circuit de référence (202) ;
la génération d'un courant somme du courant proportionnel à la température (Iptat) et du courant complémentaire à la température (Ictat) dans une première source de courant (514_1-514_3) en réponse aux première et seconde tensions de commande et
la génération d'une tension à coefficient de température, Tempco, nul à partir du courant somme dans un premier circuit de charge couplé à la première source de courant ;
caractérisé en ce que le procédé comprend en outre :

la génération d'un autre courant somme du courant proportionnel à la température (Iptat) et du courant complémentaire à la température (Ictat) dans une deuxième source de courant (715_2) en réponse aux première et seconde tensions de commande ; et
la génération d'une tension à Tempco négatif à partir de l'autre courant somme et du courant complémentaire à la température (Ictat) dans un deuxième circuit de charge couplé à la deuxième source de courant (715_2), le deuxième circuit de charge comprenant une première échelle de résistance et une deuxième échelle de résistance couplées en série entre la deuxième source de courant (715_2) et un nœud de masse (112), les première et deuxième échelles de résistance recevant l'autre courant somme, une partie de la deuxième échelle de résistance recevant le courant complémentaire à la température (Ictat), la première échelle de résistance étant configurée pour commander le niveau de la tension à Tempco négatif et la deuxième échelle de résistance étant configurée pour commander la pente de la tension à Tempco négatif.

10. Procédé selon la revendication 9, comprenant en outre :

la génération du courant somme du courant proportionnel à la température (Iptat) et du courant complémentaire à la température (Ictat) dans une réponse de troisième source de courant aux première et seconde tensions de commande ; et
la génération d'une tension à Tempco positif à partir du courant somme et du courant complémentaire à la température (Ictat) et/ou du courant proportionnel à la température (Iptat) dans un troisième circuit de charge couplé à la troisième source de courant.

11. Procédé selon la revendication 10, l'étape de génération de la tension à Tempco positif comprenant :

la fourniture d'un premier courant à Tempco positif à partir d'un premier convertisseur numérique-analogique (DAC) de courant couplé de manière commutable pour recevoir la première

tension de commande ;
la fourniture d'un second courant à Tempco positif à partir d'un second DAC de courant couplé de manière commutable pour recevoir la seconde tension de commande ; et
la conversion du courant somme plus un ou les deux du premier courant à Tempco positif et du second courant à Tempco positif en tension à Tempco positif dans un circuit à échelle de résistance.

12. Procédé selon la revendication 9, comprenant en outre :
l'injection d'un courant de correction dans le premier circuit de charge à combiner avec le courant somme.

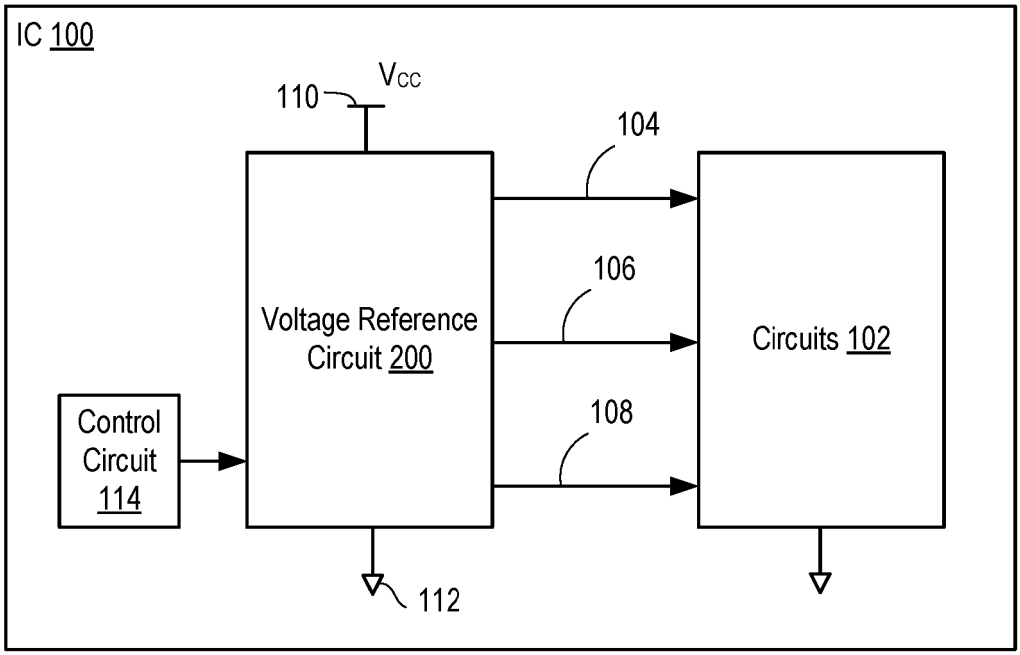
IC 100
110
V_{CC}
104
106
108
Voltage Reference Circuit 200
Control Circuit 114
Circuits 102
112

FIG. 1

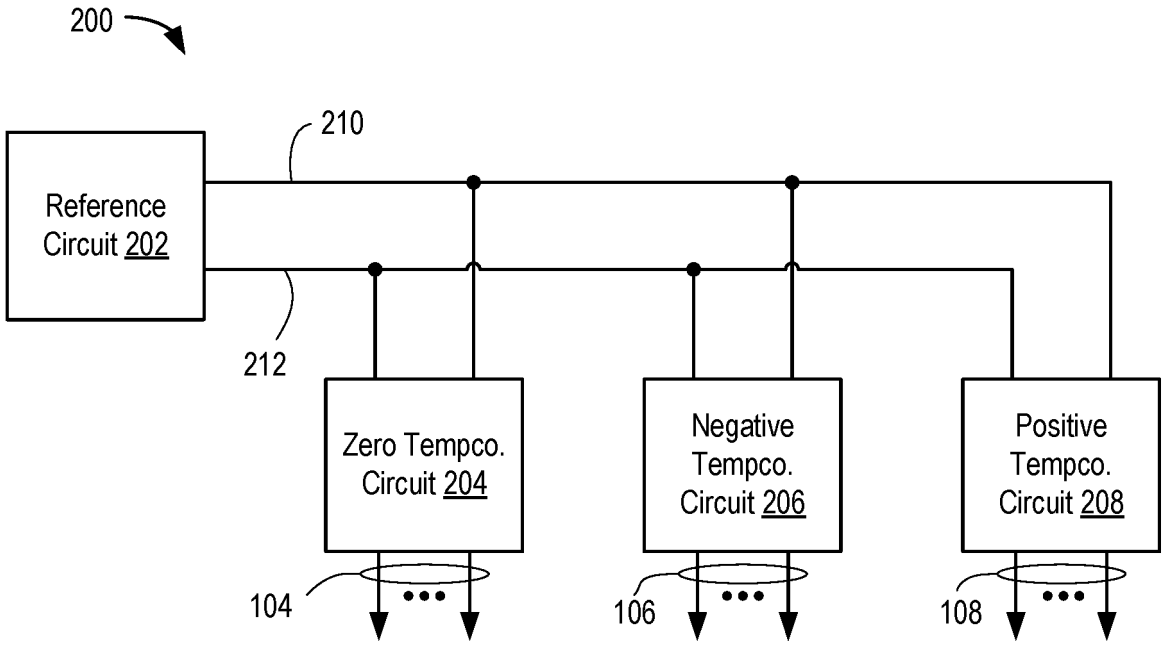
200
210
Reference Circuit 202
212
Zero Tempco. Circuit 204
Negative Tempco. Circuit 206
Positive Tempco. Circuit 208
104
106
108

FIG. 2

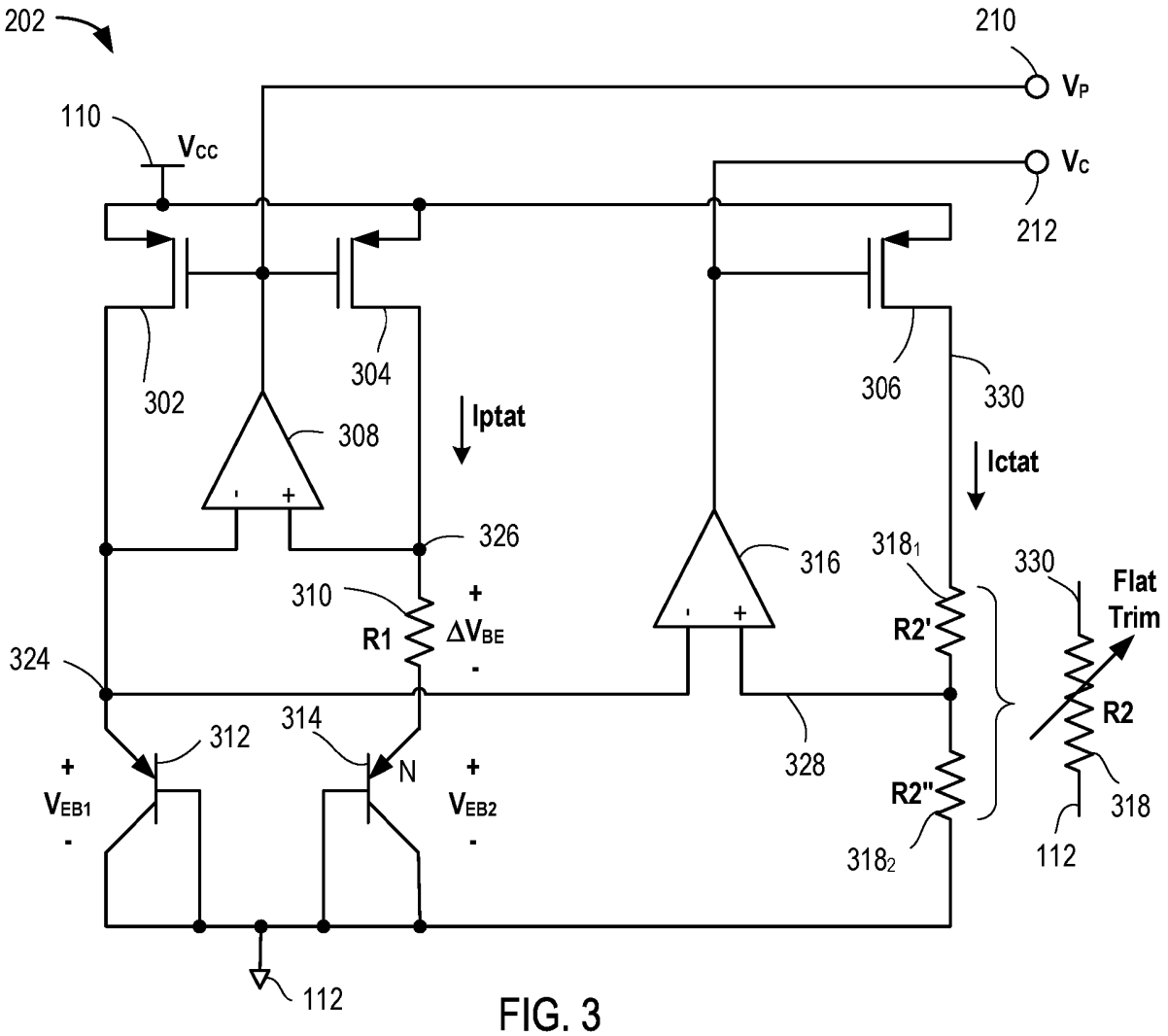
202
210
V_P
110
V_{CC}
V_C
212
302
304
306
330
308
Iptat
Ictat
326
316
318_1
330
Flat Trim
310
R1
ΔV_{BE}
R2'
324
R2
312
314
N
328
R2"
318
318_2
112
V_{EB1}
V_{EB2}
112

FIG. 3

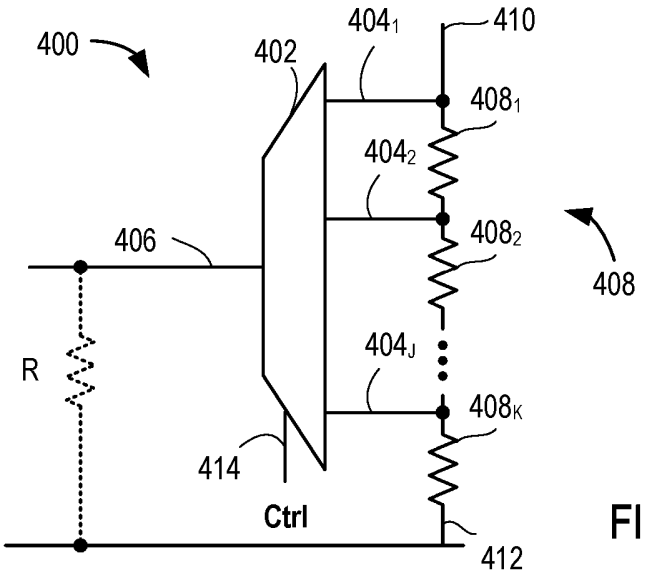
400
402
404_1
410
408_1
404_2
406
408_2
408
R
404_J
408_K
414
Ctrl
412

FIG. 4

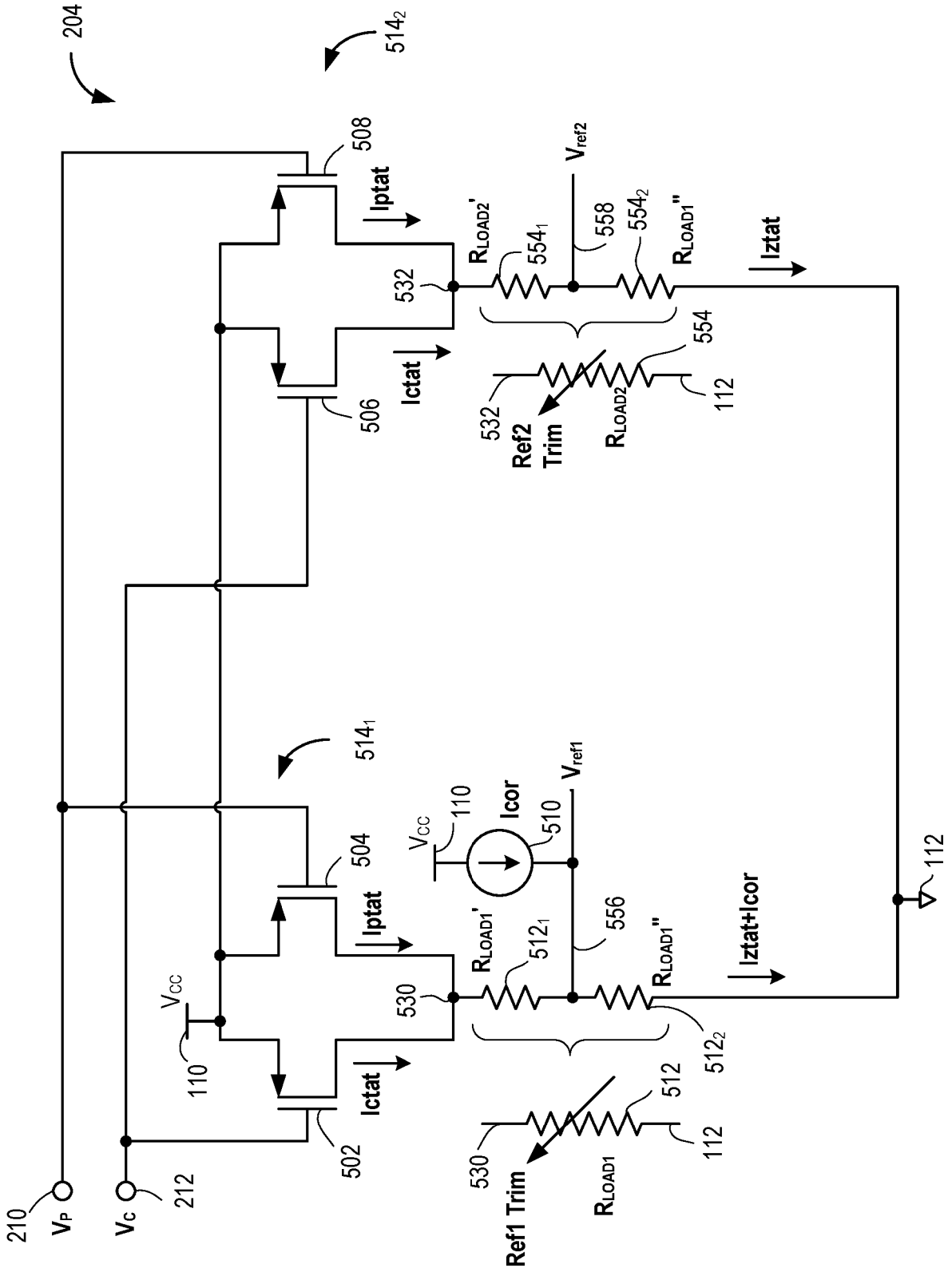
204
514_2
508
Iptat
V_{ref2}
R_{LOAD2}'
554_1
558
554_2
R_{LOAD1}''
Iztat
532
506
Ictat
554
532
Ref2 Trim
R_{LOAD2}
112
514_1
504
Iptat
V_{CC}
110
Icor
510
V_{ref1}
R_{LOAD1}'
512_1
556
R_{LOAD1}''
Iztat+Icor
112
530
512_2
V_{CC}
110
Ictat
502
512
530
Ref1 Trim
R_{LOAD1}
112
210
V_P
V_C
212

FIG. 5A

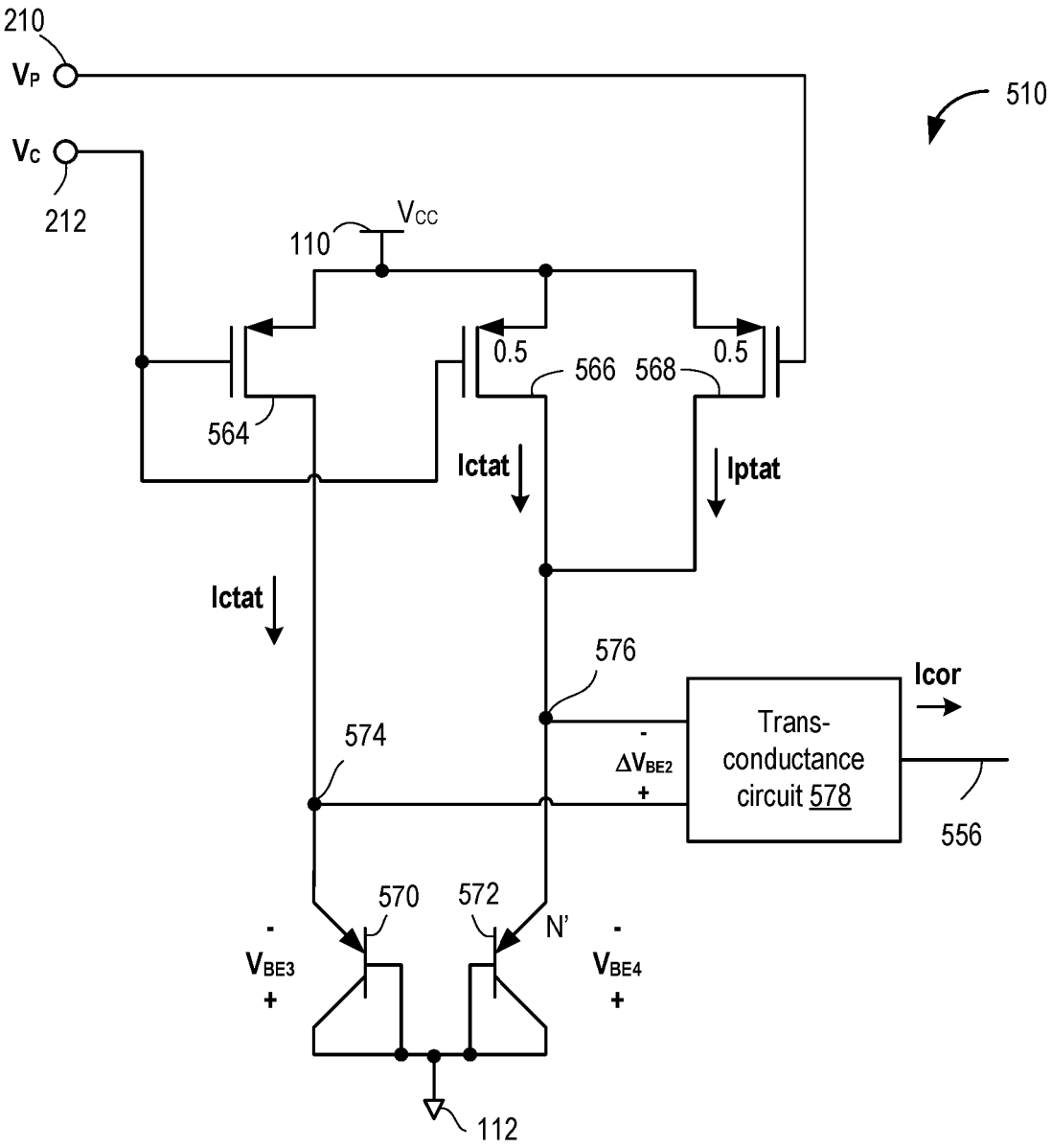
210
VP
VC
212
510
VCC
110
0.5
566
568
0.5
564
Ictat
Iptat
Ictat
576
Icor
574
-
ΔVBE2
+
Trans-
conductance
circuit 578
556
570
572
N'
-
VBE3
+
-
VBE4
+
112

FIG. 5B

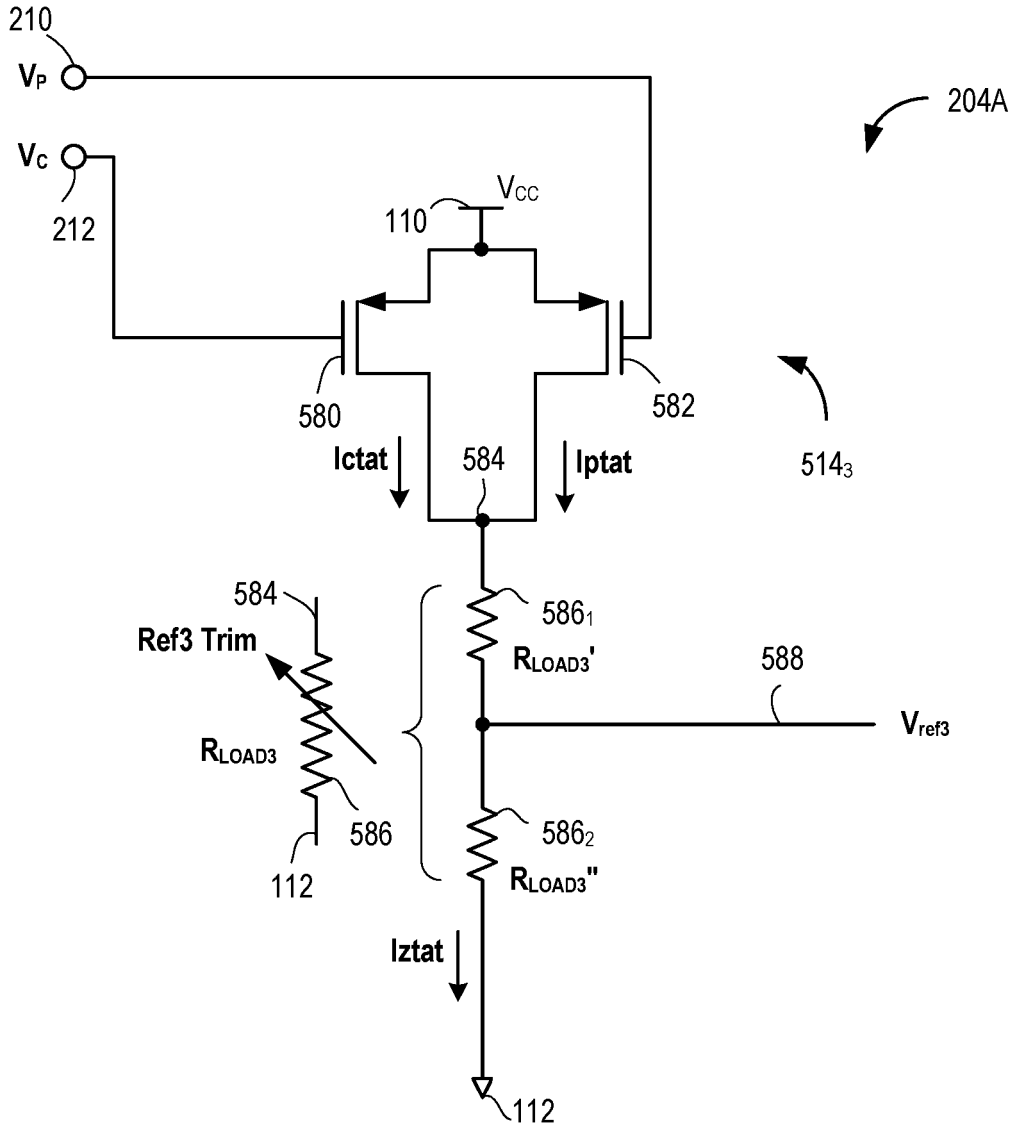
210
VP
VC
212
204A
VCC
110
580
582
Ictat
584
Iptat
514₃
584
Ref3 Trim
586₁
RLOAD3'
588
Vref3
RLOAD3
586
586₂
RLOAD3"
112
Iztat
112

FIG. 5C

512₂

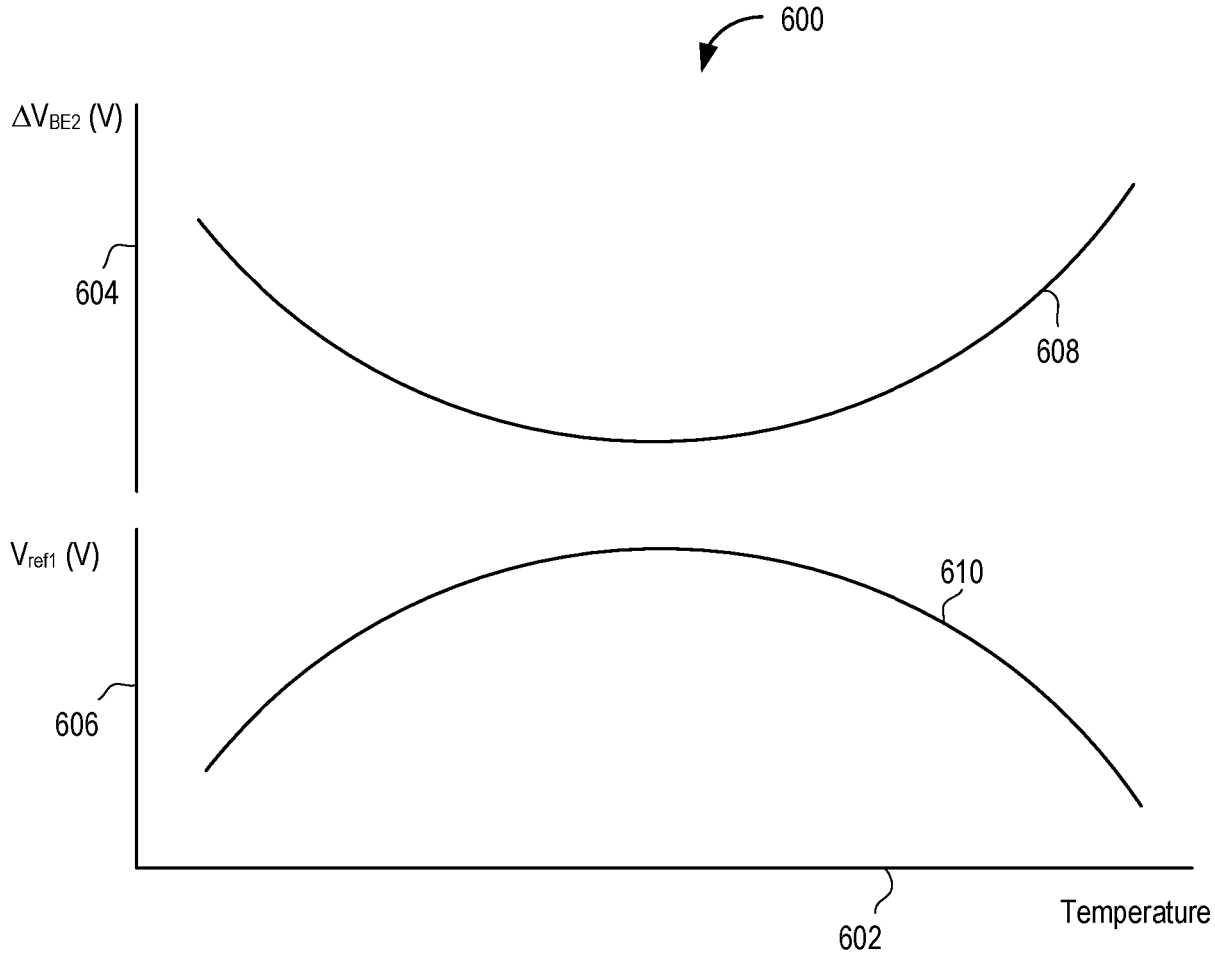

FIG. 6

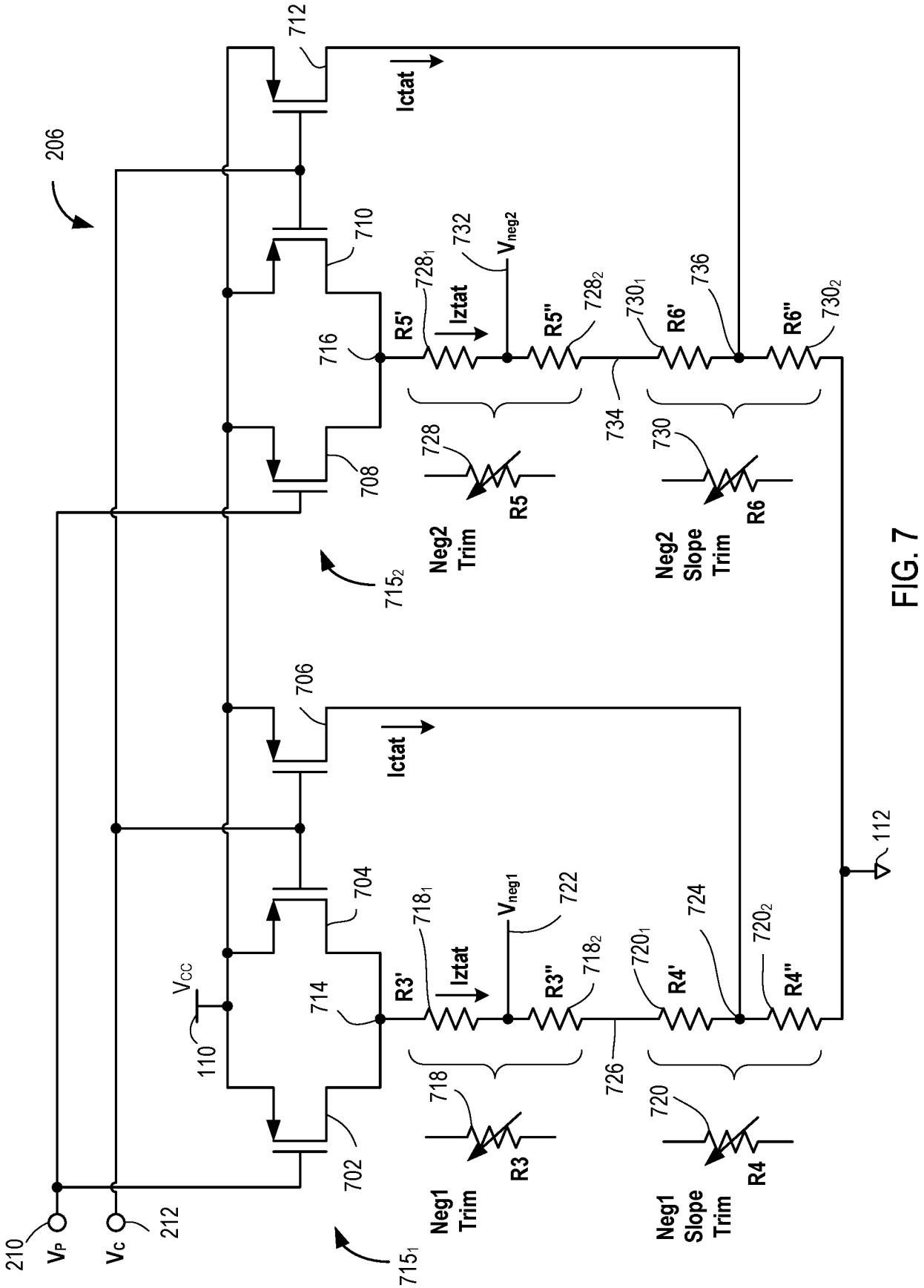
206
712
Ictat
710
716
708
R5'
728_1
732
V_{neg2}
Iztat
R5"
728_2
730_1
R6'
736
R6"
730_2
734
728
730
R5
R6
Neg2 Trim
Neg2 Slope Trim
715_2
706
Ictat
704
714
702
718_1
V_{neg1}
722
Iztat
R3'
R3"
718_2
720_1
R4'
724
720_2
R4"
V_{CC}
110
718
720
R3
R4
Neg1 Trim
Neg1 Slope Trim
726
112
210
V_P
V_C
212
715_1

FIG. 7

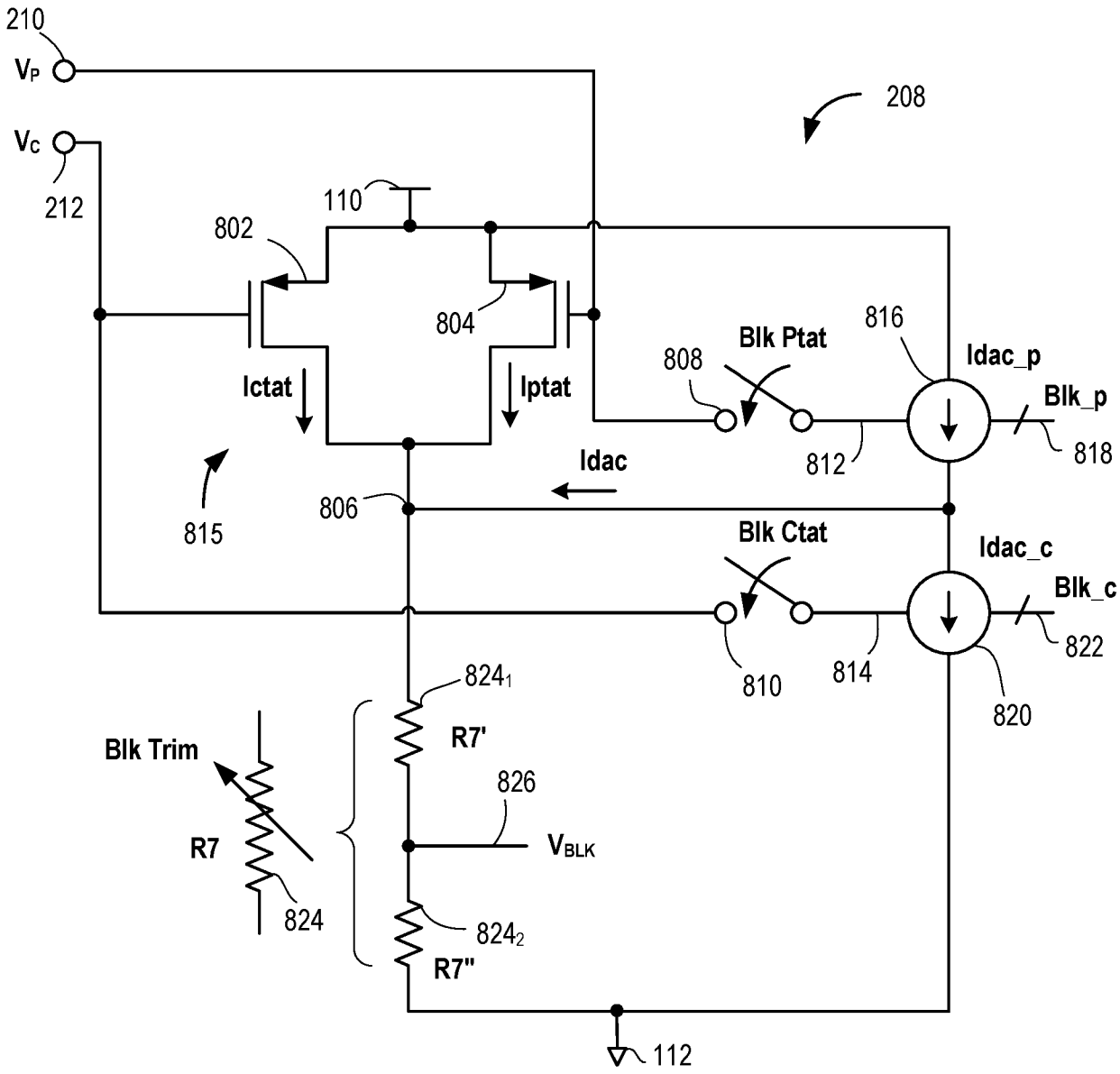
210
V_P
V_C
212
208
110
802
804
Ictat
Iptat
808
Blk Ptat
816
Idac_p
Blk_p
818
812
Idac
806
815
Blk Ctat
Idac_c
Blk_c
822
810
814
820
824_1
R7'
Blk Trim
826
R7
V_{BLK}
824
824_2
R7"
112

FIG. 8

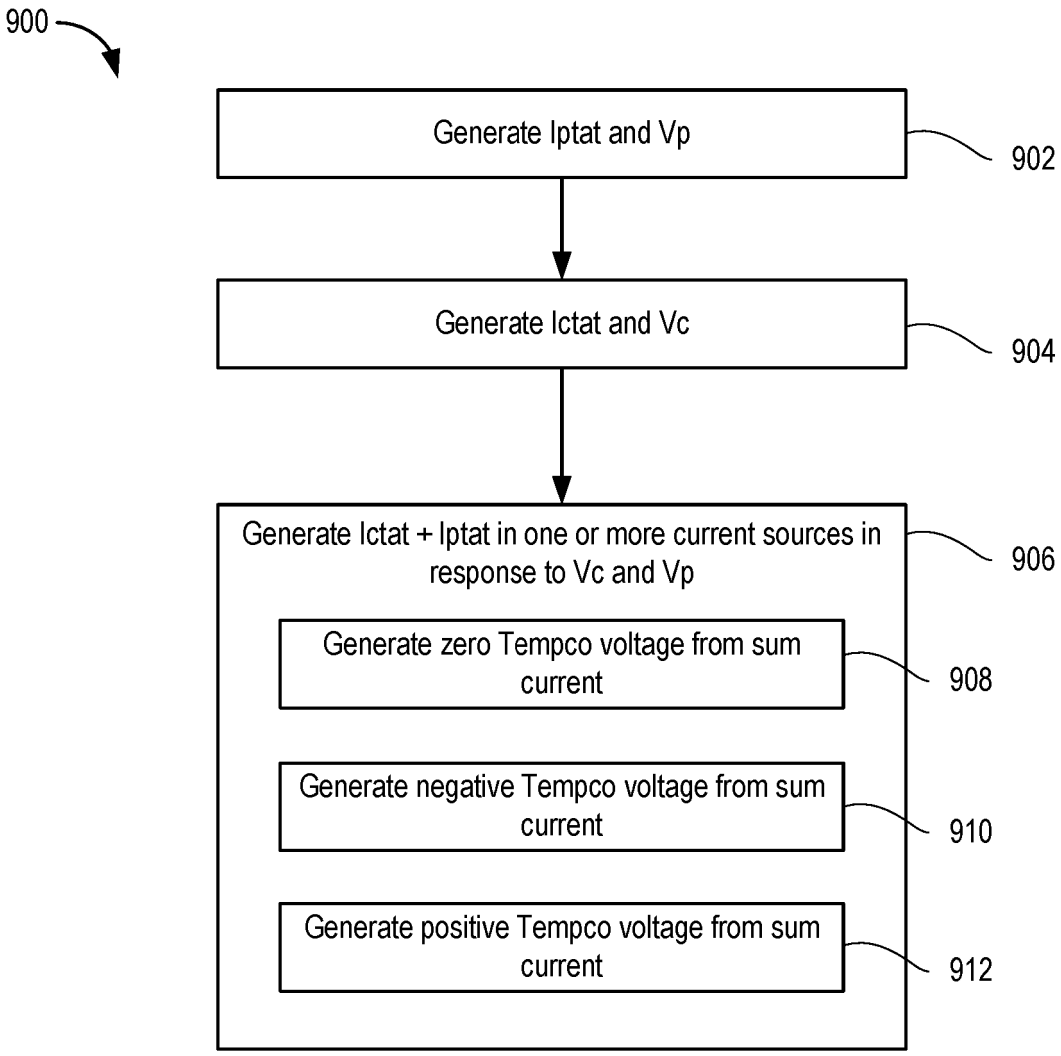
900
Generate Iptat and Vp
902
Generate Ictat and Vc
904
Generate Ictat + Iptat in one or more current sources in response to Vc and Vp
906
Generate zero Tempco voltage from sum current
908
Generate negative Tempco voltage from sum current
910
Generate positive Tempco voltage from sum current
912

FIG. 9

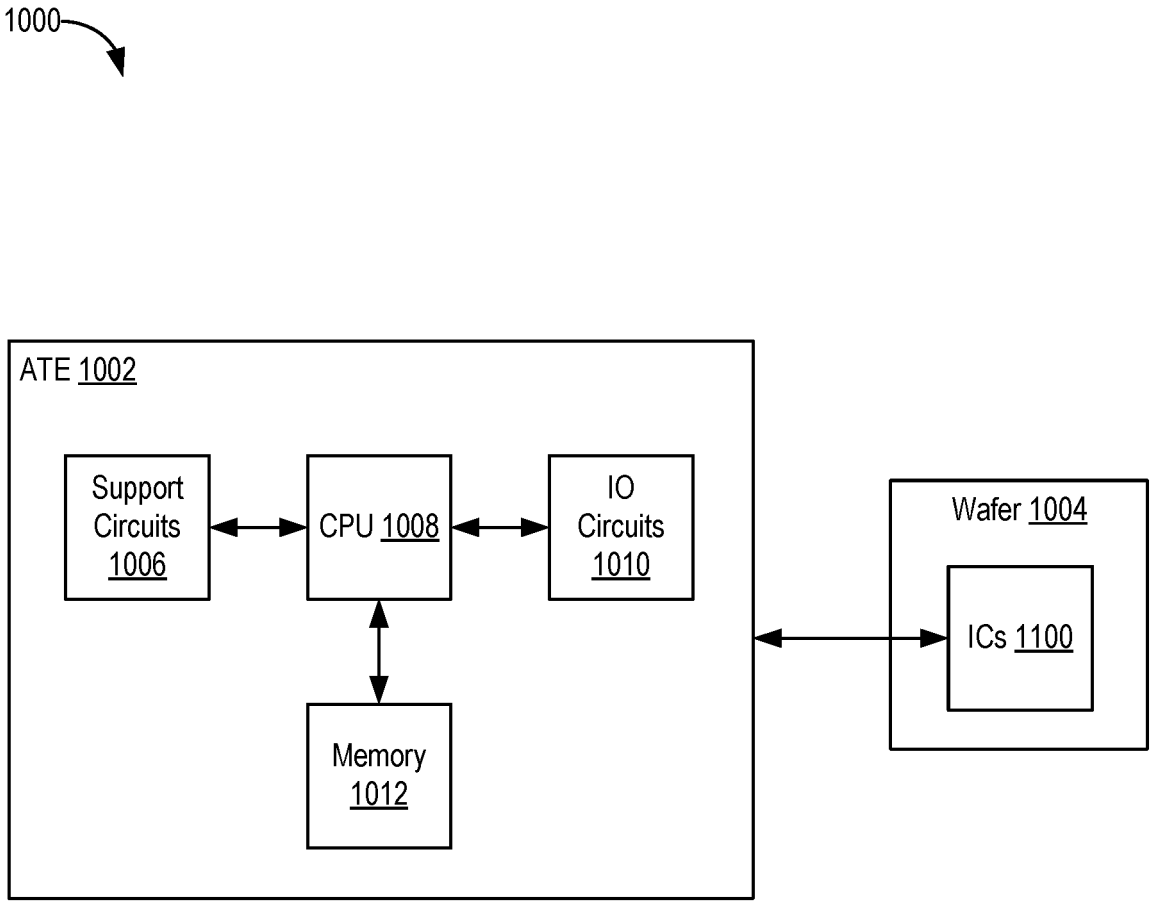
1000
ATE 1002
Support Circuits 1006
CPU 1008
IO Circuits 1010
Memory 1012
Wafer 1004
ICs 1100

FIG. 10

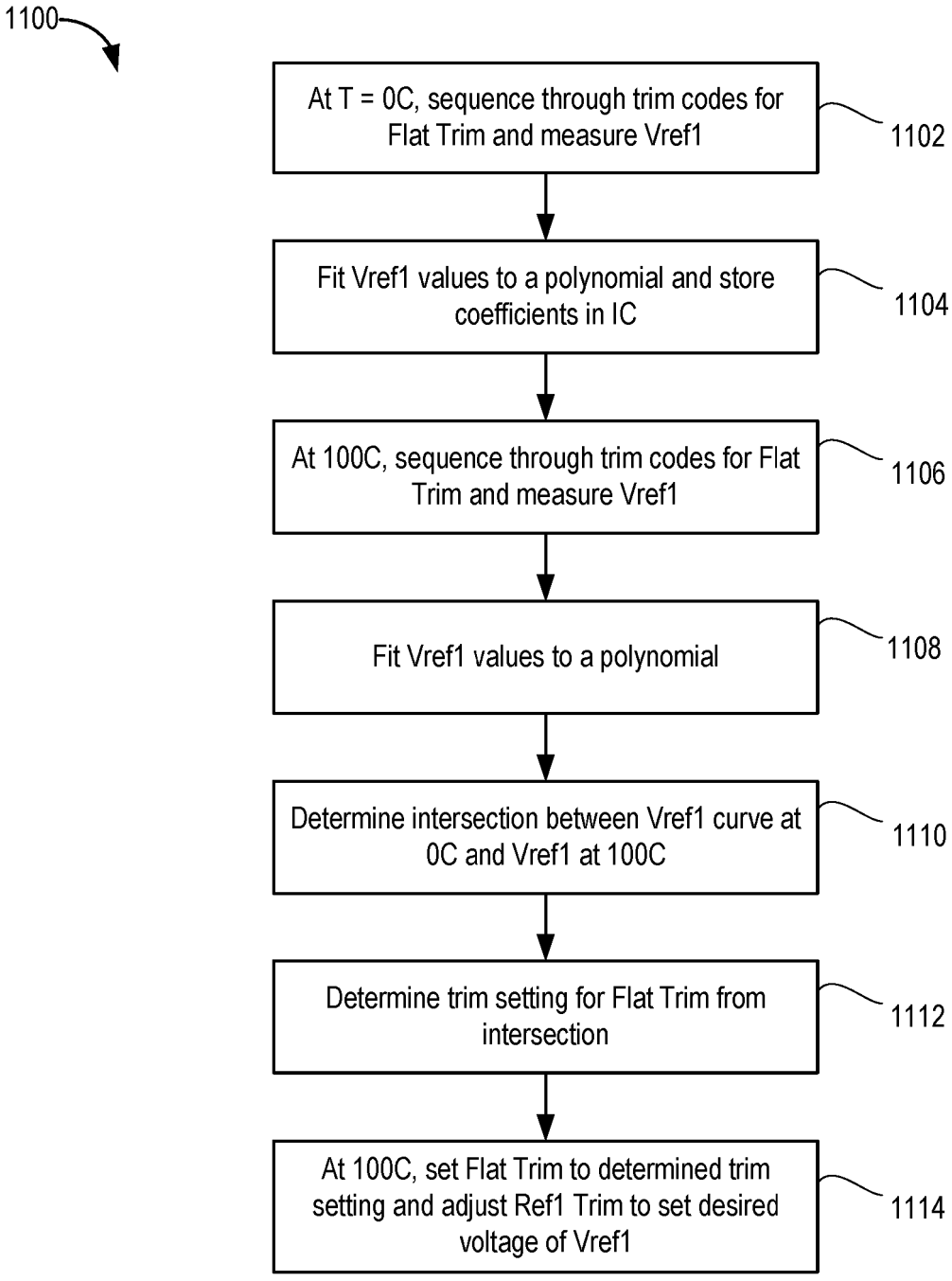
1100
At T = 0C, sequence through trim codes for Flat Trim and measure Vref1
1102
Fit Vref1 values to a polynomial and store coefficients in IC
1104
At 100C, sequence through trim codes for Flat Trim and measure Vref1
1106
Fit Vref1 values to a polynomial
1108
Determine intersection between Vref1 curve at 0C and Vref1 at 100C
1110
Determine trim setting for Flat Trim from intersection
1112
At 100C, set Flat Trim to determined trim setting and adjust Ref1 Trim to set desired voltage of Vref1
1114

FIG. 11

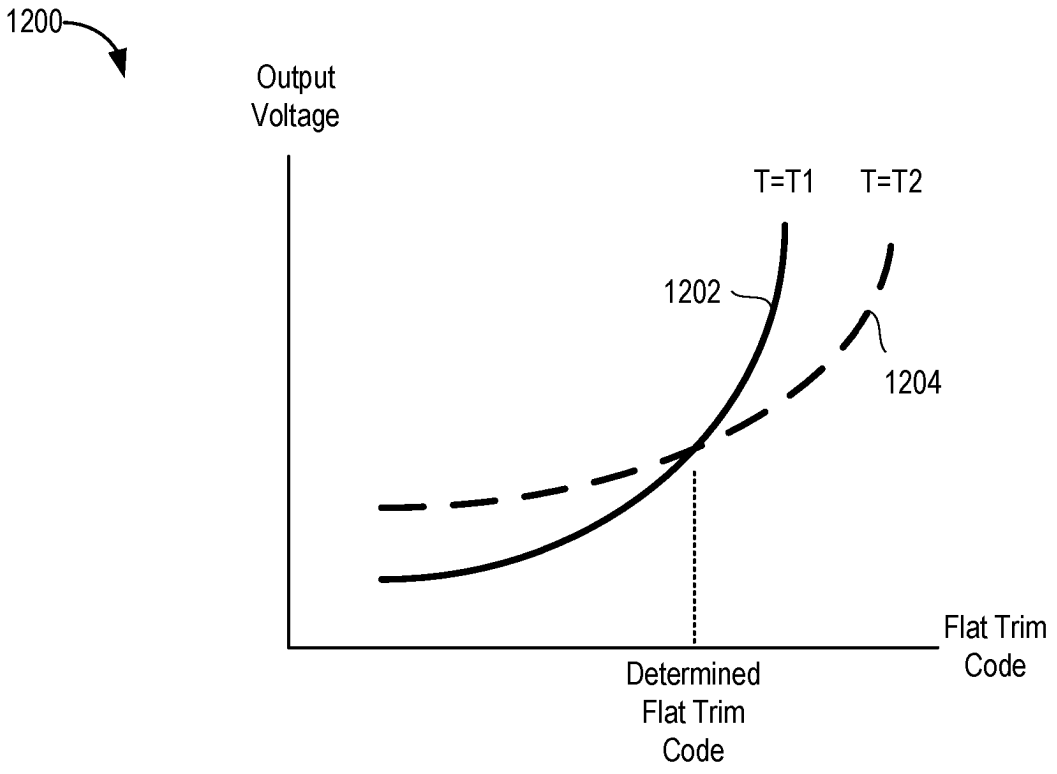

FIG. 12A

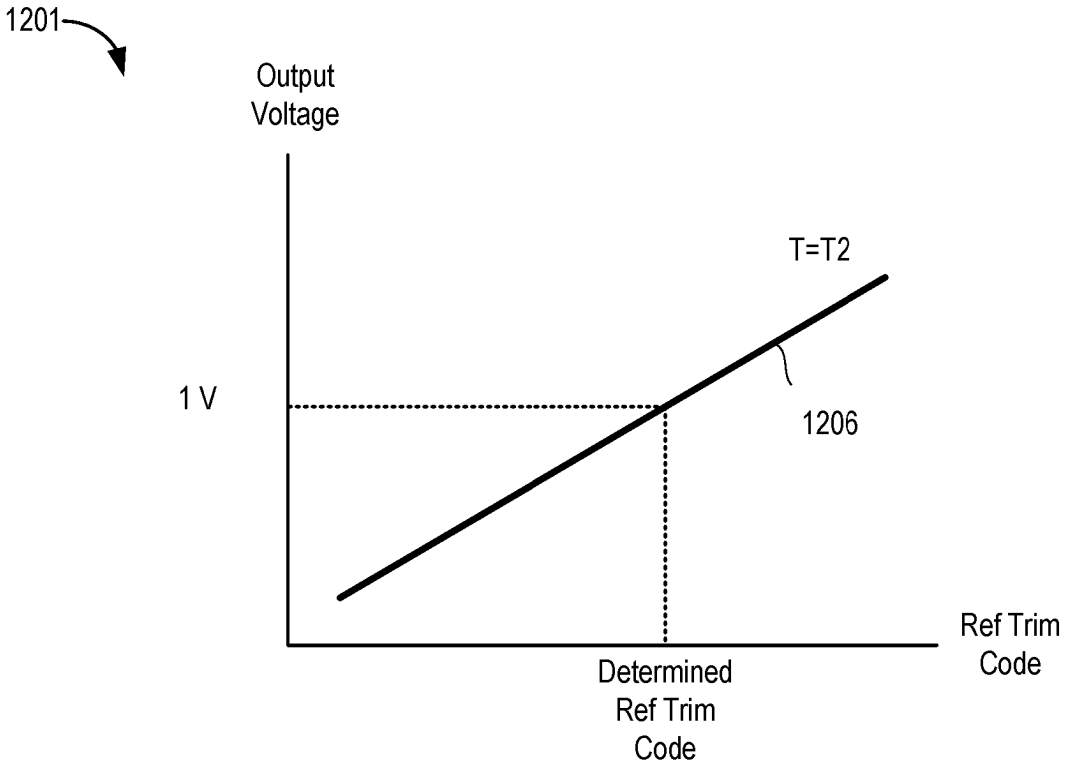

FIG. 12B

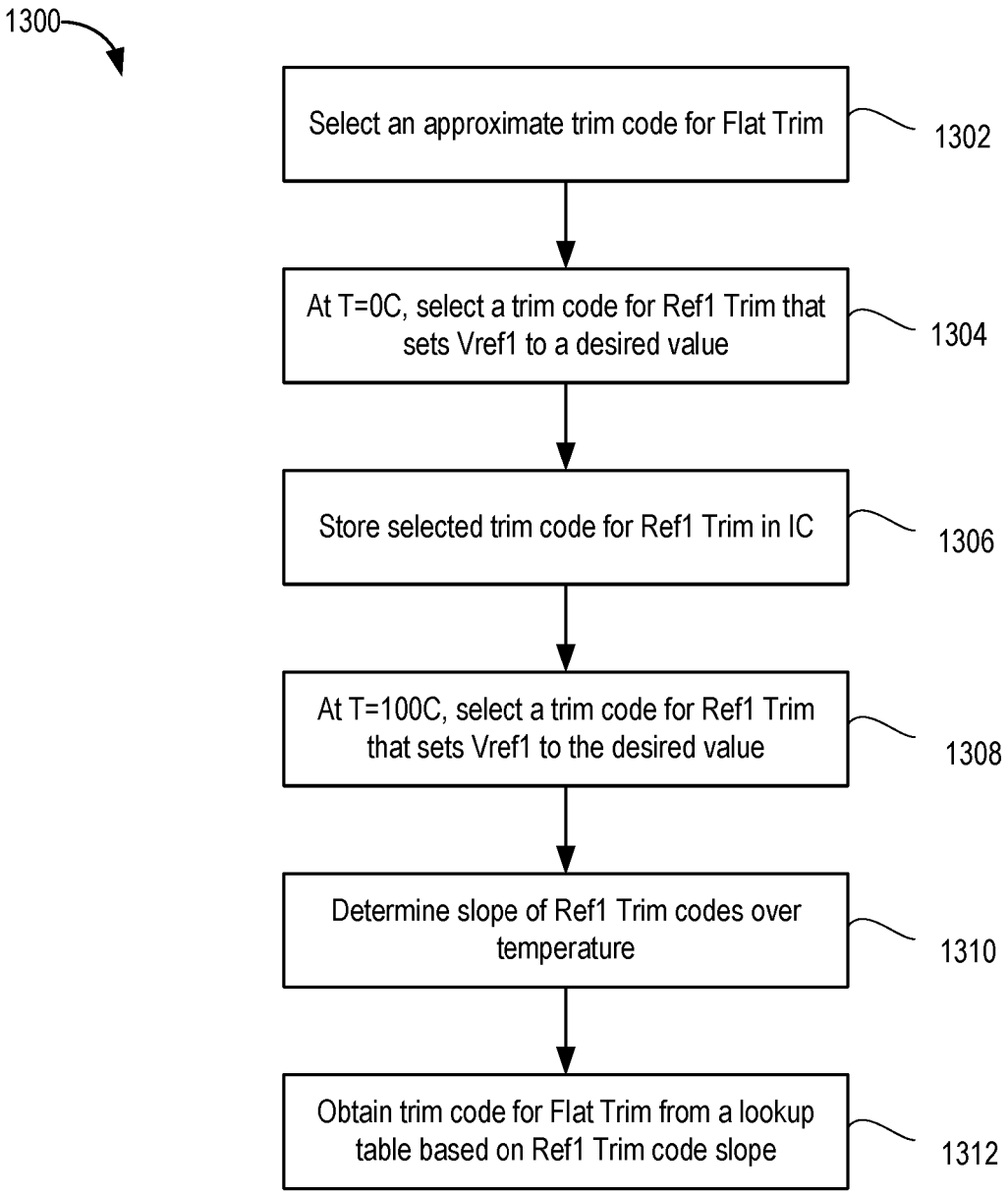
1300
Select an approximate trim code for Flat Trim
1302
At T=0C, select a trim code for Ref1 Trim that sets Vref1 to a desired value
1304
Store selected trim code for Ref1 Trim in IC
1306
At T=100C, select a trim code for Ref1 Trim that sets Vref1 to the desired value
1308
Determine slope of Ref1 Trim codes over temperature
1310
Obtain trim code for Flat Trim from a lookup table based on Ref1 Trim code slope
1312

FIG. 13

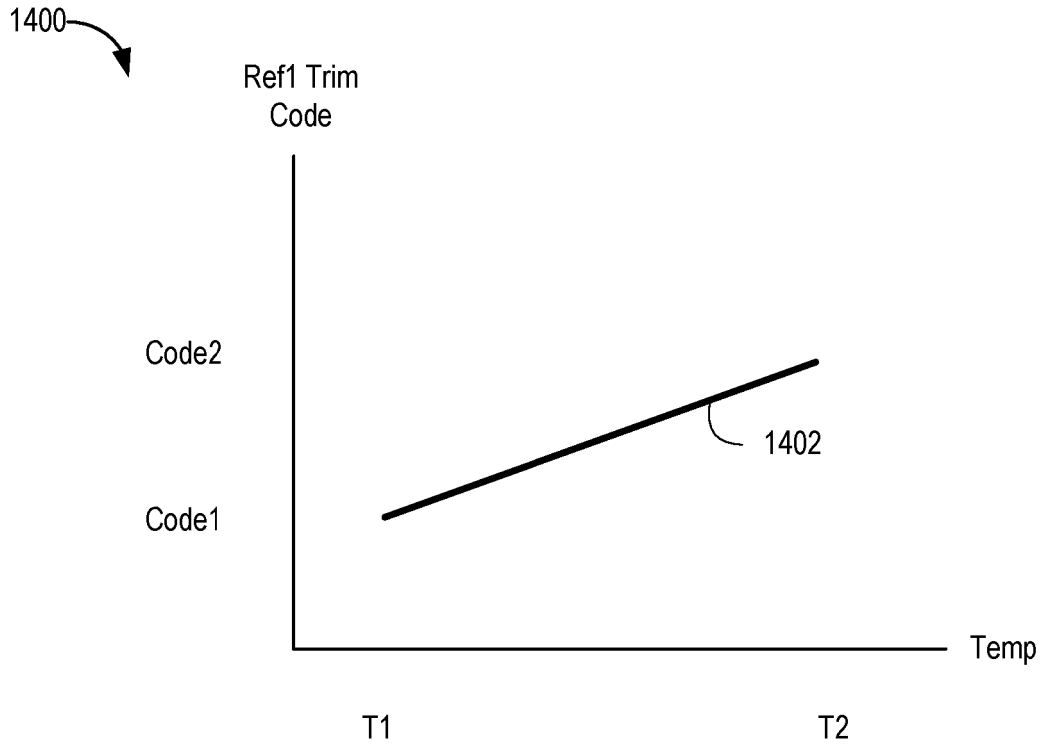

FIG. 14A

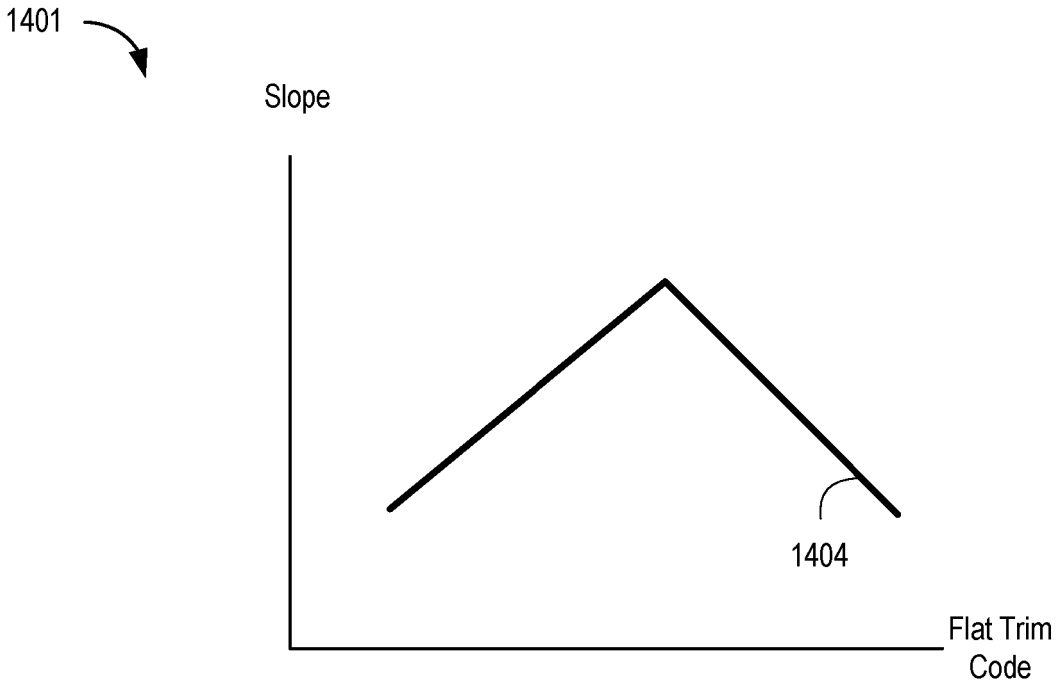

FIG. 14B

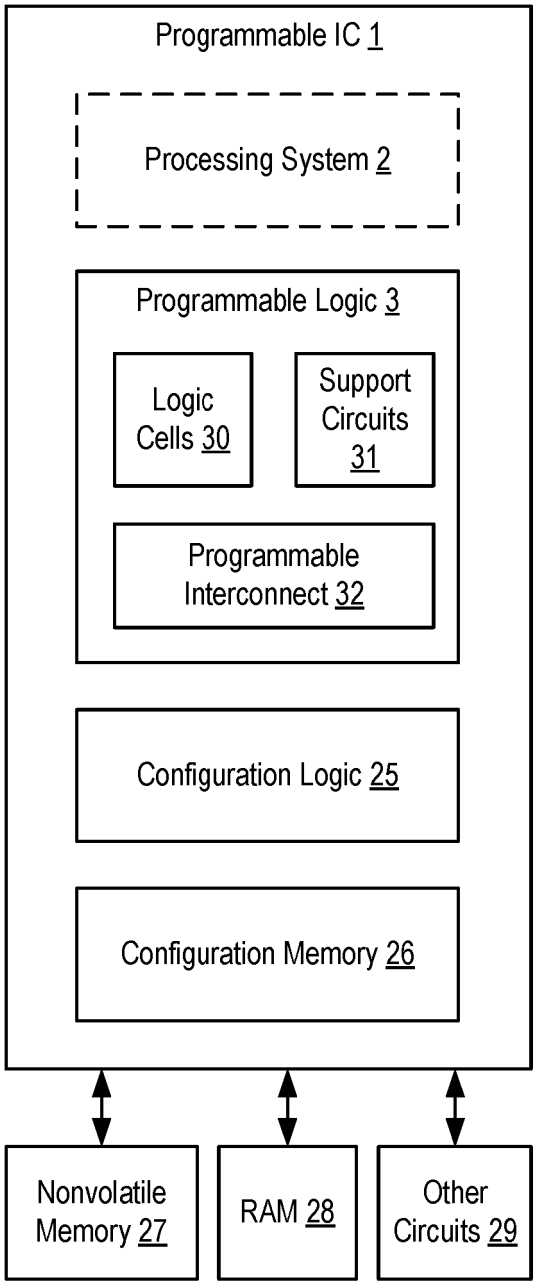
Programmable IC 1
Processing System 2
Programmable Logic 3
Logic Cells 30
Support Circuits 31
Programmable Interconnect 32
Configuration Logic 25
Configuration Memory 26
Nonvolatile Memory 27
RAM 28
Other Circuits 29

FIG. 15

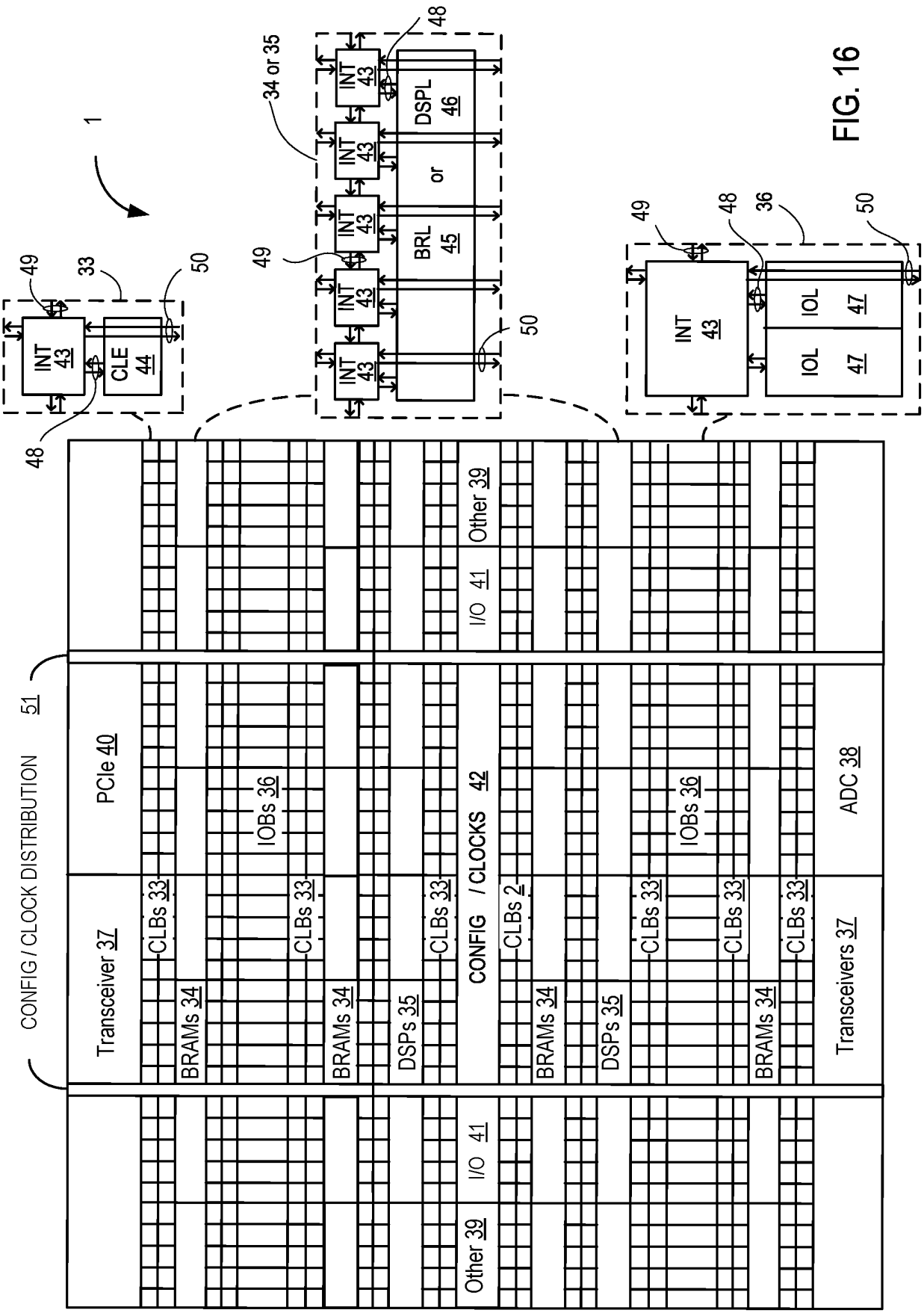
1
34 or 35
48
49
33
50
INT 43
CLE 44
BRL 45
or
DSPL 46
IOL 47
CONFIG / CLOCK DISTRIBUTION 51
PCIe 40
Transceiver 37
CLBs 33
BRAMs 34
IOBs 36
DSPs 35
CONFIG / CLOCKS 42
I/O 41
Other 39
ADC 38
Transceivers 37

FIG. 16

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2006111865 A1 **[0003]**
- US 6265857 B1 **[0004]**
- US 2010301832 A1 **[0005]**