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(54) **Title**: METHOD FOR RESIST DEVELOPMENT IN NARROW HIGH ASPECT RATIO VIAS

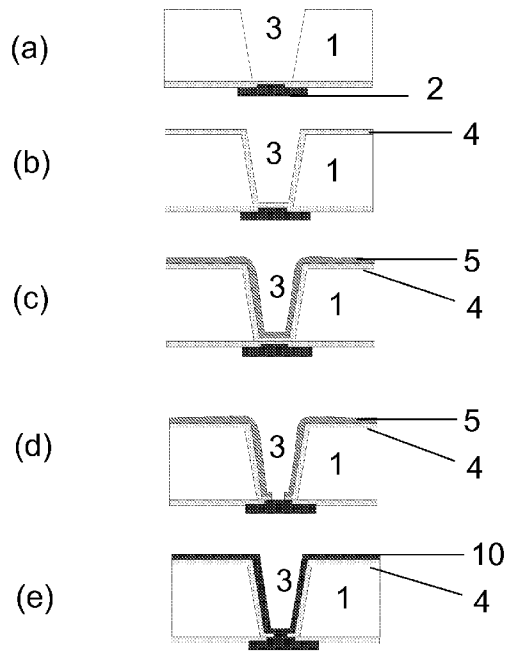


Figure 1

(57) **Abstract**: A method for developing a resist layer inside high aspect ratio vias in a substrate comprising the steps of: (a) applying masked illumination to make certain areas of the resist layer inside the vias soluble and other areas of the resist layer insoluble in a liquid developing solution; (b) applying the liquid developing solution to the resist layer during a predetermined development time for developing the resist layer; (c) removing the liquid developing solution from the resist layer after the predetermined development time. Step b) comprises applying ultrasonic agitation for a predetermined duration to ensure full development of the soluble areas within the predetermined development time.

WO 2010/072246 A1

Method for resist development in narrow high aspect ratio vias

Technical field of the invention

The invention relates to development of a resist layer in a high aspect ratio via in a substrate, particularly applied in the field of semiconductor processing technology, more specifically three-dimensional integration of semiconductor chips.

Background of the invention

R.H. Nilson et al. (in Microsystem Technologies 9, p113-118, 2002) use acoustic agitation to develop LIGA resist. The acoustic agitation is only used to increase the development rate, but does not increase the opening efficiency of the resist layer. Moreover the resist layer is not located in vias.

C. Formato in US 7,029,798 describes a method for forming a pattern in the surface of a resist layer whereby ultrasonic agitation is used for the development of the resist layer. This allows increasing the contrast between the exposed and unexposed regions of the resist layer. Again the method does not increase the opening efficiency of the resist layer and the resist layer is not located in vias.

Nga et al. (in Electronics Packaging Technology Cenference 2006, p831 – 836) describe a method to create through wafer interconnects whereby deep vias are etched in a silicon wafer. Thereby patterning of a resist layer inside the etched vias and etching of holes at the bottom of the vias for contacting underlying devices is done. It was found that not all holes at the bottom of the vias were open and yield loss was observed in case of narrow high aspect ratio vias.

Disclosure of the invention

It is an aim of the current invention to present a method for more effectively developing a resist layer in high aspect ratio vias on a substrate. This aim is achieved according to the invention by the method comprising the steps of claim 1.

As used herein, with ‘via' is intended to mean a cavity, opening, recess, trench, channel, hole or any other via in a substrate.

As used herein, with 'aspect ratio' is meant the ratio of the depth (d) of the via over the diameter at the bottom of the via, or ratio of the depth of a trench (d) over the width at the bottom of the trench (w_{bottom}), i.e. AR = d / w_{bottom} .

As used herein, with 'high aspect ratio' is meant an aspect ratio larger than 1.

The method according to the invention comprises the following steps:

a) applying masked illumination to make certain areas of the resist layer inside the vias soluble and other areas of the resist layer insoluble in a liquid developing solution;

b) applying the liquid developing solution to the resist layer during a predetermined development time for developing the resist layer;

c) removing the liquid developing solution from the resist layer after the predetermined development time;

An analysis of the prior art has shown that yield loss is observed because resist in high aspect ratio vias is not fully developed after the resist development time. Enlarging the resist development time would not be a solution, since this may cause the resist to dissolve at unwanted locations, such as on top of the substrate.

According to the invention, ultrasonic agitation is applied for a predetermined duration to ensure full development of the soluble areas within the predetermined development time.

It has been found that by applying ultrasonic agitation for a duration, chosen in function of a number of parameters, such as for example size and shape of the vias, resist material and thickness, it can be ensured that the soluble areas are effectively developed within the development time.

In preferred embodiments, the predetermined duration comprises at least a first interval, preferably at the beginning of the predetermined development time, i.e. preferably at the start or shortly after the start of the development, for establishing full contact between the developing solution and the soluble areas.

In preferred embodiments, the ultrasonic agitation is applied for enhancing circulation of the liquid developing solution, which might help for example the refreshment of the developing solution inside the vias.

In preferred embodiments, the predetermined duration is chosen such that the soluble areas inside the vias are developed at substantially the same rate as soluble areas of the resist layer outside the vias, for example areas on top of the substrate. This has the advantage that in cases where areas of resist layer are to be developed

both on top of the substrate and inside high aspect ratio vias, the development can be achieved without separate measures to account for different development rates of the different areas (e.g. a thicker resist layer or an additional protective layer on top of the substrate).

In preferred embodiments, the predetermined duration is a total time of 5s to 100s. It has been found that a duration of about 5s can be sufficient, for example for establishing full contact between the developing solution and the soluble areas. A longer period is however preferred for example to enhance the development of the resist. For example, a duration of 15s to 45s can be suitable in most cases, depending on the thickness of the resist layer and the dimensions of the via.

In preferred embodiments, said predetermined duration is divided over a number of time intervals, for example 1x 15 seconds, or 2x 15 seconds, or 3x 15 seconds.

In preferred embodiments, the ultrasonic agitation is within a frequency range of 20kHz - 800kHz, preferably in the range 50 kHz - 400 kHz, for example 40kHz or 50 kHz.

In preferred embodiments, the ultrasonic agitation is applied when resist is to be developed inside vias having a minimum dimension at the bottom below 250µm and an aspect ratio larger than 1. It was observed that the problem of insufficient resist development occurs more in narrow vias with high aspect ratio, especially if the dimensions of the via at the bottom become smaller than 250µm and the aspect ratio is lager than 1.

The resist layer is preferably deposited by spray coating. It has been found that spray coating can give good step coverage.

The invention can be used for example in 3D integration of semiconductor chips, where connection between devices located on different substrates can be achieved by through silicon vias (TSV).

Brief description of the drawings

The invention will be further elucidated by means of the following description and the appended drawings.

Figure 1: Embodiment of a process flow according to the invention for the formation of through wafer interconnects.

Figure 2: Embodiment of process steps according to the invention until etching a hole at the bottom of a deep via hole: (a) a wafer with devices; (b) via holes are etched at the backside of a wafer; (c) deposition of the layer to be etched; (d) resist deposition; (e) illumination of the resist; (f) resist development; (g) result after removal of the developing solution

Figure 3: (a) Bubble prevents development solution to get contact with the resist surface; (b) Immersion development results in incomplete or not open resist layer.

Figure 4: Resist patterned at the bottom of a 100µm deep via using immersion development without ultrasonic agitation.

Figure 5: (a) Immersion in developer during 2 min 30s without ultrasonic agitation; (b) Immersion development during 2min 30s with ultrasonic agitation of 15s.

Figure 6: (a) Immersion development at the bottom of 100µm deep trenches without ultrasonic agitation; (b) Immersion development at the bottom of 100µm deep trenches with 15s ultrasonic agitation.

Detailed description of preferred embodiments

Through silicon via (TSV) technology is an enabling technology for three-dimensional (3D) integrated circuits, 3D packaging and advanced microstructures. In this case through wafer interconnects i.e. electrical connections from one side of the wafer to the other side are made with deep holes or deep vias, also called via in the description below.

To realize the electrical connection to devices, a number of process steps are used, such as forming a deep via in the wafer, electrical isolation and metallization of the vias. In case holes have to be etched in layers at the bottom of the deep vias, for example for electrically contacting underlying devices through (electrically insulating) layer(s), lithographic patterning and etching is done on high topography. According to the invention, embodiments of which are described below, ultrasonic agitation is applied in this process.

Figure 1 shows an embodiment of a method according to the invention, in which different steps used for realising electrical connection to devices in a substrate, for example a silicon wafer. A device or metal layer (2) is fabricated on the front side of the substrate (1). Optionally an electrically insulating layer or dielectric layer (4) is

present between the substrate (1) and the metal layer or device (2) . Furthermore a deep via (3) is etched from the back side in the substrate (1) down to the device at the front side of the substrate (see Figure 1(a)). To electrically isolate the substrate from the conductive filling of the via, an electrically insulating layer or dielectric (4) is deposited in the vias (see Figure 1(b)). At the bottom of the via, this insulating layer is removed or a hole is etched in the insulating layer to realise electrical contact. Therefore a resist layer (5) is deposited on the substrate, in the vias at the sidewalls and at the bottom (see Figure 1(c)). In a next step the resist layer is illuminated in certain areas at the bottom of the vias and developed. During the development time, ultrasonic agitation is applied to ensure development of the illuminated areas. In a next step, holes are etched in the underlying dielectric layer (Figure 1(d)). Finally a conducting layer (10) is deposited in the via thereby realising electrical contact between the back side of the substrate and the device or metal layer (2) at the front side.

The resist layer is preferably deposited by spray coating. Spray coating can be used to realise good step coverage over high topography. Other deposition methods known to the person skilled in the art can however also be used. Another example is spin coating, even though it is somewhat more difficult to realise good step coverage in case of spin coating.

It was found that without applying ultrasonic agitation as it is done according to the invention, not all holes at the bottom of narrow high aspect ratio vias are fully open. In some vias the holes are open (O), in some vias the holes are partially open (P), and in some vias the holes are not open at all (N). This results in yield loss when electrically connecting devices. Possible explanations for the problem that not all soluble areas are fully developed will be described below.

The different steps, including the lithography with the development of the resist layer, are illustrated in Figure 2. A device or metal layer (2) that is to be contacted through the substrate (1) can be located in or on the back side of a substrate (1): see Figure 2(a) respectively left and right. A via (3) is etched in the substrate (1). The via etching can stop in the substrate (1), for example in an intermediate layer, before the metal layer or the device (2) is reached (see left via in Figure 2(b)). The via can also be etched down to the metal layer or device (2) (see right via in Figure 2(b)). To electrically isolate the substrate from the conductive filling of the via an electrically insulating layer or dielectric (4) can be deposited in the vias

(Figure 2(c)). This layer is not necessary in case an insulating substrate (1) is used or in case electrical contact is not realised. For patterning the bottom of the via or trench (3), a resist layer (5) is deposited (Figure 2(d)). The resist layer is deposited at the sidewalls and the bottom of the via or trench, thereby leaving a vacancy or unfilled region in the centre of the trench or the via. Then the resist layer is illuminated (7) on certain locations, called first areas (5b), for example through a mask (6) (Figure 2(e)) and developer (8) is introduced on the substrate (Figure 2(f)), for example by immersion of the substrate in the developing solution. In case of a positive resist, the resist becomes soluble in a developer at the illuminated areas and the resist will be removed at these locations (Figure 2(g)). The resist can be illuminated at first areas at the bottom of the vias or trenches and meanwhile second areas at the surface can be illuminated (Figure 2(g)). In case of a negative resist, the resist becomes insoluble in a developer at the illuminated areas and the resist will be removed at locations that are not illuminated. While the developing solution is present on the substrate and in the vias, ultrasonic agitation is applied to ensure development of the soluble areas. After development of the resist layer (Figure 2(g)), the underlying layer(s) can be etched at these locations.

The problems with opening the holes at the bottom of narrow high aspect ratio vias can be caused by problems with the development of the resist layer inside narrow high aspect ration vias. In that case, the illuminated resist layer is not always fully developed at the bottom of the vias. The result is that in some vias the holes in the resist layer are fully open (O), in some vias the holes are partially open (P), and in some vias the holes are not open at all (N).

Through silicon via (TSV) technology is one example where patterning is needed at the bottom of narrow high aspect ratio vias. The shape of the vias may vary. Seen from the top the vias can be holes with circular, oval, square, cross, star, … shape. The vias can also be trenches. Patterning in deep narrow trenches may also be used for certain applications. Seen from the top the trenches can be straight or curved, rectangular, meander-shaped or irregular, ….Also in that case it may be difficult to fully develop a resist layer at the bottom of deep narrow trenches. The description below relates to different applications, such as the fabrication of 3D structures, multi-level bulk micromachining structures, etc. ….

In cross section, the deep vias or trenches can be straight, but they can also be tapered. The diameter at the bottom of the vias or the width at the bottom of the

trenches can be smaller than the diameter at the top of the vias or the width at the top of the trenches. The angle of the sidewall of the via or the trench with the plane of the substrate can be between 45° and 90°, more preferably between 60° and 90°, but any other angle is possible. Furthermore the sidewalls of the vias or the trenches can be straight, but can also have curvature.

In case of narrow vias with for example a diameter at the bottom < 250μm or < 200μm, with a high aspect ratio (AR), for example with AR > 1 or AR > 2 the development of the resist layer at the bottom of the vias becomes difficult. For trenches the development of the resist layer at the bottom becomes difficult with a width at the bottom < 150μm or < 200μm, with a high aspect ratio (AR), for example with AR > 1 or AR > 2 or AR >4. In fact the method can be used to develop a resist in other high aspect ratio vias in a substrate, including but not limited to trenches, vias, circular holes, oval holes, cross-shaped holes, ...

The present invention relates to an improved method to fully develop a resist layer, preferably a positive resist layer, inside or preferably at the bottom of high aspect ratio vias.

It was found that applying a short ultrasonic agitation improves the development of resist, especially at the bottom of the vias. By optimisation of the exact duration of the ultrasonic agitation and the number of times the ultrasonic agitation is used, full development of the soluble areas of the resist can be ensured, both at the surface of the substrate and in the vias.

The duration of the ultrasonic agitation depends among others on the thickness of the resist layer at the bottom of the via. Ultrasonic agitation can accelerate the dissolving rate of the illuminated resist therefore the thicker the resist layer the longer the ultrasonic agitation could be added. The duration of the ultrasonic agitation can for example vary between 5 sec and 100 sec. The dimensions of the vias, the AR, and the resist material are other parameters which can influence the development time and the duration of ultrasonic agitation.

The duration of ultrasonic agitation is chosen to ensure that the resist is fully developed. On the other hand the ultrasonic agitation can not be too long as long ultrasonic agitation times may cause resist delamination, especially at the surface of the substrate. Delamination of resist from the surface depends on the surface of the substrate, for example the nature of the substrate. Also the cleaning of the surface

can have an influence on the adhesion. Furthermore the density of the vias or holes has an influence on the delamination, especially on the surface of the substrate, for example at the areas with very dense structures. In that sense several times a short ultrasonic agitation (for example of 5 sec – 20 sec) is better than one long time.

The frequency of the ultrasonic duration can vary between 20kHz and 800 kHz, or between 30 kHz and 500 kHz or preferably between 50 and 400 kHz. A higher frequency will limit the risk of delamination of the resist layer. A lower frequency increases the development rate. The frequency can be optimized depending on the adhesion properties of the resist layer to the surface, resist thickness, and the time the ultrasonic is applied.

A possible explanation for the problem of opening the resist layer can be that in case of narrow vias or trenches with high aspect ratio (AR), it is more difficult for resist solution to fully reach the bottom. In case of narrow high aspect ratio vias, for example when using immersion development, the developing solution cannot fully reach to the bottom of high aspect ratio vias, resulting in partly or non open resist pattern at the bottom of at least part of the vias. This results in yield loss. Poor wetting, bubbles can prohibit the contact of resist solution to the resist surface at the bottom of the vias.

This is illustrated in Figure 3. Bubbles in Figure 3(a) prevent the developer to reach all the illuminated resist. As such the illuminated resist is not developed everywhere, as represented in Figure 3(b). A short ultrasonic agitation can make the developing solution fully reach the bottom of high aspect vias and can assist the development of resist.

Another possible explanation is that in narrow high aspect vias the circulation of developing solution inside via or trench is also limited. Applying an short ultrasonic agitation may assist the circulation, refreshment of development solution and increase the dissolving rate of illuminated resist at the bottom of the vias.

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Example 1: patterns in via

For characterizing the photoresist coating process, sloped vias with the bottom dimensions ranging from 20µm to 150µm in diameter were etched on 200mm Si wafer. The via depth was between 60 µm and100µm. The AR varied between 1 and 3. Wafers were spray coated with AZ4562 (using EVG101 system) and AZ9260

resist (using Delta-AltaSpray). A photolithography step was applied to pattern the resist layer at the bottom of the via. Contact holes at the bottom of the vias were illuminated using UV broadband (wavelength 350-450nm) followed by a resist development step. The development was done by immersion using solution of 351:DI (1:3) (alkaline based developer). The wafer was dipped in a beaker (tank) filled with this development solution.

Figure 5 (a) shows vias after immersion in developer during 2 min 30s without ultrasonic agitation. It can be observed that no pattern is open inside 150µm via. In this case, the illuminated resist pattern on top surface is open but the same pattern on bottom of 100µm deep via is not open.

A development time of 2.5 min was enough to open resist pattern with thickness up to 4µm on the surface. Due to wetting problems and/or bubbles in the vias, the development solution could not reach to the bottom of the vias. In that case a longer time was needed. Therefore resist at the bottom of via could not be resolved. Even after a development time of 5 min still not 100% of the patterns were open at the bottom of the via (as can be seen in Figure 4). Figure 4 shows a resist patterned at bottom of vias with a diameter of 100µm and a depth of 100µm using immersion development without ultrasonic agitation: some patterns are open (O), some partly open (P) and some not open (N).

A longer development could not solve the problem and very long development times damaged resist patterns at the surface of the substrate, especially with the resist pattern on the top surface which requires only normal development time (2.5 min) to open.

In order to fully open the patterns at the bottom of the vias, a short time ultrasound agitation of 15s was added. An ultrasonic duration and a standard development time could resolve the pattern at the bottom of vias in case of a resist thickness between 1 and 4µm. The ultrasonic agitation of 15s was added during the development process 2.5 min. This may improve the contact of developer solution to the resist surface and enhance the circulation of solution inside the high aspect ratio structure (via diameter of 20-50µm with via depth of 60-100µm respectively). Using ultrasonic agitation, the resist pattern at the bottom of the vias were fully opened.

Figure 5 (b) shows vias after immersion development 2min 30s with ultrasonic agitation of 15s. The patterns are 100% open at the bottom of 150µm via. All resist patterns at bottom of the vias are open. Different dimension of resist patterns on

each row were used: pattern resist diameter of 75 µm, 50 µm, and 30µm are open at the bottom of 150µm via.

For ultrasonic agitation, the development tank was placed in an ultrasonic bath with the frequency of 50kHz. The ultrasonic was only applied for the first 15s of the development process. After that the ultrasonic power was set off

Example 2: patterns in trenches

A similar experiment has been carried out to pattern the resist at the bottom of high aspect ratio trenches. The coating, resist exposure and development were as described in the previous experiment. In this case the trenches had a width between 20 µm and 150µm, length of 450µm, and depth between 90 µm and 120µm, respectively. The resist thickness at the bottom of the trench was about 5µm. The development time was 2 min and 30s.

Figure 6(a) represents trenches after immersion development without ultrasonic agitation). Patterns are partly opened at the bottom of 100µm deep trenches. In this figure, row 1, 2 ,3 are trenches with the width of 150, 100 and 75µm respectively. Patterns with size 70x40µm, 50x30µm, 40x25µm were exposed at the bottom of the trenches with the width of 150, 100, 75µm, respectively After 2.5 min development, only some resist patterns were open at the bottom of the trench but not all. In the trench a with of 150µm, one pattern at the right side was not resolved. In the trench with a width of 100µm, 2 patterns were not open. However more patterns were open in trenches as compared to the case of vias. Although the aspect ratio is the same, the trench length is larger than the via diameter. This may help the solution to reach to the bottom of the trenches easier.

To get 100% yielded open pattern in the resist at the bottom of the trenches, the sample was developed during 2.5 min, using ultrasonic agitation. The method for development with ultrasonic agitation is described in the previous experiment.

Figure 6(b) represents trenches after 2 min 30 s immersion development with 15s ultrasonic agitation. The patterns are fully open at the bottom of the trenches. This shows that ultrasonic agitation is able to open the holes at the bottom of the trenches.

Example 3 resist thickness and ultrasonic time

As mentioned in previous experiments, for the resist thickness up to 4µm, only 1 time 15s for ultrasonic agitation was applied during development. In case of the thicker resist at the bottom of via (up to 15µm), the development time was longer (5min). In this case, 3 times ultrasonic of 15s was applied during the whole development period of 5 min. All vias were found to be completely open. The explanation can be that the ultrasonic agitation enhances the circulation of solution, i.e. refreshment of development inside high AR via, thus accelerating the dissolving rate of resist in the developer. Applying 3 times 15s, but not 1 time 45s allows to refresh several times the development solution inside the vias.

Applying the ultrasonic agitation more times did give the same result, i.e the resist is open on all locations. For thicker resist layers, longer ultrasonic time agitation can be used to speed up the development.

Example 4:

It was found that resist has a better adhesion on a Ti surface than on a Si surface. For an ultrasonic agitation duration of 15s (at a frequency of 40kHz-50kHz) no delamination of resist on Ti or Si was observed. In case of Si, delamination was observed with ultrasonic times longer than 2 min in dense via areas (via of 10µm diameter at a spacing of 90µm). Only limited delamination was observed in case of resist on Ti using the same conditions.

Claims

1. A method for developing a resist layer inside high aspect ratio vias in a substrate comprising the steps of:
   a) applying masked illumination to make certain areas of the resist layer inside the vias soluble and other areas of the resist layer insoluble in a liquid developing solution;
   b) applying the liquid developing solution to the resist layer during a predetermined development time for developing the resist layer;
   c) removing the liquid developing solution from the resist layer after the predetermined development time;

   characterised in that step b) comprises applying ultrasonic agitation for a predetermined duration to ensure full development of the soluble areas within the predetermined development time.
2. A method according to claim 1, wherein the predetermined duration comprises at least a first interval at the beginning of the predetermined development time for establishing full contact between the developing solution and the soluble areas.
3. A method according to claim 1 or 2, wherein the ultrasonic agitation is applied for enhancing circulation of the liquid developing solution.
4. A method according to any one of the previous claims, wherein the predetermined duration is chosen such that the soluble areas inside the vias are developed at substantially the same rate as soluble areas of the resist layer outside the vias.
5. A method according to any one of the previous claims, wherein said predetermined duration of said ultrasonic agitation is a total time between 5s and 100s.
6. A method according to any one of the previous claims, wherein said predetermined duration of said ultrasonic agitation is a total time between 15s and 45s.
7. A method according to any one of the previous claims, wherein said predetermined duration is divided over a number of time intervals, said time intervals varying between 5s and 45s.

8. A method according to any one of the previous claims, wherein said ultrasonic agitation is within a frequency range between 20kHz and 800kHz.
9. A method according to any one of the previous claims, wherein said ultrasonic agitation is within a frequency range between 50kHz and 400kHz
10. A method according to any of the previous claims wherein the vias have a minimum dimension at the bottom below 250 μm and an aspect ratio larger than 1.
11. A method according to any of the previous claims wherein the thickness of the resist layer is between 1μm and 15μm.
12. A method for fabricating a semiconductor device, comprising the step of developing a resist layer according to the method of any one of the previous claims.
13. A method according to claim 12, comprising the steps of, before developing the resist layer:
    a) providing the substrate;
    b) manufacturing at least one device or metal layer on a front side of the substrate;
    c) etching a high aspect ratio via in a back side of the substrate towards the device or metal layer;
    d) depositing the resist layer on the back side of the substrate and in the via.
14. A method according to claim 13, further comprising the step of depositing a dielectric layer on the back side before depositing the resist layer.
15. A method according to claim 13 or 14, further comprising the steps of, after developing the resist layer, etching a hole in the part of the substrate in the high aspect ratio via exposed by development of the soluble area of the resist layer, and depositing a conductive layer in the via to establish a conductive contact with the device or metal layer on the front side of the substrate.
16. A method according to any one of the claims 13-15, wherein the resist layer is deposited by spray coating.

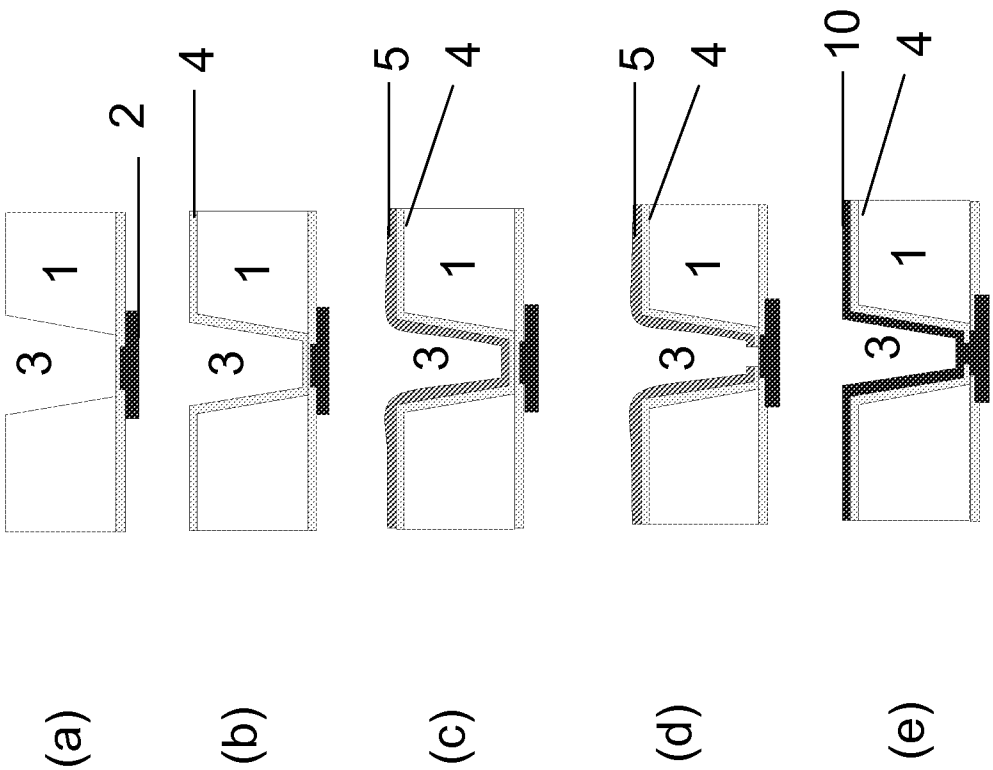


Figure 1

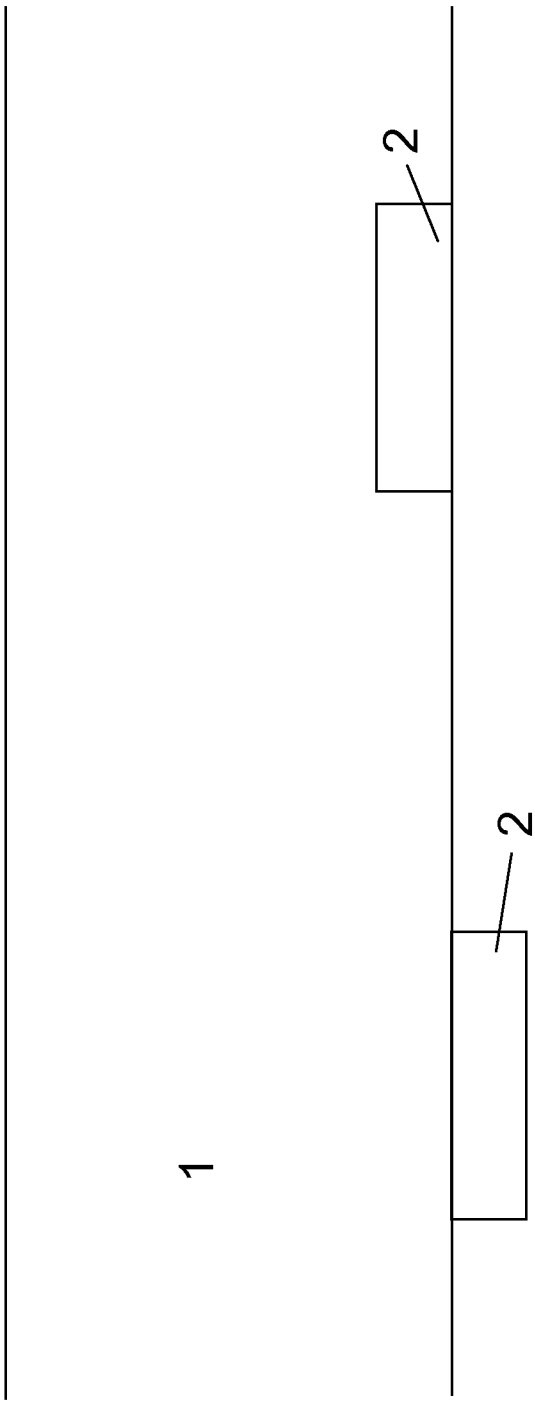


Figure 2(a)

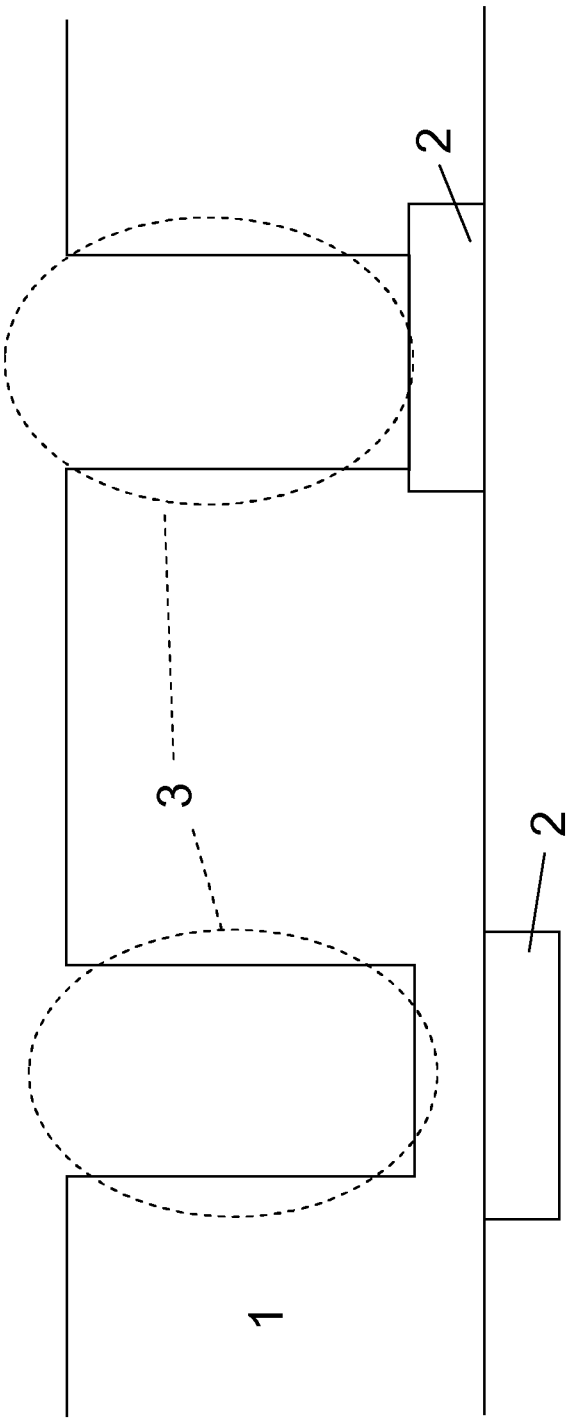


Figure 2(b)

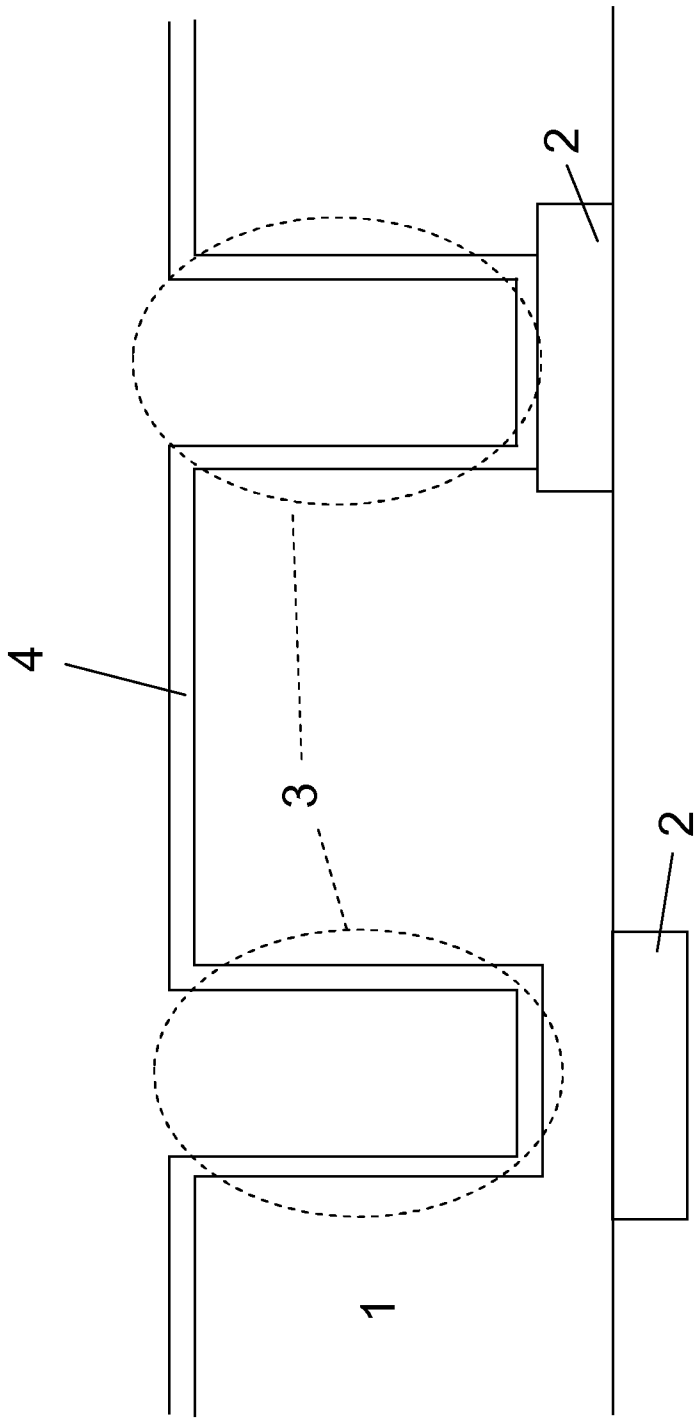


Figure 2(c)

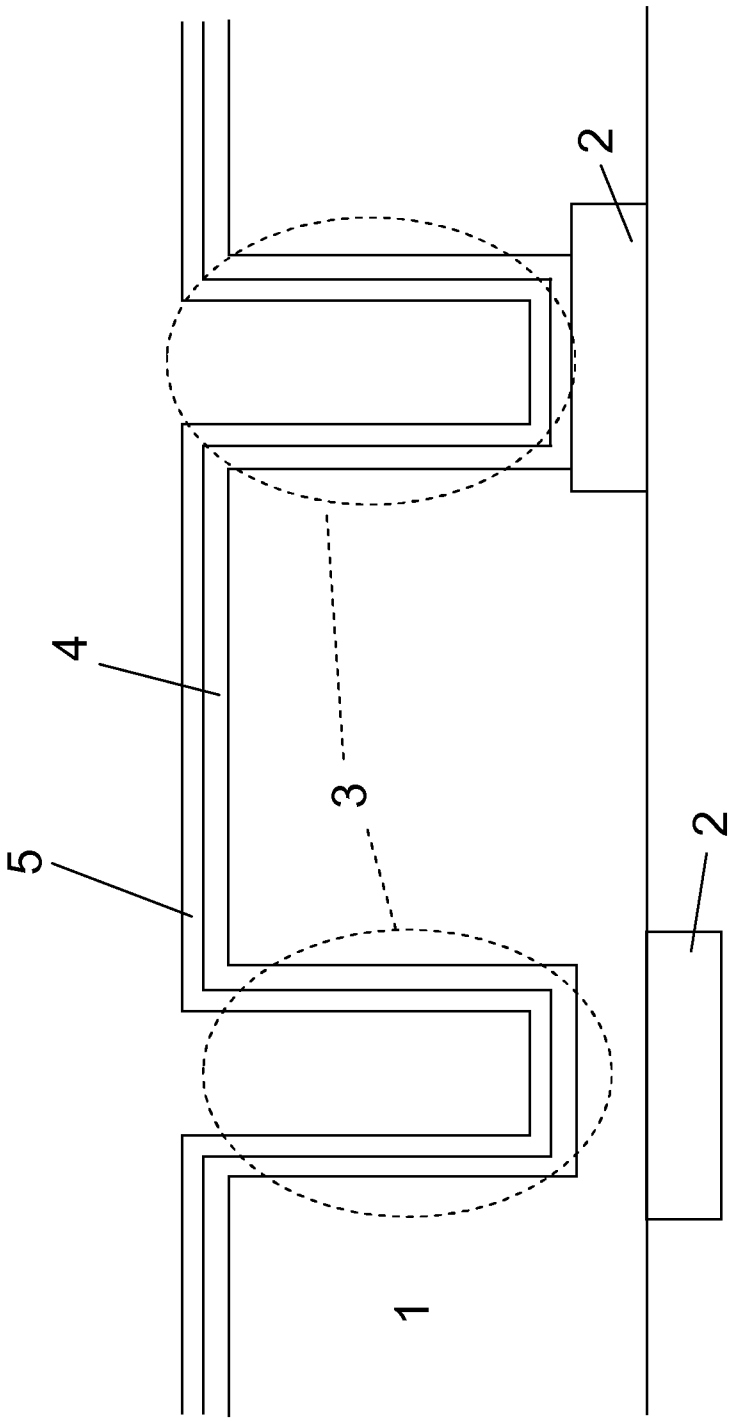


Figure 2(d)

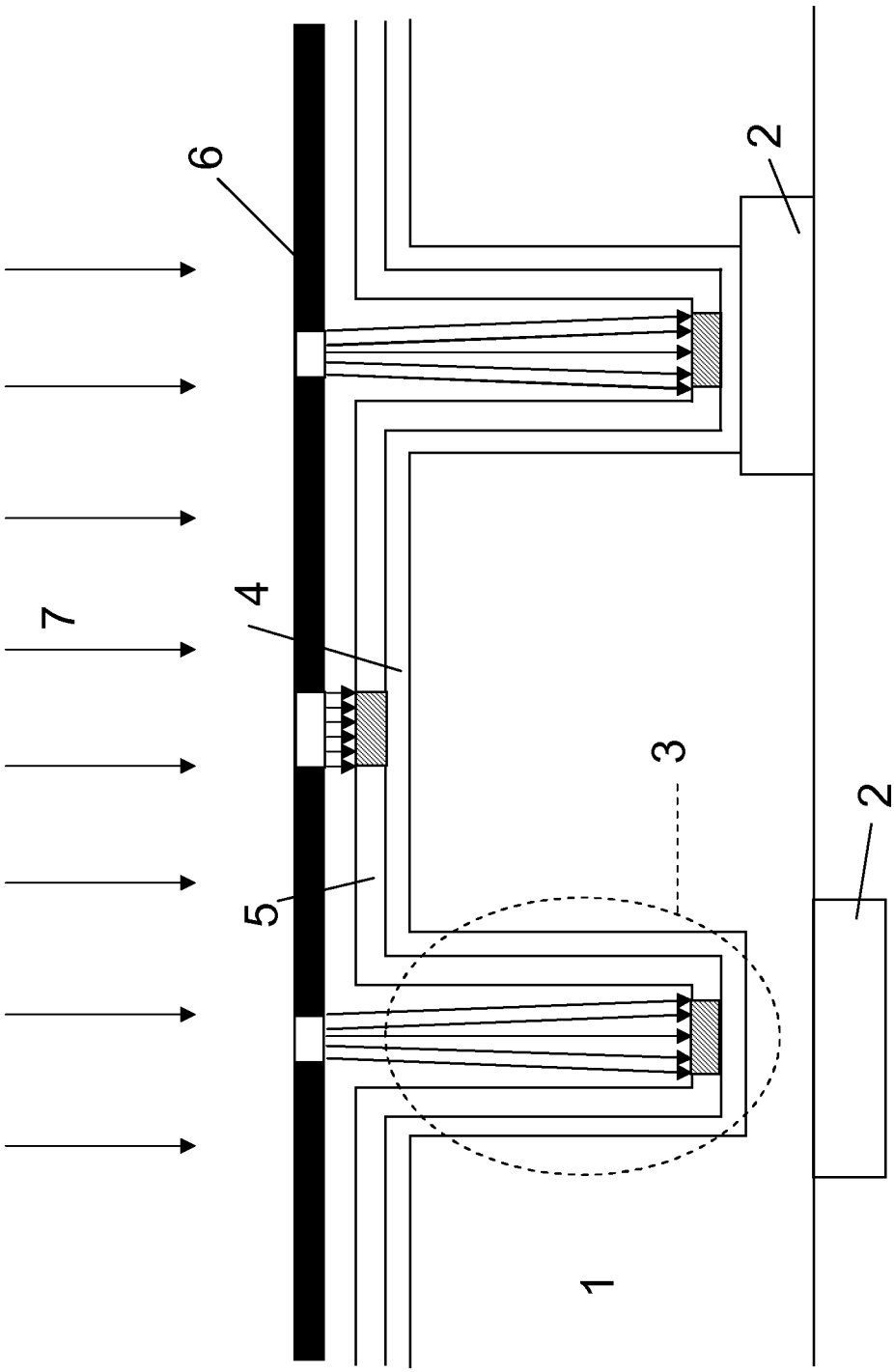


Figure 2(e)

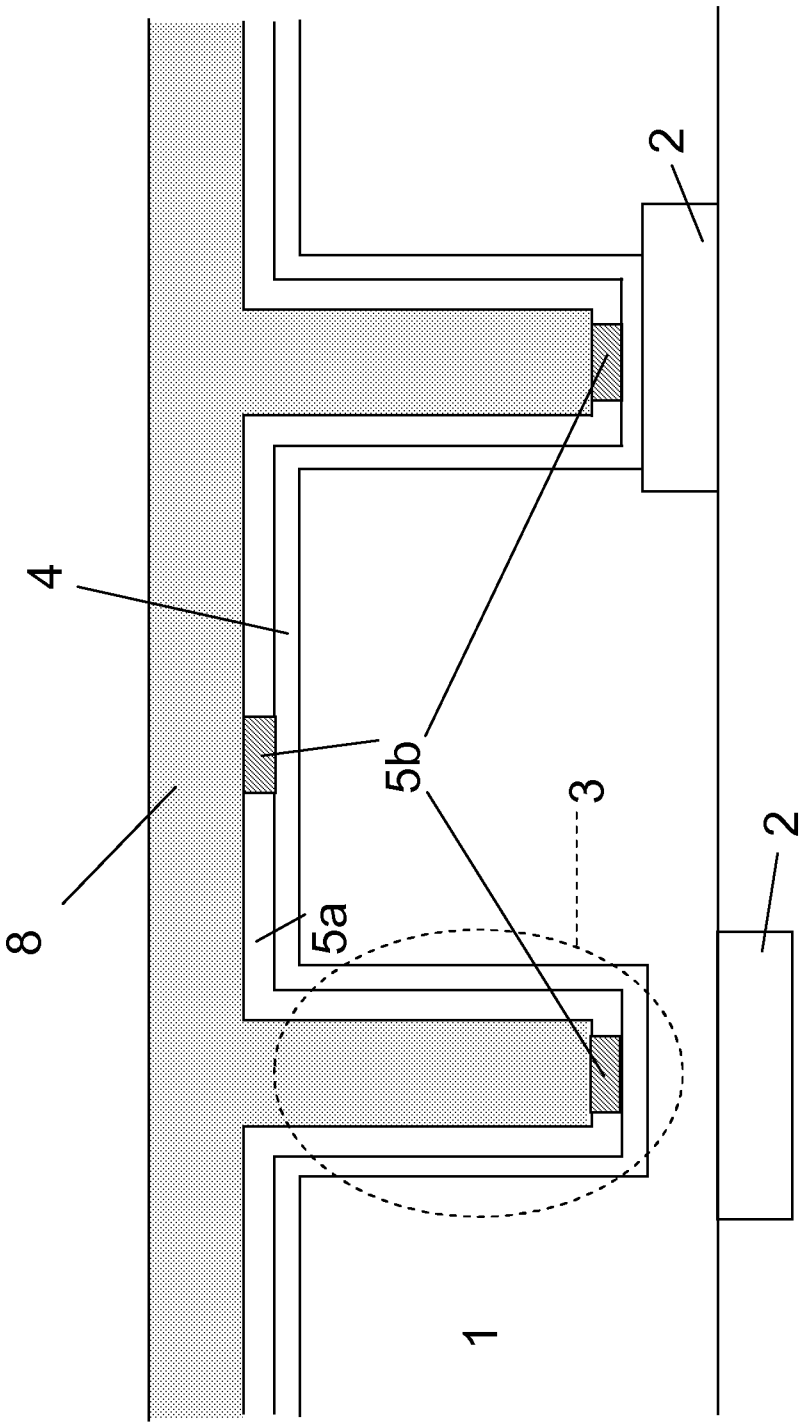


Figure 2(f)

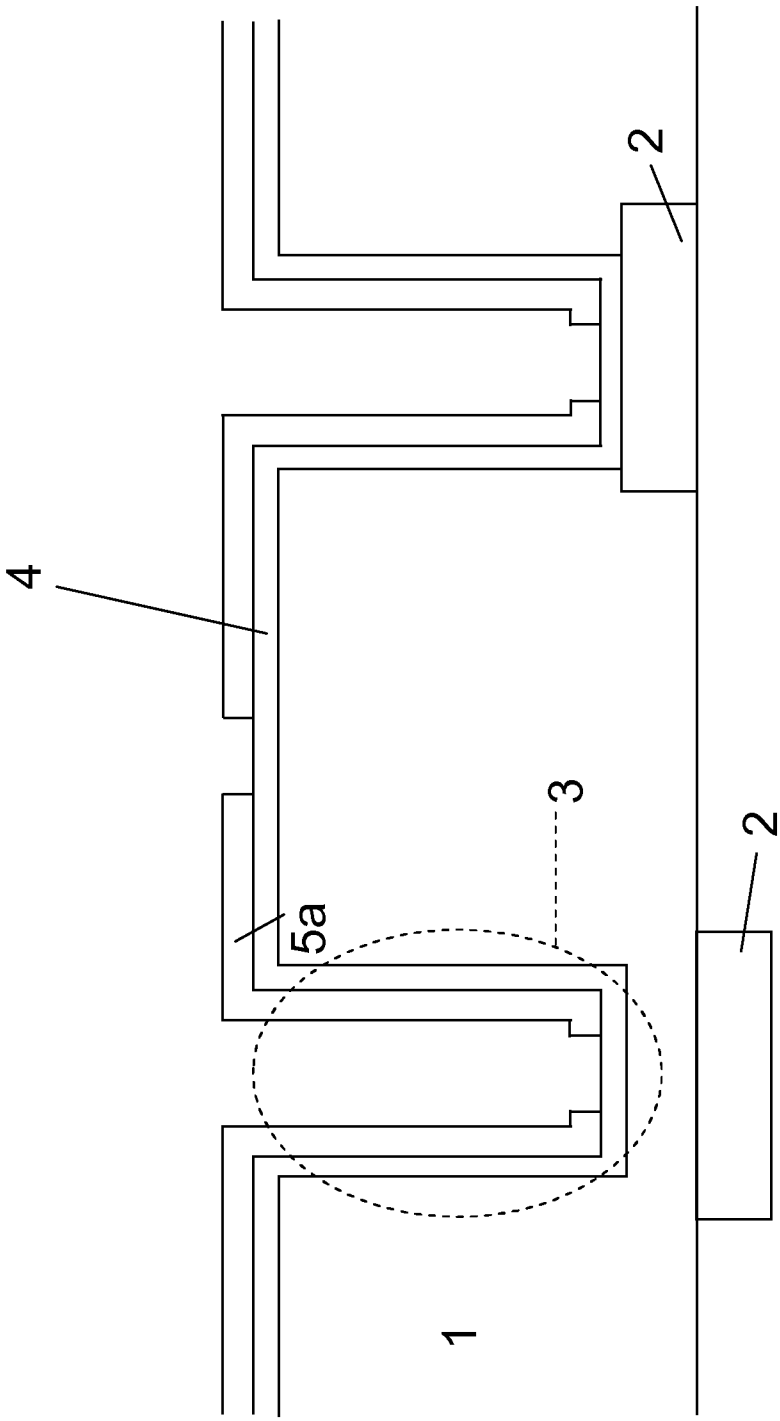


Figure 2(g)

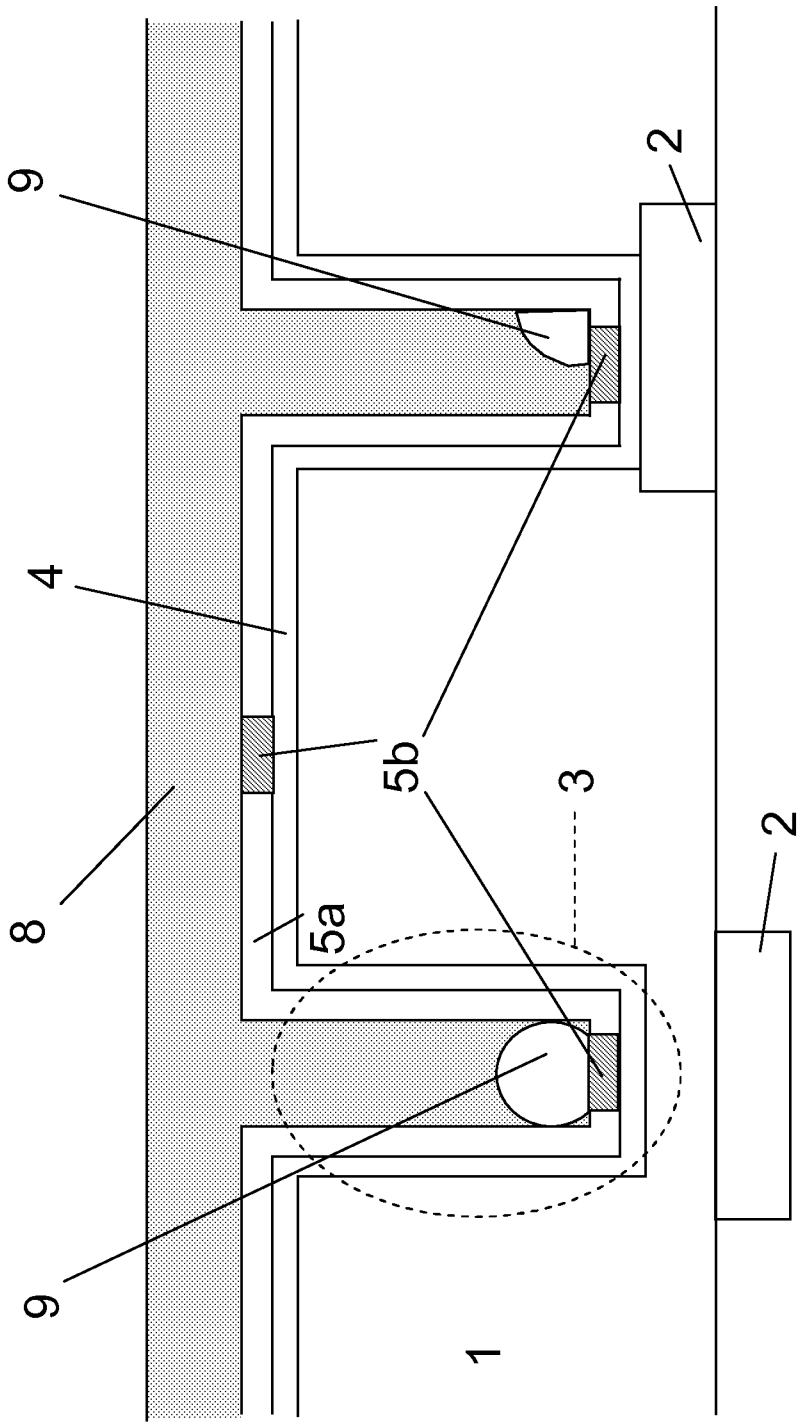


Figure 3(a)

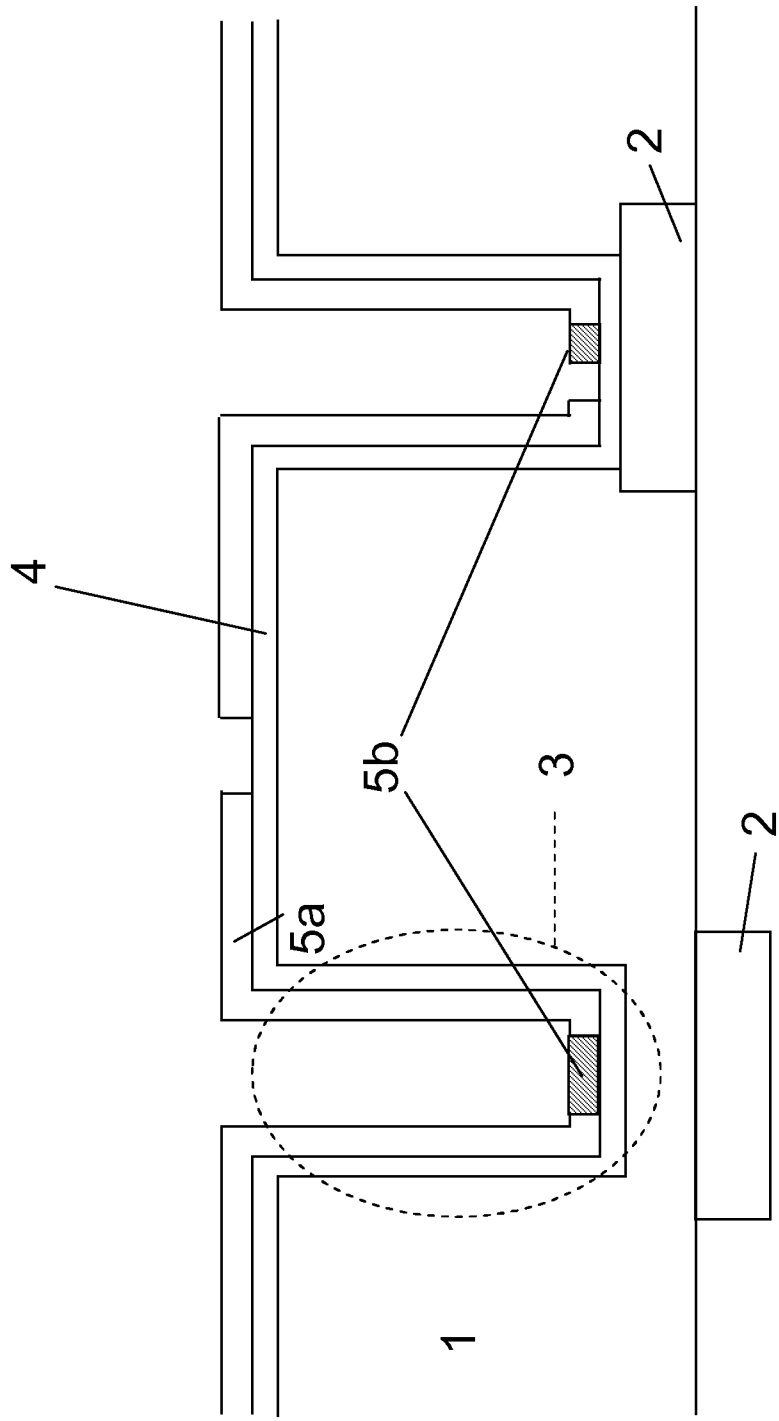


Figure 3(b)

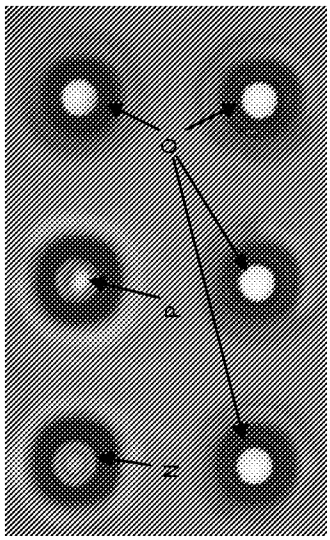
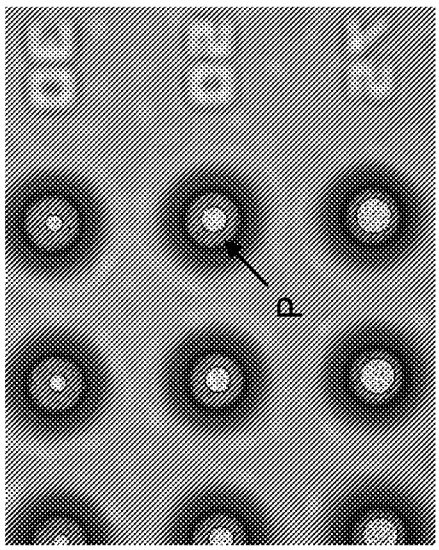
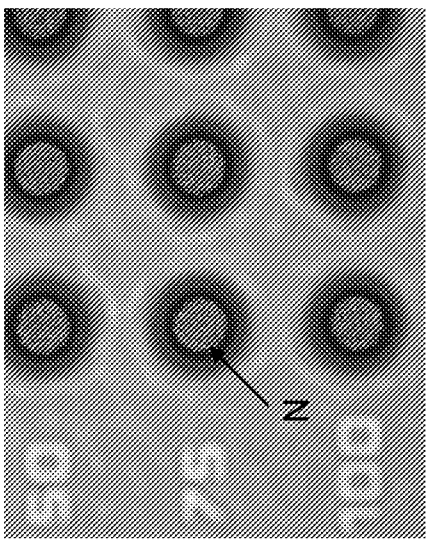


Figure 4

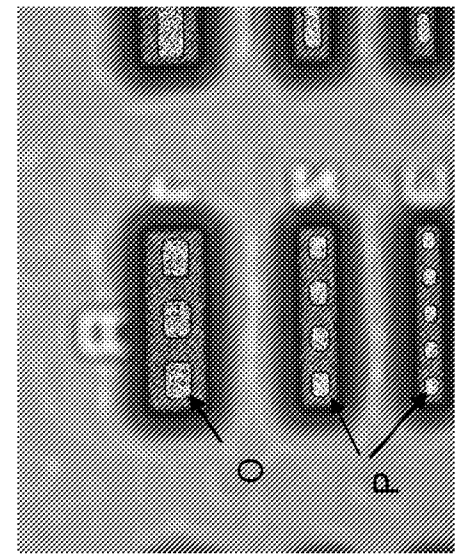


(b)

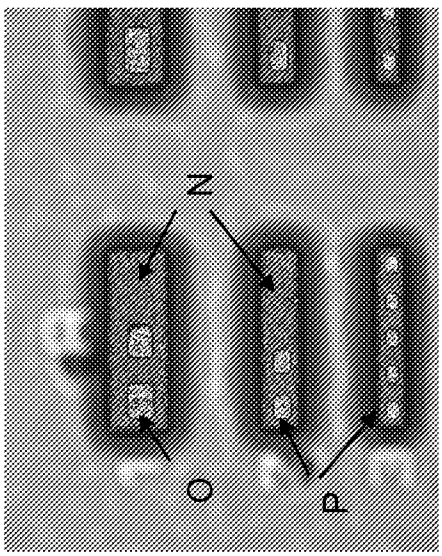


(a)

Figure 5



(b)



(a)

Figure 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2008/068143

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/027 H01L21/311 H01L21/768

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, INSPEC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 526 243 A (FUJITSU LTD [JP]) 3 February 1993 (1993-02-03) column 1, lines 1-12 column 4, line 45 - column 5, line 45; figures 1a-f column 7, lines 13-55; figures 3a-d -----	1,11,12
X	PHAM N P ET AL: "Lithography for Patterning inside through-Si Vias" ELECTRONICS PACKAGING TECHNOLOGY CONFERENCE, 2007. EPTC 2007. 9TH, IEEE, PISCATAWAY, NJ, USA, 10 December 2007 (2007-12-10), pages 120-124, XP031238110 ISBN: 978-1-4244-1324-9 the whole document -----	1-16
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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
13 May 2009	02/06/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Szarowski, Anne

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2008/068143

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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A	EL-KHOLI A ET AL: "Ultrasonic supported development of irradiated micro-structures" MICROELECTRONIC ENGINEERING, ELSEVIER PUBLISHERS BV., AMSTERDAM, NL, vol. 23, no. 1-4, 1 January 1994 (1994-01-01), pages 219-222, XP024484560 ISSN: 0167-9317 [retrieved on 1994-01-01] the whole document	1-12
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