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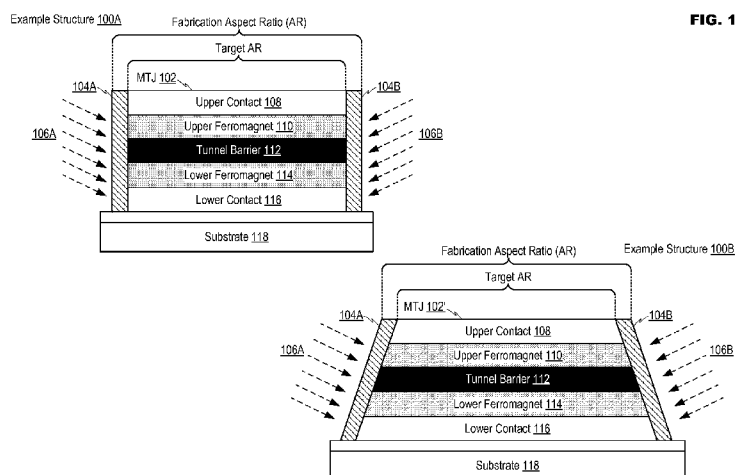
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(57) Abstract: This disclosure is directed to aspect ratio modification via angled implantation. For a structure fabricated on a substrate during integrated circuit (IC) manufacture, achieving a certain target aspect ratio (AR) may be important for proper operation of the IC. The target AR may be based on internal dimensions of the structure (e.g., a magnetic tunnel junction). Fabricating the structure to have the target AR employing typical semiconductor fabrication operations may be difficult, expensive, etc. However, the requirements to achieve the target AR may be relaxed, and angled implantation may be used to modify the internal dimensions resulting from fabrication (e.g., a fabrication AR) to the target AR. For example, ions of amorphizing material may be accelerated at an angle into portions of the structure to deactivate at least some material in the structure, which may modify the fabrication AR to the target AR.

ASPECT RATIO MODIFICATION VIA ANGLED IMPLANTATION

TECHNICAL FIELD

The present disclosure relates to semiconductor fabrication, and more particularly, to
5 a system to modify an aspect ratio of integrated circuit structures using angled implantation.

BACKGROUND

Integrated circuit (IC) fabrication may involve a series of fabrication operations that result in layers of material being deposited on a substrate, the layering of materials resulting
10 in the formation of features that may operate alone or cooperatively to provide functionality. In many instances, these features are based on groups of transistors configured to operate in a certain manner. The amount of functionality that can be implemented in an IC may depend on the size of the transistors and other devices formed on the substrate. As the footprint of each component (e.g., transistor) is reduced in size, the amount of functionality that may be
15 implemented on a single substrate increases while still be able to operate within power, heat, etc. requirements. It is in this manner, functionality (e.g., data processing, memory, I/O, etc.) that was previously only able to be implemented in separate physical IC packages may now be implemented in a single system-on-chip (SOC) IC package.

As set forth above, the ability to integrate more and more functionality in a single IC
20 may depend heavily on the ability to shrink the footprint of each feature. IC fabrication may, for example, employ a series of material deposition, mask and etch operations to fabricate an IC. A layer of semiconductor material may be deposited followed by photoresist. Narrow wavelength light may then be passed through a mask to draw patterns onto the photoresist. During etching, portions of the material may be removed (e.g., either the material portions
25 that were exposed to light, or were not exposed to light, depending on whether a positive or negative photoresist was used), the material that remains may form parts of the features that may make up the IC. When the light wavelength is narrower the features may be fabricated to be smaller, and thus, more functionality may be included on a single substrate. However, as the patterning in the lithographic process is narrowed to facilitate the fabrication of smaller
30 features, the cost, complexity, etc. of the fabrication may increase. These factors may make it prohibitive to shrink the features, which may limit the amount of functionality that may be incorporated into an IC physical package and impede technological development, in general.

BRIEF DESCRIPTION OF THE DRAWINGS

Features and advantages of various embodiments of the claimed subject matter will become apparent as the following Detailed Description proceeds, and upon reference to the Drawings, wherein like numerals designate like parts, and in which:

5 FIG. 1 illustrates example structures in accordance with at least one embodiment of the present disclosure;

 FIG. 2 illustrates an example first configuration for an integrated circuit structure in accordance with at least one embodiment of the present disclosure;

 FIG. 3 illustrates an example second configuration for an integrated circuit structure
10 in accordance with at least one embodiment of the present disclosure;

 FIG. 4 illustrates an example third configuration for an integrated circuit structure in accordance with at least one embodiment of the present disclosure;

 FIG. 5 illustrates an example integrated circuit configuration and a first fabrication operation in accordance with at least one embodiment of the present disclosure;

15 FIG. 6 illustrates an example integrated circuit configuration and a second fabrication operation in accordance with at least one embodiment of the present disclosure;

 FIG. 7 illustrates example operations for aspect ratio modification via angled implantation in accordance with at least one embodiment of the present disclosure; and

 FIG. 8 illustrates an example system that may employ a device such as illustrated in
20 any of FIG. 1 to 4 in accordance with at least one embodiment of the present disclosure.

Although the following Detailed Description will proceed with reference being made to illustrative embodiments, many alternatives, modifications and variations thereof will be apparent to those skilled in the art.

DETAILED DESCRIPTION

25 This disclosure is directed to aspect ratio modification via angled implantation. For a structure fabricated on a substrate during integrated circuit (IC) manufacture, achieving a certain target aspect ratio (AR) may be important for proper operation of the IC. In at least one embodiment, the target AR may be based on internal dimensions of the structure (e.g., a
30 magnetic tunnel junction). Fabricating the structure to have the target AR employing typical semiconductor fabrication operations may be difficult, expensive, etc. However, consistent with the present disclosure, the requirements to achieve the target AR may be relaxed (e.g., it may not be necessary to achieve the target AR as part of the primary fabrication process), and angled implantation may be used to modify the internal dimensions resulting from fabrication

(e.g., a fabrication AR) to the target AR. For example, ions of amorphizing material may be accelerated at an angle into portions of the structure to deactivate at least some material in the structure, which may result in the fabrication AR being modified to the target AR.

In at least one embodiment, an integrated circuit device may comprise, for example, a substrate and at least one structure. The at least one structure may be fabricated on the substrate in an orientation perpendicular to a surface of the substrate, wherein a fabrication aspect ratio resulting from the fabrication of the at least one structure is based on internal dimensions of the structure. The fabrication aspect ratio may be modified to a target aspect ratio via angled implantation.

In at least one embodiment, the at least one structure may be a magnetic tunnel junction. The fabrication may comprise at least a series of material deposition operations, material masking operations and material etching operations. Angled implantation may comprise accelerating ions of an amorphizing atom or molecule within an electric field at an angle of travel relative to a device surface to cause the ions to impact at least a portion of the at least one structure. The fabrication aspect ratio may be modified to the target aspect ratio by the ions impacting at least a portion of the at least one structure to amorphize material within the at least one structure and reduce the internal dimensions

In at least one embodiment, a plurality of structures may be formed on the substrate, the plurality of structures having substantially similar shape, height and being arranged in a uniformly spaced pattern on the substrate separated by a predetermined length. An angle at which the at least one ion is accelerated may be based on at least the height and spacing length of the plurality of structures. The fabrication aspect ratio may be modified to the desired aspect ratio based on performing angled implantation uniformly around the structure. Alternatively, the fabrication aspect ratio may be modified to the desired aspect ratio based on performing angled implantation only on a portion of the structure. In at least one embodiment, the fabrication aspect ratio may be modified to the desired aspect ratio based on performing angled implantation only on two sides of the structure. Consistent with the present disclosure, an example method for modifying aspect ratio in a structure may comprise providing a substrate on which an integrated circuit device is fabricated, fabricating at least one structure on the substrate, wherein a fabrication aspect ratio resulting from the fabrication of the at least one structure is based on internal dimensions of the structure and modifying the fabrication aspect ratio to a target aspect ratio via angled implantation.

FIG. 1 illustrates example structures in accordance with at least one embodiment of the present disclosure. Initially, reference may be made to various semiconductor assemblies

and/or structures such as a magnetic tunnel junction (MTJ), a perpendicular MTJ (pMTJ), an in-plane MTJ (iMTJ), etc. These example assemblies and/or structures have been referenced to provide a readily comprehensible perspective from which to understand the embodiments disclosed herein, and are not intended to limit actual implementations to only these particular assemblies or structures. In addition, the inclusion of an apostrophe after an item number in a drawing figure (e.g., 100') may indicate that an example embodiment of the particular item is being shown. These example embodiments are not intended to limit the present disclosure to only what is illustrated, and have been presented herein merely for the sake of explanation.

Consistent with the present disclosure, angled implantation of an amorphizing agent may be used to achieve a target AR in a structure following the completion of semiconductor fabrication. The target AR may be based on, for example, internal dimensions of at least one structure fabricated on an IC device. The target AR may be desirable or necessary to provide certain functionality, performance, etc. In at least one embodiment, subtractive patterning of high density MTJ devices with critical dimensions (CDs) below 30nm with conventional immersion lithographic techniques is very difficult, and typically requires multiple exposure techniques and several lithographic masks. Instead of relying on this method of fabrication, a relaxed device fabrication AR may be used that then achieves the target AR via implantation at an appropriate angle with the appropriate species to deactivate the periphery of the device.

Utilizing angled implantation of an atom or molecule with large enough nuclear mass such as, but not limited to, Boron (B), Carbon (C), Nitrogen (N), Phosphorus (P), Germanium (Ge), Xenon, (Xe), etc., periphery material of a structure may be amorphized. As referenced herein, amorphizing a material may comprise converting the material from an electronically and/or magnetically reactive crystalline material into a deactivated amorphous material. This effect may be used in at least two potential applications to effectively make a desired MTJ device with dimensions smaller than are possible with state-of the art immersion lithography.

Example structures 100A and 100B are illustrated in FIG. 1. Structure 100A may comprise MTJ 102 mounted on substrate 118. While structure 100A may include MTJ 102, the embodiments described herein may be applicable to other semiconductor structures. MTJ 102 in example 100A may be considered an "ideal" MTJ structure in that it is substantially cylindrical (e.g., having sides that are perpendicular to substrate 118). MTJ 102 may include one or more layers deposited via a series of semiconductor fabrication operations. Example semiconductor deposition technologies for depositing layers of semiconductor material may include, but are not limited to, molecular beam epitaxy (MBE), physical vapor deposition

(PVD), chemical vapor deposition (CVD), electrochemical deposition (ECD), atomic layer deposition (ALD), etc. Junctions between layers 108 to 116 may be modified to incorporate various features using photolithography. In at least one example implementation, MTJ 102 may comprise layers including upper contact 108, upper ferromagnet 110, tunnel barrier 112, lower ferromagnet 114 and lower contact 116. Tunnel barrier 112 may be a thin insulator (e.g., a few nanometers) that separates upper ferromagnet 110 from lower ferromagnet 114. In certain conditions, electrons may pass between ferromagnets 110 and 114 by “tunneling” through tunnel barrier 112. This quantum mechanical effect may be used to set memory bit states, and thus as a basis for nonvolatile memories including, for example, hard disk drives, magnetoresistive random access memory (MRAM), thermal assisted switching (TAS) memory, spin torque transfer (STT) memory and various other semiconductor devices.

Example structure 100B is substantially similar to example structure 100A except that the shape of MTJ 102' may be more trapezoidal than cylindrical. The trapezoidal shape may be the result of, for example, the limitations of common IC device manufacturing processes. As a result, while the trapezoidal shape of MTJ 102' may be more typical in mass production, more advanced assembly processes may be able to yield structures having a cylindrical shape that more closely resembles MTJ 102. The remaining elements of MTJ 102' may be identical to those described in regard to MTJ 102, and thus, identical item numbering has been applied. While the cylindrical shape of MTJ 102 may differ from the trapezoidal shape of MTJ 102', their operation may be, in general, substantially similar with some variation in operational characteristics occurring from device-to-device based on the inherent inexactness of the IC manufacturing process. To provide simplicity and clarity in the following disclosure, any reference to “MTJ 102” is intended to be generally applicable to MTJ 102 and/or MTJ 102'.

Consistent with the present disclosure, semiconductor fabrication may result in MTJ 102 with a fabrication AR based on, for example, the limitations of the particular fabrication technology. For example, the fabrication AR may comprise the internal dimensions of MTJ 102 at least from a cross-sectional perspective as shown in FIG. 1 to 5. The fabrication AR may not be suitable for all use cases for MTJ 102, and thus, it may be desirable (and possibly necessary) to modify the fabrication AR to achieve a target AR. In at least one embodiment, the fabrication AR may be modified to the target AR through the use of angled implantation 106A and 106B. Angled implantation 106A and 106B may comprise accelerating ions of an amorphizing atom or molecule within an electric field at an angle of travel (e.g., relative to a device surface) to cause the ions to impact at least a portion of the at least one structure (e.g., MTJ 102). As a result, areas of deactivated material, such as shown at 104A and 104B, may

be generated within MTJ 102 that causes the fabrication AR to be modified to the target AR. In particular, deactivated material 104A and 104B may form a longitudinal boundary or wall in MTJ 102 that is no longer a functional part of layers 108 to 116. The location, orientation, thickness, etc. of deactivated material 104A and 104B in MTJ 102 may be based on the type and amount of modification needed to arrive at the target AR, wherein the characteristics of deactivated material 104A and 104B may be controlled utilizing parameters including, for example, a type of amorphizing atoms/molecules, angle, power, duration, etc. For example, implantation using higher power and/or for longer durations of time may result in a greater thickness of deactivated material 104. While shown to be symmetrical, the characteristics of deactivated material 104A and 104B may be different, which may allow for “tweaking” the fabrication AR into the target AR.

FIG. 2 illustrates an example first configuration for an integrated circuit structure in accordance with at least one embodiment of the present disclosure. Example structure 200 may include at least perpendicular MTJ (pMTJ) 202 shown from a perspective view and a top view. Viewed from the top, pMTJ 102 may be substantially circular and, while not pictured, may comprise at least one spin transfer torque switching path that may run radially along at least the X-axis, and thermal agitation switching paths that may run axially. pMTJ 202 may further include deactivated material 204 that, consistent with the present disclosure, may be generated by angled implantation 206. As shown in detail in the top view of structure 200, angled implantation 206 may be performed in a substantially uniform manner around the periphery of pMTJ 202 to generate a substantially uniform layer of deactivated material 204. Angled implantation 206 may occur all at once over the entire periphery of pMTJ 202, or may occur repeatedly traversing peripheral sections of pMTJ 202 based on, for example, the capabilities of the implantation equipment. The AR of structure 200, which may be based on the ratio of the X and Y internal dimensions as shown in FIG 2, may remain constant in that the thickness of deactivated material 204 may be substantially uniform as a result of uniform angled implantation 206. However, at least the degree of thickness of deactivated material 204 in structure 200 may be used to modify a fabrication CD to a target CD (e.g., to control the area of the material defined by the X and Y dimensions within deactivated material 204).

FIG. 3 illustrates an example second configuration for an integrated circuit structure in accordance with at least one embodiment of the present disclosure. Example structure 300 may include at least perpendicular MTJ (pMTJ) 302 shown from a perspective view and a top view. Viewed from the top, pMTJ 102 may be substantially circular and, while not pictured, may comprise at least one spin transfer torque switching path that may run radially along at

least the X-axis, and thermal agitation switching paths that may run axially. pMTJ 302 may further include deactivated material 304 that, consistent with the present disclosure, may be generated by angled implantation 306A and 306B. As shown in detail in the top view of structure 300, angled implantation 306A may generate deactivated material 304A, while
5 angled implantation 306B may generate deactivated material 304B. The location, orientation, thickness, etc. of each of deactivated material 304A and 304B may be used to modify the fabrication AR to the target AR, which may be based on the ratio of the X and Y internal dimensions as shown in FIG 3.

FIG. 4 illustrates an example third configuration for an integrated circuit structure in accordance with at least one embodiment of the present disclosure. Example structure 400
10 may include at least in-plane MTJ (iMTJ) 402 shown from a perspective view and a top view. Viewed from the top, iMTJ 402 may be substantially oval-shaped and, while not pictured, may comprise spin transfer torque switching paths that may run radially at least along the y-axis and axially, and thermal agitation switching paths that may run radially along the x-axis.
15 iMTJ 402 may be subjected to angled implantation from only two directions as shown at 406A and 406B, and thus deactivated material 404A and 204B may not have uniformly thickness in the perimeter surrounding iMTJ 402. This lack of uniformity allows the internal dimensions of iMTJ 402 to be flexibly modified to attain the target AR. In particular, while shown to be symmetrical, deactivated material 404A and 404B may in practice be different in
20 orientation, thickness, etc. based on the modifications needed to achieve the target AR. As in FIG. 2, the AR may be based on the ratio of the X and Y dimensions.

FIG. 5 illustrates an example integrated circuit configuration and a first fabrication operation in accordance with at least one embodiment of the present disclosure. Example device 500 may comprise a plurality of iMTJs 402' that are fabricated on substrate 118'. The
25 plurality of iMTJs 402' may be fabricated on substrate 118' in a uniform pattern (e.g., a grid pattern) so that the plurality of iMTJs 402' may be equally spaced on the surface of substrate 118'. Consistent with the example illustrated in FIG. 4, angled implantation 406B' may be used to adjust the internal dimensions of iMTJs 402' by implanting an amorphizing material. For example, implantation from a first direction 406B' may accelerate atoms or molecules of
30 the amorphizing material towards iMTJs 402' at an angle that may generate deactivated material 405B' on one side of iMTJs 402'.

Example parameters for determining an appropriate angle for implantation are shown at 502 in FIG. 5. Example device 500' may comprise a plurality of iMTJs 402' in a uniform arrangement wherein iMTJ 402A' may correspond to a first row of iMTJs 402', iMTJ 402B'

may correspond to a second row of iMTJs 402' and iMTJ 402C' may correspond to a third row of iMTJs 402. An implantation angle θ relative to, for example, surface 504 of device 500 may be determined based on at least the height H of iMTJs 402' and a length L of a distance between iMTJs 402'. Utilizing at least these two parameters, an implantation angle θ may be selected that will allow angled implantation to occur over the entirety of a side of iMTJ 402'. More specifically, the implantation angle θ may be selected to ensure that that iMTJs 402' in a first row (e.g., iMTJ 402B') don't block the angled implantation for iMTJs 402' arranged in subsequent rows (e.g., iMTJ 402C'). If implantation angle θ was smaller than the example angle illustrated in FIG. 5, the blocking of subsequent rows could occur.

FIG. 6 illustrates an example integrated circuit configuration and a second fabrication operation in accordance with at least one embodiment of the present disclosure. For example, a second portion of the plurality of iMTJs 402' may be exposed to angled implantation 406A' to generate deactivated material 404A' on a side of iMTJs 402' opposing the side one which angled implantation was performed in FIG 5. The performance of angled implantation 406A' and 406B' are variable. Even though angled implantation 406B' was described before angled implantation 406A', these operations may be performed in reverse order, simultaneously, etc. Moreover, while FIG. 5 and 6 demonstrate angled implantation from only two sides, angled implantation may occur uniformly from all sides to form pMTJ 202 such as shown in FIG. 2.

FIG. 7 illustrates example operations for aspect ratio modification via angled implantation in accordance with at least one embodiment of the present disclosure. In operation 700 a substrate may be provided onto which an IC may be fabricated. Fabrication of the IC may comprise, for example, a series of semiconductor fabrication operations that may include the deposition of one or more layers of semiconductor material, which may be followed by a masking/etching operation. Semiconductor fabrication may occur in operation 702, which may yield a structure with incorrect feature sizes (e.g., a fabrication AR that does not comply with a target AR). In operation 704 a determination may be made as to the amount of change required to modify the internal dimensions to the target AR. Parameters for angled implantation may then be determined in operation 706. For example, an angle of implantation may be determined based at least on the height and spacing of structures in the device. Moreover, other parameters may be determined such as the particular amorphizing material to implant, implantation power, implantation duration, etc. The angled implantation may then be performed in operation 708. In at least one embodiment, operation 708 may be performed more than once depending on, for example, the characteristics of the implantation (e.g., type, location, orientation, angle, power duration, etc.), the abilities of the implantation

equipment, etc. For example, implantation may be performed twice (e.g., on two different sides of a structure) in a manufacturing scenario such as illustrated in FIG. 2 to 5, or may be performed repeatedly for uniform peripheral implantation to generate a substantially uniform distribution of deactivated material 204 such as illustrated in regard to pMTJ 202 in FIG. 2.

5 FIG. 8 illustrates an example system that may employ a device such as illustrated in FIG. 4 in accordance with at least one embodiment of the present disclosure. System 800 is an example of a platform in which one or more devices such as device 500 may be installed, and is not intended to limit the present disclosure to any particular manner of implementation. Examples of system 800 may include, but are not limited to, a mobile communication device
10 such as a cellular handset or a smartphone based on the Android® OS from the Google Corporation, iOS® or Mac OS® from the Apple Corporation, Windows® OS from the Microsoft Corporation, Tizen® OS from the Linux Foundation, Firefox® OS from the Mozilla Project, Blackberry® OS from the Blackberry Corporation, Palm® OS from the Hewlett-Packard Corporation, Symbian® OS from the Symbian Foundation, etc., a mobile
15 computing device such as a tablet computer like an iPad® from the Apple Corporation, Surface® from the Microsoft Corporation, Galaxy Tab® from the Samsung Corporation, Kindle® from the Amazon Corporation, etc., an Ultrabook® including a low-power chipset from the Intel Corporation, a netbook, a notebook, a laptop, a palmtop, etc., a typically
20 stationary computing device such as a desktop computer, a server, a smart television, small form factor computing solutions (e.g., for space-limited applications, TV set-top boxes, etc.) like the Next Unit of Computing (NUC) platform from the Intel Corporation, etc.

System circuitry 802 may manage the operation of system 800. System circuitry 802 may include, for example, processing circuitry 804, memory circuitry 806, power circuitry 808, user interface circuitry 810 and communication interface circuitry 812. System 800 may
25 further include communication module 814. While communication module 814 is illustrated as separate from system circuitry 802, the example configuration shown in FIG. 8 is provided merely for the sake of explanation. For example, some or all of the functionality associated with communication module 814 may also be incorporated into system circuitry 802.

In system 800, processing circuitry 804 may comprise one or more processors situated
30 in separate components, or alternatively one or more cores in a single component (e.g., in a System-on-a-Chip (SoC) configuration), along with processor-related support circuitry (e.g., bridging interfaces, etc.). Example processors may include, but are not limited to, various x86-based microprocessors available from the Intel Corporation including those in the Pentium, Xeon, Itanium, Celeron, Atom, Quark, Core i-series, Core M-series product

families, Advanced RISC (e.g., Reduced Instruction Set Computing) Machine or “ARM” processors, etc. Examples of support circuitry may include chipsets (e.g., Northbridge, Southbridge, etc. available from the Intel Corporation) configured to provide an interface through which processing circuitry 804 may interact with other system components that may
5 be operating at different speeds, on different buses, etc. in system 800. Moreover, some or all of the functionality commonly associated with the support circuitry may also be included in the same physical package as the processor (e.g., such as in the Sandy Bridge family of processors available from the Intel Corporation).

Processing circuitry 804 may be configured to execute various instructions in system
10 800. Instructions may include program code configured to cause processing circuitry 804 to perform activities related to reading data, writing data, processing data, formulating data, converting data, transforming data, etc. Information (e.g., instructions, data, etc.) may be stored in memory circuitry 806. Memory circuitry 806 may comprise random access memory (RAM) and/or read-only memory (ROM) in a fixed or removable format. RAM may include
15 volatile memory configured to hold information during the operation of system 800 such as, for example, static RAM (SRAM) or Dynamic RAM (DRAM). ROM may include non-volatile (NV) memory modules configured based on BIOS, UEFI, etc. to provide instructions when system 800 is activated, programmable memories such as electronic programmable ROMs (EPROMS), Flash, etc. Other fixed/removable memory may include, but are not
20 limited to, magnetic memories such as, for example, floppy disks, hard drives, etc., electronic memories such as solid state flash memory (e.g., embedded multimedia card (eMMC), etc.), removable memory cards or sticks (e.g., micro storage device (uSD), USB, etc.), optical memories such as compact disc-based ROM (CD-ROM), Digital Video Disks (DVD), Blu-Ray Disks, etc.

Power circuitry 808 may include internal power sources (e.g., a battery, fuel cell, etc.) and/or external power sources (e.g., electromechanical or solar generator, power grid, external fuel cell, etc.), and related circuitry configured to supply system 800 with the power needed to operate. User interface circuitry 810 may include hardware and/or software to allow users to interact with system 800 such as, for example, various input mechanisms (e.g.,
25 microphones, switches, buttons, knobs, keyboards, speakers, touch-sensitive surfaces, one or more sensors configured to capture images and/or sense proximity, distance, motion, gestures, orientation, biometric data, etc.) and various output mechanisms (e.g., speakers, displays, lighted/flashing indicators, electromechanical components for vibration, motion, etc.). The hardware in user interface circuitry 810 may be incorporated within system 800
30

and/or may be coupled to system 800 via a wired or wireless communication medium. User interface circuitry 810 may be optional in certain circumstances such as, for example, a situation wherein system 800 is a server (e.g., rack server, blade server, etc.) that does not include user interface circuitry 810, and instead relies on another device (e.g., a management terminal) for user interface functionality.

Communication interface circuitry 812 may be configured to manage packet routing and other control functions for communication module 814, which may include resources configured to support wired and/or wireless communications. In some instances, system 800 may comprise more than one communication module 814 (e.g., including separate physical interface modules for wired protocols and/or wireless radios) managed by a centralized communication interface circuitry 812. Wired communications may include serial and parallel wired mediums such as, for example, Ethernet, USB, Firewire, Thunderbolt, Digital Video Interface (DVI), High-Definition Multimedia Interface (HDMI), etc. Wireless communications may include, for example, close-proximity wireless mediums (e.g., radio frequency (RF) such as based on the RF Identification (RFID) or Near Field Communications (NFC) standards, infrared (IR), etc.), short-range wireless mediums (e.g., Bluetooth, WLAN, Wi-Fi, etc.), long range wireless mediums (e.g., cellular wide-area radio communication technology, satellite-based communications, etc.), electronic communications via sound waves, etc. In one embodiment, communication interface circuitry 812 may be configured to prevent wireless communications that are active in communication module 814 from interfering with each other. In performing this function, communication interface circuitry 812 may schedule activities for communication module 814 based on, for example, the relative priority of messages awaiting transmission. While the embodiment disclosed in FIG. 2 illustrates communication interface circuitry 812 being separate from communication module 814, it may also be possible for the functionality of communication interface circuitry 812 and communication module 814 to be incorporated into the same module.

While FIG. 7 illustrates operations according to an embodiment, it is to be understood that not all of the operations depicted in FIG. 7 are necessary for other embodiments. Indeed, it is fully contemplated herein that in other embodiments of the present disclosure, the operations depicted in FIG. 7, and/or other operations described herein, may be combined in a manner not specifically shown in any of the drawings, but still fully consistent with the present disclosure. Thus, claims directed to features and/or operations that are not exactly shown in one drawing are deemed within the scope and content of the present disclosure.

As used in this application and in the claims, a list of items joined by the term “and/or” can mean any combination of the listed items. For example, the phrase “A, B and/or C” can mean A; B; C; A and B; A and C; B and C; or A, B and C. As used in this application and in the claims, a list of items joined by the term “at least one of” can mean any
5 combination of the listed terms. For example, the phrases “at least one of A, B or C” can mean A; B; C; A and B; A and C; B and C; or A, B and C.

As used in any embodiment herein, the terms “system” may refer to, for example, software, firmware and/or circuitry configured to perform any of the aforementioned operations. Software may be embodied as a software package, code, instructions, instruction
10 sets and/or data recorded on non-transitory computer readable storage mediums. Firmware may be embodied as code, instructions or instruction sets and/or data that are hard-coded (e.g., nonvolatile) in memory devices. “Circuitry”, as used in any embodiment herein, may comprise, for example, singly or in any combination, hardwired circuitry, programmable circuitry such as computer processors comprising one or more individual instruction
15 processing cores, state machine circuitry, and/or firmware that stores instructions executed by programmable circuitry. The modules may, collectively or individually, be embodied as circuitry that forms part of a larger system, for example, an integrated circuit (IC), system on-chip (SoC), desktop computers, laptop computers, tablet computers, servers, smartphones, etc.

Any of the operations described herein may be implemented in a system that includes one or more storage mediums (e.g., non-transitory storage mediums) having stored thereon, individually or in combination, instructions that when executed by one or more processors perform the methods. Here, the processor may include, for example, a server CPU, a mobile device CPU, and/or other programmable circuitry. Also, it is intended that operations
20 described herein may be distributed across a plurality of physical devices, such as processing structures at more than one different physical location. The storage medium may include any type of tangible medium, for example, any type of disk including hard disks, floppy disks, optical disks, compact disk read-only memories (CD-ROMs), compact disk rewritables (CD-RWs), and magneto-optical disks, semiconductor devices such as read-only memories
25 (ROMs), random access memories (RAMs) such as dynamic and static RAMs, erasable programmable read-only memories (EPROMs), electrically erasable programmable read-only memories (EEPROMs), flash memories, Solid State Disks (SSDs), embedded multimedia cards (eMMCs), secure digital input/output (SDIO) cards, magnetic or optical cards, or any
30

type of media suitable for storing electronic instructions. Other embodiments may be implemented as software modules executed by a programmable control device.

Thus, this disclosure is directed to aspect ratio modification via angled implantation. For a structure fabricated on a substrate during integrated circuit (IC) manufacture, achieving
5 a certain target aspect ratio (AR) may be important for proper operation of the IC. The target AR may be based on internal dimensions of the structure (e.g., a magnetic tunnel junction). Fabricating the structure to have the target AR employing typical semiconductor fabrication operations may be difficult, expensive, etc. However, the requirements to achieve the target AR may be relaxed, and angled implantation may be used to modify the internal dimensions
10 resulting from fabrication (e.g., a fabrication AR) to the target AR. For example, ions of amorphizing material may be accelerated at an angle into portions of the structure to deactivate at least some material in the structure, which may modify the fabrication AR to the target AR.

The following examples pertain to further embodiments. The following examples of
15 the present disclosure may comprise subject material such as a device, a method, at least one machine-readable medium for storing instructions that when executed cause a machine to perform acts based on the method, means for performing acts based on the method and/or a system for aspect ratio modification via angled implantation.

According to example 1 there is provided an integrated circuit device. The integrated
20 circuit device may comprise a substrate and at least one structure fabricated on the substrate in an orientation perpendicular to a surface of the substrate, wherein a fabrication aspect ratio resulting from the fabrication of the at least one structure is based on internal dimensions of the structure, the fabrication aspect ratio being modified to a target aspect ratio via angled implantation.

25 Example 2 may include the elements of example 1, wherein the at least one structure is a magnetic tunnel junction.

Example 3 may include the elements of example 2, wherein the device comprises at least an upper contact, an upper ferromagnet, a tunnel barrier, a lower ferromagnet, and a lower contact.

30 Example 4 may include the elements of any of examples 1 to 3, wherein the fabrication comprises at least a series of material deposition operations, material masking operations and material etching operations.

Example 5 may include the elements of any of examples 1 to 4, wherein the angled implantation comprises accelerating ions of an amorphizing atom or molecule within an

electric field at an angle of travel relative to a device surface to cause the ions to impact at least a portion of the at least one structure.

Example 6 may include the elements of example 5, wherein the amorphizing atom or molecules comprises at least one of Boron (B), Carbon (C), Nitrogen (N), Phosphorus (P),
5 Germanium (Ge) or Xenon (Xe).

Example 7 may include the elements of any of examples 5 to 6, wherein the fabrication aspect ratio is modified to the target aspect ratio by the ions impacting at least a portion of the at least one structure to amorphize material within the at least one structure and reduce the internal dimensions

10 Example 8 may include the elements of any of examples 5 to 7, wherein a plurality of structures are formed on the substrate, the plurality of structures having substantially similar shape, height and being arranged in a uniformly spaced pattern on the substrate separated by a predetermined length.

Example 9 may include the elements of example 8, wherein an angle at which the at
15 least one ion is accelerated is based on at least the height and spacing length of the plurality of structures.

Example 10 may include the elements of any of examples 8 to 9, wherein a plurality ions are accelerated and an angle at which the at least one ion is accelerated is based on the plurality of ions impacting on an entire side of each of the plurality of the structures.

20 Example 11 may include the elements of any of examples 1 to 10, wherein the fabrication aspect ratio is modified to the desired aspect ratio based on performing angled implantation uniformly around the structure.

Example 12 may include the elements of any of examples 1 to 11, wherein the fabrication aspect ratio is modified to the desired aspect ratio based on performing angled
25 implantation only on a portion of the structure.

Example 13 may include the elements of example 12, wherein the fabrication aspect ratio is modified to the desired aspect ratio based on performing angled implantation only on two sides of the structure.

According to example 14 there is provided a method for modifying aspect ratio in a
30 structure. The method may comprise providing a substrate on which an integrated circuit device is fabricated, fabricating at least one structure on the substrate, wherein a fabrication aspect ratio resulting from the fabrication of the at least one structure is based on internal dimensions of the structure and modifying the fabrication aspect ratio to a target aspect ratio via angled implantation.

Example 15 may include the elements of example 14, wherein the at least one structure is a magnetic tunnel junction.

Example 16 may include the elements of example 15, wherein the device comprises at least an upper contact, an upper ferromagnet, a tunnel barrier, a lower ferromagnet, and a lower contact.

Example 17 may include the elements of any of examples 14 to 16, wherein fabricating at least one structure comprises performing a series of material deposition operations, material masking operations and material etching operations.

Example 18 may include the elements of any of examples 14 to 17, and may further comprise determining a dimension change required to reduce the fabrication aspect ratio to the target aspect ratio based on the internal dimensions.

Example 19 may include the elements of any of examples 14 to 18, wherein the angled implantation comprises accelerating ions of an amorphizing atom or molecule within an electric field at an angle of travel relative to a device surface to cause the ions to impact at least a portion of the at least one structure.

Example 20 may include the elements of example 19, wherein the amorphizing atom or molecules comprises at least one of Boron (B), Carbon (C), Nitrogen (N), Phosphorus (P), Germanium (Ge) or Xenon (Xe).

Example 21 may include the element of any of examples 19 to 20, wherein the fabrication aspect ratio is modified to the target aspect ratio by the ions impacting uniformly around the at least one structure to amorphize material within the at least one structure and reduce the internal dimensions.

Example 22 may include the elements of any of examples 19 to 21, wherein the fabrication aspect ratio is modified to the target aspect ratio by the ions impacting at least a portion of the at least one structure to amorphize material within the at least one structure and reduce the internal dimensions.

Example 23 may include the elements of any of examples 19 to 22, and may further comprise determining an angle at which to implant the ions to amorphize at least a portion of the structure material.

Example 24 may include the elements of example 23, wherein the integrated circuit device comprises a plurality of structures fabricated on the substrate and the angle is determined based on a height and spacing of the plurality of structures.

Example 25 may include the elements of example 24, wherein the angle is determined based on the ions impacting on an entire side of each of the plurality of the structures.

According to example 26 there is provided a system including at least a device, the system being arranged to perform the method of any of the above examples 14 to 25.

According to example 27 there is provided a chipset arranged to perform the method of any of the above examples 14 to 25.

5 According to example 28 there is provided at least one machine readable medium comprising a plurality of instructions that, in response to being executed on a computing device, cause the computing device to carry out the method according to any of the above examples 14 to 25.

10 According to example 29 there is provided at least one device configured for modifying aspect ratio in a structure, the at least one device being arranged to perform the method of any of the above examples 14 to 25.

 According to example 30 there is provided a system for modifying aspect ratio in a structure. The system may comprise means for providing a substrate on which an integrated circuit device is fabricated, means for fabricating at least one structure on the substrate,
15 wherein a fabrication aspect ratio resulting from the fabrication of the at least one structure is based on internal dimensions of the structure and means for modifying the fabrication aspect ratio to a target aspect ratio via angled implantation.

 Example 31 may include the elements of example 30, wherein the at least one structure is a magnetic tunnel junction.

20 Example 32 may include the elements of example 31, wherein the device comprises at least an upper contact, an upper ferromagnet, a tunnel barrier, a lower ferromagnet, and a lower contact.

 Example 33 may include the elements of any of examples 30 to 32, wherein the means for fabricating at least one structure comprise means for performing a series of
25 material deposition operations, material masking operations and material etching operations.

 Example 34 may include the elements of any of examples 30 to 33, and may further comprise means for determining a dimension change required to reduce the fabrication aspect ratio to the target aspect ratio based on the internal dimensions.

 Example 35 may include the elements of any of examples 30 to 34, wherein the
30 angled implantation comprises accelerating ions of an amorphizing atom or molecule within an electric field at an angle of travel relative to a device surface to cause the ions to impact at least a portion of the at least one structure.

Example 36 may include the elements of example 35, wherein the amorphizing atom or molecules comprises at least one of Boron (B), Carbon (C), Nitrogen (N), Phosphorus (P), Germanium (Ge) or Xenon (Xe).

5 Example 37 may include the elements of any of claims 35 to 36, wherein the fabrication aspect ratio is modified to the target aspect ratio by the ions impacting uniformly around the at least one structure to amorphize material within the at least one structure and reduce the internal dimensions.

10 Example 38 may include the elements of any of examples 35 to 37, wherein the fabrication aspect ratio is modified to the target aspect ratio by the ions impacting at least a portion of the at least one structure to amorphize material within the at least one structure and reduce the internal dimensions

Example 39 may include the elements of any of examples 33 to 38, and may further comprise means for determining an angle at which to implant the ions to amorphize at least a portion of the structure material.

15 Example 40 may include the elements of 39, wherein the integrated circuit device comprises a plurality of structures fabricated on the substrate and the angle is determined based on a height and spacing of the plurality of structures.

Example 41 may include the elements of example 40, wherein the angle is determined based on the ions impacting on an entire side of each of the plurality of the structures.

20 The terms and expressions which have been employed herein are used as terms of description and not of limitation, and there is no intention, in the use of such terms and expressions, of excluding any equivalents of the features shown and described (or portions thereof), and it is recognized that various modifications are possible within the scope of the claims. Accordingly, the claims are intended to cover all such equivalents.

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WHAT IS CLAIMED:

1. An integrated circuit device, comprising:
a substrate; and
5 at least one structure fabricated on the substrate in an orientation perpendicular to a surface of the substrate, wherein a fabrication aspect ratio resulting from the fabrication of the at least one structure is based on internal dimensions of the structure, the fabrication aspect ratio being modified to a target aspect ratio via angled implantation.
- 10 2. The device of claim 1, wherein the at least one structure is a magnetic tunnel junction.
3. The device of claim 1, wherein the fabrication comprises at least a series of material deposition operations, material masking operations and material etching operations.
- 15 4. The device of claim 1, wherein the angled implantation comprises accelerating ions of an amorphizing atom or molecule within an electric field at an angle of travel relative to a device surface to cause the ions to impact at least a portion of the at least one structure.
- 20 5. The device of claim 4, wherein the fabrication aspect ratio is modified to the target aspect ratio by the ions impacting at least a portion of the at least one structure to amorphize material within the at least one structure and reduce the internal dimensions
6. The device of claim 4, wherein a plurality of structures are formed on the substrate, the plurality of structures having substantially similar shape, height and being arranged in a
25 uniformly spaced pattern on the substrate separated by a predetermined length.
7. The device of claim 6, wherein an angle at which the at least one ion is accelerated is based on at least the height and spacing length of the plurality of structures.
- 30 8. The device of claim 1, wherein the fabrication aspect ratio is modified to the desired aspect ratio based on performing angled implantation uniformly around the structure.
9. The device of claim 1, wherein the fabrication aspect ratio is modified to the desired aspect ratio based on performing angled implantation only on a portion of the structure.

10. The device of claim 9, wherein the fabrication aspect ratio is modified to the desired aspect ratio based on performing angled implantation only on two sides of the structure.

5 11. A method for modifying aspect ratio in a structure, comprising:

providing a substrate on which an integrated circuit device is fabricated;

fabricating at least one structure on the substrate, wherein a fabrication aspect ratio resulting from the fabrication of the at least one structure is based on internal dimensions of the structure; and

10 modifying the fabrication aspect ratio to a target aspect ratio via angled implantation.

12. The method of claim 11, wherein the at least one structure is a magnetic tunnel junction.

15 13. The method of claim 11, wherein fabricating at least one structure comprises performing a series of material deposition operations, material masking operations and material etching operations.

14. The method of claim 11, further comprising:

20 determining a dimension change required to reduce the fabrication aspect ratio to the target aspect ratio based on the internal dimensions.

15. The method of claim 11, wherein the angled implantation comprises accelerating ions of an amorphizing atom or molecule within an electric field at an angle of travel relative to a
25 device surface to cause the ions to impact at least a portion of the at least one structure.

16. The method of claim 15, wherein the fabrication aspect ratio is modified to the target aspect ratio by the ions impacting uniformly around the at least one structure to amorphize material within the at least one structure and reduce the internal dimensions

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17. The method of claim 15, wherein the fabrication aspect ratio is modified to the target aspect ratio by the ions impacting at least a portion of the at least one structure to amorphize material within the at least one structure and reduce the internal dimensions

18. The method of claim 15, further comprising:

determining an angle at which to implant the ions to amorphize at least a portion of the structure material.

5 19. The method of claim 18, wherein the integrated circuit device comprises a plurality of structures fabricated on the substrate and the angle is determined based on a height and spacing of the plurality of structures.

10 20. A system including at least a device, the system being arranged to perform the method of any of the claims 11 to 19.

21. A chipset arranged to perform the method of any of the claims 11 to 19.

15 22. At least one machine readable medium comprising a plurality of instructions that, in response to being executed on a computing device, cause the computing device to carry out the method according to any of the claims 11 to 19.

20 23. At least one device configured for modifying aspect ratio in a structure, the at least one device being arranged to perform the method of any of the claims 11 to 19.

24. A device having means to perform the method of any of the claims 11 to 19.

FIG. 1

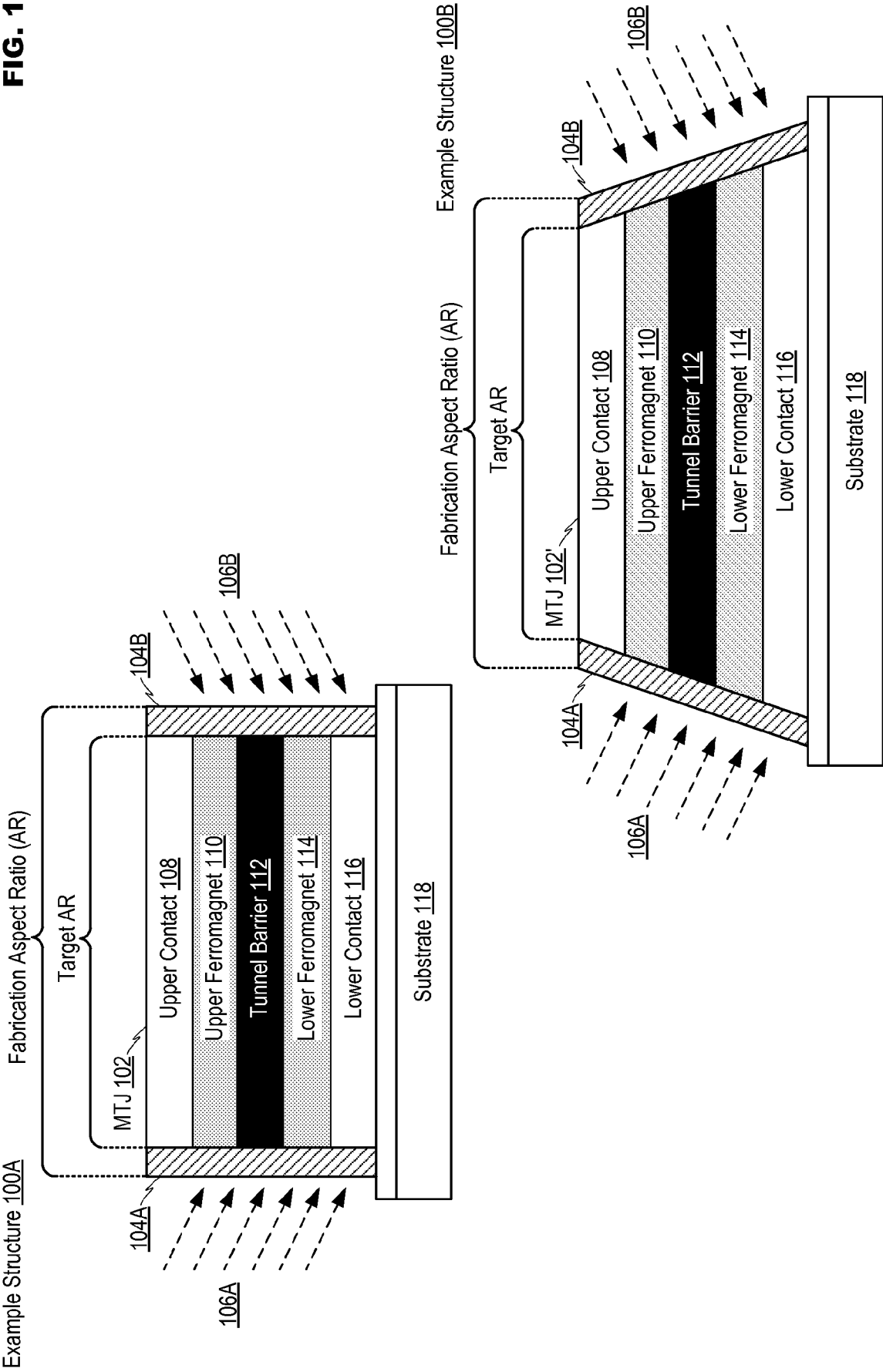


FIG. 2

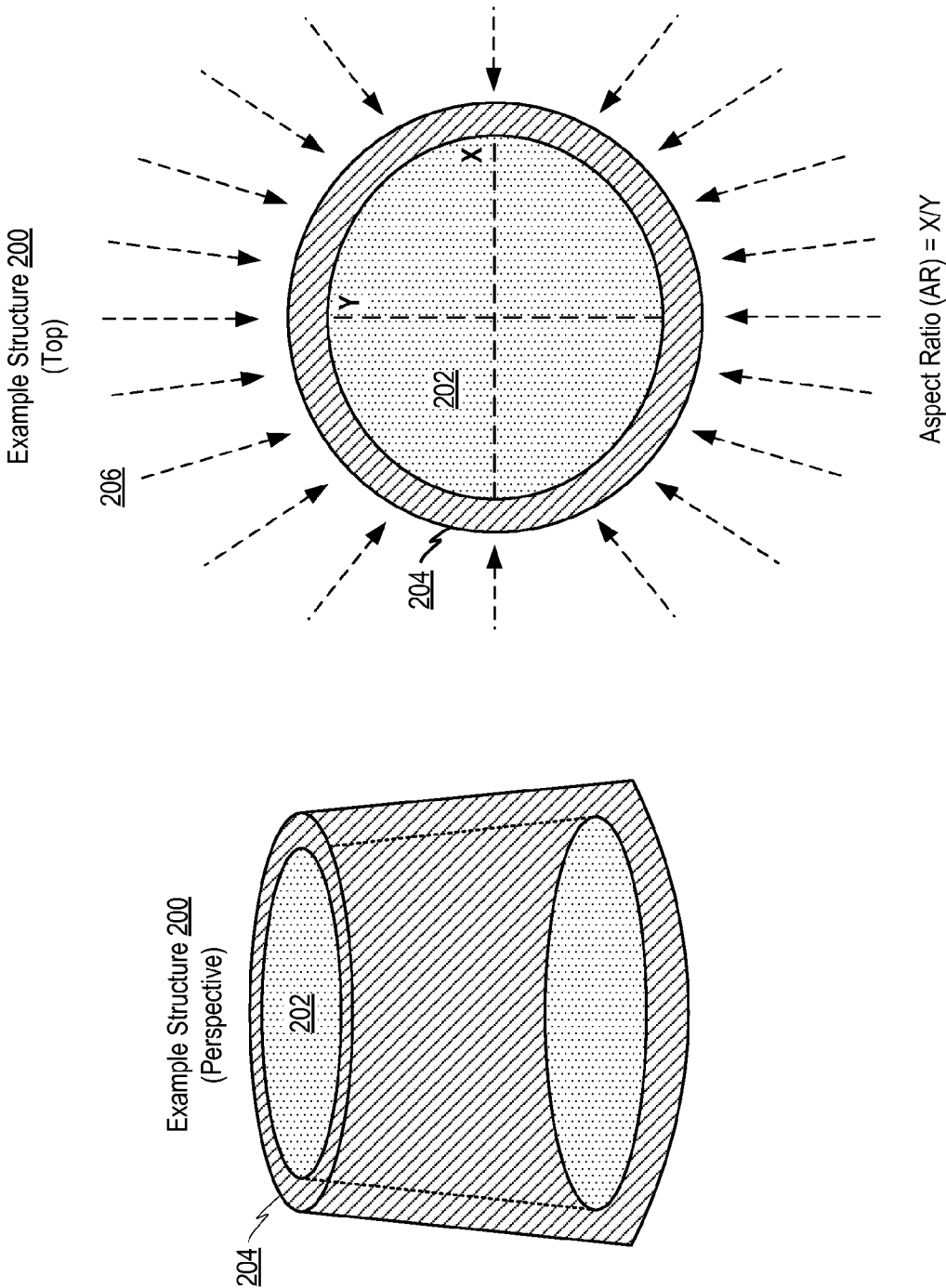


FIG. 3

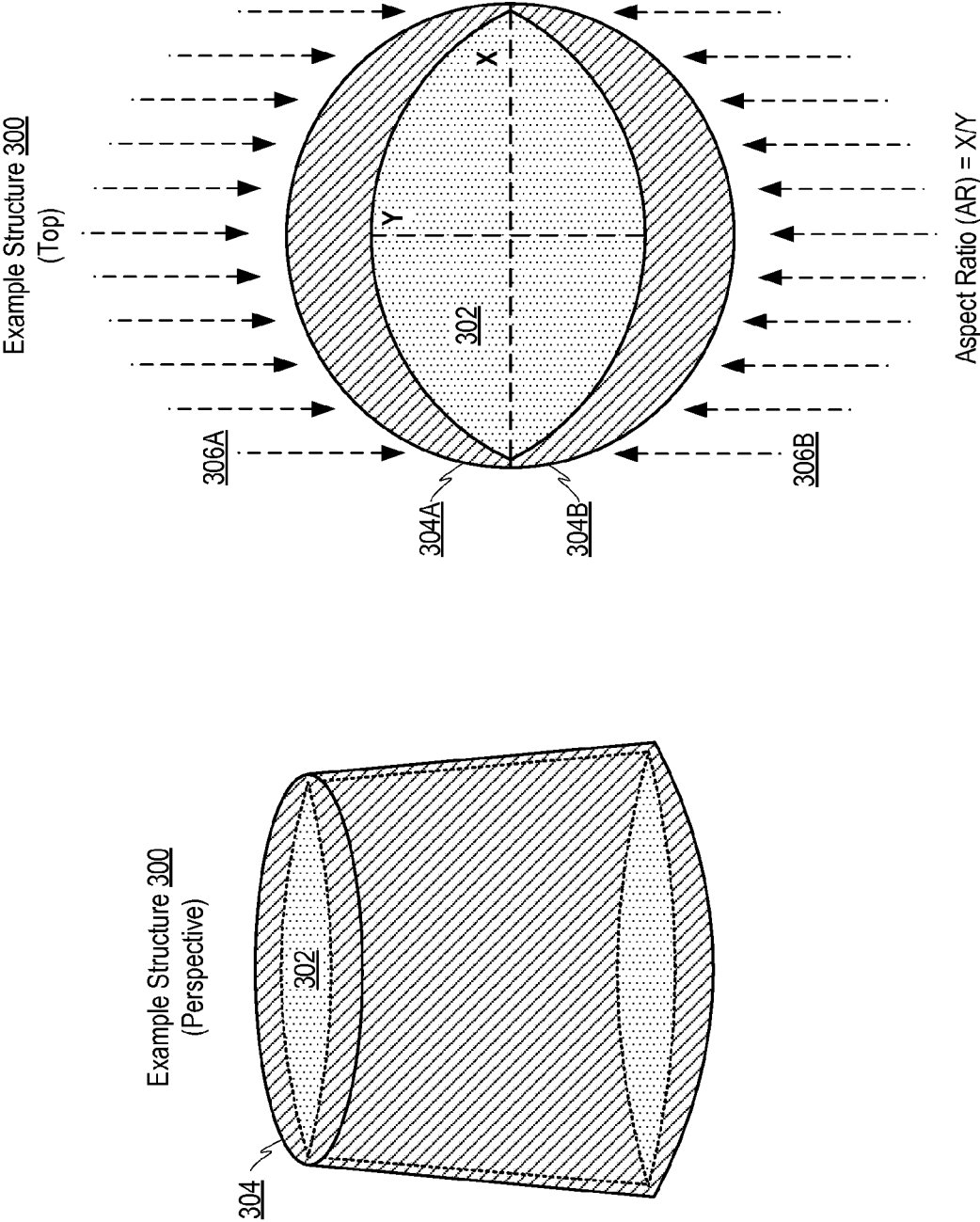


FIG. 4

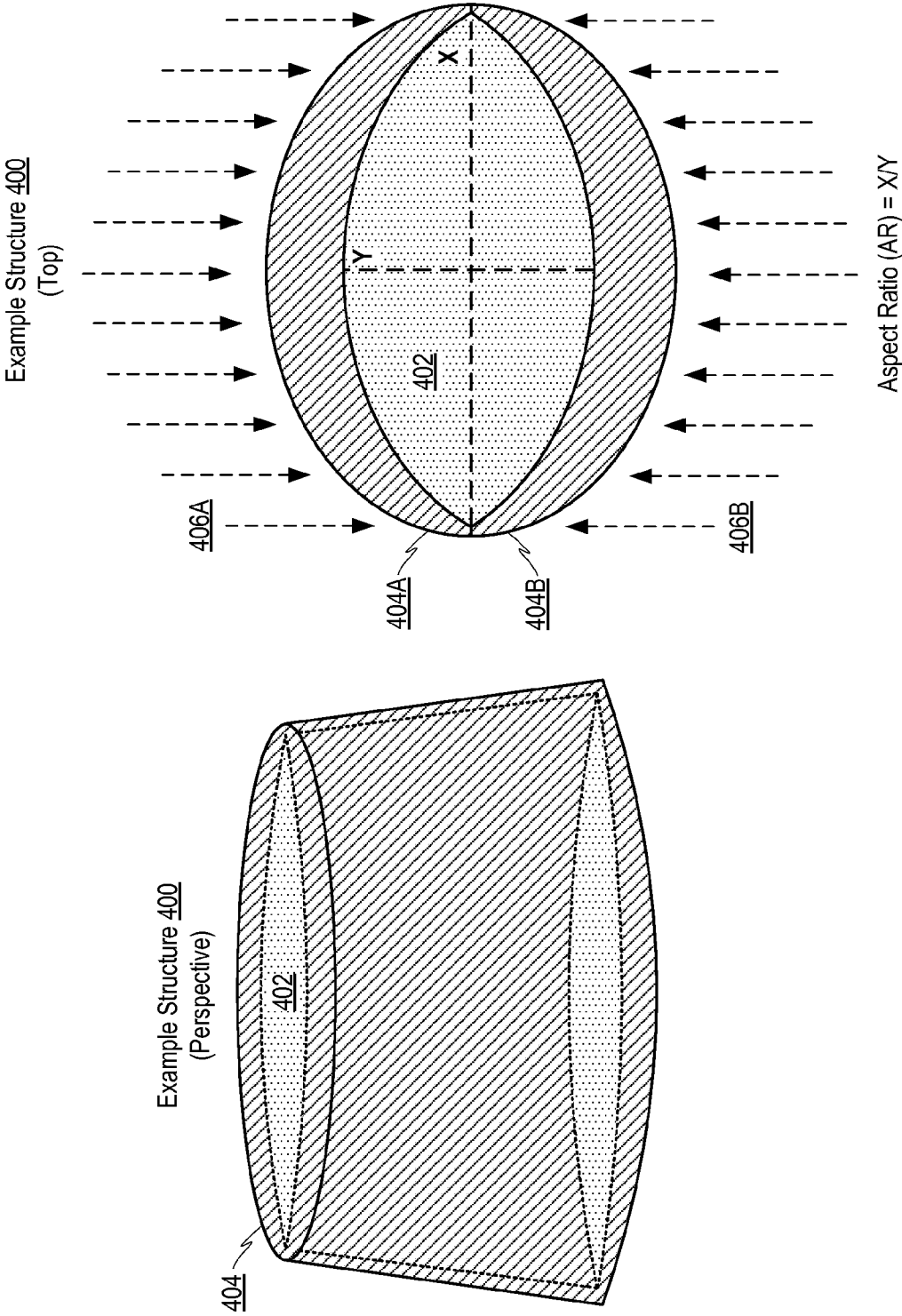


FIG. 5

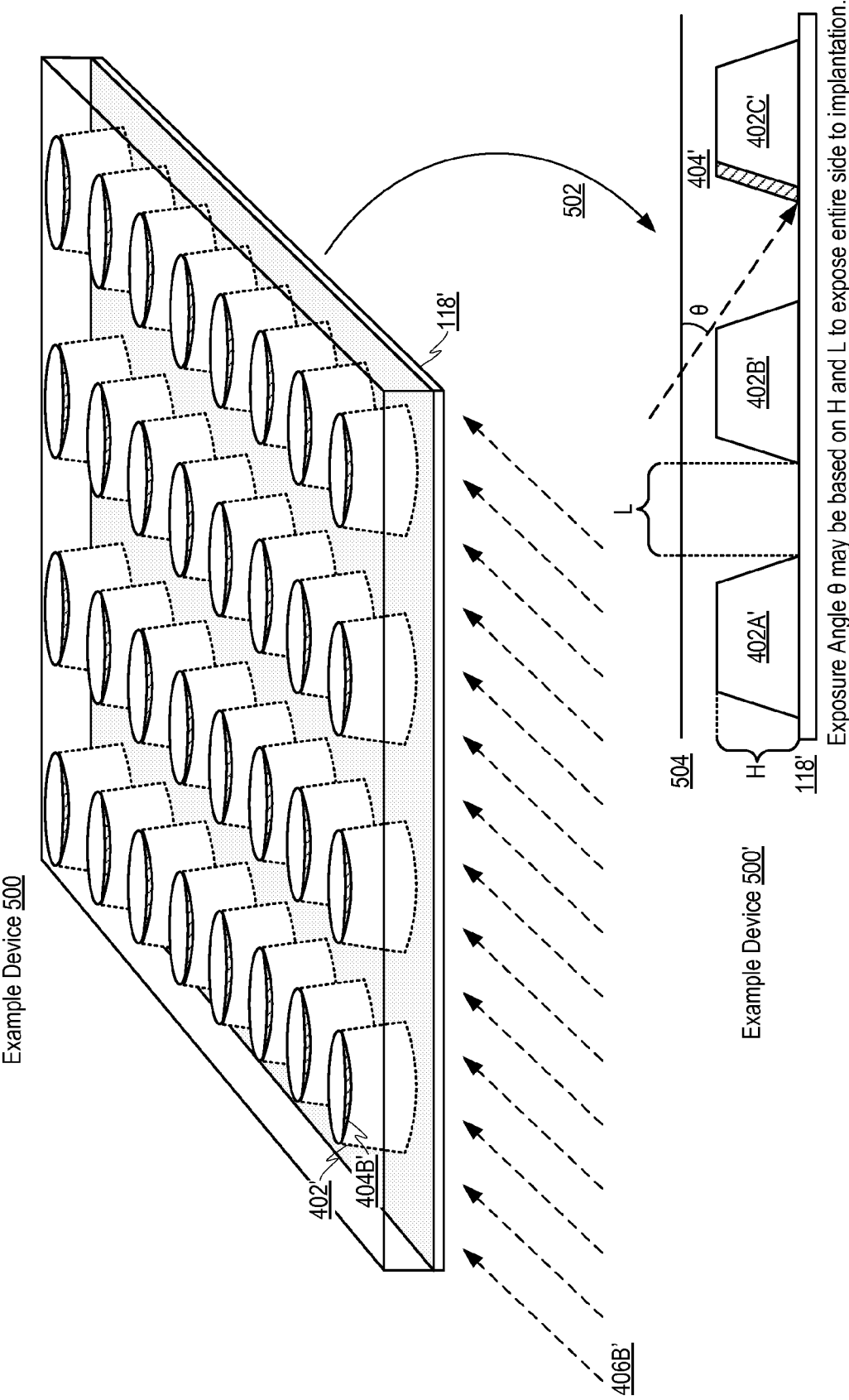


FIG. 6

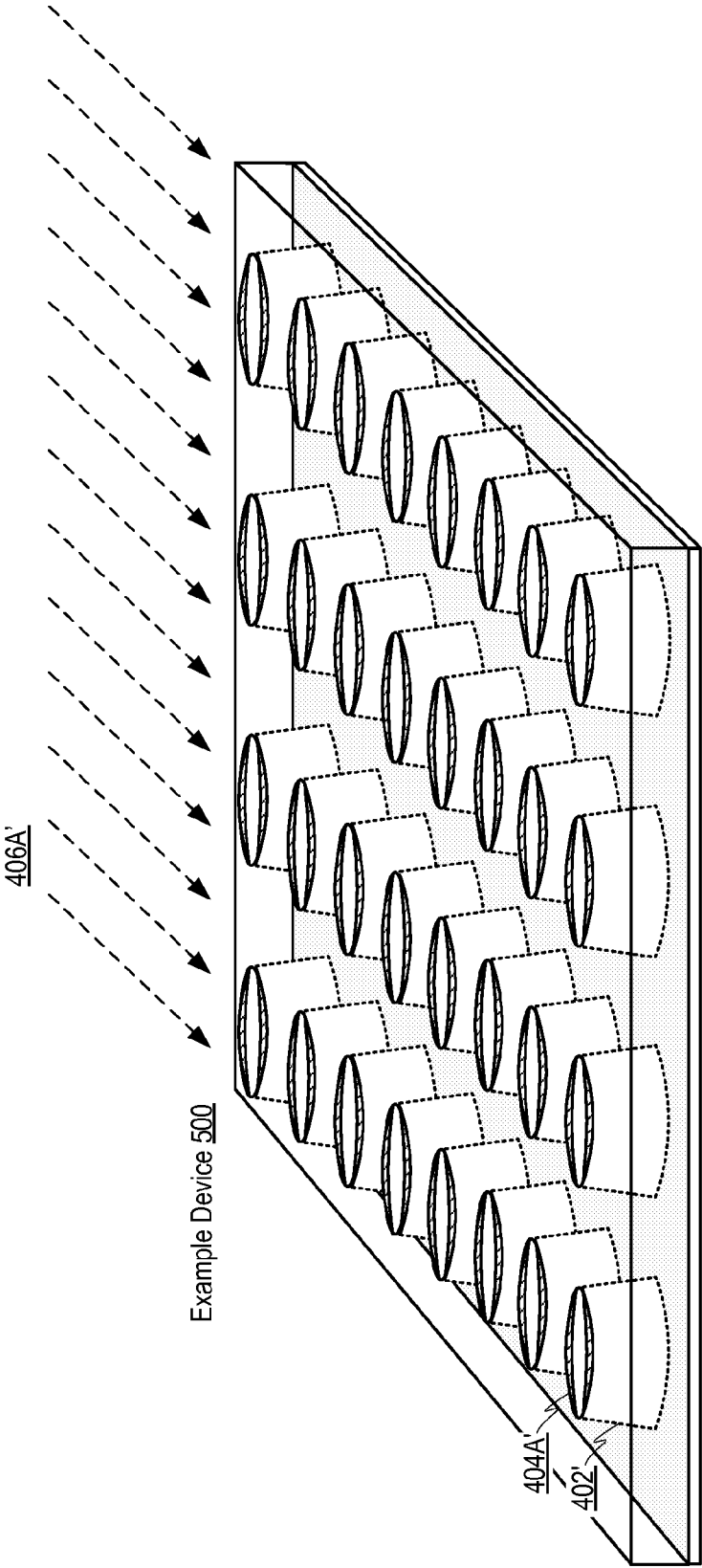


FIG. 7

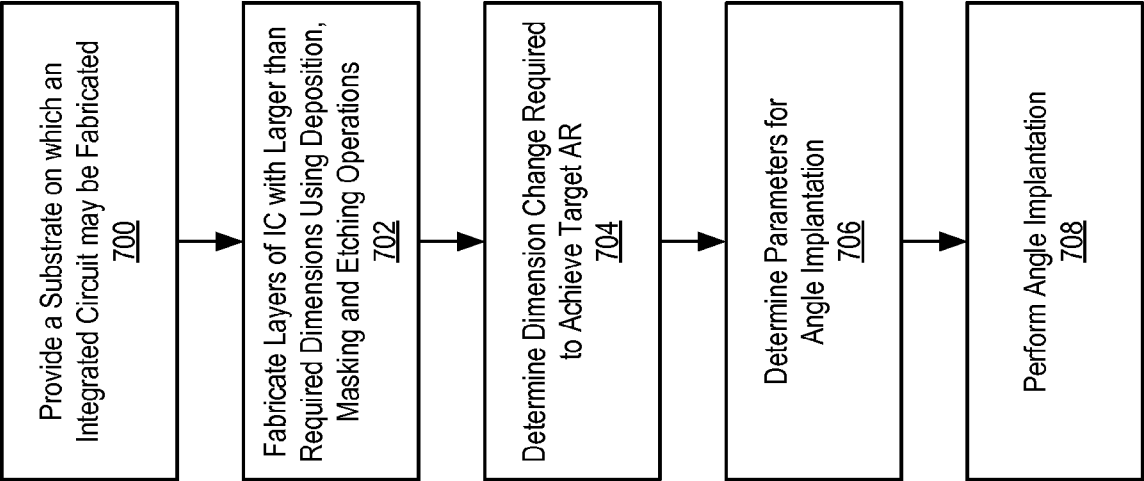
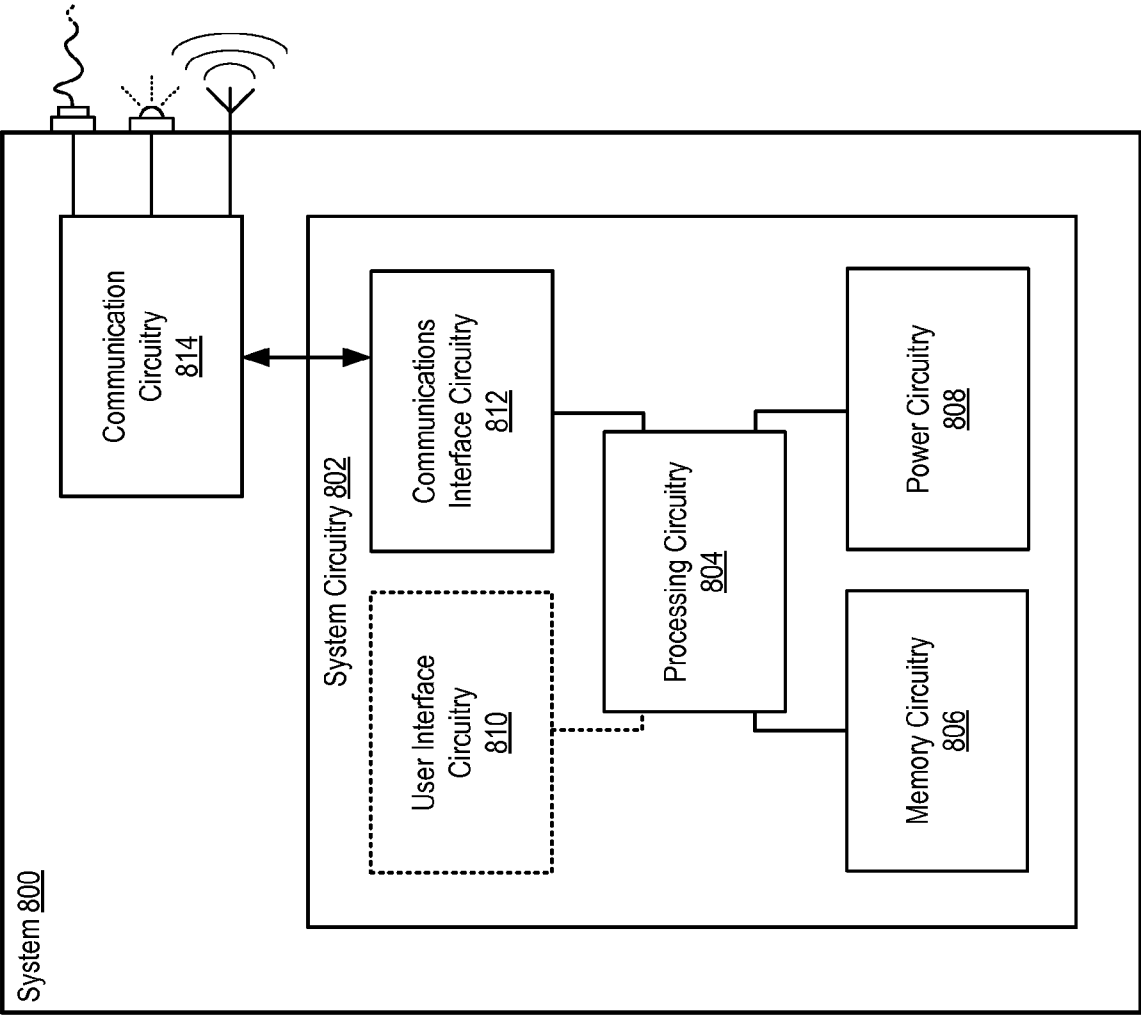


FIG. 8



A. CLASSIFICATION OF SUBJECT MATTER**H01L 43/12(2006.01)i, H01L 43/02(2006.01)i, H01L 43/08(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 43/12; H01L 43/08; H01L 21/8246; H01L 21/306; G11C 11/16; G11B 5/66; H01L 43/10; H01L 43/02

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords:magnetic tunnel junction, aspect ratio, angle, modify, ion implantation

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0029431 A1 (SHIGEKI TAKAHASHI et al.) 31 January 2013 See paragraphs [0015]-[0020], [0081]-[0095] [0152], claim 1 and figures 1, 3B.	1-24
A	US 2014-0198564 A1 (YIMIN GUO) 17 July 2014 See paragraphs [0058]-[0076], claim 1 and figure 2A.	1-24
A	JP 2007-103692 A (NEC CORP.) 19 April 2007 See paragraphs [0041]-[0049], claim 1 and figure 8.	1-24
A	US 2013-0288397 A1 (KABUSHIKI KAISHA TOSHIBA) 31 October 2013 See paragraphs [0047]-[0088], claim 1 and figure 2.	1-24
A	US 2012-0088125 A1 (KATSUYA NISHIYAMA et al.) 12 April 2012 See paragraphs [0059]-[0065], claim 1 and figure 9.	1-24



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

21 June 2016 (21.06.2016)

Date of mailing of the international search report

21 June 2016 (21.06.2016)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/051138

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