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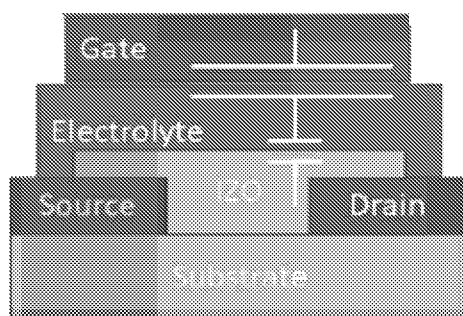


FIG. 3A

(57) Abstract: The present disclosure provides a field effect transistor (FET). The FET includes: two drive electrodes (source/ drain) a gate electrode made of conducting material and a channel layer made of semiconductor material; an additional conducting layer is coupled to the channel layer in a way that this conducting layer is wider than channel region and shorter than the channel layer to avoid contact with the drive electrodes and to enable a low resistance path for electronic transport; an insulator layer provided between the gate electrode and the channel/ conducting layer in a way that an exposed portion of the channel layer to the insulating layer near the drive electrodes makes the current switching possible. The present disclosure preferentially uses a solution processing/ printing technique to achieve fabrication of the FETs. Additionally, the present disclosure includes a circuit comprised of one or more the said FETs.

HIGH POWER PRINTED FIELD EFFECT TRANSISTORS (FET)

TECHNICAL FIELD

[1] The present disclosure relates, in general, to solution processed/printed field effect transistors (FET). In particular, the present disclosure relates to a printable FET with a geometry that helps enable short channel FETs with high ON-current and high power output, and at times a low subthreshold slope below the Boltzmann limit.

BACKGROUND

[2] The background description includes information that may be useful in understanding the present invention. It is not an admission that any of the information provided herein is prior art or relevant to the presently claimed invention, or that any publication specifically or implicitly referenced is prior art.

[3] The switching of conventional MOSFET devices is limited by a fundamental barrier arising from the Boltzmann distribution of electrons, and the phenomenon is commonly known as ‘Boltzmann Tyranny’. The subthreshold swing of a transistor that is typically extracted from the slope of the transfer curve can be expressed as:

$$S = \frac{\partial V_{GS}}{\partial \Psi_S} \cdot \frac{\partial \Psi_S}{\partial (\log I_D)}$$

[4] Herein, the first term, $\frac{\partial V_{GS}}{\partial \Psi_S}$, known as the ‘body factor’ cannot be less than 1 for standard MOSFET electrostatics, and the second term $\frac{\partial \Psi_S}{\partial (\log I_D)}$, which equals to $\frac{K_B T}{q} \ln(10)$, is about 60 mV/dec at room temperature and this determines the minimum limit of the subthreshold swing for the thermionic emission over the Boltzmann barrier. This in turn defines the steepness/ slope of the transfer curves, the signal gains and the dynamic power dissipation of the electronic switches.

[5] One way to circumvent this limit is to allow tunnelling through the barrier. However, in this case band-to-band-tunnelling (BTBT) would be required as single carrier tunnelling cannot lead to sub-thermionic transport. The BTBT field effect transistors (FETs) typically show low ON-currents. While there are large number of sub-thermionic tunnel FETs reported in the literature, the recent ones, based on 2D dichalcogenides, demonstrate

particularly high performance. An alternative approach to achieve sub-thermionic transport involves stabilizing a negative capacitance regime by placing a ferroelectric and dielectric layer in series to comprise the metal-ferroelectric-insulator semiconductor capacitor (MFISCAP). In this case, the Boltzmann activation barrier remains intact; however, an artificial voltage amplifier or step-up transformer is created using the sharp switching of the dipoles of the ferroelectric and thereby a faster change in Ψ_S (surface potential) is possible, as compared to the applied ∂V_{GS} .

[6] On the other hand, solution processed/ printed FET, fabricated from various organic or inorganic semiconductor materials (which may be made of zero, one, two, three dimensional semiconductor materials) suffer from lower ON-currents or switching speed due to limited printing resolution. Therefore, there is a need for an alternative approach for solution processed/ printed FETs that can provide short (or narrow) channel FETs or in a special embodiment a sub-thermionic transport for steep/ rapid switching of the said FET. On the other hand, the sort (narrow) channel can provide high ON current and high power output. Both of these may exist either together or separately in a given system and in either case solve present limitations of solution processed/ printed FETs and circuits fabricated thereof.

[7] In some embodiments, the numerical parameters set forth in the written description and attached claims are approximations that can vary depending upon the desired properties sought to be obtained by a particular embodiment. In some embodiments, the numerical parameters should be construed in light of the number of reported significant digits and by applying ordinary rounding techniques. Notwithstanding that the numerical ranges and parameters setting forth the broad scope of some embodiments of the invention are approximations, the numerical values set forth in the specific examples are reported as precisely as practicable. The numerical values presented in some embodiments of the invention may contain certain errors necessarily resulting from the standard deviation found in their respective testing measurements.

[8] As used in the description herein and throughout the claims that follow, the meaning of “a,” “an,” and “the” includes plural reference unless the context clearly dictates otherwise. Also, as used in the description herein, the meaning of “in” includes “in” and “on” unless the context clearly dictates otherwise.

[9] The recitation of ranges of values herein is merely intended to serve as a shorthand method of referring individually to each separate value falling within the range. Unless otherwise indicated herein, each individual value is incorporated into the specification

as if it were individually recited herein. All methods described herein can be performed in any suitable order unless otherwise indicated herein or otherwise clearly contradicted by context. The use of any and all examples, or exemplary language (e.g. “such as”) provided with respect to certain embodiments herein is intended merely to better illuminate the invention and does not pose a limitation on the scope of the invention otherwise claimed. No language in the specification should be construed as indicating any non-claimed element essential to the practice of the invention.

[10] Groupings of alternative elements or embodiments of the invention disclosed herein are not to be construed as limitations. Each group member can be referred to and claimed individually or in any combination with other members of the group or other elements found herein. One or more members of a group can be included in, or deleted from, a group for reasons of convenience and/or patentability. When any such inclusion or deletion occurs, the specification is herein deemed to contain the group as modified thus fulfilling the written description of all groups used in the appended claims.

OBJECTS OF THE INVENTION

[11] A general object of the present invention is to provide a high-ON-current/ power field effect transistor (FET) and a circuit using said FET.

[12] Another object of the present invention is to provide a solution processed/ printed FET with high-ON-current / power.

[13] Another object of the present invention is to provide an FET with a stable and static negative capacitance effect.

[14] Another object of the present invention is to provide an FET with a low sub-threshold swing, lower than Boltzmann limit.

[15] Another object of the present invention is to provide an FET with high ON-current characteristics.

[16] Another object of the present invention is to provide a solution processed/ printed FET whose channel lengths are lower than FET printed using commercial/ industrial printers.

[17] Another object of the present invention is to provide a high frequency/ high switching speed FET and a circuit using said short channel FET.

SUMMARY

[18] The present disclosure relates generally to solution processed/ printed field effect transistors (FET). In particular, the present disclosure relates to a printable and non-standard architecture where an additional conducting (metal) layer placed adjacent to the semiconductor channel layer can provide short (or, narrow) channel FETs with high current / power output, and there can be a superior high frequency performance in a circuit made out of the said FETs.

[19] In an aspect, the disclosure provides a metal-insulator-metal-semiconductor (MIMS) FET architecture which can provide a negative capacitance effect and a subthermionic transport (that is subthreshold slope below the Boltzmann limit) when an electrolytic insulator is used.

[20] In an aspect, the present disclosure provides a field effect transistor (FET). The FET includes: a channel layer made of a semiconductor material and disposed in a channel region defined by a source and a drain of the FET; a conducting layer coupled to the channel layer, the conducting layer having a length greater than the channel region defined by the source and the drain of the FET and lesser than the semiconducting channel layer to enable a low resistance path being formed on the channel layer for electronic transport and an effective reduction in the channel layer length; and an insulator layer provided between a gate of the FET and the channel layer such that an exposed portion of the channel layer between the source and the drain of the FET is in contact with the insulator layer. The conducting layer allows charge transport through the channel layer only at the exposed portion of the channel layer near the source and the drain to enable short (narrow) channel FET, thereby resulting in a high ON current and high power of the FET device.

[21] In an embodiment, the channel layer can be deposited on the substrate and the conducting layer is deposited atop the channel layer. In another embodiment, second semiconductor layer is deposited atop the conducting layer.

[22] In another embodiment, the conducting layer can be deposited on the substrate with the channel layer deposited atop the conducting layer.

[23] In another embodiment, the conducting layer is provided in such a way that there is no direct contact between the conducting layer and both of the source and the drain.

[24] In another embodiment, the FET is fabricated by solution processing or printing methods.

[25] In another embodiment, the insulator layer is made of a material selected from a group comprising an electrolytic insulator such as a solid polymer electrolyte, a liquid

electrolyte and an ion-gel; an oxide dielectric such as SiO_2 , Al_2O_3 and HfO_2 ; an organic dielectric such as PVA and PMMA; an inorganic ferroelectric such as BTO and PZT; an organic ferroelectric such as PVDF-TrFE ; and a combination thereof.

[26] In another embodiment, the insulator layer of the FET can be an electrolyte, which enables demonstrations of a negative capacitance (NC) effect and subthermionic transport with subthreshold slope below the Boltzmann limit in said FET when the conducting layer is exposed to the insulating layer.

[27] In another embodiment, the semiconductor of the channel layer can be selected from a group comprising amorphous oxides, crystalline oxides, oxide nanoparticles, nanowires, organic semiconductors, 2D semiconductors of transition metal dichalcogenides, Mxenes and other suitable inorganic materials in a form of nanoparticles, nanowires and thin film and a combination thereof.

[28] In another embodiment, the semiconductor of the channel layer is made of phase change material that shows abrupt metal-insulator transition (MIT) behaviour, and can be selected from a group comprising TiO_2 , VO_2 , other suitable materials and a combination thereof.

[29] In another embodiment, the conducting layer can be formed of a material selected from a group comprising metals such as gold, platinum, silver, copper; graphene carbon nanotubes; and PEDOT:PSS. In an exemplary embodiment, the conducting layer is formed of a metal such as any or a combination of gold, platinum and silver.

[30] In another embodiment, the source and the drain can be formed of a material selected from a group comprising a transparent conducting oxide such as indium tin oxide (ITO) and fluorine-doped tin oxide (FTO); or a pure metal such as gold, silver, copper and platinum; a conducting organic material such as PEDOT:PSS; and a combination thereof.

[31] In another embodiment, the used substrate can be any of a flexible substrate such as cellulose, paper and polymer; and a rigid substrate such as glass and silicon wafer.

[32] In another aspect, the present disclosure provides a circuit comprising a plurality of FETs of the present disclosure. The high ON current and high power output of each of the plurality of FETs enable the circuit to have high ON current and high power output characteristics. Additionally, the circuit demonstrates high frequency switching.

[33] In another embodiment, the FET exhibits ON/OFF ratio of 10^7 or higher.

[34] In another embodiment, the FET exhibits a sub-threshold swing less than 16 mV/dec or lower.

[35] In another embodiment, the FET exhibits an ON-current density value of 310 $\mu\text{A}/\mu\text{m}$ or higher.

[36] Various objects, features, aspects and advantages of the inventive subject matter will become more apparent from the following detailed description of preferred embodiments, along with the accompanying drawing figures in which like numerals represent like components.

BRIEF DESCRIPTION OF THE DRAWINGS

[37] FIGs. 1A – 1C illustrate exemplary cross-section and top views of different geometries of the proposed device, in accordance with an embodiment of the present disclosure.

[38] FIGs. 2A – 2C illustrate exemplary transfer characteristics of the proposed FET device for channel layer (a-IZO) annealed at temperatures 300, 350 and 400 °C respectively, in accordance with an embodiment of the present disclosure.

[39] FIGs. 3A and 3B illustrate exemplary schematic diagrams showing the gate and channel capacitance of standard a-IZO channel FET and FETs with additional printed Ag layer on top of a-IZO respectively.

[40] FIGs. 3C and 3D illustrate exemplary schematic representations of the applied potential distribution across MISCAP and MIMSCAP structures respectively.

[41] FIG. 4A illustrates an exemplary schematic representation of band structure of ITO, a-IZO and silver when separated.

[42] FIG. 4B illustrates an exemplary schematic representation of band structure of ITO, a-IZO and silver when the a-IZO layer is sandwiched in vertical stack of ITO and printed silver layer.

[43] FIG. 4C illustrates an exemplary schematic cross-section view of the proposed device and its functional circuit diagram, in accordance with an embodiment of the present disclosure.

[44] FIG. 5A illustrates exemplary transfer characteristics of 14 MIMS-FET devices (a-IZO annealed at 350 °C).

[45] FIG. 5B illustrates exemplary gate voltage - gate current plots of 4 MIMS-FETs.

[46] FIG. 5C illustrates an exemplary probe voltage (measuring the bulk electrolyte potential) placed in between the gate and the channel showing a sharp rise with $\frac{\partial V_P}{\partial V_{GS}}$ reaching a value greater than 3.

[47] FIG. 5D illustrates an exemplary transition and signal gain of printed transistor-resistor ($\sim 1 \text{ M}\Omega$) inverter with one MIMSFET.

[48] FIG. 5E illustrates an exemplary typical transfer characteristic of the printed MIMS FET device, where the a-IZO layer has been annealed at 350°C , showing the specific drain current and transconductance variation over the entire applied gate voltages.

[49] FIG. 5F illustrates exemplary transfer characteristic and drain voltage-drain current characteristic of the MIMS-FET device ($V_D = 0.5 \text{ V}$).

[50] FIG. 5G illustrates exemplary transfer characteristic along with transconductance with respect to applied gate voltages, plotted for MIMS-FETs, where, the a-IZO layer annealed at 300 , 350 and 400°C .

[51] FIG. 5H illustrates exemplary MIMSFET performance with respect to the thickness of the printed channel layer.

[52] FIGs. 6A – 6C illustrate exemplary transfer characteristics of a printed 2D semiconductor channel MIMSFET, in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION

[53] The following is a detailed description of embodiments of the disclosure depicted in the accompanying drawings. The embodiments are in such detail as to clearly communicate the disclosure. However, the amount of detail offered is not intended to limit the anticipated variations of embodiments; on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the present disclosure as defined by the appended claims.

[54] In an aspect, the present disclosure relates to a solution processed/ printed and preferentially electrolyte gated Metal-Oxide-SemiconductorField Effect Transistor (MOSFET) device using a non- FET) architecture. The architecture results in short (narrow) channel printed FETs with high current/ power density and provides higher switching frequency resulting in superior high frequency performance.

[55] In another aspect, an electrolytic insulator can be used, which exploits the capacitors-in-series (at gate-electrolyte and channel-electrolyte interfaces) architecture of theelectrolyte-gated FETs to obtain a negative capacitance (NC)-like regime resulting in a highly reproducible sub-thermionic transport, which, in an exemplary implementation, can be suitable for slow response sensor interfaces in order to amplify a signal by exploiting steep

slope transfer characteristics of the proposed sub-thermionic FETs. Further, the proposed FET architecture enables short (narrow)-channel printed FETs, which, beyond the sub-thermionic regime, offers a strong thermionic transport with extremely large high ON currents and transconductance values that are larger than the printed FETs fabricated using standard architecture.

[56] In another aspect, the present disclosure provides a circuit comprising said FETs.

[57] In an exemplary embodiment, the present disclosure provides a printed amorphous oxide semiconductor (AOS) FET. Further, a change in geometry is introduced by placing an additional printed metal (such as silver) layer on top of the printed AOS channel, which facilitates simultaneous observation of negative capacitance induced sub-thermionic transport and printed short (narrow)-channel FETs with high ON currents and transconductance. High ON current and transconductance values are achieved without compromising the ON-OFF ratio. The high-current, short (narrow) channel FETs fabricated using the non-standard FET architecture would enable high performance circuits with high switching frequency.

[58] In another embodiment, the insulator can be an electrolyte, and the electrolyte-gating results in formation of two capacitors in series at the channel/electrolyte and gate/electrolyte interface. The channel/ electrolyte capacitor can be tuned with gate voltage. A reversible passivation and de-passivation of the metal layer atop the semiconducting channel can result in a static negative capacitance at the channel-electrolyte interface. In electrolyte-gated MOSCAP, the applied gate voltage is shared between capacitors with a larger potential drop across a smaller one. Any mechanism that can abruptly reduce or diminish the capacitance at the channel side can induce NC like behaviour. In the proposed FET, NC behaviour is induced by an electrochemical surface passivation or de-passivation process, which can reversibly change the channel capacitance and ensure a stable and static NC effect and associated sub-thermionic transport for orders of magnitude of drain currents and nearly hysteresis-free transfer characteristics. For the proposed FET, the printed metal layer on the AOS channel renders it a short (narrow)-channel FET, as the electronic transport at the channel region occurs primarily through the metal layer atop. This results in large ON state conductance.

[59] In another aspect, the proposed FETs are processed at low temperatures, and the processing method of the present disclosure can be extended to technologies where the process temperature can be low-cost polymer substrate compatible.

[60] In an embodiment, for sub-thermionic transport, a pore-free semiconductor layer is required, which can be sandwiched between patterned drive electrodes and printed conducting (metal) layer on top. This enables the electrolytic insulator to stay on top of the semiconductor channel, thereby exerting unidirectional electric field and forcing the electronic transport to take place largely through the silver layer. The semiconductor layer underneath the conducting (metal) layer is deprived of any direct contact to the electrolytic insulator and hence no carrier accumulation takes place at the semiconductor.

[61] It can be appreciated by those skilled in the art that the present device is an illustration of an AOS device with a printed conducting (metal) layer on top of the semiconductor. The specific semiconductor used, the metal used as well as the architecture, as presented, is one embodiment and serves to describe the non-standard FET architecture, and may not be construed as a limitation of the non-standard FET architecture.

[62] In an embodiment, semiconductors used can be any, without limitations, of amorphous oxides, crystalline oxides, oxide nanoparticles, nanowires, other inorganic materials in nanoparticle, nanowire, thin film form, organic semiconductors, organic nanowires, 2D semiconductors of transition metal dichalcogenides, Mxenes etc. In an exemplary embodiment, the present disclosure provides amorphous oxides semiconductors (AOS) which can be featureless and spatially homogenous when solution processed/printed.

[63] In another embodiment, the amorphous oxides can be any of, without limitation, amorphous indium doped zinc oxide (a-IZO), indium gallium zinc oxide (IGZO), zinc tin oxide (ZTO), zinc indium oxide (ZIO), tin gallium zinc oxide (TGZO), indium gallium oxide (IGO), zinc indium tin oxide (ZITO), etc. In another embodiment, the present disclosure provides a device with solution processed/printed a-IZO semiconductor layer.

[64] In another embodiment, a printed and electrolyte-gated MOSFET device can be fully printed or fabricated with lithographically-structured passive electrodes and can have a gate geometry that can be a displaced-gate, a side gate or a top gate.

[65] In another embodiment, the electrolytic gate insulator (or, dielectric) used can be any of, without limitation, a solid polymer electrolyte, a liquid electrolyte, an ion-gel, an oxide dielectric (such as SiO_2 , Al_2O_3 , HfO_2 , TiO_2 etc.), an organic dielectric (such as PVA, PMMA etc.), an inorganic ferroelectric (such as BTO, PZT etc.) and an organic ferroelectric (such as PVDF-TrFE etc.). While, the NC-effect and subthermionic transport may only be limited to the electrolyte (including ion gels)-gated FETs, the dielectric or ferroelectric gated FETs would still be short (narrow) channel FETs and hence, show high current/ high power

transistor performance. As a result, the circuit made using said FETs would have high frequency switching and superior high frequency performance.

[66] In another embodiment, the device architecture can be top-contact, in which case the conducting (metal) layer can be directly placed on to the substrate, followed by the semiconductor layer and the source/ drain contacts on top. Here, while short (narrow) channel FET can be achieved, the NC-effect or the subthermionic transport may not be seen.

[67] In another embodiment, the conducting (metal) layer can be sandwiched between two semiconducting layers, that is, a second semiconducting layer atop the printed conducting (metal) layer. Here again, while short (narrow) channel FET can be achieved, the NC-effect or the subthermionic transport may not be seen.

[68] FIGs.1A – 1C illustrate exemplary cross-section and top views of different geometries of the proposed FET device, in accordance with an embodiment of the present disclosure.

[69] Referring to FIG. 1A, the device 100 includes a substrate 102 upon which a source electrode 104-1 and a drain electrode 104-2 are provided and a channel region is defined between the source electrode 104-1 and the drain electrode 104-2. The gap between 104-1 and 104-2 defines the channel region. A semiconducting channel layer 106 is provided on top of the substrate 102 and in the channel region. The channel layer 106 is so provided as to have a length greater than the channel region, thereby partially covering both of the source electrode 104-1 and the drain electrode 104-2. A conducting layer 108 is provided on top of the channel layer 106, the conducting layer 108 having a length greater than the channel region but lesser than the length of the channel layer 106. The conducting layer 108 is so disposed that the channel layer 106 is partially exposed, the partially exposed region being over the source electrode 104-1 and the drain electrode 104-2. On the other hand, the conducting layer 108 has no direct contact with the electrodes 104-1 and 104-2. An insulator layer 110 is provided on top of the channel layer 106 and the conducting layer 108 such that the conducting layer 108 is sandwiched between the channel layer 106 and the insulator layer 110. Due to the dimensions of the channel layer 106 and the conducting layer 108, only the exposed portions of the channel layer 106 are in contact with the insulator layer 110. A gate 112 is provided atop the insulator layer 110. Since the conducting layer 108 is longer than the channel region, the length of the channel layer 106 available for conduction of charges reduces to a few tenths of nanometers in vertical direction (FIG 1A), and the conducting layer 108 provides a low resistance path for a large portion of the channel length, typically in the range of tens of microns. The small region of the channel layer 106 that allows conduction of

charges also facilitates in the generation of short (or, narrow) channel effect in the channel region, thereby resulting in high ON-current and high power output of the FET.

[70] Referring again to FIG. 1A, in another embodiment, the insulator layer 110 of the device 100 can be made of an electrolyte. The interface between the electrolyte and the gate 112 results in formation of two capacitors in series at the channel/electrolyte and gate/electrolyte interface. The channel/electrolyte capacitor can be tuned with gate voltage. A reversible passivation and de-passivation of the conducting layer 108 atop the semiconducting channel layer 106 can result in a static negative capacitance (NC) at the channel-electrolyte interface. In electrolyte-gated MOSCAP, the applied gate voltage is shared between capacitors with a larger potential drop across a smaller one. Any mechanism that can abruptly reduce or diminish the capacitance at the channel side can induce NC like behaviour. In the proposed FET device 100, NC behaviour is induced by an electrochemical surface passivation or de-passivation process, which can reversibly change the channel capacitance and ensure a stable and static NC effect and associated sub-thermionic transport for orders of magnitude of drain currents and nearly hysteresis-free transfer characteristics.

[71] Referring to FIG. 1B, the device 140 includes a substrate 142 upon which a source electrode 144-1 and a drain electrode 144-2 are provided and a channel region is defined between the source electrode 144-1 and the drain electrode 144-2. A semiconducting channel layer 146 is provided on top of the substrate 142 and in the channel region. The channel layer 146 is so provided as to have a length greater than the channel region, thereby partially covering both of the source electrode 144-1 and the drain electrode 144-2. A conducting layer 148 is provided on top of the channel layer 146, the conducting layer 148 having a length greater than the channel region but lesser than the length of the channel layer 146. A second semiconductor layer 150 is provided on top of the conducting layer 148, the length of the second semiconducting layer 150 being more than the length of the conducting layer 148 but lesser than the length of the channel layer 146. The conducting layer 148 is thus sandwiched between the channel layer 146 and the second semiconducting layer 150. An insulator layer 152 is provided on top of the second semiconducting layer 150 such that only the exposed portions of the channel layer 146 are in contact with the insulator layer 152. A gate 154 is provided atop the insulator layer 152. Since the conducting layer 148 is longer than the channel region, the length of the channel layer 146 available for conduction of charges reduces. The small region of the channel layer 146 that allows conduction of charges also facilitates in the generation of short (or, narrow) channel effect in the channel region, thereby resulting in high ON-current and high power output of the FET.

[72] Referring to FIG. 1C, the device 170 includes a substrate 172 upon which a source electrode 174-1 and a drain electrode 174-2 are provided and a channel region is defined between the source electrode 174-1 and the drain electrode 174-2. A conducting layer 176 is placed onto the substrate 172 in the channel region, defined by the top contact electrodes 174-1 and 174-2, the length of the conducting layer 176 being greater than the length of the channel region. A semiconductor channel layer 178 is provided above the conducting layer 176, the length of the channel layer 178 being greater than the length of the conducting layer 176. On top of the semiconductor layer 178, the source and drain electrodes 174-1 and 174-2 is placed such a way that the conducting layer 176 is longer than the channel region, gap between the electrodes 174-1 and 174-2. An insulator layer 180 is provided on top of the channel layer 178 such that the region of the channel layer 178 exposed between the source electrode 174-1 and the drain electrode 174-2 is fully covered by the insulator layer 180. A gate 182 is provided atop the insulator layer 180.

[73] In another embodiment, the semiconductor of the channel layer of the devices (100, 140, 170) can be any or a combination of amorphous oxides, crystalline oxides, oxide nanoparticles, nanowires, organic semiconductors, 2D semiconductors of transition metal dichalcogenides, Mxenes and other suitable inorganic materials in a form of nanoparticles, nanowires and thin film.

[74] In another embodiment, the conducting layer of the devices (100, 140, 170) can be any or a combination of conducting metals and highly conducting non-metals.

[75] In another embodiment, the insulator layer of the devices (100, 140, 170) can be made of a material such as, without limitations, an electrolytic insulator such as a solid polymer electrolyte, a liquid electrolyte and an ion-gel; an oxide dielectric such as SiO_2 , Al_2O_3 , HfO_2 and TiO_2 ; an organic dielectric such as PVA and PMMA; an inorganic ferroelectric such as BTO and PZT; an organic ferroelectric such as PVDF-TrFE; and a combination thereof.

[76] In another embodiment, the source and the drain can formed of a material such as, without limitations, a transparent conducting oxide such as indium tin oxide (ITO) and fluorine-doped tin oxide (FTO); a pure metal such as gold and platinum; a conducting organic material such as PEDOT:PSS; and a combination thereof.

[77] In another embodiment, the used substrate can be any of a flexible substrate such as cellulose, paper and polymer; and a rigid substrate such as glass and silicon wafer.

[78] Embodiments described herein relate to the architecture and device characteristics of the device 100. It would be appreciated that the devices (140, 170) also fall

within the purview of the present application, and that any embodiments described for the device 100 can be suitably modified to fit the devices (140, 170).

[79] In an exemplary embodiment, the semiconductor material used to demonstrate the device (100, 140, 170) of the present disclosure is amorphous indium doped zinc oxide (a-IZO).

[80] In an exemplary embodiment, the material of the conducting layer used to demonstrate the device (100, 140, 170) of the present disclosure is a metal such as gold, platinum and silver. In particular, the described devices (100, 140, 170) are provided with conducting layer made of silver.

[81] In an exemplary embodiment, the insulator material used to demonstrate the device (100, 140, 170) of the present disclosure is a solid electrolyte.

[82] The difference between the proposed FET device 100 and a typical MOSFET is in the printed conducting (metal) layer that is placed on top of the printed and annealed amorphous oxide semiconductor (AOS) in such a way that the printed conducting (metal) layer remains only on the AOS layer, thereby ensuring that there is no direct contact of the conducting (metal) layer with the ITO passives beneath. The metal used can be any of, without limitation, gold, platinum, silver etc. In an alternate embodiment, other conducting materials such as graphene and carbon nanotubes (CNT) can also be used. The present disclosure provides a device having the AOS layer made of a-IZO and the metal layer made of Silver.

[83] In another embodiment, the silver layer is lengthier than the channel dimensions, and hence, the necessary electrical transport through the a-IZO semiconductor layer reduces to a distance of only a few tens of nanometres, as is shown in FIG. 1A (shown with arrows). Thus, the printed conducting (metal) layer provides a low resistance path for most of the printable channel length, which is typically in the range of tens of microns for printed FETs. Thus, for the modified architecture, the channel length becomes comparable to the thickness of the printed a-IZO layer. Therefore, the proposed FET fabricated by the fully printing compatible architecture overcomes a long-standing obstacle of printed electronics, namely, device scaling.

[84] The modified device geometry results in a stable sub-thermionic transport as well as fully printing compatible short (narrow) channel (with channel lengths of the order of a few tens of nanometres) FET and a strong thermionic transport regime characterized by high ON currents and transconductance values.

[85] It can be appreciated by those skilled in the art that the present device is an illustration of an AOS device with a printed conducting (metal) layer. The specific semiconductor used, the metal used as well as the architecture, as presented, is one embodiment and serves to describe the non-standard MIMS architecture, and may not be construed as a limitation of the non-standard MIMS architecture.

[86] FIGs. 2A – 2C illustrate exemplary transfer characteristics of the proposed FET device for channel layer (a-IZO) annealed at temperatures 300, 350 and 400 °C respectively, in accordance with an embodiment of the present disclosure. High channel conductance values are observed along with extremely steep transfer curves for the FETs, where subthreshold slope values continue to be sub-thermionic for up to four orders of magnitude of drain currents.

[87] In another embodiment, the processing temperature can vary based on the semiconductor used. For semiconductors such as oxide nanoparticles or transition metal dichalcogenides (TMD) and CNT based devices, the processing temperature can be as low as ambient temperature (about 25 °C). In the present embodiment, for a-IZO, a processing temperature as low as 300 °C has been used.

[88] Table 1 below summarises the calculated subthreshold slope (SS) for different orders of magnitude of drain currents for the devices shown in FIGs. 1D – 1F. Here, the lowest values (such as 16 mV/dec) are noted for the devices where the a-IZO has been annealed at 350 °C. However, it can be argued that SS values are actually determined by the printing accuracy of the electrolytic insulator and even lower values (as low as 5 mV/dec, or lower) can be possible with high resolution printing and minimal overlay capacitance (overlap of the electrolytic insulator with ITO passives).

T (°C)	SS (mV/dec)		
	SS ₁	SS ₂	SS ₃
300	27.6	38.4	48.4
350	16.2	19.0	23.6
400	20.7	23.9	32.0

Table 1: Subthreshold slope calculated for different orders of magnitude of drain currents.

[89] FIGs. 3A and 3B illustrate exemplary schematic diagrams showing the gate and channel capacitance of standard a-IZO channel FET and FETs with additional printed Ag layer on top of a-IZO respectively.

[90] FIGs. 3C and 3D illustrate exemplary schematic representations of the applied potential distribution across MISCAP and MIMSCAP structures respectively.

[91] In an embodiment, in contrast to oxide dielectric based MOSCAPs, in the proposed FET, there are two capacitors in series for electrolyte gating. To maximize the gate capacitance and thereby minimize the potential drop at the gate electrode-electrolyte interface (as is shown in FIG. 3A, FIG. 3B respectively), typically, a higher area gate electrode is preferred.

[92] However, for metal-insulator-metal-semiconductor FET(MIMSFET) devices with the additional silver layer, the channel capacitance increases dramatically (C_{DL} of pure metal can be as large as $20\text{-}25\text{ }\mu\text{F}/\text{cm}^2$). Consequently, this can result in an equal sharing of the applied gate potential and the actual potential drop at the channel/electrolyte interface can be substantially lower. Nevertheless, to fully explain the shift in the V_T values observed up to 1.5 V, which has earlier been only slightly positive, an insight can be sought from the band structure and the band alignment of the vertical stack (ITO/ a-IZO/ Ag) of materials at the channel.

[93] FIG. 4A illustrates an exemplary schematic representation of band structure of ITO, a-IZO and silver when separated.

[94] FIG. 4B illustrates an exemplary schematic representation of band structure of ITO, a-IZO and silver when the a-IZO layer is sandwiched in vertical stack of ITO and printed silver layer.

[95] In an embodiment, the work function (ϕ) of a-IZO is around 4.15 eV, which is only slightly smaller than the work function of ITO (4.5 eV). Consequently, the energy barrier at the ITO/ a-IZO interface is negligible. In contrast, the work function of noble metals is typically high, for example ϕ_{Ag} is about 5-5.2 eV. This creates a Schottky contact at the a-IZO/ Ag interface. As has been noted, the a-IZO at the channel region is fully covered by the printed silver layer from top, and hence devoid of access to the electrolytic insulator. As a result, carriers do not accumulate at the a-IZO across the channel and hence, the drive currents flow through the Ag-layer on top of the semiconductor channel.

[96] FIG. 4C illustrates an exemplary schematic cross-section view of the proposed device and its functional circuit diagram, in accordance with an embodiment of the present disclosure.

[97] In another embodiment, the metal-insulator-metal-semiconductor (MIMS) transistor architecture can be presented as two common-gate asymmetric (non-identical drive electrodes) short (narrow) channel (channel dimension is about the thickness of the a-IZO layer) FETs in series. Hence, at low gate voltages, when the barrier height is high, one of the a-IZO/ Ag contact (say, the contact near the drain, on the assumption that source is grounded) behaves as a reverse biased Schottky diode upon application of a drive voltage. This effect, alongside the applied gate voltage splitting can maintain the OFF-state of MIMSFETs, up to high V_{GS} values.

[98] In another embodiment, the MIMSFET architecture can result in high capacitance at the channel side and can cause a substantial potential drop at the gate/electrolyte interface. Generally, there should be a potential drop at the gate capacitor, and thus, a subthreshold slope equal to the theoretical limit is not possible with electrolyte gating. However, the present device demonstrates a reproducible sub-thermionic transport. The electrical performance of the MIMSFET devices, either in terms of the steep slope subthreshold behaviour or in relation to the high ON current and transconductance values, are found to be largely comparable when processed (the a-IZO channel) at either 350 °C or 400 °C.

[99] FIG. 5A illustrates exemplary transfer characteristics of 14 MIMS-FET devices (a-IZO annealed at 350 °C).

[100] FIG. 5B illustrates exemplary gate voltage - gate current plots of 4 MIMS-FETs.

[101] FIG. 5C illustrates an exemplary probe voltage (measuring the bulk electrolyte potential) placed in between the gate and the channel showing a sharp rise with $\frac{\partial V_P}{\partial V_{GS}}$ reaching a value greater than 3.

[102] FIG. 5D illustrates an exemplary transition and signal gain of printed transistor-resistor ($\sim 1 \text{ M}\Omega$) inverter with one MIMSFET.

[103] FIG. 5E illustrates an exemplary typical transfer characteristic of the printed MIMS FET device, where the a-IZO layer has been annealed at 350 °C, showing the specific drain current and transconductance variation over the entire applied gate voltages.

[104] FIG. 5F illustrates exemplary transfer characteristic and drain voltage-drain current characteristic of the MIMS-FET device ($V_D = 0.5 \text{ V}$).

[105] FIG. 5G illustrates exemplary transfer characteristic along with transconductance with respect to applied gate voltages, plotted for MIMS-FETs, where, the a-IZO layer annealed at 300, 350 and 400 °C.

[106] FIG. 5H illustrates exemplary MIMSFET performance with respect to the thickness of the printed channel layer.

[107] In an exemplary implementation, a device is processed at 350 °C. FIG. 5A illustrates an exemplary comparison of transfer characteristics of 14 MIMSFET devices, showing slight variations in OFF-currents, ON-currents, V_T and SS values, which again relates to the printing accuracy of the silver layer and the electrolytic insulator. FIG. 5B illustrates the corresponding I_G vs. V_{GS} plots for the group of MIMSFET devices whose transfer curves are plotted in FIG. 5A. The I_G decreases sharply at the same V_{GS} values, where the onset of the sub-thermionic transport can be noted. Here, the static negative capacitance behaviour, as evident from the sharp fall of the gate currents, has an electrochemical origin. As has earlier been mentioned, the applied gate potential in an electrolyte gated MOSFET gets split among the gate/ electrolyte and electrolyte/channel capacitors, where the potential drop at each of these capacitors is inversely proportional to their capacitance values. Additionally, the high specific capacitance of the silver layer compensates for the bigger surface area of the gate electrode and results in comparable gate and channel capacitance.

[108] A reversible passivation of the silver layer can take place around $V_{GS} = 1.5$ V, resulting in the disappearance of large C_{DL} of the silver layer. Consequently, the capacitance share, and the voltage split at the respective electrodes change abruptly; the channel capacitance becomes smaller than the gate capacitance, thereby causing the gate current to fall sharply. It can be noted that with disappearance of the silver layer, the I_G does not drop to zero, which can be due to the presence of the a-IZO at both edges of silver layer and the overlay capacitance of the ITO passives. While the size of the printed Ag layer largely controls the initial potential share at each electrode and the applied gate voltage value at which the passivation can take place, the overlay capacitance coming from the ITO passives determines the remaining capacitance at the channel side and the degree of the negative capacitance effect, i.e., the lowest possible SS value that can be achieved. With a minimal overlay capacitance of ITO passive, it can be possible to witness a complete insulator-metal transition within a very narrow V_{GS} value. This also explains the little variation in the transfer curves observed in terms of V_T and SS values originating from the variation in the size of the printed Ag-layer and the electrolyte coverage of the ITO passives, respectively. It can be inferred that the effect is due to the silver layer passivation, as the negative capacitance effect can also be observed without the a-IZO channel in place.

[109] In another embodiment, the passivation of the Ag-electrode shows a de-passivation phenomenon as well at the reverse cycle, resulting in transfer curves with negligible hysteresis. A further demonstration of the negative capacitance effect can be by introducing a probe electrode in between the gate and the channel. The idea is to probe the bulk electrolyte potential (V_{BE}) between the respective capacitors. The probe voltage (V_P) is recorded at the time of a standard gate sweep.

[110] FIG. 5C illustrates the $\frac{\partial V_P}{\partial V_{GS}}$ with respect to applied V_{GS} . As has been stated before, irrespective of the large area of the gate electrode designed, there is present a fraction of the applied potential drop at the gate/ electrolyte interface, and consequently, for regular MOSFET devices, the $\frac{\partial V_P}{\partial V_{GS}}$ value is less than 1, i.e., ∂V_P is less than ∂V_{GS} .

[111] However, here we observe a sharp rise in $\frac{\partial V_P}{\partial V_{GS}}$ at around an identical voltage value corresponding to the onset of the negative capacitance and it reaches a maximum value greater than 3. By exploiting the steep slope transfer curves, a fully printed inverter based on transistor-resistor (TR) logic is achieved with a signal gain of around 23. Here again, the negative capacitance can be seen to overlap with the sharp transition; the input current (I_{IN}) is actually the gate current of the pull-down transistor of the TR logic. This indicates that the present concept can be a suitable approach to achieve printed steep slope FETs, and with a more precise control over the printing process, it can result in a printed metal-insulator transition device that shows drive current variation by many orders of magnitude.

[112] FIG. 5E illustrates an exemplary re-plot for one of the devices as shown in FIG. 5A to clearly mark different transport regimes, followed by the sub-thermionic transport. A strong thermionic transport regime can be noted, which can result in an absolute drain current value of around 5 mA for a supply voltage of $V_{DS}=0.5$ V. ON-state currents in excess of 200 $\mu A/\mu m$ and specific transconductance values in excess of 200 $\mu S/\mu m$ can be observed for devices fabricated at process temperature of either 350 or 400 °C.

[113] In another embodiment, the values of ON-state current and transconductance can be increased to up to 1 mA/ μm and 1 mS/ μm respectively by optimising different parameters.

[114] FIGs. 6A – 6C illustrate exemplary transfer characteristics of a printed 2D semiconductor channel MIMSFET, in accordance with an embodiment of the present disclosure.

[115] It can be observed that the printed MIMSFET exhibit high performance – a large ON/OFF ratio ($> 10^7$), a low sub-threshold swing (about 17mV/dec) and maximum ON-current ($I_{D,ON}$) noted is 310 $\mu\text{A}/\mu\text{m}$). It would be appreciated that performance parameters can be bettered with further optimisation of the device.

[116] The exemplary MIMSFET device illustrated is an n-type metal oxide semiconductor (NMOS) device. It would further be appreciated that a similar methodology can be employed to develop a p-type metal oxide semiconductor (PMOS) MIMSFET or using other p-type semiconductor materials. Here, again NC-effect or subthermionic transport may not be prevalent; however, high values of ON currents can be anticipated, for the PMOS devices as well.

[117] The printed MIMSFET device can be implemented to enable a fully printed 2D semiconductor based complementary metal oxide semiconductor (CMOS) platform.

[118] The printed MIMSFET device of the present disclosure can be implemented in a circuit. The high ON current and high power output of the FETs can enable the circuit to have high ON current and high power output characteristics. Further, due to low values of subthreshold swing, the FETs demonstrate high frequency switching, which can enable the circuit to have high frequency switching characteristics by selectively switching any of one or more FETs in the circuit.

[119] The circuits formed using the proposed FETs with NC effect can be implemented for low voltage operation, steep slope, high gain applications. These circuits can be applied to printed electronics along with sensors to amplify low response sensor signals. Further, as the circuits can be operated at high frequencies, the circuit can be applied to display backplanes, radio frequency identification tags (RFID) and high load applications such as alongside actuators and speakers.

Methods and Materials

[120] The following section describes the method and materials used for fabrication of the exemplary embodiment as described in the above section. The method and materials may not be construed as a limitation for the fabrication of the device, as can be appreciated by those skilled in the art.

[121] In an embodiment, the printable precursor solution of a-IZO can be prepared by dissolving indium (III) nitrate hydrate ($[\text{In}(\text{NO}_3)_3 \cdot x\text{H}_2\text{O}]$) and zinc acetate ($[\text{Zn}(\text{CH}_3\text{COO})_2]$) in 2-methoxyethanol ($[\text{CH}_3\text{OCH}_2\text{CH}_2\text{OH}]$) and polyethylene glycol (PEG, $(\text{C}_3\text{H}_8\text{O}_2)_n$). The

In- and Zn- precursors can be taken such that an In: Zn atomic ratio of 70:30 is maintained. To improve the printing experience and to obtain superior spatial homogeneity of the printed semiconductor layers, polyethylene glycol can be added under continuous stirring to obtain a 2-methoxyethanol: PEG volume ratio of 70:30. The final solution is stirred for about 1 hour to obtain a homogeneous printable ink. In another embodiment, the molarity of the precursor solution is maintained at 0.1 M.

[122] In another embodiment, the composite solid polymer electrolyte (CSPE) can be comprised of a synthetic polymer, poly(vinyl alcohol) (PVA); a plasticizer, propylene carbonate (PC); a solvent, dimethyl sulfoxide (DMSO); and supporting electrolyte/salt lithium perchlorate (LiClO_4). An amount 0.3 g of PVA is dissolved in 6 g of DMSO and stirred at about 90 °C for about 1 hour; at the same time, 0.07 g of LiClO_4 is dissolved in 0.63 g of PC at room temperature. Finally, both the solutions are mixed together at room temperature and stirred for about 24 hours to obtain a completely homogeneous printable composite solid polymer electrolyte solution.

[123] In another embodiment, the prepared homogenous printable inks (semiconductor and electrolytic insulator) are filtered through 0.2 μm hydrophilic, regenerated cellulose (RC) syringe filters in order to ensure easy printability. The filtered inks are printed using a desktop inkjet printer at room temperature; the semiconductor ink printing is followed by a post-annealing treatment at either 300 °C, 350 °C or 400 °C for about 1 hour.

[124] In another embodiment, the structural characterization of the a-IZO films is carried out using a grazing incidence X-ray diffractometer machine with $\text{CuK}_{\alpha 1}$ radiation as source (45 kV, 100 mA) with a constant grazing incidence angle of 0.5°. The morphological characterization of the printed films is carried out using an atomic force microscope in tapping mode. The print profiles are characterized using a stylus profilometer (tip radius-12.5 μm , load-3 mg). Transmission electron microscopy (TEM) samples are prepared on 30 nm free-standing silicon nitride TEM grids and characterized using a microscope attached with an EDS detector for super-fast elemental mapping analysis and triple dark-field and bright-field detectors for simultaneous scanning transmission electron microscopy (STEM) imaging.

[125] In another embodiment, high quality, commercially available ITO coated float glass (180 nm, <10 Ω sheet resistance) is used for the device fabrication. The ITO layer is lithographically structured to define the passive electrodes (source, drain and in-plane gate). The channel width (W) and length (L) of the FETs are maintained at 60 μm and 40 μm , respectively. Initially, a set of a-IZO channel in-plane FETs are fabricated and characterized,

followed by multiple batches of devices with the MIMSFET structure with an additional printed Ag-layer on top of the annealed a-IZO. Here, the annealing temperature can be varied between 300 °C, 350 °C and 400 °C for a-IZO layer and the printed commercial silver layer is heated at 250 °C, for about 30 minutes, to ensure high conductivity. Finally, the CSPE layer is printed and allowed to dry at room temperature.

[126] In another embodiment, Inkjet printable MoS₂ nano ink can be prepared using a liquid phase exfoliation (LPE) methodology. Readily available MoS₂ particles are stirred in ethylene diamine for about 24 hours. The solution is then taken and centrifuged at about 8000 rpm for 10 minutes so that the EDA-adsorbed MoS₂ settles down. The sediment is washed with di-methyl formamide twice before sonicating it for 2 hours in a 100 W bath sonicator. The size selection of nano-dispersed sheets is done by centrifugation at different speeds. Firstly, it is rotated at 1000 rpm for 1 hour, to settle down the un-exfoliated flakes. Next, centrifugation is done at 2000 rpm and the sediment is collected to be used as the ink for printing.

[127] Sputtered tin doped indium oxide (ITO) film coated high quality float glass is used as a substrate, where the lithographically defined ITO lines serve as source and drain electrodes. Optical lithography followed by wet etching in HCl is used for the passive element structuring. Only one pass (one layer) of MoS₂ (semiconductor) ink is printed at the channel region, followed by printing of one layer of commercial silver nanoparticle ink, which is printed on the top of semiconductor layer. The silver printed silver layer is wider than the channel length, however, shorter than the width of the printed MoS₂ layer in order to avoid a physical/ electrical short with the ITO passives beneath. This follows annealing at 200 °C. Next, multiple layer of electrolyte is printed above the semiconductor and silver layer followed by printing of PEDOT:PSS on top the printed electrolyte layer as the top gate electrode.

[128] In another embodiment, the electrical measurements are carried out at room temperature at ambient conditions.

[129] While the foregoing describes various embodiments of the invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof. The scope of the invention is determined by the claims that follow. The invention is not limited to the described embodiments, versions or examples, which are included to enable a person having ordinary skill in the art to make and use the invention when combined with information and knowledge available to the person having ordinary skill in the art.

ADVANTAGES OF THE INVENTION

[130] The present invention provides a high-ON-current/ power field effect transistor (FET) and a circuit using said FET.

[131] The present invention provides a solution processed/ printed FET with high-ON-current/ power.

[132] The present invention provides an FET with a stable and static negative capacitance effect.

[133] The present invention provides an FET with a low sub-threshold swing, lower than Boltzmann limit.

[134] The present invention provides an FET with high ON-current characteristics.

[135] The present invention provides a solution processed/ printed FET whose channel lengths are lower than FET printed using commercial/ industrial printers.

[136] The present invention provides a high frequency/ high switching speed FET and a circuit using said short channel FET.

We claim:**1.** A field-effect transistor (FET) comprising:

a channel layer made of a semiconductor material and disposed in a channel region defined by a source and a drain of the FET;

a conducting layer coupled to the channel layer, the conducting layer having a length greater than the channel region defined by the source and the drain of the FET and lesser than the semiconducting channel layer to enable a low resistance path being formed for electronic transport and an effective reduction in the channel layer length; and

an insulator layer provided between a gate of the FET and the channel layer such that an exposed portion of the channel layer between the source and the drain of the FET is in contact with the insulator layer, wherein, the conducting layer allows charge transport through the channel layer only at the exposed portion of the channel layer near the source and the drain to enable short (narrow) channel FET, thereby resulting in a high ON current and high power of the FET device.

- 2.** The FET as claimed in claim 1, wherein the channel layer is deposited on the substrate and the conducting layer is deposited atop the channel layer.
- 3.** The FET as claimed in claim 2, wherein a second semiconductor layer is deposited atop the conducting layer.
- 4.** The FET as claimed in claim 1, wherein the conducting layer is deposited on the substrate with the channel layer deposited atop the conducting layer.
- 5.** The FET as claimed in claim 1, wherein the conducting layer is provided in such a way that there is no direct contact between the conducting layer and neither of the source and the drain electrodes.
- 6.** The FET as claimed in claim 1, wherein the insulator layer of the FET is an electrolyte, and wherein a negative capacitance (NC) effect and subthermionic transport with subthreshold slope below the Boltzmann limit is demonstrated in said FET.
- 7.** The FET as claimed in claim 1, wherein the FET is fabricated by solution processing or printing methods.
- 8.** The FET as claimed in claim 1, wherein the insulator layer is made of a material selected from a group comprising an electrolytic insulator such as a solid polymer

electrolyte, a liquid electrolyte and an ion-gel; an oxide dielectric such as SiO_2 , Al_2O_3 , HfO_2 and TiO_2 ; an organic dielectric such as PVA and PMMA; an inorganic ferroelectric such as BTO and PZT; an organic ferroelectric such as PVDF-TrFE; and a combination thereof.

9. The FET as claimed in claim 1, wherein the semiconductor of the channel layer is selected from a group comprising amorphous oxides, crystalline oxides, oxide nanoparticles, nanowires, organic semiconductors, 2D semiconductors of transition metal dichalcogenides, Mxenes and other suitable inorganic materials in a form of nanoparticles, nanowires and thin film and a combination thereof.
10. The FET as claimed in claim 1, wherein the semiconductor of the channel layer is made of phase change material that shows abrupt metal-insulator transition (MIT) behaviour, and is selected from a group comprising TiO_2 , VO_2 , other suitable materials and a combination thereof.
11. The FET as claimed in claim 1, wherein the conducting layer is formed of a material selected from a group comprising metals, such as gold, platinum, silver, copper; or carbon allotropes such as graphene, carbon nanotubes or organic material such as PEDOT:PSS or a mixture thereof.
12. The FET as claimed in claim 1, wherein the FET electrodes are made of a material from a group comprising a transparent conducting oxides such as indium tin oxide (ITO) and fluorine-doped tin oxide (FTO); a pure metal such as gold and platinum, silver, copper; a conducting organic material such as PEDOT:PSS; and a combination thereof.
13. The FET as claimed in claim 1, wherein the used substrate is any of a flexible substrate such as cellulose, paper and polymer; and a rigid substrate such as glass and silicon wafer.
14. The FET as claimed in claim 1, wherein the short channel, high power FETs would lead to higher switching frequency that is high frequency applications.

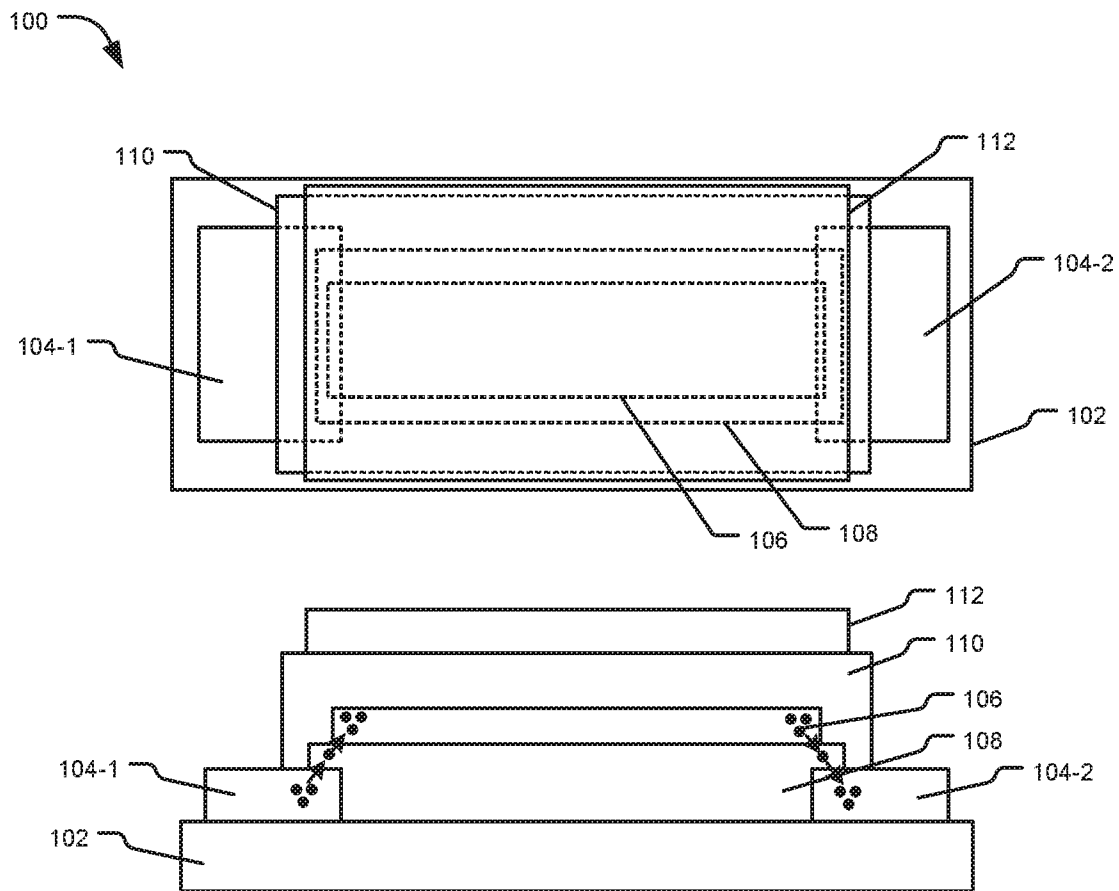


FIG. 1A

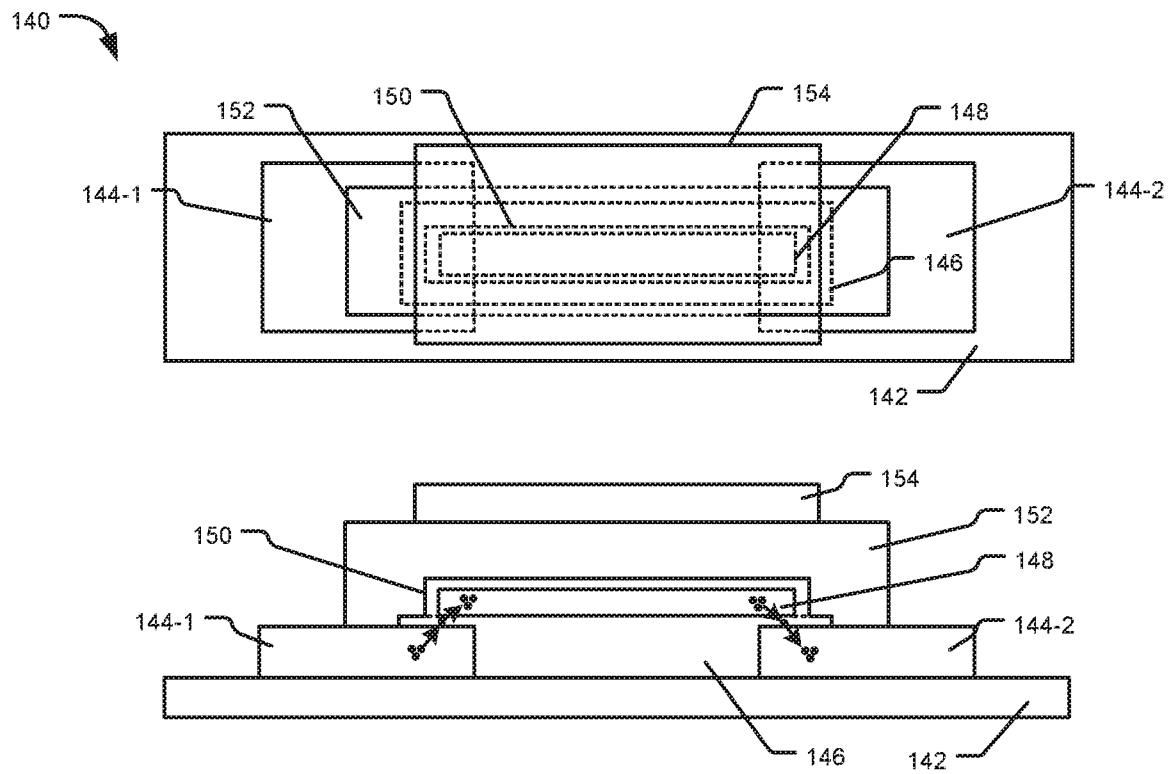


FIG. 1B

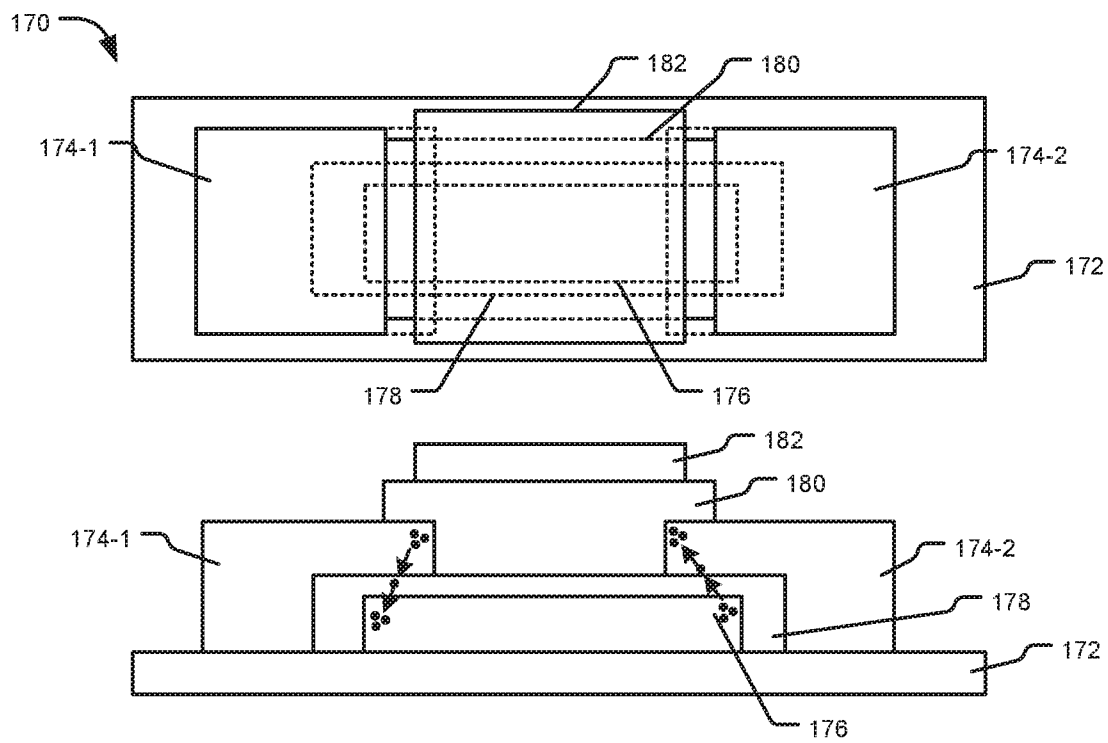


FIG. 1C

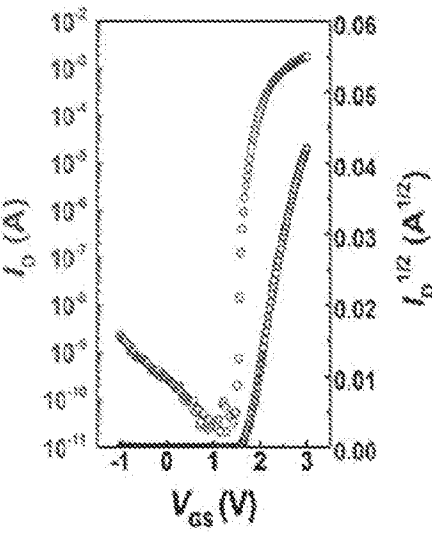


FIG. 2A

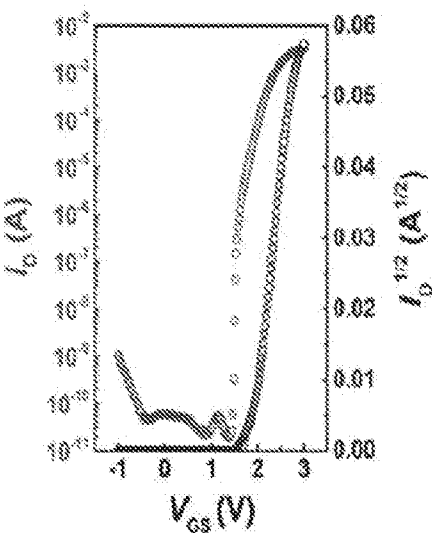


FIG. 2B

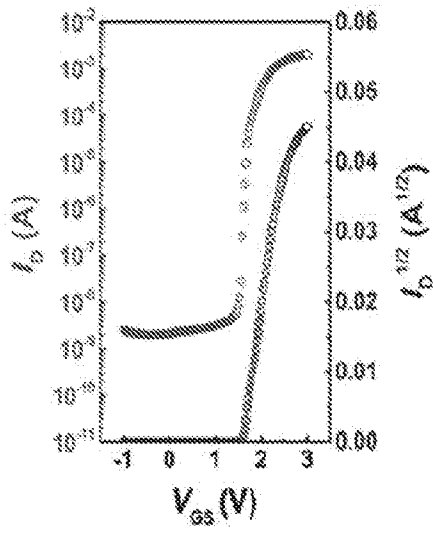


FIG. 2C

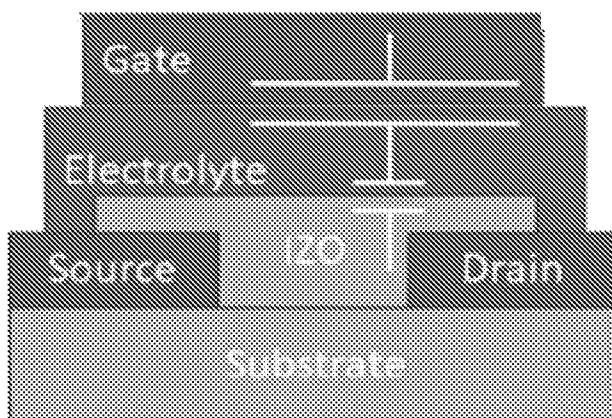


FIG. 3A

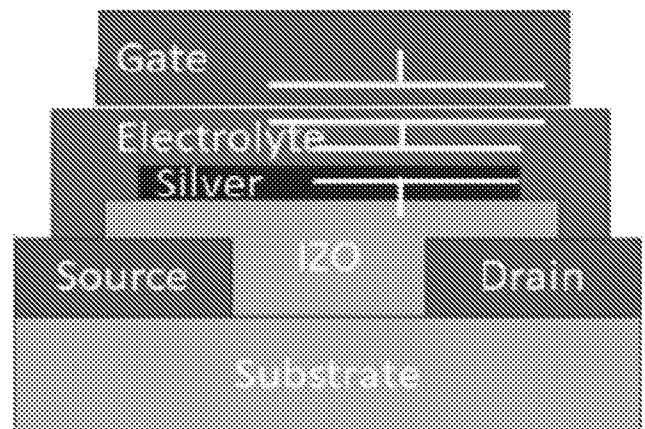


FIG. 3B

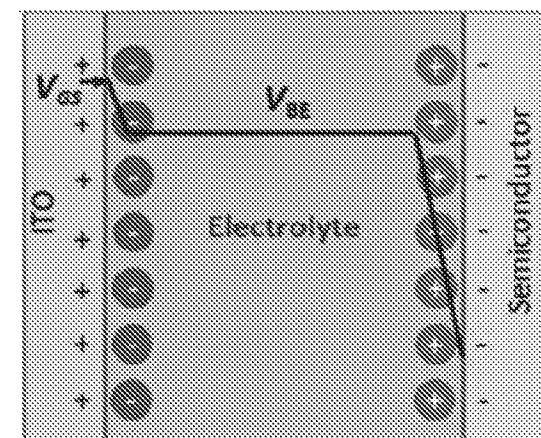


FIG. 3C

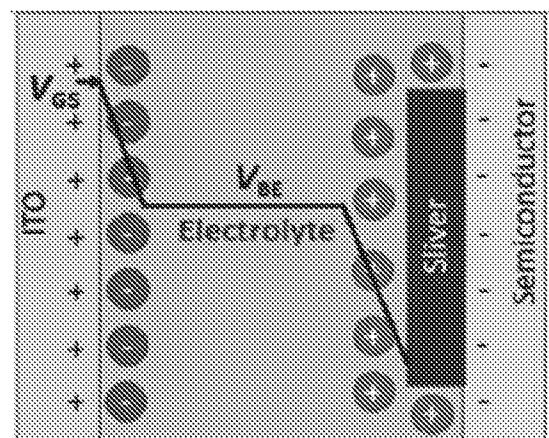


FIG. 3D

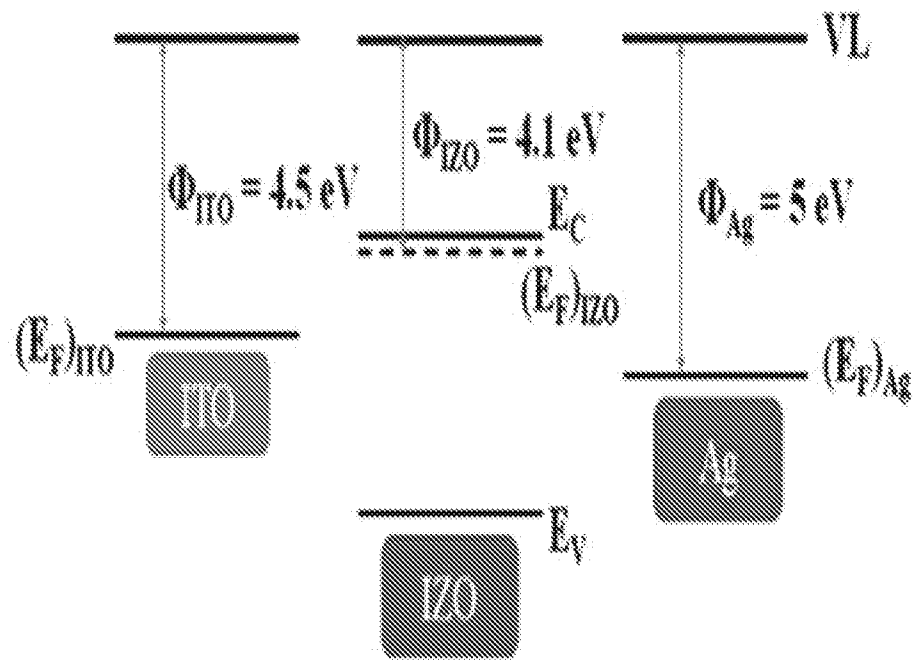


FIG. 4A

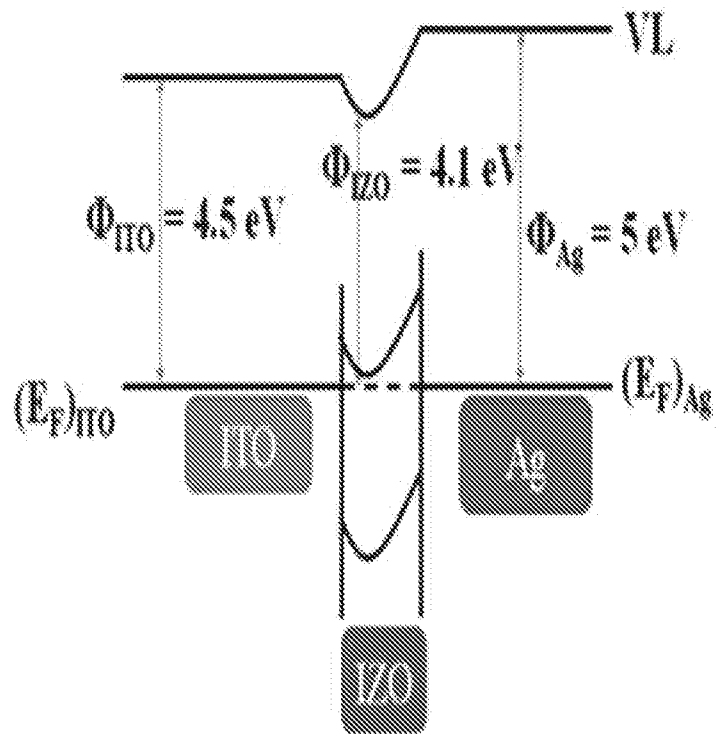


FIG. 4B

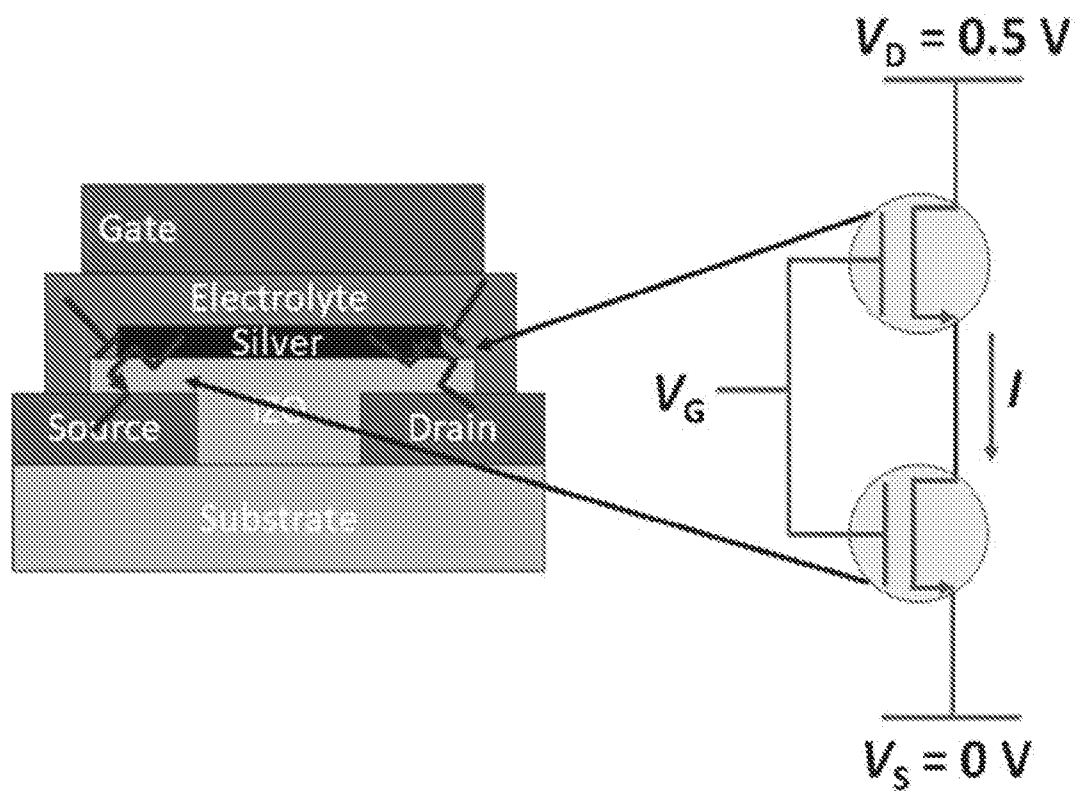


FIG. 4C

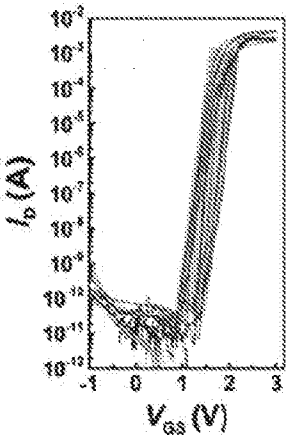


FIG. 5A

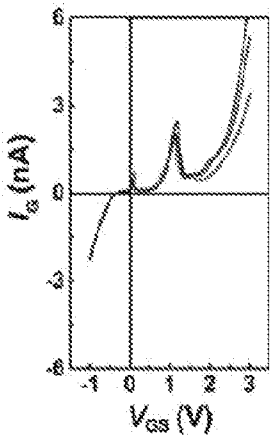


FIG. 5B

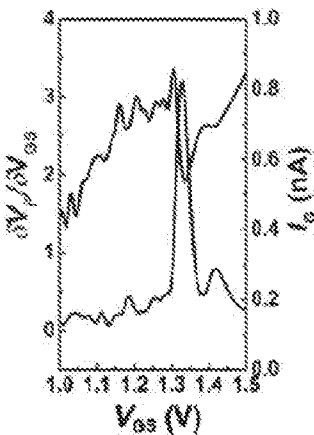


FIG. 5C

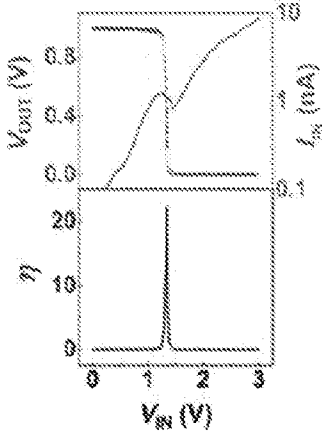


FIG. 5D

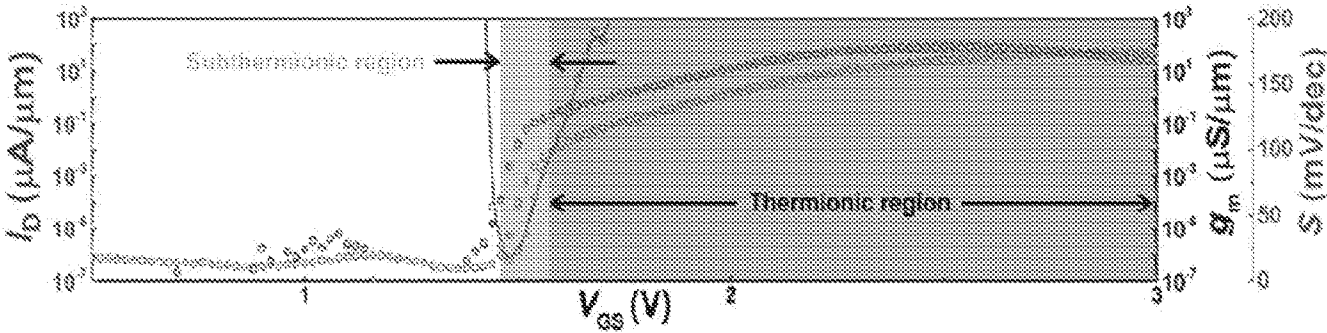


FIG. 5E

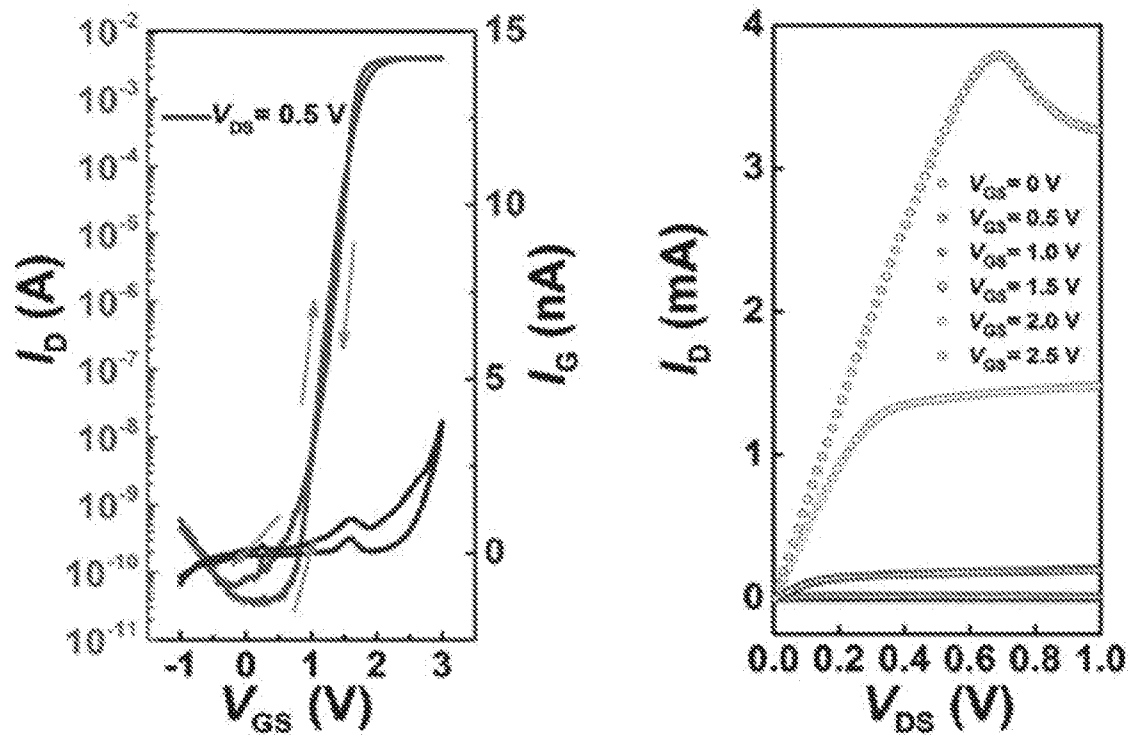


FIG. 5F

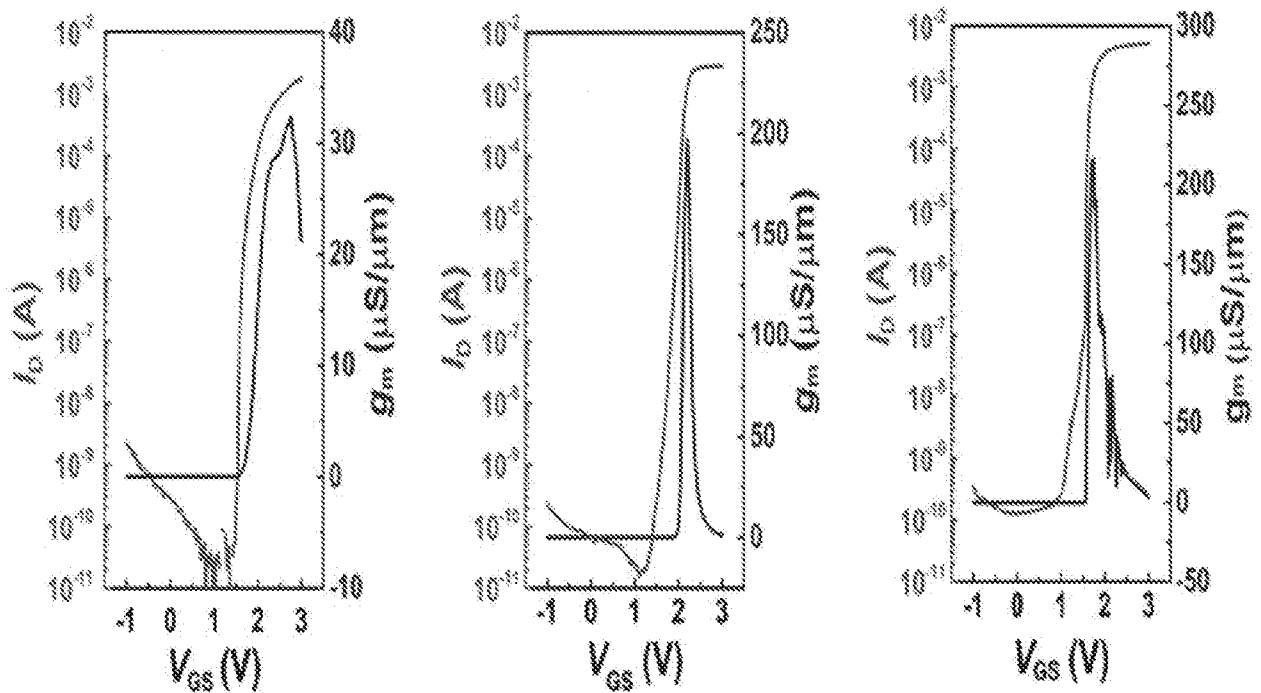


FIG. 5G

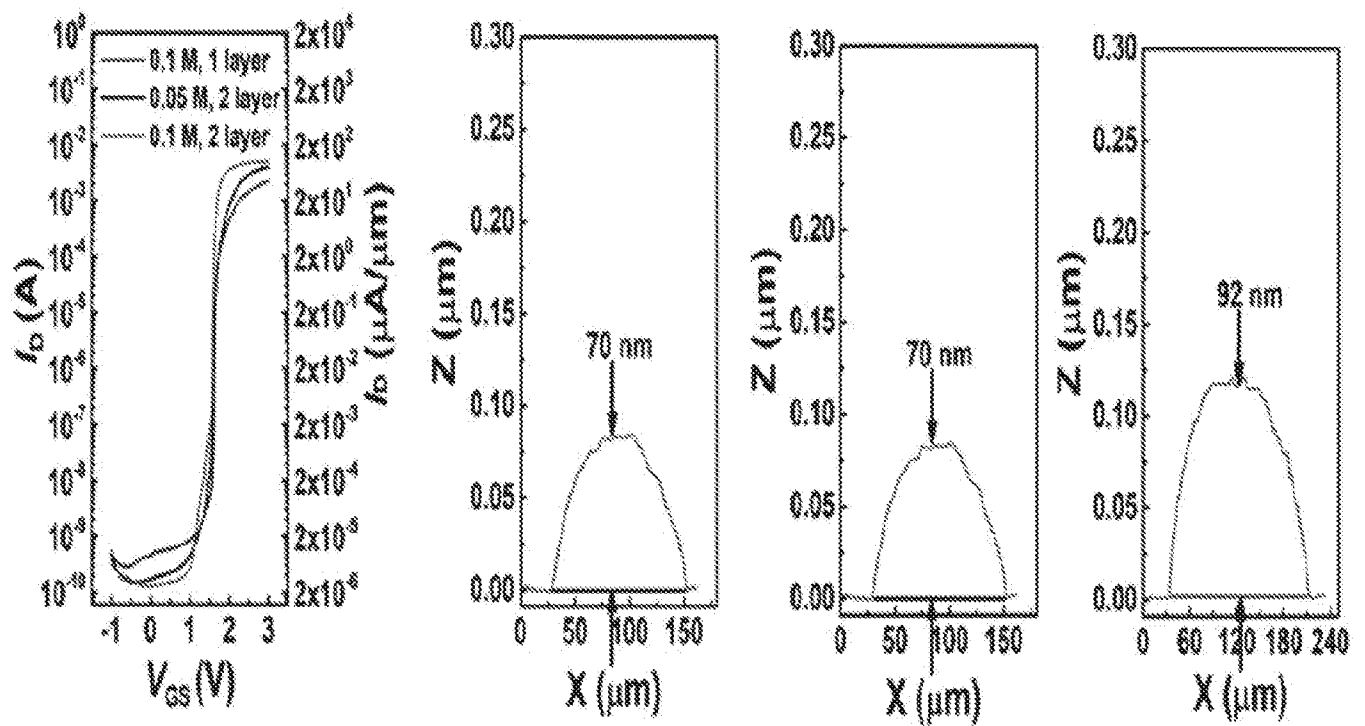


FIG. 5H

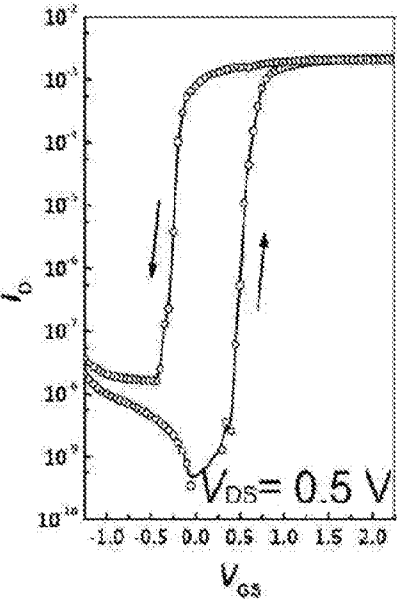


FIG. 6A

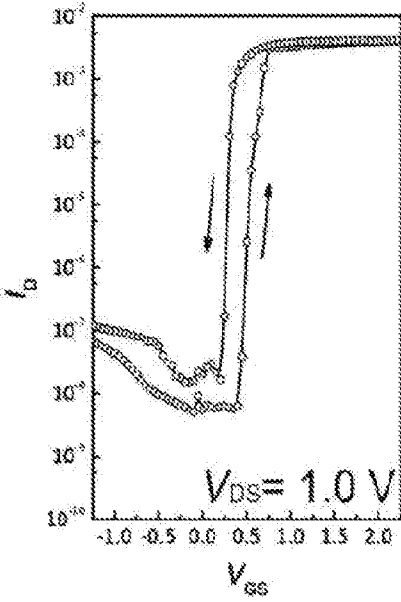


FIG. 6B

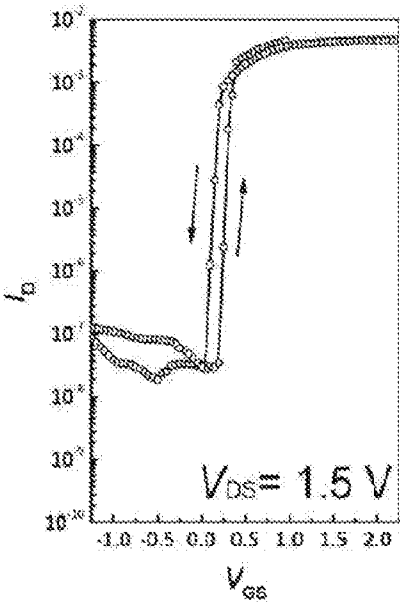


FIG. 6C

INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB2020/051360

A. CLASSIFICATION OF SUBJECT MATTER

H01L21/027, H01L29/06, H01L51/05 Version=2020.01

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Databases: TotalPatent One, IPO Internal Database

Keywords: FET, Conducting layer, Insulating layer, Electrolyte

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	Marques GC et.al. "Electrolyte-gated FETs based on oxide semiconductors: Fabrication and modeling" IEEE Transactions on Electron Devices; 64(1):279-85; 11 November 2016 (11-11-2016) *Abstract; Fig.1(a), (b); Pages 2-5*	1-14

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"E" earlier application or patent but published on or after the international filing date

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"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

07-07-2020

Date of mailing of the international search report

07-07-2020

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