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SUBSTITUTE FOR MISSING XR

- [54] PLURAL TRANSCEIVER ALARM SYSTEM
USING CODED ALARM MESSAGE AND
EVERY STATION DISPLAY OF ALARM
ORIGIN
- | | | | |
|-----------|--------|----------|-----------|
| 3,689,888 | 9/1972 | Wootton | 340/224 |
| 3,693,155 | 9/1972 | Crafton | 340/310 R |
| 3,713,142 | 1/1973 | Getchell | 340/164 R |

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Emhardt & Naughton

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- [21] Appl. No.: 393,343

- [52] U.S. Cl. 340/412; 340/224; 325/143

- [51] Int. Cl. G08b 23/00

- [58] Field of Search..... 340/224, 164 R, 207, 183,
340/150, 412, 413; 343/203; 325/143

- [56] References Cited

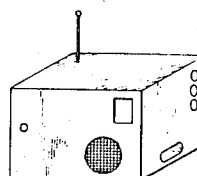
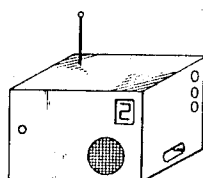
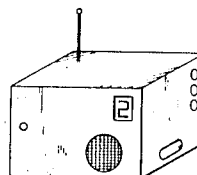
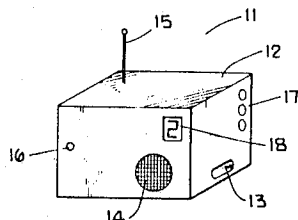
UNITED STATES PATENTS

- 3,629,837 12/1971 Fraunfelder 340/224

[57] ABSTRACT

An alarm system to detect emergency conditions, such as unauthorized intrusion or fire, comprising a plurality of individual alarm units remote from one another. Each unit includes a radio transmitter for transmitting a coded signal unique to that unit when an emergency condition is detected. Each unit also includes a radio receiver and decoder for receiving coded signals from any other alarm unit in the system and for determining which other alarm unit is transmitting.

20 Claims, 6 Drawing Figures



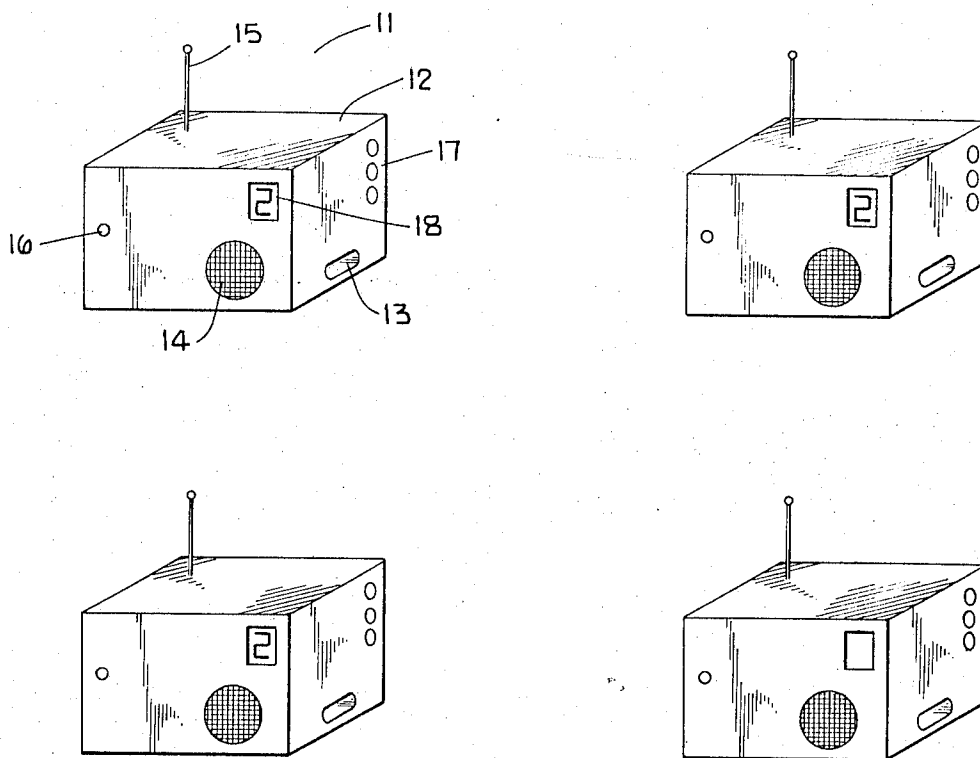


Fig. 1

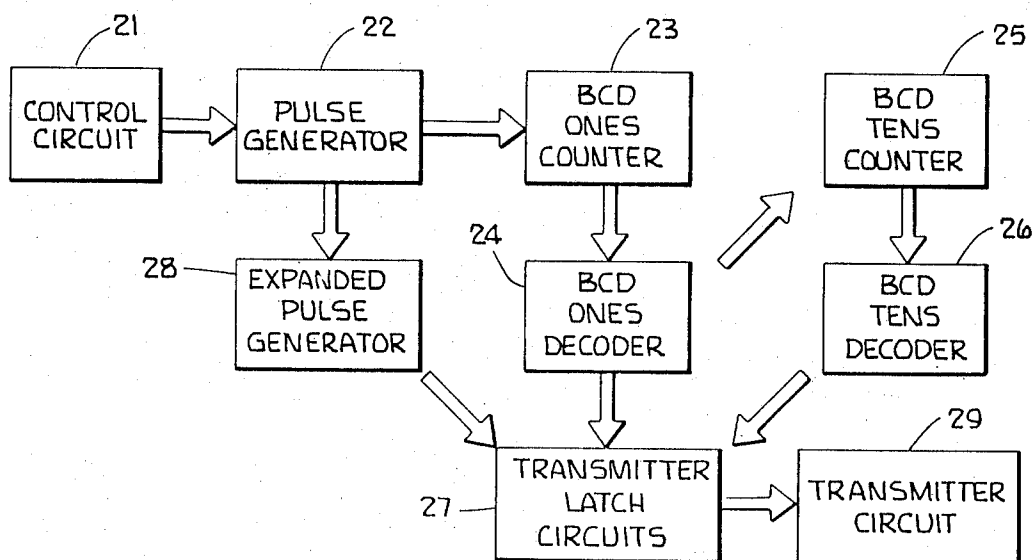


Fig. 2

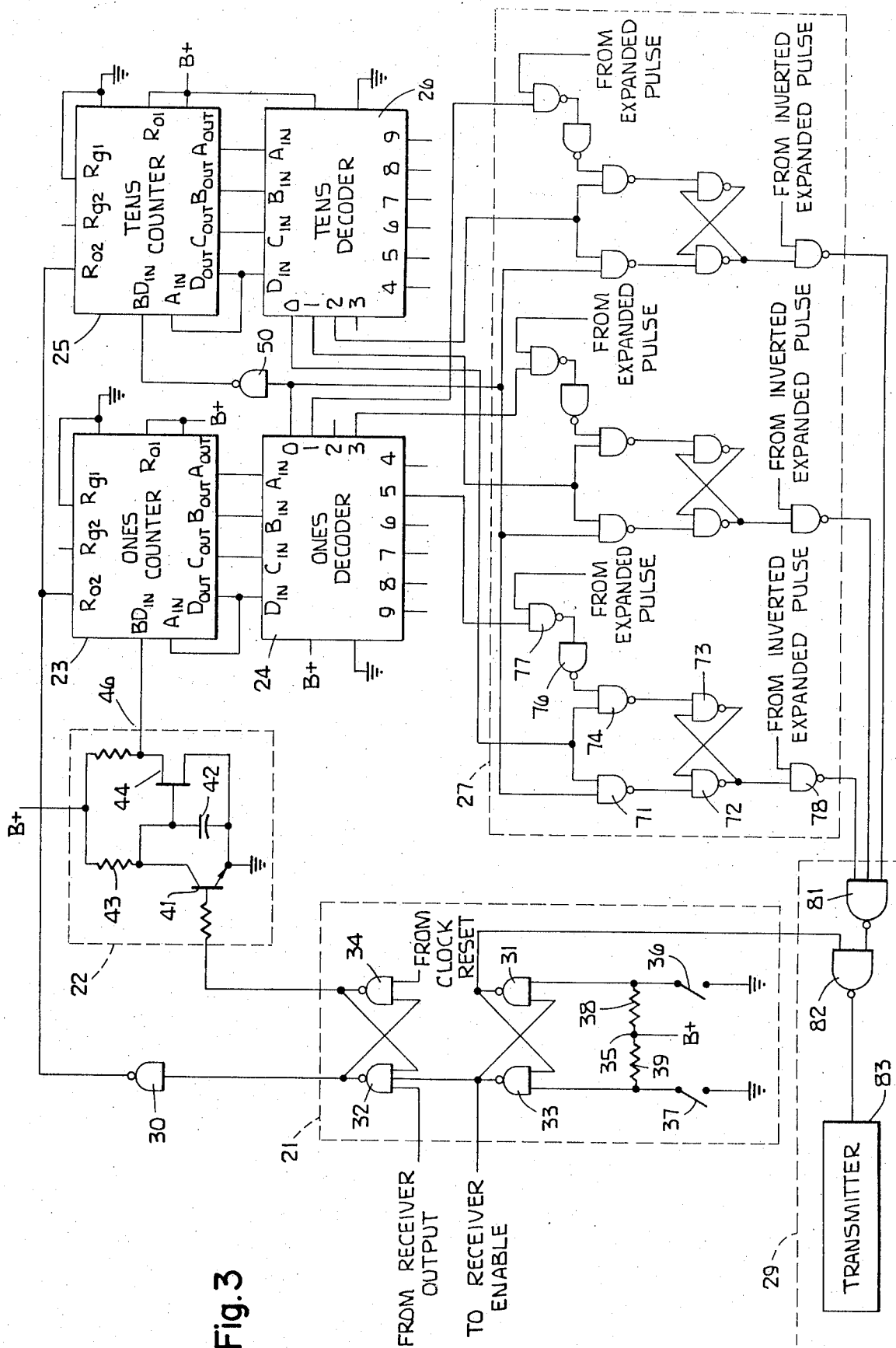


Fig. 3

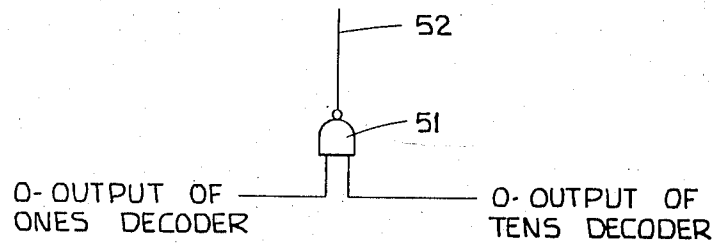


Fig. 4

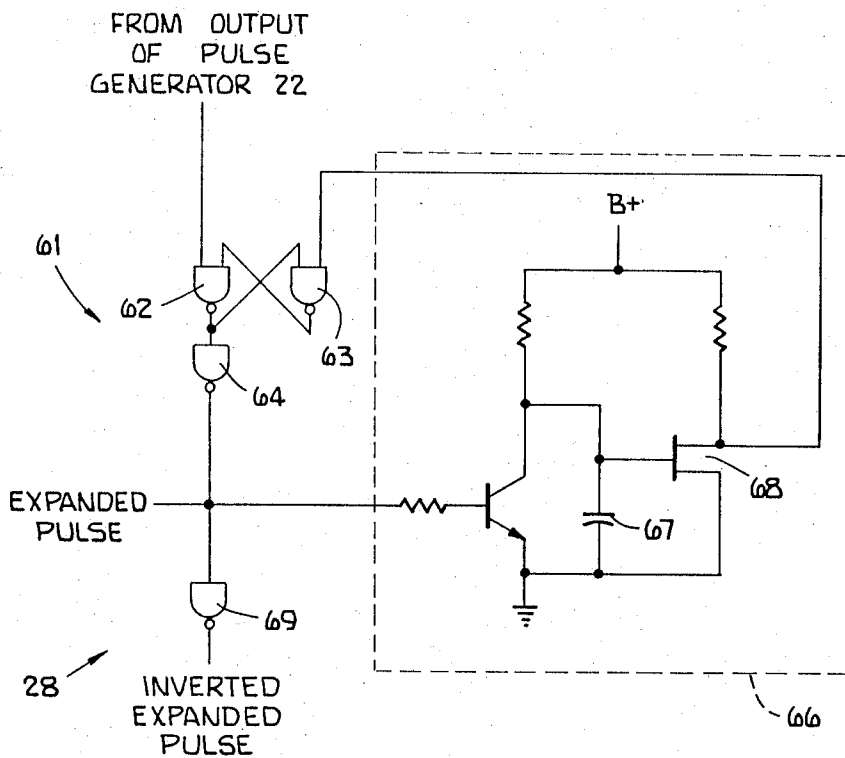
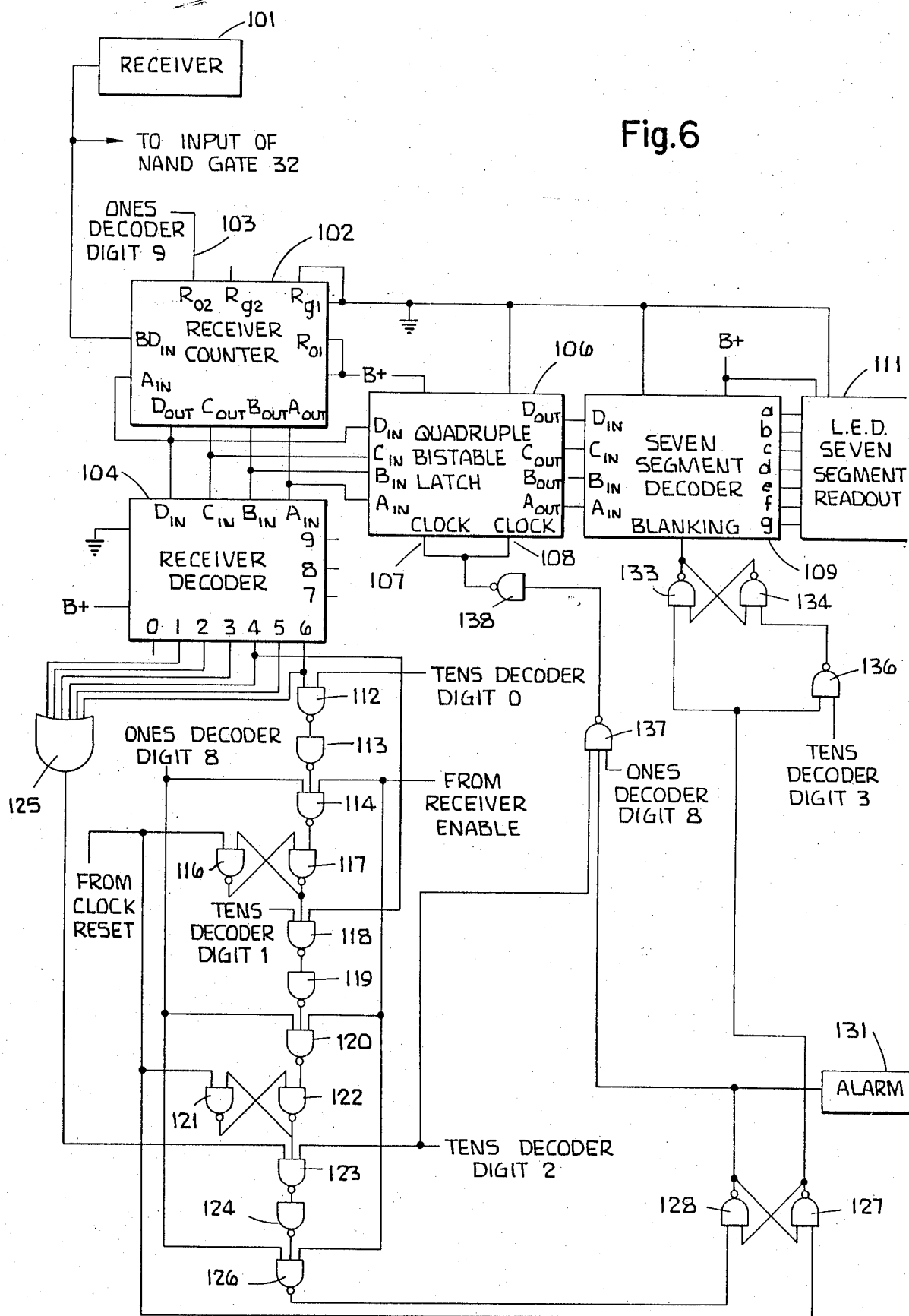


Fig. 5

Fig. 6



PLURAL TRANSCEIVER ALARM SYSTEM USING CODED ALARM MESSAGE AND EVERY STATION DISPLAY OF ALARM ORIGIN

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to electrical communication systems automatically responsive to conditions.

2. Description of the Prior Art

Alarm systems for protection against burglary or fire are known which employ a radio transmitter on the premises to be protected. When an intrusion trip switch is closed, for example, the transmitter sends a signal to a central receiving station, which is equipped to receive signals from many alarm transmitters, and assistance is dispatched to the premises either by or through the personnel at the central receiving station. Such a system is shown in U.S. Pat. No. 2,899,674 to Sierer. These systems have the disadvantage that assistance is often sent to the premises to be protected from a considerable distance away, and damage done by a fire or goods taken by an intruder can be substantial before assistance arrives. Also, one receiving station is depended upon, and any difficulty at that station can result in no assistance whatsoever being dispatched.

An alarm system wherein a plurality of alarm units is distributed among homes in a neighborhood is shown in U.S. Pat. No. 3,133,276 to Miller. The system disclosed therein, however, utilizes wires to connect the units together, which is impractical in all cases and impossible where the homes to be protected are located any distance apart. The system disclosed provides for each unit to receive an alarm signal from any unit detecting an emergency condition.

SUMMARY OF THE INVENTION

One embodiment of the present invention is an alarm system comprising a plurality of alarm units remote from one another with each alarm unit comprising sensing means for detecting an emergency condition, coding means coupled to the sensing means for producing a coded electrical signal unique to the alarm unit when the sensing means detects an emergency condition, a radio transmitter coupled to the coding means for transmitting a coded radio frequency signal which contains the information in the coded electrical signal, a radio receiver for receiving other coded radio frequency signals from other of the plurality of alarm units in the alarm system, decoding means coupled to the radio receiver for decoding the received radio frequency signals, and display means coupled to the decoding means for indicating the specific decoded radio frequency signals received.

An object of the present invention is to provide an alarm system wherein alarm units in the system are placed on different premises to be protected and each unit serves as an alarm receiver as well as an alarm transmitter without physical connections between the units.

Another object of the present invention is to provide an alarm system comprising a plurality of alarm units each of which is operable to transmit and receive uniquely coded alarm signals.

Related objects and advantages of the present invention will be apparent from the following detailed descriptions.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a perspective view of a plurality of alarm units in accordance with the present invention.

FIG. 2 is a simplified block diagram of the transmitter section of one of the alarm units of FIG. 1.

FIG. 3 is a schematic diagram of the transmitter section of one of the alarm units of FIG. 1.

FIG. 4 shows the clock reset pulse generator for one of the alarm units of FIG. 1.

FIG. 5 shows the expanded pulse generator of one of the alarm units of FIG. 1.

FIG. 6 is a schematic diagram of the receiver section of one of the alarm units of FIG. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENT

For the purposes of promoting an understanding of the principles of the invention, reference will now be made to the embodiment illustrated in the drawings and specific language will be used to describe the same. It will nevertheless be understood that no limitation of the scope of the invention is thereby intended, such alterations and further modifications in the illustrated device, and such further applications of the principles of the invention as illustrated therein being contemplated as would normally occur to one skilled in the art to which the invention relates.

Referring in particular to FIG. 1, there are illustrated a plurality of alarm units in an alarm system in accordance with the present invention. Alarm unit 11 is typical of the units in the system and comprises a case 12 and internal circuitry (not shown). Connector 13 is supplied for a power-supply input, and the unit may additionally contain internal power sources such as batteries. Audio alarm 14 is provided as well as antenna 15 and manual reset switch 16. Connectors 17 are provided for attaching external trip switches. Light-emitting diode readout panel 18 is provided to display the identity of a unit in the system transmitting an alarm signal.

The circuitry for the alarm units is in two sections; a transmitter section and a receiver section, although parts of the transmitter section operate in aid of the receiver section when an alarm unit is receiving. It is contemplated that, for example, four or five alarm units would be deployed as an alarm system with each unit being placed in a residence. An intrusion trip-switch or fire sensor would be attached to an alarm unit such as 11 at one of its connectors such as 17, and if the switch or sensor were tripped the alarm unit would transmit a coded alarm signal to each other unit in the system. Each receiving alarm unit would decode the received signal, sound an audio alarm, and display the identifying digit of the transmitting alarm unit.

FIG. 2 shows a simplified block diagram of the transmitter section of one of the alarm units of FIG. 1. Control circuit 21 may include the tripping mechanism which initiates transmission of an alarm signal or the trip switch may be connected externally. Control circuit 21 activates pulse generator 22 to produce a series of pulses which are coupled to binary coded decimal (BCD) ones counter 23. Ones counter 23 counts through each set of ten pulses from pulse generator 22 and provides a binary signal to ones decoder 24 reflecting that count. Each ten count shall be referred to as a base time interval herein. Every tenth pulse into ones

counter 23 advances tens counter 25 and tens decoder 26.

The transmitter latch circuits 27 take a preselected set of code digits from ones decoder 24. Each digit is in a different base time interval as controlled by an input from tens decoder 26. The transmitter latch circuits 27 also utilize a series of expanded pulses from expanded pulse generator 28 which are initiated by pulse generator 22 but are longer in duration. The transmitter latch circuits 27 provide an appropriately-coded series of expanded pulses to the transmitter circuit 29 for transmission to other alarm units in the system.

FIG. 3 shows a schematic diagram of the transmitter section of one of the alarm units of FIG. 1. The control circuit 21 is shown as a dashed line portion of FIG. 3. In the control circuit manual reset switch 37 is normally open and may be closed momentarily to reset the control circuit when trip switch 36 is open. Trip switch 36 initiates transmission of an alarm signal when it is closed. Trip switch 36 may alternatively be two or more switches in series so that all but one may be manually closed, for example before leaving the home, and the remaining unclosed switch can detect intruders. An alternative trip switch or another trip switch in parallel with switch 36 may be used to detect fire or other emergency conditions. Trip switch 36 may be easily located remote from the alarm unit and connected by wires.

A positive potential (B+) of about five volts is applied at point 35 between resistors 38 and 39 and is the source voltage used throughout the alarm unit circuitry. This source voltage is preferably derived from AC line voltage, with a five volt battery-powered back-up supply, as in conventional power supply circuits.

Resistors 38 and 39 are provided for current limiting when switches 36 and 37 are closed. The operation of control circuit 21, beginning with the closing of trip switch 36, shall be explained. The NAND gates used herein are positive NAND gates, whose outputs are low only when all inputs are high.

When switch 36 is closed one input to NAND gate 31 goes low causing the output to go high. Thereupon both inputs to NAND gate 33 are high and its output goes low. The low output of NAND gate 33 is connected to an input of NAND gate 32 and latches gate 32's output high. It can be seen that whether trip switch 36 is now opened or remains closed, the output of NAND gate 31 will remain high, and the output of NAND gate 33 will remain low. The original condition of the terminals of NAND gates 31 and 33 is restored by momentarily closing reset switch 37. NAND gates 31 and 33 comprise a latch which serves as a sensing means for detecting an emergency condition as evidenced by a low input to NAND gate 31.

The output of NAND gate 31 serves as a transmitter-enable signal which shall be treated in detail in reference to the transmitter circuit 29. The output of NAND gate 33 serves as a receiver-enable signal which shall be treated in detail with regard to the receiver section of the alarm unit.

NAND gates 32 and 34 constitute a second latch in control circuit 21. The clock reset input to gate 34 is normally high and pulses low to reset the latch, analogous to manual reset switch 37. The generation of the clock reset pulse shall be explained infra.

When switch 36 is tripped, the output of NAND gate 33, which is one input of NAND gate 32 latches low,

while the other inputs to gate 32 are high. This causes the output of NAND gate 32 to go high and the output of NAND gate 34 to go low. These output conditions will persist until a low clock reset pulse at the input to gate 34 occurs or a high signal appears at each of the inputs to gate 32. The output of NAND gate 32 is connected to the reset terminals of the BCD counters as shall be explained. The output of NAND gate 34 is connected to the input of pulse generator 22, which is indicated within dashed lines in FIG. 3.

When the output of gate 34 goes low, for example, when trip switch 36 is closed, transistor 41 is biased off, and capacitor 42 charges through resistor 43. Capacitor 42 charges to a critical level, firing unijunction transistor 44 and sending the output 46 of the pulse generator low momentarily. Output 46 then returns high after pulsing low, and capacitor 42 recharges to initiate another pulse. These pulses are about five microseconds wide and separated by about one millisecond. The series of pulses at the output 46 of pulse generator 22 is connected to the input of the BCD ones counter 23. Ones counter 23 is a binary coded decimal counter such as a type N7490 integrated circuit from Signetics of Sunnyvale, California. The input to ones counter 23 is at the BD-in terminal, and the A-input of counter 23 is externally connected to the D output to provide a divide-by-ten count. Counter 23 has standard ground and power supply connections, and the reset terminals are connected as shown. The output of NAND gate 32 is normally low and the output of inverter 30 normally high. The output of inverter 30 serves as the reset signal for ones counter 23 and tens counter 25, and when it is high the counters are held at zero, or reset, position. When the latch consisting of NAND gates 32 and 34 changes state to activate pulse generator 22, the output of inverter 30 goes low and the counters 23 and 25 begin to count. When the clock reset pulse at the input to NAND gate 34 resets the latch, the counters naturally reset also.

The outputs of ones counter 23 are designated D, C, B, and A, and they have a weight of eight, four, two, and one respectively. These outputs contain a binary representation of the count from zero through nine of the pulses at the input to ones counter 23, and they are connected to a binary coded decimal (BCD) decoder 24 such as a type N7441 integrated circuit from Signetics. Decoder 24 has standard ground and power supply connections and also A, B, C, and D, inputs corresponding to the similarly designated outputs of counter 23. Decoder 24 has ten outputs, each corresponding to a digit from zero through nine. The latest count information from counter 23 is indicated by a positive pulse at the appropriate output terminal of counter 24.

Ones counter 23 receives the series of pulses from pulse generator 22, and decoder 24 makes available the decoded pulse count at its ten outputs for the transmitter latch circuits 27. The zero-count output from the ones decoder 24 is coupled to the input of tens counter 25 through an inverter 50. Tens counter 25 and tens decoder 26 are preferably the same type of integrated circuits as ones counter 23 and ones decoder 24; that is, a type N7490 and N7441, respectively. The tens counter 25 has an input from the ones decoder as stated and also has ground, power supply and reset connections identical to those of ones counter 23. The tens decoder 26 has A, B, C, and D inputs corresponding to the similarly lettered outputs from tens counter 25.

Tens decoder 26 also has outputs of zero through nine, indicating counts of 0, 10, 20 etc.

It can be seen that after alarm switch 36 is closed, and pulse generator 22 begins producing a series of pulses, the decoder outputs indicate the pulse count from zero through reset (which is 90). For example, after 24 pulses, the two output of the tens decoder and the four output of the ones decoder would be high, or have a positive pulse thereon, and all the other outputs of the decoders would be low.

The clock reset pulse mentioned in connection with the second latch in control circuit 21 is produced as shown by the NAND gate in FIG. 4. NAND gate 51 has an input from the zero output of the ones decoder 24 and the nine output of the tens decoder 26. Therefore, the output 52 of NAND gate 51, which is the clock reset pulse, will be normally high except at each count of ninety pulses from pulse generator 22.

FIG. 5 shows the expanded pulse generator 28 which produces an expanded pulse corresponding to each pulse produced by pulse generator 22. The width of the expanded pulses is approximately half of the period between the pulses produced by pulse generator 22. NAND gates 62 and 63 comprise a latch wherein a low input pulse from pulse generator 22 causes the output of NAND gate 62 to go high and the output of inverter 64 to go low. The portion of the circuit 66 within the dashed lines is similar to the normal pulse generator 22 with a larger capacitor 67 to lengthen the time required to fire unijunction transistor 68. The output of inverter 64, which is the output of the expanded pulse generator, remains low until the unijunction transistor fires causing one input to NAND gate 63 to go low and resetting the latch. Inverter 69 is connected at its input to the expanded pulse and produces at its output an inverted expanded pulse.

In FIG. 3, three latch circuits are indicated within the dashed lines as 27. Any number of these latches may be employed to code the transmitted signal, but the present embodiment preferably contains three transmitter latch circuits. The first latch allows a predetermined number of the first ten expanded pulses to reach transmitter circuit 29; the second latch allows a second predetermined number of the second ten expanded pulses to reach the transmitter circuit; and the third latch allows a third predetermined number of the third ten expanded pulses to reach the transmitter circuit. Each of the latches functions in a similar manner, and therefore only one shall be explained in detail.

For example, during the first base time interval of ten pulses, the first of the three coded digits is transmitted. The zero output of tens decoder 26 is an input to NAND gate 71 and also an input to NAND gate 74. The zero output of the tens decoder 26 is normally low but is high during pulses zero through nine (the first base time interval). As can be seen in FIG. 3, during the interval between pulses ten and ninety, the low zero output of tens decoder 26 is a low input to NAND gate 71 which causes the output of NAND gate 71 to be high. NAND gates 72 and 73 as shown constitute a latch. The high input from NAND gate 71 to NAND gate 72 latches the output of NAND gate 72 low. Therefore, one input to NAND gate 78 is low and the output of NAND gate 78 is high. When the output of NAND gate 78 is high no transmission due to this latch circuit will occur.

To illustrate transmission due to this latch circuit: during the first time period, when the zero output of tens decoder 26 is high, and pulses zero through nine are being counted, the input from the zero output of tens decoder 26 to NAND gate 71 is high. The other input to NAND gate 71 is from the zero output of ones decoder 24, which is high for each zero count in the ones position. Therefore, at the count of zero in the first base time interval, both inputs to NAND gates 71 are positive and therefore its output is low. Thus, one input to NAND gate 72 is low and its output, which is an input to NAND gate 78, is high. The other input to NAND gate 78 is the inverted expanded pulse from expanded pulse generator 28, which is normally low and pulses high. As the input to NAND gate 78 from NAND gate 72 goes high on the zero count, the inverted expanded pulse also occurs and is high; therefore, the output of NAND gate 78 goes low for the duration of the first inverted expanded pulse. The output of NAND gate 72 is now latched high until a reset condition at the input to NAND gate 73 arises through the branch from NAND gates 77 and 76. Therefore, until the latch consisting of NAND gates 72 and 73 has reset, both inputs to NAND gate 78 will be high for each successive inverted expanded pulse. These lows from gate 78 to gate 81 permit transmission if gate 82 is enabled.

When the input to NAND gate 77 from the five output of ones decoder 24 goes high, indicating a count of five, the other input to NAND gate 77 from the expanded pulse generator is pulsing low. During the duration of the pulse from the five output of ones decoder 24 the expanded pulse input to NAND gate 77 returns high and the output of NAND gate 77 goes low and the output of inverter 76 goes high. This provides a low input to NAND gate 74; the output of NAND gate 74 then goes high resetting the latch consisting of NAND gates 72 and 73 so that the output of the latch goes low. The output of the latch circuit cannot again go high until both inputs to NAND gates 71 are high, at the beginning of another count through the first base time interval.

It can be seen that this particular latch circuit, connected to the five output of the ones decoder 24, has allowed a series of six pulses to be sent to the transmitter circuit 29. One pulse passes through the latch for each count from zero through five, inclusive. The second latch is connected to produce a second digit of four and is set when a pulse appears at the zero output of the ones decoder and also at the one output of the tens decoder, at the beginning of the second base time interval. The connection from the three-output of ones decoder 24 to the second latch circuit provides the count of four in this time period. The third latch operates within the third base time interval as indicated by the connection from the two output of tens decoder 26. The transmitted digit selected for the third latch is a two as indicated by the connection to the third latch from the one output of ones decoder 24.

As described above, when any one of the three inputs to transmitter circuit 29, as shown within the dashed lines of FIG. 3, is low, then the transmitter circuit is activated if NAND gate 82 is enabled. A low input to NAND gate 81 from any latch causes the output of NAND gate 81 to go high, and therefore one input to NAND gate 82 is high. The other input to NAND gate 82 is a transmitter enabling signal which comes from control circuit 21 as shown. This transmitter enabling

signal is from the output of NAND gate 31 and is low unless trip switch 36 has been tripped. If trip switch 36 is in fact closed, then the output of NAND gate 31 is high and this input to NAND gate 82 is high. Thus, if a series of pulses is being passed by one of latch circuits 27, and the trip switch 36 is closed, both inputs to NAND gate 82 will be high for the duration of each inverted expanded pulse and the output of NAND gate 82 will be low for the duration of each successive inverted expanded pulse. The low input to radio transmitter 83 is preferably amplitude modulated on a carrier signal and broadcast to the other alarm units in the system.

The same connections from ones decoder 24 to the first two latch circuits are made in each alarm unit in an alarm system to eliminate erroneous signals from other, differently coded, alarm units in other systems nearby. Thus, for example, all the alarm units in the system of FIG. 1 might have 6 and 4 for the first two digits, and the third digit would be different for each unit.

FIG. 6 illustrates the receiver section of each of the alarm units of FIG. 1. This receiver section shall be described as being in the same unit as that containing the transmitter section described, thereby allowing it to indicate the reception of, for example, a 6-4-1 coded signal as transmitted by another alarm unit in the same system.

The output of radio receiver 101 (FIG. 6) is normally high unless pulses (or possibly noise) are received on the proper carrier frequency from an alarm transmitter. A low output from receiver 101 is coupled to an input of NAND gate 32 (FIG. 3), which starts pulse generator 22 and its associated counters and decoders. When pulse generator 22 has been triggered by a noise pulse from receiver 101, the clock reset input to NAND gate 34 will return the pulse generator to its quiescent state after 90 pulses. If pulse generator 22 has been triggered by a legitimate alarm signal from receiver 101, it will be activated again after each reset as long as the alarm signal is received. The counters 23 and 25, and decoders 24 and 26, provide a series of base time intervals for the receiver circuit when the receiver 101 activates pulse generator 22, while transmission of these pulses is prohibited at NAND gate 82. Pulse generator 22, of course, also continues after each reset when trip switch 36 has been closed. However, only by closing trip switch 36 may a transmitter enabling signal be coupled from the output of NAND gate 31 to an input of NAND gate 82 (FIG. 3).

Again referring to FIG. 6, the output of receiver 101 also is connected to the input of receiver counter 102. Receiver counter 102 is preferably the same type of integrated circuit as ones counter 23 and tens counter 25. Counter 102 has reset connections similar to those of the ones and tens counters except that reset control connection 103 is coupled from the digit 9 terminal of ones decoder 24. Thus receiver counter 102 counts the pulses from receiver 101 within each base time interval determined by counting the pulses generated by pulse generator 22.

The outputs of receiver counter 102 are coupled to the inputs of receiver decoder 104, which is preferably the same type of integrated circuit as ones decoder 24 and tens decoder 26. The outputs of receiver counter 102 are also coupled to quadruple bistable latch 106, which is preferably a type N7475 integrated circuit

from Signetics. The binary coded inputs to latch 106 input terminals A, B, C and D are coupled to the A, B, C, and D outputs of latch 106 when clock inputs 107 and 108 are high. When the clock inputs change to low, the information that was present at the inputs to latch 106 at the time the transition occurred is retained at the latch outputs until the clock terminals are again permitted to go high. The binary coded information from the output of latch 106 is coupled to the inputs of seven segment decoder 109, which is preferably a type N 7447 integrated circuit from Signetics. The outputs of decoder 109 drive a standard light emitting diode seven segment readout in such a manner as to display in decimal digit form the binary information at the inputs to decoder 109.

Receiver decoder 104 couples its decoded count information to a series of latches, which then activate an alarm if the count and sequence has been correct. All alarm units within a given system are set to transmit and receive a predetermined pair of first digits. The third digit associated with each alarm unit within a system is its own identification. As an example, the operation of the receiver circuit shown in FIG. 6 shall be described in detail for the reception of a coded series of digits 6-4-1.

When receiver 101 couples the first of the six pulses, representing the first digit, to counter 102, the input to NAND gate 32 (FIG. 3) from the receiver output also initiates pulse generator 22 and starts the counters 23 and 25 and decoders 24 and 26 running in the transmitter section. During the first base time interval, consisting of the first ten pulses generated in the transmitter section, receiver counter 102 counts the six pulses first received by receiver 101 and couples this information to receiver decoder 104. The digit six output of decoder 104 is preset as an input to NAND gate 112, and the other input to NAND gate 112 is from the digit zero on tens decoder 26 (FIG. 3). Since six pulses have been counted and decoded, the six output of receiver decoder 104 is high and since this is the first base time interval, the digit zero from tens decoder 26 is also high; therefore, the output of NAND gate 112 is low and the output of inverter 113 is high.

This high output from inverter 113 is an input to NAND gate 114. The input to NAND gate 114 from the receiver enable signal is high as shown at the output of NAND gate 33 in FIG. 3 when trip switch 36 is open. On the count of eight from ones decoder 24 (FIG. 3) all three inputs to NAND gate 114 are high so the output goes low. This output from NAND gate 114 is an input to the latch made up of NAND gates 116 and 117. When the output from NAND gate 114, which is the input to NAND gate 117, goes low, the output of NAND gate 117 is latched high. The output of NAND gate 117 will remain latched high until the count of 90 when the clock reset pulse resets the latch as an input to NAND gate 116. Thus the presence of the digit six has placed the first latch in condition for triggering the alarm.

As stated, the input to NAND gate 118 from NAND gate 118 from NAND gate 117 will remain high until a count of 90. During the second base time interval, the input to NAND gate 118 from the digit one output of tens decoder 26 (FIG. 3) is high, and if the proper count of four pulses is present at the digit four output of receiver decoder 104 in the second base time interval, the third input to NAND gate 118 is high. If all

three inputs to NAND gate 118 are high, its output is low, and the output of inverter 119 is high. This provides one high input to NAND gate 120, and a second high input is present from the receiver enable signal as at the first latch. The third input to NAND gate 120 goes high on the count of eight from ones decoder 24 (FIG. 3) which pulses the output of NAND gate 120 low. This provides a low input to the latch consisting of NAND gates 121 and 122. When the input to NAND gate 122 goes low its input is latched high. Again, this high latch output will persist until the count of 90 from the clock reset pulse. At this stage both the conditions of a six in the first base time interval and a four in the second base time interval have been met.

The latched-high output of NAND gate 122 is one input to NAND gate 123. The second input is from the digit 2 output of tens decoder 26 (FIG. 3) and this input is high during the third base time interval. The third input to NAND gate 123 is the output of OR gate 125. This output will be high whenever a pulse count of one through six is present at the appropriate output of receiver decoder 104. In other words, one of the six usable code digits must be present in order to bring the output of OR gate 125 high. In the present example, during the third base time interval the digit one output of receiver decoder 104 is high and the output of OR gate 125 is high. Therefore, all three inputs to NAND gate 123 are high during the third time interval, and its output is low, making the output of inverter 124 high. Again, if the receiver enable signal from the output of NAND gate 33 (FIG. 3) is high, on a count of eight from ones decoder 24 (FIG. 3) all three inputs to NAND gate 126 are high and its output is low. This low input to NAND gate 128 latches the output of NAND gate 127 high through the latch combination of NAND gates 127 and 128, until the count of 90 from the clock reset pulse.

When the output of NAND gate 128 is high this activates audio alarm 131. As long as a properly coded signal is received by receiver 101 the three sequential latches just described will reset and then relatch after each 90 count from the clock reset pulse.

The visual display, indicating which of the alarm units in the system is transmitting, operates as follows. The output of NAND gate 127 is normally high and is an input to the latch made up of NAND gates 133 and 134. This high input to NAND gate 133 makes its output low. This output is coupled to the input-blanking terminal of seven segment decoder 109. When the blanking input to seven segment decoder 109 is low, no output is displayed on the light emitting diode seven segment readout 111. When the output of NAND gate 127 goes low, indicating a properly received alarm signal, then the output of NAND gate 133 latches high. The output of NAND gate 133 will remain high until the input to NAND gate 134 goes low and the input to NAND gate 133 from NAND gate 127 also returns high. The output of NAND gate 136, which is coupled to the input of NAND gate 134, will be low only when both its inputs are high. The input to NAND gate 136 from the output of NAND gate 127 will be high only when no properly coded alarm signal has been received, and the other input to NAND gate 136 will be high only during the fourth base time interval as designated by a high from the digit three of tens decoder 26 (FIG. 3). The resultant operation of the blanking latch of NAND gates 133 and 134 is that when the latch con-

sisting of NAND gates 127 and 128 activate alarm 131, the blanking signal is removed from seven segment decoder 109. During the interval from the 90 count of the clock reset input to NAND gate 127 to the time that the receiver latches relatch at about a 28 count, the latch consisting of NAND gates 133 and 134 maintains the blanking input to decoder 109 high so that the light emitting diode readout will persist.

The output from NAND gate 128 is one input to NAND gate 137, and when it goes high, indicating a properly coded alarm signal, this input to NAND gate 137 also goes high. A second input to NAND gate 137 is from the digit two of tens decoder 26 (FIG. 3) which is high during the third base time interval. The third input to NAND gate 137 is from the digit 8 of ones decoder 24 (FIG. 3). Therefore, if there is an alarm signal, or high at the output of NAND gate 128, on the count of 28 all inputs to NAND gate 137 will be high and its output will be low, thereby making the output of inverter 138 high. This high output from NAND gate 138 is coupled to the clock inputs 107 and 108 of quadruple bistable latch 106, allowing the binary coded information at the input to latch 106 to be transferred to its outputs. After the count of 28, the output of NAND gate 137 goes high and the output of inverter 138 goes low, thereby freezing the outputs of latch 106 with the count that was received at its inputs during the third base time interval. Since it was necessary for alarm 131 to be activated in order to have all inputs to NAND gates 137 high to set latch 106, it can be seen that only the appropriate third code digit will be transferred to the outputs of latch 106 during the third base time interval.

In the operation of the alarm units in an alarm system as disclosed herein, the frequencies of the pulse generators in each unit must be set approximately the same since the base time intervals in the receive mode are determined by the pulse generator in the receiving unit. This condition is not critical, however, because only the digits one through six are transmitted, while the receiver latches check for a proper count in the receiver decoder 104 only after a count of eight has been reached in each base time interval established by the receiving unit's pulse generator.

For the preferred decoders disclosed herein, a resistor must be coupled from each decoder output to the five volt B+ supply.

It can be seen that the present invention provides an alarm system wherein alarm units in the system are placed on different premises to be protected and each unit serves as an alarm receiver as well as an alarm transmitter without physical connections between the units.

It can also be seen that the present invention provides an alarm system comprising a plurality of alarm units each of which is operable to transmit and receive uniquely coded alarm signals.

While the invention has been illustrated and described in detail in the drawings and foregoing description, the same is to be considered as illustrative and not restrictive in character, it being understood that only the preferred embodiment has been shown and described and that all changes and modifications that come within the spirit of the invention are desired to be protected.

What is claimed is:

1. An alarm system comprising a plurality of alarm units remote from one another, each said alarm unit comprising:

sensing means for detecting an emergency condition;
coding means coupled to said sensing means for producing a coded electrical signal unique to said unit when said sensing means detects an emergency condition;

a radio transmitter coupled to said coding means for transmitting a coded radio frequency signal which contains the information in said coded electrical signal;

a radio receiver for receiving other coded radio frequency signals from other of said plurality of alarm units in the alarm system;

decoding means coupled to said radio receiver for decoding said received radio frequency signals; and

display means coupled to said decoding means for indicating the specific decoded radio frequency signals received.

2. The alarm system of claim 1 in which each said alarm unit includes in its coding means;

a pulse generator;

a first counting means coupled to said pulse generator for counting pulses produced by said pulse generator; and

first latching means coupled to said first counting means for coupling a predetermined count of pulses from said pulse generator to said radio transmitter.

3. The alarm system of claim 2 in which each said alarm unit includes in its decoding means;

second counting means for counting pulses coupled from said radio receiver; and

second latching means coupled to said second counting means for coupling predetermined counts of pulses to said display means.

4. The alarm system of claim 3 in which said first counting means comprises a binary coded decimal ones-counter and decoder and a binary coded decimal tens-counter and decoder.

5. The alarm system of claim 4 in which said second counting means comprises a binary coded decimal counter and decoder.

6. The alarm system of claim 5 in which said binary coded decimal counters and decoders are integrated circuits.

7. The alarm system of claim 2 in which said first latching means includes a plurality of pairs of NAND gates, the output of each NAND gate in each of said pairs being an input to the other NAND gate in each of said pairs.

8. The alarm system of claim 3 in which said second latching means includes a plurality of pairs of NAND

gates, the output of each NAND gate in each of said pairs being an input to the other NAND gate in each of said pairs.

9. The alarm system of claim 4 in which said first latching means includes a plurality of pairs of NAND gates, the output of each NAND gate in each of said pairs being an input to the other NAND gate in each of said pairs.

10. The alarm system of claim 5 in which said second latching means includes a plurality of pairs of NAND gates, the output of each NAND gate in each of said pairs being an input to the other NAND gate in each of said pairs.

11. The alarm system of claim 9 in which each of said pairs of NAND gates in said first latching means has inputs coupled from an output of said binary coded decimal ones-decoder and an input of said binary coded decimal tens-decoder.

12. The alarm system of claim 10 in which each of said pairs of NAND gates in said second latching means has inputs coupled from an output of said binary coded decimal ones-decoder, and an output of said binary coded decimal tens-decoder, and an output of said binary coded decimal decoder in said second counting means.

13. The alarm system of claim 11 in which there are three of said pairs of NAND gates in said first latching means.

14. The alarm system of claim 12 in which there are three of said pairs of NAND gates in said second latching means.

15. The alarm system of claim 3 in which said pulse generator and said first counting means are activated by said radio receiver to produce outputs coupled to said second latching means, said outputs providing a time base for the input to said second latching means from said second counting means.

16. The alarm system of claim 1 in which said display means includes an audio alarm and a light-emitting diode readout.

17. The alarm system of claim 5 in which said display means includes an audio alarm and a light-emitting diode readout.

18. The alarm system of claim 1 in which said sensing means also includes an intrusion detector switch.

19. The alarm system of claim 1 in which said sensing means also includes a fire detector switch.

20. The alarm system of claim 8 in which said first latching means includes a plurality of pairs of NAND gates, the output of each NAND gate in each of said pairs being an input to the other NAND gate in each of said pairs.

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