

(19)



**Octrooi Centrum
Nederland**

(11)

2018487

(12) B1 OCTROOI

(21)

Aanvraagnummer: **2018487**

(51)

Int. Cl.:
H01L 25/07 (2017.01) H01L 23/495 (2017.01)

(22)

Aanvraag ingediend: **09/03/2017**

(30)

Voorrang:
11/03/2016 JP PCT/JP2016/057766
13/07/2016 JP PCT/JP2016/070664

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Aanvraag ingeschreven:
20/09/2017

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Aanvraag gepubliceerd:
02/10/2017

(74)

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(47)

Octrooi verleend:
16/11/2017

(45)

Octrooischrift uitgegeven:
29/01/2018

(54)

SEMICONDUCTOR DEVICE AND LEAD FRAME

(57)

A semiconductor device according to a first aspect of the present invention includes a device main body, a single power supply wiring board, a plurality of output wiring boards, and a plurality of semiconductor elements. In a long-side direction of the device main body, the narrow portion of one of any two adjacent wiring boards faces the wide portion of another one of the any two adjacent wiring boards. In a short-side direction of the device main body, the narrow portion and the wide portion of each of the output wiring boards respectively face the wide portion and the narrow portion, in a single pair, of the power supply wiring board. In the long-side direction of the device main body a width of each of the output wiring boards is smaller than a sum of widths of the narrow portion and the wide portion, in a single pair, of the power supply wiring board.

DESCRIPTION

SEMICONDUCTOR DEVICE AND LEAD FRAME

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TECHNICAL FIELD

[0001]

The present invention relates to a semiconductor device and a lead frame.

Priority is claimed based on the international application PCT/JP2016/057766
filed on Japan on March 11, 2016 and the international application PCT/JP2016/070664
10 filed on Japan on July 13, 2016, the contents of which are incorporated herein by
reference.

BACKGROUND ART

[0002]

15

Conventionally, there is known a semiconductor device in which external
connection terminal units (terminal boards) protruding from a sealing resin is integrally
formed on electrode boards exposed on a lower surface of the sealing resin (for example,
Patent Document 1). In this semiconductor device, base end portions of the external
connection terminal units extend in parallel with the electrode boards and function as
20 heat dissipation surfaces together with the lower surfaces of the electrode boards.

CITATION LIST

[Patent Document]

[0003]

25

[Patent Document 1] Japanese Patent No. 5669866

DISCLOSURE OF THE INVENTION

Problems to be Solved by the Invention

[0004]

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However, in the above semiconductor device, the width dimension of each
external connection terminal unit is constant from the base end portion to the tip end
portion. Therefore, when a plurality of external connection terminal units are arranged,
it is necessary to set the width dimension of each external connection terminal unit in

consideration of a pitch between adjacent external connection terminal units (particularly, the pitch between the tip end portions of the adjacent external connection terminal units). As a result, there is a limit to increasing the heat dissipation area of the semiconductor device.

5 [0005]

The present invention has been made to solve the above problems, and it is an object of the present invention to provide a semiconductor device and a lead frame for the semiconductor device capable of increasing the heat dissipation area while securing a pitch between adjacent terminal boards and further reducing the size thereof.

10

Means for Solving the Problems

[0006]

In order to solve the above problem, a semiconductor device according to a first aspect of the present invention includes a device main body, a single power supply wiring board, a plurality of output wiring boards, and a plurality of semiconductor elements.

15 The device main body has a first main surface, a second main surface, a first side surface, and a second side surface. The second main surface opposes the first main surface. The second side surface opposes the first side surface in a short-side direction of the first main surface. The single power supply wiring board has plural pairs of narrow portions and wide portions connected alternately in a long-side direction of the first main surface.

20 The wide portions protrude toward a side of the first side surface with respect to the narrow portions. The plurality of output wiring boards are arranged in the long-side direction along the power supply wiring board. The number of the output wiring boards is equal to the number of the pairs of narrow portions and wide portions of the power

25 supply wiring board. Each of the output wiring boards has a narrow portion and a wide portion connected in the long-side direction. The wide portion protrudes toward a side of the second side surface with respect to the narrow portion. Each of the plurality of semiconductor elements is disposed on a different one of the wide portions of the power supply wiring board and the wide portions of the output wiring boards. In the long-side

30 direction, the narrow portion of one of any two adjacent output wiring boards faces the wide portion of another one of the any two adjacent output wiring boards. In the short-side direction, the narrow portion and the wide portion of each of the output wiring boards respectively face the wide portion and the narrow portion, in a single pair, of the

power supply wiring board. In the long-side direction, a width of each of the output wiring boards is smaller than a sum of widths of the narrow portion and the wide portion, in a single pair, of the power supply wiring board.

[0007]

5 A lead frame according to a second aspect of the present invention is a lead frame for the semiconductor device according to the above first aspect. The lead frame includes a plurality of terminal boards, and a plurality of connecting portions connecting the terminal boards.

10 Effects of the Invention

[0008]

 According to the semiconductor device of the aspects of the present invention, it is possible to increase the heat dissipation area while securing the pitch between the adjacent terminal boards, and to further reduce the size of the semiconductor device.

15

BRIEF DESCRIPTION OF THE DRAWINGS

[0009]

 FIG. 1 is a structural plan view showing an example of a semiconductor device according to the present embodiment.

20 FIG. 2 is a perspective view showing the example of the semiconductor device according to the present embodiment.

 FIG. 3 is an example of a circuit diagram of the semiconductor device according to the present embodiment.

25 FIG. 4 is a structural plan view showing another example of a semiconductor device according to the present embodiment.

 FIG. 5 is another example of a circuit diagram of the semiconductor device according to the present embodiment.

 FIG. 6 is a perspective view showing an example of a lead frame according to the present embodiment.

30

MODE FOR CARRYING OUT THE INVENTION

[0010]

[Semiconductor device]

Hereinafter, a semiconductor device according to an embodiment of the present invention will be described with reference to the drawings.

[0011]

As shown in FIGS. 1 and 2, the semiconductor device 10 of the present
 5 embodiment includes: a device main body having a first main surface 20a and a second main surface 20b that face each other, and a first side surface 20c and a second side surface 20d that face each other in a short-side direction Y (up-down direction of FIG. 1) of the first main surface 20a; a plurality of terminal boards (power supply terminal boards (leads) 31, 32, 33 and ground terminal boards (leads) 37, 38, 39) extending
 10 outward from the first side surface 20c of the device main body 20; and a plurality of terminal boards (output terminal boards (leads) 34, 35, 36 and gate terminal boards (leads) 61 to 66) extending outward from the second side surface 20d.

[0012]

The device main body 20 is formed by integrating device units 21, 22, 23
 15 corresponding respectively to a plurality of circuit units 41, 42, 43. The circuit units 41, 42, 43 are arranged in this order along a long-side direction X (left-right direction in FIG. 1) of the device main body 20.

[0013]

The device units 21, 22, 23 include: a plurality of wiring boards (a power supply
 20 wiring board 24, ground wiring boards 25, 26, 27, output wiring boards 28, 29, 30, and gate wiring boards 81-86) arranged separately from one another; and semiconductor elements 91 to 96 arranged on the first main surface of some of the wiring boards and electrically connected to the wiring boards.

[0014]

25 The semiconductor device 10 further includes a sealing resin 50 covering the device units 21, 22, 23.

[0015]

The first circuit unit 41 includes: a first device unit 21; a first power supply terminal board 31 and a first ground terminal board 37 which protrude from the first side
 30 surface 20c of the first device unit 21; and a first output terminal board 34 protruding from the second side surface 20d of the first device unit 21.

[0016]

The second circuit unit 42 includes: a second device unit 22; a second power

supply terminal board 32 and a second ground terminal board 38 which protrude from the first side surface 20c of the second device unit 22; and a second output terminal board 35 protruding from the second side surface 20d of the second device unit 22.

[0017]

5 The third circuit unit 43 includes: a third device unit 23; a third power supply terminal board 33 and a third ground terminal board 39 which protrude from the first side surface 20c of the third device unit 23; and a third output terminal board 36 protruding from the second side surface 20d of the third device unit 23.

[0018]

10 The first circuit unit 41, the second circuit unit 42, and the third circuit unit 43 have substantially the same shape when viewed in plan view.

[0019]

 The first device unit 21 includes one unit of the power supply wiring board 24, a first ground wiring board 25, a first output wiring board 28, a first semiconductor
15 element 91, and a fourth semiconductor element 94.

[0020]

 The second device unit 22 includes one unit of the power supply wiring board 24, a second ground wiring board 26, a second output wiring board 29, a second semiconductor element 92, and a fifth semiconductor element 95.

20 [0021]

 The third device unit 23 includes one unit of the power supply wiring board 24, a third ground wiring board 27, a third output wiring board 30, a third semiconductor element 93, and a sixth semiconductor element 96.

[0022]

25 The sealing resin 50 seals the power supply wiring board 24, the ground wiring boards 25, 26, 27, the output wiring boards 28, 29, 30, the semiconductor elements 91 to 96, the power supply terminal boards 31, 32, 33, the output terminal boards 34, 35, 36, and the ground terminal boards 37, 38, 39, such that the second main surfaces of the power supply wiring board 24, the ground wiring boards 25, 26, 27, and the output
30 wiring boards 28, 29, 30 are exposed.

[0023]

 For example, as shown in FIG. 2, the sealing resin 50 seals the power supply wiring board 24, the ground wiring boards 25, 26, 27, the output wiring boards 28, 29, 30,

the semiconductor elements 91 to 96, the power supply terminal boards 31, 32, 33, the output terminal boards 34, 35, 36, and the ground terminal boards 37, 38, 39, such that the second main surface 24b of the power supply wiring board 24, the second main surfaces 25b, 26b, 27b of the ground wiring boards 25, 26, 27, and the second main surfaces 28b, 29b, 30b of the output wiring boards 28, 29, 30 are exposed.

[0024]

The second main surface 24b of the power supply wiring board 24, the second main surfaces 25b, 26b, 27b of the ground wiring boards 25, 26, 27 and the second main surfaces 28b, 29b, 30b of the output wiring boards 28, 29, 30, and a surface (lower surface) 50a, exposed on the second main surface side, of the sealing resin 50 are arranged on the same surface.

[0025]

The second main surface 24b of the power supply wiring board 24, the second main surfaces 25b, 26b, 27b of the ground wiring boards 25, 26, 27, and the second main surfaces 28b, 29b, 30b of the output wiring boards 28, 29, 30 constitute a lower surface of the device main body 20.

[0026]

The power supply terminal boards 31, 32, 33, the output terminal boards 34, 35, 36, and the ground terminal boards 37, 38, 39 protrude from the sealing resin 50.

[0027]

The output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 protrude perpendicularly from the side surfaces, along the long-side direction X, of the device main body 20 (the side surfaces of the sealing resin 50) in respectively opposite directions. Specifically, the ground terminal boards 37, 38, 39 protrude perpendicularly from the first side surface 20c of the device main body 20, while the output terminal boards 34, 35, 36 protrude perpendicularly from the second side surface 20d of the device main body 20.

[0028]

The power supply terminal boards 31, 32, 33 protrude in the same direction as the ground terminal boards 37, 38, 39. Specifically, both the power supply terminal boards 31, 32, 33 and the ground terminal boards 37, 38, 39 protrude perpendicularly from the first side surface 20c of the device main body 20.

[0029]

The power supply terminal boards 31, 32, 33 are arranged shifted in a direction (the long-side direction X of the device main body 20) orthogonal to an arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20).

5 [0030]

The arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20) indicates a direction from the first output terminal board 34 toward the first ground terminal board 37, a direction from the second output terminal board 35 toward the second ground terminal board 38, and the direction from the third output terminal board 36 toward the third ground terminal board 39.

[0031]

In other words, the arrangement such that the power supply terminal boards 31, 32, 33 are shifted in the direction (the long-side direction X of the main body 20) orthogonal to the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 means that the power supply terminal boards 31, 32, 33 are not on a straight line connecting the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39.

[0032]

20 The circuit units 41, 42, 43 may include gate terminal boards 61 to 66 protruding from the second side surface 20d of the device main body 20 (device units 21, 22, 23).

[0033]

In this case, the power supply terminal boards 31, 32, 33 and the gate terminal boards 61 to 66 protrude perpendicularly from the side surfaces, along the long-side direction X, of the device main body 20 in respectively opposite directions. Specifically, the power supply terminal boards 31, 32, 33 protrude perpendicularly from the first side surface 20c of the device main body 20, while the gate terminal boards 61 to 66 protrude perpendicularly from the second side surface 20d of the device main body 20. The gate terminal boards 61 to 66 protrude from the sealing resin 50.

30 [0034]

In the long-side direction X of the device main body 20, the power supply terminal boards 31, 32, 33, the output terminal boards 34, 35, 36, and the ground terminal boards 37, 38, 39 are preferably larger in width than the gate terminal boards 61 to 66.

[0035]

The plurality of terminal boards (the power supply terminal boards 31, 32, 33, the output terminal boards 34, 35, 36, and the ground terminal boards 37, 38, 39, and the gate terminal boards 61 to 66) are folded in their middle portions in the long-side direction thereof. The tip end portions (31B to 39B, 61B to 66B), in the long-side direction, of the respective terminal boards extend substantially perpendicular to the base end portions (31A to 39A, 61A to 66A).

[0036]

Additionally, the tip end portions (31B to 39B, 61B to 66B), in the long-side direction, of the respective terminal boards extending from the plurality of wiring boards extend in a direction opposite to the facing directions of the second main surfaces of the plurality of wiring boards (the second main surface 24b of the power supply wiring board 24, the second main surfaces 25b, 26b, 27b of the wiring boards 25, 26, 27, and the second main surfaces 28b, 29b, 30b of the output wiring boards 28, 29, 30).

[0037]

In other words, the tip end portions of the respective terminal boards extending from the plurality of wiring boards extend in the thickness direction of the wiring boards so as to protrude from the first main surfaces of the wiring boards (*e.g.*, the first main surface 24a of the power supply wiring board 24).

[0038]

The device main body 20 includes: a power supply wiring board 24 in common to the three device units 21, 22, 23; ground wiring boards 25, 26, 27 provided respectively in the device units 21, 22, 23; and output wiring boards 28, 29, 30 provided respectively in the device units 21, 22, 23.

[0039]

The power supply wiring board 24, the ground wiring boards 25, 26, 27, and the output wiring boards 28, 29, 30 are arranged separately from one another.

[0040]

The power supply wiring board 24 extends in the long-side direction X of the device main body 20. In plan view, the power supply wiring board 24 has plural pairs of narrow portions 24A and wide portions 24B alternately connected along the long-side direction X of the device main body 20, thereby having a periodic concave-convex shape in the long-side direction X.

[0041]

In other words, the power supply wiring board 24 has three pairs of narrow portions 24A and wide portions 24B continuously extending in the direction (the long-side direction X of the device main body 20) orthogonal to the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20),

[0042]

The narrow portion 24A of the power supply wiring board 24 is smaller in width than the wide portion 24B in the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20).

[0043]

The wide portion 24B of the power supply wiring board 24 is larger in width than the narrow portion 24A in the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20).

[0044]

The wide portion 24B of the power supply wiring board 24 protrudes on one side of the narrow portion 24A (toward the upper side in FIG. 1) in the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20). Specifically, in the short-side direction Y of the device main body 20, the wide portion 24B of the power supply wiring board 24 protrudes toward the first side surface 20c side of the device main body 20 with respect to the narrow portion 24A.

[0045]

The power supply wiring board 24 extends over the entire three circuit units 41, 42, 43. The three power supply terminal boards 31, 32, 33 are integrally connected to the respective wide portions 24B of the power supply wiring board 24, and protrude from the respective wide portions 24B toward the first side surface 20c side of the device main body 20 in plan view. In other words, the three power supply terminal boards 31, 32, 33 and the power supply wiring board 24 are integrally formed.

[0046]

The ground wiring boards 25, 26, 27 are arranged so as to be adjacent to the

respective narrow portions 24A of the power supply wiring board 24 on the first side surface 20c side of the power supply wiring board 24 toward which the wide portions 24B of the power supply wiring board 24 protrude.

[0047]

5 More specifically, each of the ground wiring boards 25, 26, 27 is disposed on a different one of regions each surrounded by two adjacent wide portions 24B of the power supply wiring board 24 in the long-side direction X of the device main body 20, and one narrow portion 24A of the power supply wiring board 24 connecting these two wide portions 24B.

10 [0048]

The ground terminal boards 37, 38, 39 are integrally connected respectively to the ground wiring boards 25, 26, 27, and protrude respectively from the ground wiring boards 25, 26, 27 toward the first side surface 20c side of the device main body 20 in plan view. In other words, the ground terminals 37, 38, 39 and the ground wiring

15 boards 25, 26, 27 are integrally formed.

[0049]

The output wiring boards 28, 29, 30 are arranged on the second side surface 20d side of the device main body 20 that is opposite to the first side surface 20c thereof toward which the wide portions 24B of the power supply wiring board 24 protrude.

20 [0050]

The output wiring boards 28, 29, 30 are arranged along the power supply wiring board 24 in the long-side direction X of the device main body 20, and the number of output wiring boards is equal to the number of pairs of narrow portion 24A and wide portions 24B of the power supply wiring board 24, that is, the number of circuit units of the device main body 20 (the number of device units of the semiconductor device 10).

25 the device main body 20 (the number of device units of the semiconductor device 10).

[0051]

Additionally, each output wiring board of the output wiring boards 28, 29, 30 has a narrow portion 28A (29A, 30A) and a wide portion 28B (29B, 30B) connected in the long-side direction X of the device main body 20.

30 [0052]

More specifically, in plan view, the output wiring boards 28 (29, 30) has the narrow portion 28A (29A, 30A) and the wide portion 28B (29B, 30B) continuously arranged in a direction (the long-side direction X of the device main body 20) orthogonal

to the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20).

[0053]

The narrow portions 28A, 29A, 30A of the output wiring boards 28, 29, 30 are smaller in width than the wide portions 28B, 29B, 30B in the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20),.

[0054]

The wide portions 28B, 29B, 30B of the output wiring boards 28, 29, 30 are larger in width than the narrow portions 28A, 29A, 30A in the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20).

[0055]

The wide portions 28B, 29B, 30B of the output wiring boards 28, 29, 30 protrude on one side of the narrow portions 28A, 29A, 30A (toward the lower side of FIG. 1) in the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20). In other words, the wide portion of each output wiring board protrudes toward the second side surface 20d side of the device main body 20 with respect to the narrow portion thereof.

[0056]

The output terminal boards 34, 35, 36 are integrally connected respectively to the wide portions 28B, 29B, 30B of the output wiring boards 28, 29, 30, and protrude respectively from the wide portions 28B, 29B, 30B toward the second side surface 20d side of the device main body 20 in plan view. In other words, the output terminal boards 34, 35, 36 and the output wiring boards 28, 29, 30 are integrally formed.

[0057]

Regarding the output wiring boards 28, 29, 30, the narrow portion (28A) of one output wiring board (28) of any two adjacent output wiring boards (*e.g.*, 28 and 29) faces the wide portion (29B) of the other one output wiring board (29) in the long-side direction X of the device main body 20.

[0058]

Additionally, in the short-side direction Y of the device main body 20, the

narrow portion (*e.g.*, 28A) and the wide portion (28 B) of each output wiring board respectively face the wide portion 24 B and the narrow portion 24A, in a single pair, of the power supply wiring board 24.

[0059]

5 Further, in the long-side direction X, the width of each output wiring board (*e.g.*, 28) is smaller than a sum of the widths of the narrow portion 24A and the wide portion 24B, in a single pair, of the power supply wiring board 24.

[0060]

10 The ground wiring boards 25, 26, 27 are arranged so as to respectively face the wide portions 28B, 29B, 30B of the output wiring boards 28, 29, 30 via the narrow portions 24A of the power supply wiring board 24 in the short-side direction Y of the device main body 20.

[0061]

15 The narrow portion 24A and the wide portion 24B, in each pair, of the power supply wiring board 24 are arranged so as to respectively face the wide portion and the narrow portion of one output wiring board of the output wiring boards 28, 29, 30 in the short-side direction Y of the device main body 20.

[0062]

20 In a case where the circuit units 41, 42, 43 include the gate terminal boards 61 to 66, the device main body 20 has the gate wiring boards 81 to 86 provided respectively for the gate terminal boards 61 to 66 in the device units 21, 22, 23.

[0063]

25 The gate wiring boards 81 to 86 include: a plurality of first gate wiring boards 82, 84, 86 each disposed between two adjacent output wiring boards (*e.g.*, 28 and 29) in the long-side direction X of the device main body 20; and a plurality of second gate wiring boards 81, 83, 85 each disposed in a different one of regions each surrounded by one first gate wiring board (*e.g.*, 82), the narrow portion (28A) of one output wiring board (28) adjacent to the one first gate wiring board (82), and the wide portion (28B) connected to the narrow portion (28A) of the one first gate wiring board (82).

30 [0064]

The gate terminal boards 61 to 66 are integrally connected respectively to the gate wiring boards 81 to 86, and protrude respectively from the gate wiring boards 81 to 86 toward the second side surface 20d side of the device main body 20 in plan view.

[0065]

In the first circuit unit 41, the second gate wiring board 81 is disposed so as to be adjacent to the narrow portion 28A of the first output wiring board 28. Additionally, the first gate wiring board 82 is disposed between the first output wiring board 28 and the
5 second output wiring board 29.

[0066]

Thereby, the first circuit unit 41 includes one pair of the narrow portion 24A and the wide portion 24B of the power supply wiring board 24, one output wiring board 28, one ground wiring board 25, one first gate wiring board 82, and one second gate wiring
10 board 81.

[0067]

In the second circuit unit 42, the second gate wiring board 83 is disposed so as to be adjacent to the narrow portion 29A of the second output wiring board 29. Additionally, the first gate wiring board 84 is disposed between the second output wiring
15 board 29 and the third output wiring board 30.

[0068]

Thereby, the second circuit unit 42 includes one pair of the narrow portion 24A and the wide portion 24B of the power supply wiring board 24, one output wiring board 29, one ground wiring board 26, one first gate wiring board 84, and one second gate
20 wiring board 83.

[0069]

In the third circuit unit 43, the second gate wiring board 85 is disposed so as to be adjacent to the narrow portion 30A of the third output wiring board 30. Additionally, the first gate wiring board 86 is disposed along the arrangement direction of the third
25 output terminal board 36 and the third ground terminal board 39 (the short-side direction Y of the device main body 20).

[0070]

Thereby, the third circuit unit 43 includes one pair of the narrow portion 24A and the wide portion 24B of the power supply wiring board 24, one output wiring board
30 30, one ground wiring board 27, one first gate wiring board 86, and one second gate wiring board 85.

[0071]

The base end portions 31A, 32A, 33A, in the extending direction, of the power

supply terminal boards 31, 32, 33 are formed to be larger in width than the other portions (the tip end portions 31B, 32B, 33B) of the power supply terminal boards 31, 32, 33.

[0072]

5 It is preferable that a step is provided between the base end portion 31A (32A, 33A) of the power supply terminal board 31 (32, 33) and the tip end portion 31B (32B, 33B) of the power supply terminal boards 31 (32, 33).

[0073]

10 The base end portions 34A, 35A, 36A, in the extending direction, of the output terminal boards 34, 35, 36 are formed to be larger in width than the other portions (the tip end portions 34B, 35B, 36B) of the output terminal boards 34, 35, 36.

[0074]

It is preferable that a step is provided between the base end portion 34A (35A, 36A) of the output terminal board 34 (35, 36) and the tip end portion 34B (35B, 36B) of the output terminal board 34 (35, 36).

15 [0075]

The base end portions 37A, 38A, 39A, in the extension direction, of the ground terminal boards 37, 38, 39 are formed to be larger in width than the other portions (the tip end portions 37B, 38B, 39B) of the ground terminal boards 37, 38, 39.

[0076]

20 It is preferable that a step is provided between the base end portion 37A (38A, 39A) of the ground terminal board 37 (38, 39) and the tip end portion 37B (38B, 39B) of the ground terminal board 37 (38, 39).

[0077]

25 In the illustrated example, the base end portions 61A to 66A, in the extending direction, of the gate terminal boards 61 to 66 are formed to be larger in width than the other portions (the tip end portions 61B to 66B) of the gate terminal boards 61 to 66. Here, for example, the base end portions 61A to 66A may be substantially equal in width dimension to the tip end portions 61B to 66B.

[0078]

30 In a case where the base end portions 61A to 66A are larger in width than the tip end portions 61B to 66B, it is preferable that a step is provided between the base end portion (61A to 66A) of each gate terminal board (61 to 66) and the tip end portion (61B to 66B) of the gate terminal board (61 to 66).

[0079]

The step between the base end portion (31A to 39A, 61A to 66A) and the tip end portion (31B to 39B, 61B to 66B) of each terminal board means a shape such that the width dimension of each terminal board greatly changes at a boundary between the base end portion (31A to 39A, 61A to 66A) and the tip end portion (31B to 39B, 61B to 66B).

[0080]

In the illustrated example, the step is provided between the base end portion (31A to 39A, 61A to 66A) and the tip end portion (31B to 39B, 61B to 66B) of each terminal board, so that both ends, in the width direction, of the tip end portion (31B to 39B, 61B to 66B) of each terminal board is positioned inside both ends, in the width direction, of the base end portion (31A to 39A, 61A to 66A) of the terminal board.

[0081]

Terminal main surfaces (lower surfaces) 31b, 32b, 33b of the base end portions 31A, 32A, 33A of the power supply terminal boards 31, 32, 33; terminal main surfaces (lower surfaces) 34b, 35b, 36b of the base end portions 34A, 35A, 36A of the output terminal boards 34, 35, 36; terminal main surfaces (lower surfaces) 37b, 38b, 39b of the base end portions 37A, 38A, 39A of the ground terminal boards 37, 38, 39; lower surfaces 61b to 66b of the base end portions 61A to 66A of the gate terminal boards 61 to 66; a second main surface (lower surface) 24b of the power supply wiring board 24; second main surfaces (lower surfaces) 25b, 26b, 27b of the ground wiring boards 25, 26, 27; and second main surfaces (lower surfaces) 28b, 29b, 30b of the output wiring boards 28, 29, 30, are arranged on the same surface.

[0082]

Each of the semiconductor elements 91 to 96 is arranged on a different one of the wide portions 24B of the power supply wiring board 24 and the wide portions 28B to 30B of the output wiring boards 28 to 30.

[0083]

More specifically, the semiconductor elements 91, 92, 93 are mounted respectively on the first main surfaces 24a of the portions (the wide portions 24B) of the power supply wiring board 24, which are adjacent to the base end portions 31A, 32A, 33A of the power supply terminal boards 31, 32, 33.

[0084]

These semiconductor elements 91, 92, 93 are electrically connected respectively

to the narrow portions 28A, 29A, 30A of the output wiring boards 28, 29, 30 via connectors 101, 102, 103. The semiconductor elements 91, 92, 93 are electrically connected respectively to the first gate wiring boards 82, 84, 86 via connectors 104, 105, 106.

5 [0085]

The semiconductor elements 94, 95, 96 are mounted respectively on the first main surfaces 28a, 29a, 30a of the portions (the wide portions 28B, 29B, 30B) of the output wiring boards 28, 29, 30, which are adjacent to the base end portions 34A, 35A, 36A of the output terminal boards 34, 35, 36.

10 [0086]

These semiconductor elements 94, 95, 96 are electrically connected respectively to the ground wiring boards 25, 26, 27 via connectors 107, 108, 109. The semiconductor elements 94, 95, 96 are electrically connected respectively to the second gate wiring boards 81, 83, 85 via connectors 110, 111, 112.

15 [0087]

As shown in FIG. 1, bonding wires are used as the connectors 101, 102, 103, 107, 108, 109. Additionally, bonding wires are used as the connectors 104, 105, 106, 110, 111, 112.

[0088]

20 In the first circuit unit 41, the first power supply terminal board 31, the power supply wiring board 24, the first semiconductor element 91, the first connector 101, the first output wiring board 28, and the first output terminal board 34 form a first current path 71. Here, the connector 104 is disposed so as to be away from the first current path 71 as the connector 104 extends from the first semiconductor element 91 toward the first gate wiring board 82.

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[0089]

In the second circuit unit 42, the second power supply terminal board 32, the power supply wiring board 24, the second semiconductor element 92, the second connector 102, the second output wiring board 29, and the second output terminal board 35 form a first current path 73. Here, the connector 105 is disposed so as to be away from the first current path 73 as the connector 105 extends from the second semiconductor element 92 toward the first gate wiring board 84.

30

[0090]

In the third circuit unit 43, the third power supply terminal board 33, the power supply wiring board 24, the third semiconductor element 93, the third connector 103, the third output wiring board 30, and the third output terminal board 36 form a first current path 75. Here, the connector 106 is disposed so as to be away from the first current path 75 as the connector 106 extends from the third semiconductor element 93 toward the first gate wiring board 86.

[0091]

In the first circuit unit 41, the first output terminal board 34, the first output wiring board 28, the fourth semiconductor element 94, the fourth connector 107, the first ground wiring board 25, and the first ground terminal board 37 form a second current path 72. Here, the connector 110 is disposed so as to be away from the second current path 72 as the connector 110 extends from the fourth semiconductor element 94 toward the second gate wiring board 81.

[0092]

In the second circuit unit 42, the second output terminal board 35, the second output wiring board 29, the fifth semiconductor element 95, the fifth connector 108, the second ground wiring board 26, and the second ground terminal board 38 forms a second current path 74. Here, the connector 111 is disposed so as to be away from the second current path 74 as the connector 111 extends from the fifth semiconductor element 95 toward the second gate wiring board 83.

[0093]

In the third circuit unit 43, the third output terminal board 36, the third output wiring board 30, the sixth semiconductor element 96, the sixth connector 109, the third ground wiring board 27, and the third ground terminal board 39 form a second current path 76. Here, the connector 112 is disposed so as to be away from the second current path 76 as the connector 112 extends from the sixth semiconductor element 96 toward the second gate wiring board 85.

[0094]

The semiconductor elements 91, 92, 93 disposed respectively on the three wide portions 24B of the power supply wiring board 24 are arranged separately in a direction (the long-side direction X of the device main body 20) orthogonal to the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20) to constitute a first element

group.

[0095]

Meanwhile, the semiconductor elements 94, 95, 96 disposed respectively on the wide portions 28B, 29B, 30B of the three output wiring boards 28, 29, 30 are arranged separately in a direction (the long-side direction X of the device main body 20) orthogonal to the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20) to constitute a second element group.

[0096]

The center of the fifth semiconductor element 95 included in the second element group is disposed between the centers of the first semiconductor element 91 and the second semiconductor element 92 which are included in the first element group, in the direction (the long-side direction X of the device main body 20) orthogonal to the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20).

[0097]

Additionally, the center of the sixth semiconductor element 96 included in the second element group is disposed between the centers of the second semiconductor element 92 and the third semiconductor element 93 which are included in the first element group, in the direction (the long-side direction X of the device main body 20) orthogonal to the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20).

[0098]

The sealing resin 50 seals the power supply wiring board 24, the output wiring boards 28, 29, 30, and the ground wiring boards 25, 26, 27 so that the second main surfaces of the power supply wiring board 24, the output wiring boards 28, 29, 30 and the ground wiring boards 25, 26, 27 (the surface opposite to the first main surface, *i.e.*, the lower surface 20b of the device main body 20) are exposed.

[0099]

Additionally, as shown in FIG. 1, through holes 51, 51 penetrating, in the thickness direction of, the power supply wiring board 24, the output wiring boards 28, 29, 30, and the ground wiring boards 25, 26, 27 may be formed in the sealing resin 50.

[0100]

As shown in FIG. 1, it is preferable that the through holes 51, 51 of the sealing resin 50 are formed at both ends of the sealing resin 50 in a direction (the long-side direction X of the device main body 20) orthogonal to the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20).

[0101]

Materials of the power supply wiring board 24, the ground wiring boards 25, 26, 27, the output wiring boards 28, 29, 30, the gate wiring boards 81 to 86, the power supply terminal boards 31, 32, 33, the output terminal boards 34, 35, 36, the ground terminal boards 37, 38, 39, and the gate terminal boards 61 to 66 are not particularly limited, but may be, for example, materials to be used for general lead frames, such as copper.

[0102]

The sealing resin 50 is not particularly limited, but may be, for example, a material to be generally used for sealing a semiconductor device.

[0103]

An example of a circuit diagram of the semiconductor device 10 of the present embodiment is as shown in FIG. 3.

[0104]

In the embodiment shown in FIGS. 1 and 3, the first semiconductor element 91, the second semiconductor element 92, the third semiconductor element 93, the fourth semiconductor element 94, the fifth semiconductor element 95, and the sixth semiconductor element 96 are switching elements each including a drain electrode, a source electrode, and a gate electrode. In this case, the semiconductor device 10 of the present embodiment can be used for controlling operation of a motor (*e.g.*, a three-phase motor).

[0105]

In the semiconductor device 10 of the present embodiment, the power supply terminal boards 31, 32, 33 are connected to a DC power supply (not shown). When a direct current flows through the power supply terminal boards 31, 32, 33, and a gate signal is intermittently applied to the gate electrodes of the semiconductor elements 91, 92, 93 which are switching elements, a direct current intermittently flows in the first current paths 71, 73, 75 from the power supply terminal boards 31, 32, 33 toward the

output terminal boards 34, 35, 36.

[0106]

On the other hand, when a gate signal is intermittently applied to the gate electrodes of the semiconductor elements 94, 95, 96 which are switching elements, an alternate current flows in the second current paths 72, 74, 76 between the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39.

[0107]

Although the semiconductor device 10 including the three circuit units 41, 42, 43 has been illustrated in present embodiment, the present embodiment is not limited thereto. It is sufficient that the semiconductor device of the present embodiment includes at least one circuit unit.

[0108]

Although the case where bonding wires are used as the connectors 101, 102, 103, 107, 108, 109 has been illustrated in the present embodiment as shown in FIG. 1, the present embodiment is not limited thereto. As shown in FIG. 4, the connectors 101, 102, 103, 107, 108, 109 according to present embodiment may be conductive board materials.

[0109]

As shown in FIG. 5, the semiconductor device 10 of the present embodiment may be configured such that the power supply wiring board 24 and the output wiring boards 28, 29, 30 are connected by first capacitors 121, 122, 123, and the output wiring boards 28, 29, 30 and the ground wiring boards 25, 26, 27 are connected by second capacitors 124, 125, 126. In other words, the circuit units 41, 42, 43 of the present embodiment may include the capacitors 121 to 126.

[0110]

In FIG. 5, the first capacitors 121 to 123 are connected in parallel with the semiconductor elements 91 to 93, between the power supply wiring board 24 and the output wiring boards 28 to 30. Additionally, the second capacitors 124 to 126 are connected in parallel with the semiconductor elements 94 to 96, between the output wiring boards 28, 29, 30 and the ground wiring boards 25, 26, 27.

[0111]

According to the present embodiment, the semiconductor device 10 includes the device main body 20, the single power supply wiring board 24, the plurality of output wiring boards 28 to 30, and the plurality of semiconductor elements 91 to 96. The

device main body 20 has the first main surface 20a, the second main surface 20b, the first side surface 20c, and the second side surface 20d. The second main surface 20b opposes the first main surface 20a. The second side surface 20d opposes the first side surface 20c in the short-side direction Y of the first main surface 20a. The single power supply wiring board 24 has plural pairs of narrow portions 24A and wide portions 24B connected alternately in the long-side direction X of the first main surface 20a. The wide portions protrude toward the first side surface 20c side with respect to the narrow portions 24A. The plurality of output wiring boards 28 to 30 are arranged in the long-side direction X along the power supply wiring board 24. The number of the output wiring boards 28 to 30 is equal to the number of the pairs of narrow portions 24A and wide portions 24B of the power supply wiring board 24. Each of the output wiring boards 28 to 30 has a narrow portion 28A and a wide portion 28B connected in the long-side direction X. The wide portion 28B protrudes toward the second side surface 20d side with respect to the narrow portion 28A. Each of the plurality of semiconductor elements 91 to 96 is disposed on a different one of the wide portions 24B of the power supply wiring board 24 and the wide portions 28B to 30B of the output wiring boards 28 to 30. In the long-side direction X, the narrow portion (28A) of one of any two adjacent output wiring boards (*e.g.*, 28 and 29) faces the wide portion (29B) of another one (29) of the any two adjacent output wiring boards (28 and 29). In the short-side direction Y, the narrow portion (28A) and the wide portion (28B) of each of the output wiring boards respectively face the wide portion 24B and the narrow portion 24A, in a single pair, of the power supply wiring board 24. In the long-side direction X, a width of each of the output wiring boards (*e.g.*, 28) is smaller than a sum of widths of the narrow portion 24A and the wide portion 24B, in a single pair, of the power supply wiring board 24.

[0112]

This makes it possible to secure regions for providing wiring boards other than the power supply wiring board and the output wiring boards, between two adjacent wide portions of the power supply wiring board 24 in the long-side direction X, that is, between each narrow portion 24A of the power supply wiring board 24 and the first side surface 20c of the device main body 20 in the short-side direction Y.

[0113]

Further, it is also possible to secure regions for providing wiring boards other than the power supply wiring board and the output wiring boards, between two adjacent

output wiring boards (*e.g.*, 28 and 29) in the long-side direction X, and between the narrow portion of each output wiring board and the second side surface 20d of the device main body 20.

[0114]

5 Therefore, the above-described ground wiring board, the first gate wiring boards, and the second gate wiring boards can be arranged in those regions while ensuring the pitch among terminal boards to be connected to the respective wiring boards. Accordingly, by disposing these wiring boards, it is possible to increase the heat dissipation area while securing the pitch between the adjacent terminal boards.

10 [0115]

 Additionally, those regions secured in this way cannot be secured in a case where the power supply wiring board 24 and each output wiring board are disposed so as to be engaged with each other, that is, in a case where the wide portion 24B of the power supply wiring board 24 protrudes toward the second side surface 20d side of the device main body 20, instead of the first side surface 20c side thereof, and the wide portion of each output wiring board protrudes toward the first side surface 20c side of the device main body 20, instead of the second side surface 20d side thereof.

[0116]

 For this reason, further downsizing of the semiconductor device 10 can be realized by the arrangement configuration of the power supply wiring board 24 and the plurality of output wiring boards 28 to 30 according to the present embodiment.

[0117]

 Additionally, according to the present embodiment, the semiconductor device further includes a plurality of ground wiring boards 25 to 27 each disposed on a different one of regions each surrounded by two adjacent wide portions 24B, in the long-side direction X, of the power supply wiring board 24 and one narrow portion 24A of the power supply wiring board 24 which connects the two adjacent wide portions 24B. In the short-side direction Y, each ground wiring board (*e.g.*, 25) of the ground wiring boards 25 to 27 faces the wide portion 28B of one output wiring board 28 via one narrow portion 24A of the power supply wiring board 24.

30

[0118]

 This makes it possible to, similarly to the above, increase the heat dissipation area while securing the pitch between the adjacent terminal boards, and to further reduce

the size of the semiconductor device.

[0119]

Further, according to the present embodiment, the semiconductor device 10 further includes: a plurality of first gate wiring boards 82, 84, 86 and a plurality of
 5 second gate wiring boards 81, 83, 85. Each of the first gate wiring boards 82, 84, 86 is disposed between two adjacent output wiring boards (*e.g.*, 28 and 29) in the long-side direction X. Each of the second gate wiring boards 82, 84, 86 is disposed on a different one of regions each surrounded by one first gate wiring board (*e.g.*, 82), the narrow portion (28A) of one output wiring board (28) adjacent to the one first gate wiring board
 10 (82), and the wide portion (28B) of the one output wiring board (28) which is connected to the narrow portion (28A) thereof.

[0120]

This makes it possible to, similarly to the above, increase the heat dissipation area while securing the pitch between the adjacent terminal boards, and to further reduce
 15 the size of the semiconductor device.

[0121]

Moreover, according to the present embodiment, the device main body 20 includes a plurality of circuit units 41, 42, 43. Each circuit unit (*e.g.*, 41) of the circuit units 41, 42, 43 includes the narrow portion (24A) and the wide portion (24B), in a single
 20 pair, of the power supply wiring board (24), one output wiring board (28), one ground wiring board (25), one first gate wiring board (82), and one second gate wiring board (81).

[0122]

This makes it possible to, similarly to the above, increase the heat dissipation
 25 area while securing the pitch between the adjacent terminal boards, and to further reduce the size of the semiconductor device.

[0123]

Additionally, since each circuit unit has the same configuration, the process of manufacturing the semiconductor device 10 can be simplified. More specifically, since
 30 the shape and arrangement of each wiring board and each semiconductor element are the same between each circuit unit, it is no longer necessary to position the semiconductor element for each circuit unit in a step of mounting each of the semiconductor elements 91 to 96 on a different one of the wide portions 24B of the power supply wiring board 24

and the wide portions 28B to 30B of the output wiring boards 28 to 30.

[0124]

Further, according to the semiconductor device 10 of the present embodiment, each of the circuit units (*e.g.*, 41) further includes the first connector (101), the second
 5 connector (107), the third connector (104), and the fourth connector (110). The first connector (101) electrically connects the first semiconductor element (91) disposed on the wide portion 24B of the power supply wiring board 24 and the narrow portion (28A) of one output wiring board (28). The second connector (107) electrically connects the second semiconductor element (94) disposed on the wide portion (28B) of one output
 10 wiring board (28) and one ground wiring board (25). The third connector (104) electrically connects the first semiconductor element (91) and one first gate wiring board (82). The fourth connector (110) electrically connects the second semiconductor element (94) and the one second gate wiring board (81).

[0125]

15 Thus makes it possible to increase the heat dissipation area while ensuring the pitch between the adjacent terminal boards, and to further reduce the size of the semiconductor device.

[0126]

Additionally, since each circuit unit has the same configuration, the process of
 20 manufacturing the semiconductor device 10 can be simplified. More specifically, since the shape and arrangement of each wiring board and each semiconductor element are the same between each circuit unit, electrical connection with high accuracy is enabled without rotationally moving the device main body 20 in a step of electrically connecting the first semiconductor element and the first gate wiring board with the first connector,
 25 and in a step of electrically connecting the second semiconductor element and the second gate wiring board with the second connector.

[0127]

Further, according to the present embodiment, the semiconductor device 10 further includes the plurality of power supply terminal boards 31 to 33, the plurality of
 30 ground terminal boards 37 to 39, the plurality of output terminal boards 34 to 36, the plurality of first gate terminal boards 62, 64, 66, and the plurality of second gate terminal boards 61, 63, 65. The plurality of power supply terminal boards 31 to 33 are integrally connected respectively to the wide portions 24B of the power supply wiring board 24 and

protrude respectively from the wide portions 24B toward the first side surface 20c side of the device main body 20 in plan view. The plurality of ground terminal boards 37 to 39 are integrally connected respectively to the ground wiring boards 25 to 27 and protrude respectively from the ground wiring boards 25 to 27 toward the first side surface 20c side of the device main body 20 in plan view. The plurality of output terminal boards 34 to 36 are integrally connected respectively to the wide portions 28B to 30B of the output wiring boards 28 to 30 and protrude respectively from the wide portions 28B to 30B of the output wiring boards 28 to 30 toward the second side 20d surface of the device main body 20 in plan view. The plurality of first gate terminal boards 62, 64, 66 are integrally connected respectively to the first gate wiring boards 82, 84, 86 and protrude toward the second side surface 20d side of the device main body 20 in plan view. The plurality of second gate terminal boards 61, 63, 65 are integrally connected respectively to the second gate wiring boards 81, 83, 85 and protrude toward the second side surface 20d side of the device main body 20 in plan view. The power supply terminal boards 31 to 33 and the output terminal boards 34 to 36 are larger in width in the long-side direction X than the first gate terminal boards 62, 64, 66 and the second gate terminal boards 61, 63, 65.

[0128]

This makes it possible to, similarly to the above, increase the heat dissipation area while securing the pitch between the adjacent terminal boards, and to further reduce the size of the semiconductor device.

[0129]

Moreover, according to the present embodiment, in each of the circuit units (*e.g.*, 41), the third connector (104) is disposed so as to be away from a first current path (71) as the third connector (104) extends from the first semiconductor element (91) toward one first gate wiring boards (82), the first current path (71) extending from one power supply terminal board (31) to one output terminal board (34) via the power supply wiring board 24, the first semiconductor element (91), the first connector (101), and one output wiring board (28). In each of the circuit units (*e.g.*, 41), the fourth connector (110) is disposed so as to be away from a second current path (72) as the fourth connector (110) extends from the second semiconductor element (94) toward one second gate wiring board (81), the second current path (72) extending from one output terminal board (34) to one ground terminal board (37) via one output wiring board (28), the fourth

semiconductor element (94), the fourth connector (107), and the one ground wiring board (25).

[0130]

5 This makes it possible to, similarly to the above, increase the heat dissipation area while securing the pitch between the adjacent terminal boards, and to further reduce the size of the semiconductor device.

[0131]

10 Additionally, in a step of connecting the first semiconductor element (91) and the narrow portion (28A) of the output wiring board (28) with the first connector (101), and in a step of connecting the first semiconductor element (91) and the first gate wiring board (82) with the third connector (104), even if a distance between the first connector (101) and the third connector (104) is short, connection failure can be avoided more than in the case where the first connector (101) and the third connector (104) are arranged in parallel to each other. Further, electrical interference with the current path can be more
15 suppressed than in the case where the first connector (101) and the third connector (104) are arranged in parallel to each other.

[0132]

20 Moreover, according to present embodiment, the base end portions 31A to 39A, 61A to 66A, in an extending direction, of respective terminal boards of the power supply terminal boards 31 to 33, the ground terminal boards 37 to 39, the output terminal boards 34 to 36, the first gate terminal boards 62, 64, 66, and the second gate terminal boards 61, 63, 65 form a terminal main surface that is the same flat surface as the second main surface 20b of the device main body 20. The base end portions 31A to 39A, 61A to 66A of the respective terminal boards are larger in width than the other portions 31B to 39B,
25 61B to 66B of the respective terminal boards.

[0133]

30 This makes it possible to, similarly to the above, increase the heat dissipation area while securing the pitch between the adjacent terminal boards. Therefore, the heat generated in the semiconductor elements 91 to 96 can be efficiently released to the outside. Further, the semiconductor device can be further downsized.

[0134]

Additionally, according to the present embodiment, a step is provided between the base end portion (31A to 39A, 61A to 66A) of each terminal board (the power supply

terminal boards 31, 32, 33, the output terminal boards 34, 35, 36, and the ground terminal boards 37, 38, 39, and the gate terminal boards 61 to 66) and the other portion (31B to 39B, 61B to 66B) of the terminal board.

[0135]

5 Thus makes it possible to use this step as a mark of a bending position of the terminal board.

[0136]

Further, according to the present embodiment, the wiring boards (the power supply wiring board 24, the ground wiring boards 25, 26, 27, the output wiring boards 28, 29, 30, the gate wiring boards 81 to 86) are integrally formed respectively with the

10 corresponding terminal boards (the power supply terminal boards 31, 32, 33, the output terminal boards 34, 35, 36, the ground terminal boards 37, 38, 39, and the gate terminal boards 61 to 66).

[0137]

15 This makes it possible to reduce the size of the semiconductor device 10 while suppressing the electrical loss in the semiconductor device 10.

[0138]

Moreover, according to the present embodiment, the base end portions (31A to 39A, 61A to 66A) of the terminal boards (the power supply terminal boards 31, 32, 33, the output terminal boards 34, 35, 36, and the ground terminal boards 37, 38, 39, the gate terminal boards 61 to 66), and the lower surfaces of the wiring boards (the second main surface 24b of the power supply wiring board 24, the second main surfaces 25b, 26b, 27b of the ground wiring boards 25, 26, 27, and the second main surfaces 28b, 29b, 30b of the output wiring boards 28, 29, 30) are arranged on the same surface. Additionally, the

20 semiconductor elements 91 to 96 are arranged on the first main surface of some of the wiring boards.

[0139]

Thereby, heat generated in the semiconductor elements 91 to 96 can be efficiently released to the outside.

30 [0140]

Further, according to present embodiment, the plurality of terminal boards include: the power supply terminal boards 31, 32, 33; the output terminal boards 34, 35, 36 extending from the device main body 20 in an opposite direction to the power supply

terminal boards 31, 32, 33; and the ground terminal boards 37, 38, 39 extending from the device main body 20 in the same direction as the power supply terminal boards 31, 32, 33. The plurality of wiring boards include: the power supply wiring board 24 connected to the power supply terminal boards 31, 32, 33; the ground wiring boards 25, 26, 27
 5 connected to the ground terminal boards 37, 38, 39; and the output wiring boards 28, 29, 30 connected to the output terminal boards 34, 35, 36. The power supply wiring board 24 has a plurality of narrow portions 24A and wide portions 24B which are continuously arranged in a direction orthogonal to the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39.

10 [0141]

Thereby, the heat generated in the three semiconductor elements 91, 92, 93 arranged respectively on the wide portions 24B of the power supply wiring board 24 can be uniformly dissipated throughout the power supply wiring board 24. In other words, it is possible to improve the heat dissipation efficiency.

15 [0142]

Moreover, according to the present embodiment, the semiconductor elements 91, 92, 93 arranged on the first main surface 24a of the wide portions 24B of the power supply wiring board 24 and the narrow portions 28A, 29A, 30A of the output wiring boards 28, 29, 30 are connected respectively by the connectors 101, 102, 103.

20 Additionally, the semiconductor elements 94, 95, 96 arranged respectively on the first main surfaces 28a, 29a, 30a of the wide portions 28B, 29B, 30B of the output wiring boards 28, 29, 30 and the ground wiring boards 25, 26, 27 are connected respectively by the connectors 107, 108, 109.

[0143]

25 Thereby, the heat generated in the semiconductor elements 91, 92, 93 can be efficiently transferred to the narrow portions 28A, 29A, 30A of the output wiring boards 28, 29, 30 through the connectors 101, 102, 103. Additionally, heat generated in the semiconductor elements 94, 95, 96 can be efficiently transmitted to the ground wiring boards 25, 26, 27 through the connectors 107, 108, 109. Therefore, the heat dissipation
 30 efficiency of the semiconductor device 10 can be improved.

[0144]

Further, according to the present embodiment, the connectors 101, 102, 103, 107, 108, 109 are conductive board materials.

[0145]

Since board materials are smaller in electric resistance than bonding wires, the electrical loss in the semiconductor device 10 can be reduced. Additionally, since the board materials are higher in thermal conductivity than bonding wires, it is possible to further improve the heat dissipation efficiency of the semiconductor device 10.

[0146]

Further, according to the present embodiment, the through holes 51, 51 penetrating in the thickness direction of the power supply wiring board 24, the output wiring boards 28, 29, 30, and the ground wiring boards 25, 26, 27 are formed in the sealing resin 50.

[0147]

Thereby, the semiconductor device 10 can be fixed to a heat dissipation member by screwing using the through holes 51, 51. By this fixing, the second main surfaces of the power supply wiring board 24, the output wiring boards 28, 29, 30, and the ground wiring boards 25, 26, 27 (the lower surface of the device main body 20) can be pressed against the heat dissipation member.

[0148]

This makes it possible to ensure contact between the heat dissipation member and the second main surfaces of the power supply wiring board 24, the output wiring boards 28, 29, 30, and the ground wiring boards 25, 26, 27, so that the heat generated in the semiconductor elements 91 to 96 can be efficiently released from the second main surfaces of the wiring boards to the heat dissipation member.

[0149]

Moreover, the through holes 51, 51 are formed at both ends of the sealing resin 50 in a direction orthogonal to the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39.

[0150]

This makes it possible to secure surface contact between the heat dissipation member and the second main surfaces of the power source wiring board 24, the output wiring boards 28, 29, 30, and the ground wiring boards 25, 26, 27 (the lower surface 20b of the device main body 20).

[0151]

This makes it possible to more efficiently release the heat generated in the

semiconductor elements 91 to 96 from the second main surfaces of these wiring boards to the heat dissipation member.

[0152]

5 Additionally, according to present embodiment, the plurality of terminal boards include the gate terminal boards 61 to 66 extending from the device main body 10 in the opposite direction to the power supply terminal boards 31, 32, 33.

[0153]

10 For this reason, the semiconductor device 10 can be miniaturized in the long-side direction while securing the pitch between the power supply terminal boards 31, 32, 33 and the ground terminal boards 37, 38, 39, and the pitch between the output terminal boards 34, 35, 36 and the gate terminal boards 61 to 66.

[0154]

15 Further, according to the present embodiment, the wiring boards include gate wiring boards 81, 83, 85. The terminal boards include: the power supply terminal boards 31, 32, 33 connected to the power supply wiring board 24; the ground terminal boards 37, 38, 39 connected to the ground wiring boards 25, 26, 27; the output terminal boards 34, 35, 36 connected to the output wiring boards 28, 29, 30; and the gate terminal boards 61 to 66 connected to the gate wiring boards 81, 83, 85. The power supply terminals 31, 32, 33, the output terminal boards 34, 35, 36, and the ground terminal
20 boards 37, 38, 39 are larger in width than the gate terminals 61 to 66.

[0155]

25 For this reason, it is possible to reduce the size of the semiconductor device 10 while suppressing the electrical loss in the semiconductor device 10. Since a large current flows through the power supply terminal boards 31, 32, 33, the output terminal boards 34, 35, 36, and the ground terminal boards 37, 38, 39, by widening these terminal boards, electrical resistance of these terminal boards can be suppressed, and electric loss in these terminal boards can be suppressed.

[0156]

30 On the other hand, since only a small current flows through the gate terminal boards 61 to 66, even if these terminal boards are decreased in width, it is possible to suppress electrical loss in these terminal boards.

[0157]

Moreover, according to the present embodiment, the semiconductor elements 91,

92, 93 arranged on the respective wide portions 24B of the power supply wiring board 24 are arranged separately in the direction (the long-side direction X of the device main body 20) orthogonal to the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20) to constitute the first element group. The semiconductor elements 94, 95, 96 arranged on the respective wide portions 28B, 29B, 30B of the output wiring boards 28, 29, 30 are arranged separately in the direction (the long-side direction X of the device main body 20) orthogonal to the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20) to constitute the second element group. The center of each of the semiconductor elements 95, 96 included in the second element group are positioned between the centers of two of the semiconductor elements 91, 92, 93 included in the first element group in the direction (the long-side direction X of the device main body 20) orthogonal to the arrangement direction of the output terminal boards 34, 35, 36 and the ground terminal boards 37, 38, 39 (the short-side direction Y of the device main body 20).

[0158]

For this reason, the first current paths 71, 73, 75 and the second current paths 72, 74, 76 can be further simplified. Additionally, it is possible to equalize the heat distribution in the device main body 20 based on the heat generated in the semiconductor elements 91 to 96. In other words, it is possible to prevent the concentration of heat in the device main body 20 and to improve the heat dissipation efficiency of the semiconductor device 10.

[0159]

Further, according to the present embodiment, the tip end portions of the power supply terminals 31, 32, 33, the output terminals 34, 35, 36, and the ground terminals 37, 38, 39 extending from the power supply wiring board 24, the output wiring boards 28, 29, 30, and the ground wiring boards 25, 26, 27 extend in the thickness direction of these wiring boards so as to protrude from the first main surfaces of these wiring boards.

[0160]

For this reason, the semiconductor device 10 can be connected to a circuit board or the like at a position away from the heat dissipation member with which the lower surface of the semiconductor device 10 contacts.

[0161]

Moreover, according to the present embodiment, the power supply wiring board 24 and each of the output wiring boards 28, 29, 30 are connected by the capacitors 121, 122, 123, while the output wiring boards 28, 29, 30 and the ground wiring boards 25, 26, 27 are connected by the capacitors 124, 125, 126.

[0162]

In a case where the semiconductor elements 91 to 96 are switching elements such as MOF-FETs and IGBTs to be mounted on on-vehicle electrical equipment, a current is intermittently flowed by switching of the semiconductor elements 91 to 96.

By providing the semiconductor device 10 with the capacitors 121 to 126, voltage fluctuation at the time of switching of the semiconductor elements 91 to 96 can be reduced.

[0163]

[Lead frame]

Hereinafter, a lead frame according to an embodiment of the present invention will be described with reference to the drawings.

[0164]

As shown in FIG. 6, a lead frame 200 of the present embodiment is configured such that the plurality of wiring boards (the power supply wiring board 24, the ground wiring boards 25, 26, 27, the output wiring boards 28, 29, 30, and the gate wiring boards 81 to 86), the plurality of terminal boards (the power supply terminal boards (leads) 31, 32, 33, the output terminal boards (leads) 34, 35, 36, the ground terminal boards (leads) 37, 38, 39, and the gate terminal boards 61 to 66) are integrally formed, and the plurality of terminal boards are connected by connecting portions (tie bars 201, 202, and a frame portion 203).

[0165]

In the present embodiment, in the lead frame 200 shown in FIG. 6, the same components as those of the semiconductor device 10 shown in FIG. 1 are appended with the same reference numerals, and description of these components are omitted here.

[0166]

The tie bars 201, 202 of the connecting portions are formed so as to connect, in the arrangement direction of the terminal boards, the portions of the terminal boards adjacent to the wiring boards (the base end portions (31A to 39A, 61A to 66A)).

[0167]

The frame portion 203 of the connecting portions is formed so as to connect portions of the terminal boards on the side opposite to the wiring boards (the top end portions (31B to 39B, 61B to 66B)) and portions of the tie bars 201, 202 to be separated from the terminal boards, and to surround the wiring boards and the terminal boards.

[0168]

The lead frame 200 of the present embodiment is used as a lead frame for the semiconductor device 10.

[0169]

In other words, the lead frame 200 of the present embodiment is used as the plurality of wiring boards (the power supply wiring board 24, the ground wiring boards 25, 26, 27, the output wiring boards 28, 29, 30, and the gate wiring boards 81 to 86) and the plurality of terminal boards (the power supply terminal boards (leads) 31, 32, 33, the output terminal boards (leads) 34, 35, 36, and the ground terminal boards (leads) 37, 38, 39, the gate terminal boards 61 to 66).

[0170]

The above-described semiconductor device 10 can be manufactured using the lead frame 200 of the present embodiment.

DESCRIPTION OF REFERENCE NUMERALS

[0171]

- 10 semiconductor device
- 20 device main body
- 21, 22, 23 device unit
- 24 power supply wiring board
- 25, 26, 27 ground wiring board
- 28, 29, 30 output wiring board
- 31, 32, 33 power supply terminal board
- 34, 35, 36 output terminal board
- 37, 38, 39 ground terminal board
- 41, 42, 43 circuit unit
- 50 sealing resin

	51	through hole
	61, 62, 63, 64, 65, 66	gate terminal board
	71, 73, 75	first current path
	72, 74, 76	second current path
5	81, 82, 83, 84, 85, 86	gate wiring board
	91, 92, 93, 94, 95, 96	semiconductor element
	101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112	connector
	121, 122, 123, 124, 125, 126	capacitor
	200	lead frame
10	201, 202	tie bar
	203	frame portion

Conclusies

1. Halfgeleiderinrichting omvattende:
 een hoofdlichaam met een eerste hoofdoppervlak, een tweede hoofdoppervlak,
 een eerste zijvlak en een tweede zijvlak, met het tweede hoofdoppervlak
 tegenover het eerste hoofdoppervlak, en met het tweede zijvlak tegenover het
 5 eerste zijvlak in een korte-zijde richting van het eerste hoofdoppervlak;
 een enkele voeding-bedradingsplaat met verscheidene paren van smalle
 gedeelten en brede gedeelten die elkaar afwisselen en onderling verbonden zijn
 in de lange-zijde richting van het eerste hoofdoppervlak, waarbij de brede
 gedeelten uitsteken naar een zijde van het eerste zijvlak ten opzichte van de
 10 smalle gedeelten;
 verscheidene uitgang-bedradingsplaten aangebracht in de lange-zijde richting
 langs de voeding-bedradingsplaat, waarbij een aantal van de uitgang-
 bedradingsplaten gelijk is aan een aantal paren van smalle gedeelten en brede
 gedeelten van de voeding-bedradingsplaat, waarbij elk van de uitgang-
 15 bedradingsplaten een smal gedeelte en een breed gedeelte heeft die in de lange-
 zijde richting onderling zijn verbonden, waarbij het brede gedeelte uitsteekt naar
 een zijde van het tweede zijvlak ten opzichte van het smalle gedeelte; en
 verscheidene halfgeleiderelementen die elk aangebracht zijn op een andere van
 de brede gedeelten van de voeding-bedradingsplaat en de brede gedeelten van de
 20 uitgang-bedradingsplaten,
 waarbij in de lange-zijde richting het smalle gedeelte van om het even welk van
 twee aangrenzende uitgang-bedradingsplaten toegekeerd is naar het brede
 gedeelte van de andere van de twee van om het even welke aangrenzende
 uitgang-bedradingsplaten,
 25 waarbij in de korte-zijde richting het smalle gedeelte en het brede gedeelte van
 elk van de uitgang-bedradingsplaten respectievelijk toegekeerd zijn naar het
 brede gedeelte en het smalle gedeelte, in een enkel paar, van de voeding-
 bedradingsplaat en

waarbij in de lange-zijde richting, een breedte van elk van de uitgang-bedradingsplaten kleiner is dan een som van breedten van het smalle gedeelte en het brede gedeelte, in een enkel paar, van de voeding-bedradingsplaat.

- 5 2. De halfgeleiderinrichting volgens conclusie 1, verder omvattende:
 verscheidene massa-bedradingsplaten elk aangebracht op een andere van
 gebieden en elk omringd door twee aangrenzende brede gedeelten, op de lange-
 zijde richting van de voeding-bedradingsplaat en één smal gedeelte van de
 voeding-bedradingsplaat die de twee aangrenzende brede gedeelten verbindt,
 10 waarbij in de korte-zijde richting, elk van de massa-bedradingsplaten toegekeerd
 is naar het brede gedeelte van één van de uitgang-bedradingsplaten met
 daartussen een van de smalle gedeelten van de voeding-bedradingsplaat.

3. De halfgeleiderinrichting volgens conclusie 2, verder omvattende:
 15 verscheidene eerste poort-bedradingsplaten elk aangebracht tussen twee
 naburige uitgang-bedradingsplaten op de lange-zijde richting; en
 verscheidene tweede poort-bedradingsplaten elk aangebracht op een andere van
 gebieden en elk omringd door een van de eerste poort bedradingsplaten, het
 smalle gedeelte van één van de uitgang-bedradingsplaten die grenst aan die van
 20 de eerste poort-bedradingsplaten en het brede gedeelte van de ene van de
 uitgang-bedradingsplaten die is verbonden met het smalle gedeelte van een van
 de uitgang-bedradingsplaten.

4. De halfgeleiderinrichting volgens conclusie 3, waarbij
 25 het hoofdlichaam omvat verscheidene schakelingseenheden en
 elk van de schakelingseenheden omvat het smalle gedeelte en het brede gedeelte,
 in een enkel paar, van de voeding-bedradingsplaat, een van de uitgang-
 bedradingsplaten, een van de massa-bedradingsplaten, een van de eerste poort-
 bedradingsplaten en een van de tweede poort-bedradingsplaten.

5. De halfgeleiderinrichting volgens conclusie 4, waarbij elk van de schakelingseenheden verder omvat:

een eerste verbindingselement dat een eerste halfgeleiderelement aangebracht op het brede gedeelte van de voeding-bedradingsplaat en het smalle gedeelte van

5 de ene van de uitgang-bedradingsplaten elektrisch verbindt;

een tweede verbindingselement dat een tweede halfgeleiderelement aangebracht op het brede gedeelte van de ene van de uitgang-bedradingsplaten en de ene van de massa-bedradingsplaten elektrisch verbindt;

10 een derde verbindingselement dat het eerste halfgeleiderelement en de ene van de eerste poort-bedradingsplaten elektrisch verbindt; en

een vierde verbindingselement dat het tweede halfgeleiderelement en de ene van de tweede poort-bedradingsplaten elektrisch verbindt.

6. De halfgeleiderinrichting volgens een der conclusies 3-5, verder omvattende:

15 verscheidene voeding-aansluitplaten die respectievelijk integraal zijn verbonden met de brede gedeelten van de voeding-bedradingsplaat en in bovenaanzicht respectievelijk uitsteken vanaf de brede gedeelten naar de zijkant van het eerste zijvlak van het hoofdlichaam;

20 verscheidene massa-aansluitplaten die respectievelijk integraal zijn verbonden met de verscheidene massa-bedradingsplaten en die in bovenaanzicht respectievelijk uitsteken vanaf de verscheidene massa-bedradingsplaten naar de zijde van het eerste zijvlak van het hoofdlichaam;

25 verscheidene uitgang-aansluitplaten die respectievelijk integraal zijn verbonden met de brede gedeelten van de uitgang-bedradingsplaten en die in bovenaanzicht respectievelijk uitsteken vanaf de brede gedeelten van de uitgang-

bedradingsplaten naar de zijde van het tweede zijvlak van het hoofdlichaam;

verscheidene eerste poort-aansluitplaten die respectievelijk integraal zijn verbonden met de eerste poort-bedradingsplaten en die in bovenaanzicht uitsteken naar de zijde van het tweede zijvlak van het hoofdlichaam; en

verscheidene tweede poort-aansluitplaten die respectievelijk integraal zijn verbonden met de tweede poort-bedradingsplaten en die in bovenaanzicht uitsteken naar de zijde van het tweede zijvlak van het hoofdlichaam, waarbij de voeding-aansluitplaten en de uitgang-aansluitplaten een grotere
 5 breedte in de lange-zijde richting hebben dan de eerste poort-aansluitplaten en de tweede poort-aansluitplaten.

7. De halfgeleiderinrichting volgens conclusie 6, waarbij
 in elk van de schakelingseenheden, het derde verbindingselement is aangebracht
 10 om op afstand te zijn van een eerste stroompad, doordat het derde verbindingselement zich uitstrekt vanaf het eerste halfgeleiderelement naar het ene van de eerste poort-bedradingsplaten, waarbij het eerste stroompad zich vanaf een van de voeding-aansluitplaten uitstrekt naar één van de uitgang-aansluitplaten via de voeding-bedradingsplaat, het eerste halfgeleiderelement,
 15 het eerste verbindingselement, en de ene van de uitgang-bedradingsplaten en in elk van de schakelingseenheden, het vierde verbindingselement is aangebracht om op afstand te zijn van een tweede stroompad doordat het vierde verbindingselement zich uitstrekt vanaf het tweede halfgeleiderelement naar de ene van de tweede poort-bedradingsplaten, waarbij het tweede stroompad zich
 20 vanaf een van de uitgang-aansluitplaten uitstrekt naar een van de massa-aansluitplaten via een van de uitgang-bedradingsplaten, het vierde halfgeleiderelement, het vierde verbindingselement, en de ene van de massa-bedradingsplaten.

25 8. De halfgeleiderinrichting volgens conclusie 6, waarbij basis eindgedeelten, in een uitbreidingsrichting, van respectieve aansluitplaten van de voeding-aansluitplaten, de massa-aansluitplaten, de uitgang-aansluitplaten, de eerste poort-aansluitplaten, en de tweede poort-aansluitplaten een aansluit-hoofdoppervlak hebben dat hetzelfde vlakke oppervlak is als het
 30 tweede hoofdoppervlak van het hoofdlichaam, en

de basis eindgedeelten van de respectievelijke aansluitplaten een grotere breedte hebben dan andere gedeelten van de respectievelijke aansluitplaten.

9. De halfgeleiderinrichting volgens conclusie 8, waarbij

- 5 een stap is voorzien tussen het basis eindgedeelte van elke aansluit plaat en het andere gedeelte van de aansluitplaat.

10. De halfgeleiderinrichting volgens conclusie 8 of 9, waarbij

- de halfgeleiderelementen worden aangebracht op eerste hoofdoppervlakken van
10 de voeding-bedradingsplaat en de uitgang bedradingsplaten en
tweede hoofdoppervlakken van de respectievelijke bedradingsplaten vormen het
tweede hoofdoppervlak van het hoofdlichaam.

11. De halfgeleiderinrichting volgens conclusie 5, waarbij

- 15 het eerste verbindingselement tot en met het vierde verbindingselement
geleidende plaatmaterialen zijn.

12. De halfgeleiderinrichting volgens conclusie 10 of 11, waarbij

- het hoofdlichaam omvat verder een hars die de respectieve bedradingsplaten
20 afdicht zodat de tweede hoofdoppervlakken van de respectievelijke
bedradingsplaten zijn blootgesteld en
de hars aan beide uiteinden doorgaande gaten heeft, in de richting van de lange-
zijde van het hoofdlichaam, waarbij de doorgaande gaten doordringen in een
dikterichting van de respectievelijke bedradingsplaten.

25

13. De halfgeleiderinrichting volgens een der conclusies 10 tot 12, waarbij

uiteindedelen van de respectievelijke aansluitplaten uitstrekken in de
dikterichting van de respectievelijke bedradingsplaten teneinde uit te steken
naar een zijde van het eerste hoofdoppervlak.

30

14. De halfgeleiderinrichting volgens een der conclusies 2-13, verder omvattende:

verscheidene eerste condensatoren die elk de voeding-bedradingsplaat met een andere van de uitgang-bedradingsplaten verbinden; en
 verscheidene tweede condensatoren die respectievelijk de uitgang bedradingsplaten en de massa-bedradingsplaten .

5

15. Een hoofdframe voor de halfgeleiderinrichting volgens één van de conclusies 6 tot 14, waarbij het hoofdframe omvat:

verscheidene aansluitplaten omvattende de verscheidene voedings-
 aansluitplaten, de verscheidene massa-aansluitplaten, de verscheidene uitgang-
 10 aansluitplaten, de verscheidene eerste poort-aansluitplaten, en de verscheidene
 tweede poort-aansluitplaten; en
 verscheidene verbindingsdelen die de verscheidene aansluitplaten verbinden.

FIG. 1

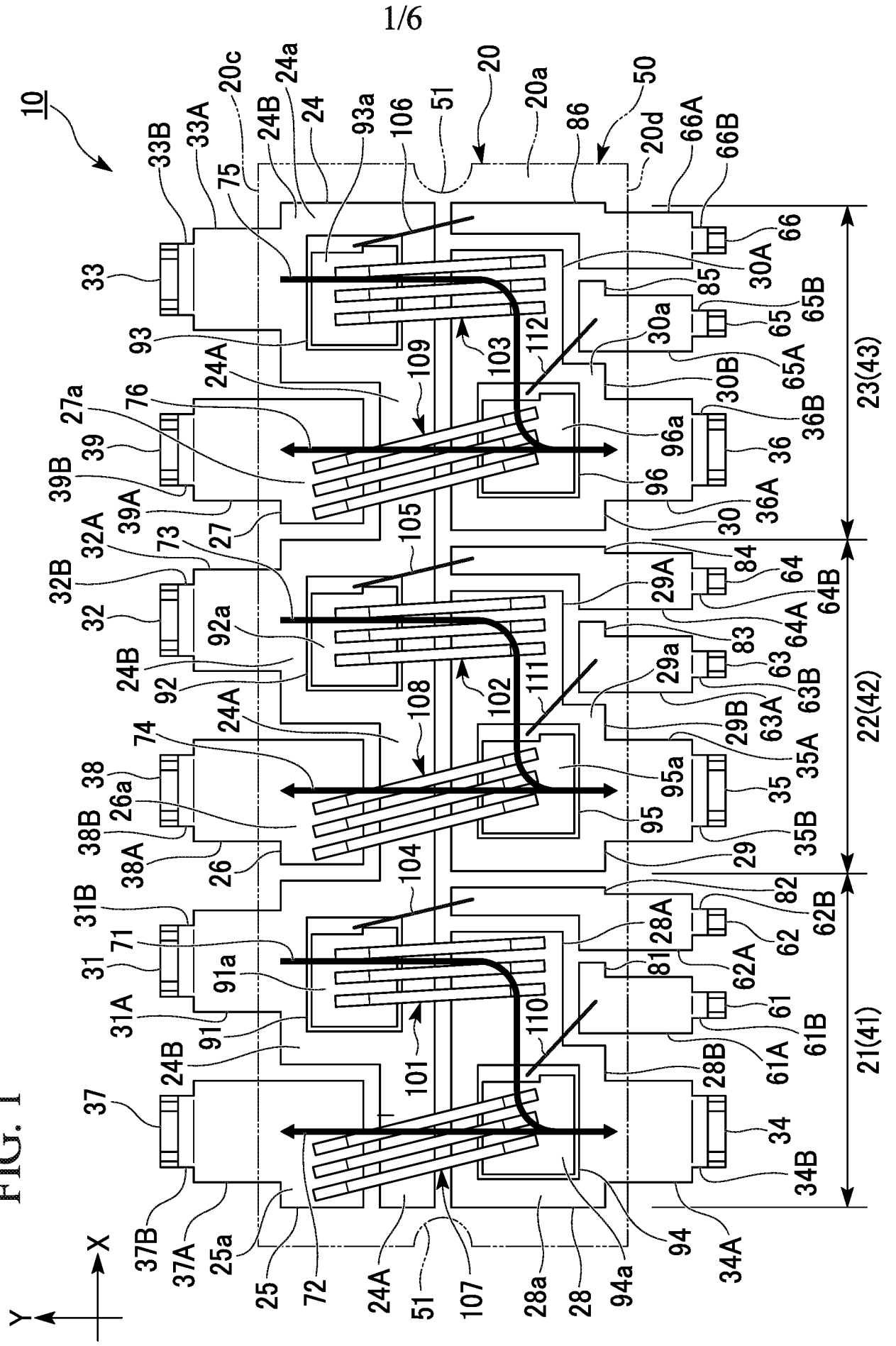


FIG. 2

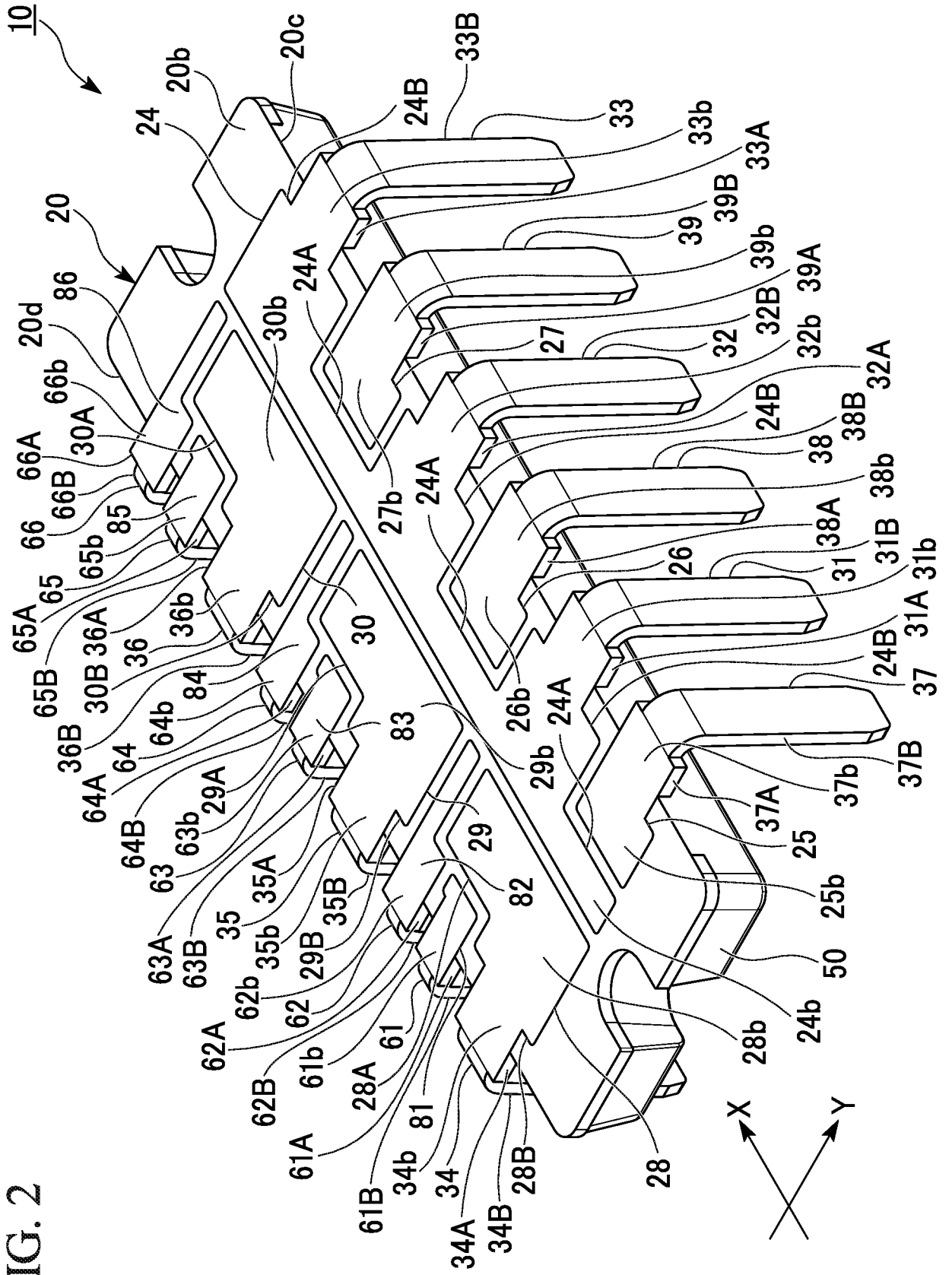


FIG. 3

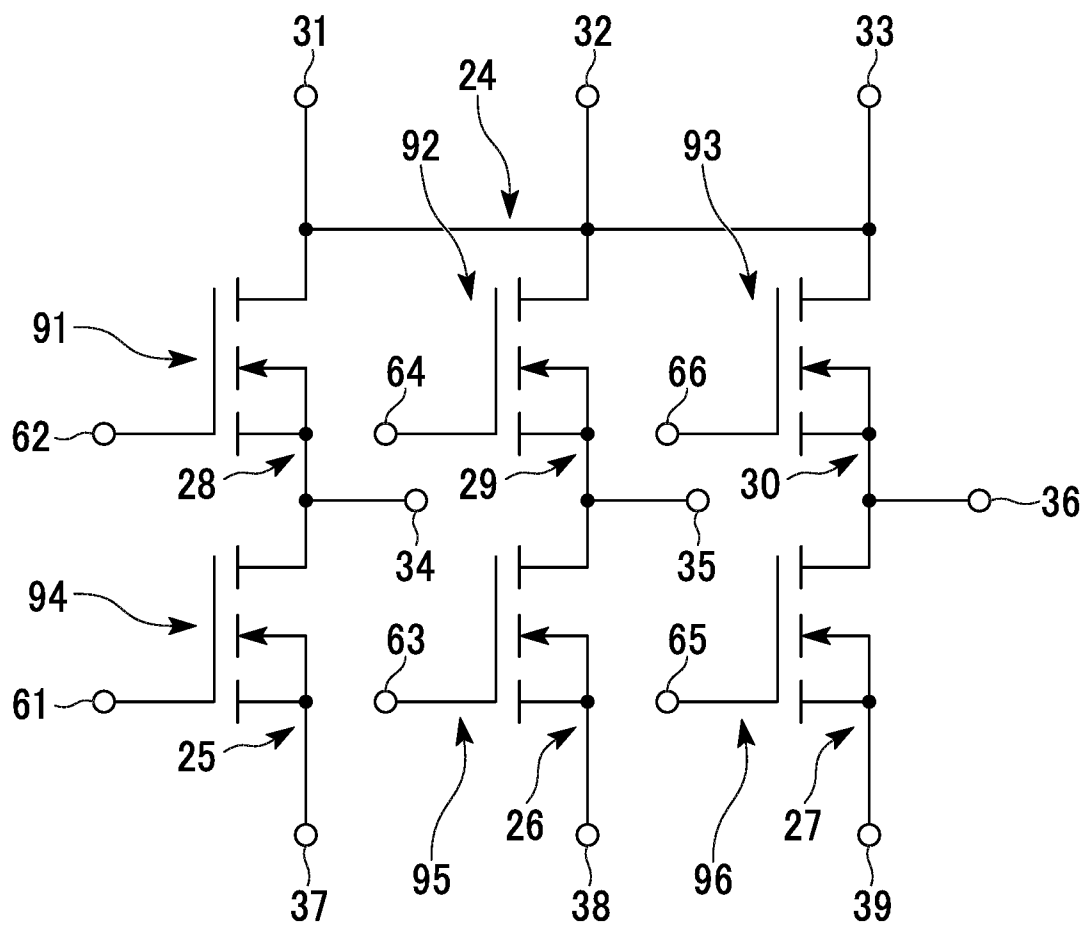


FIG. 4

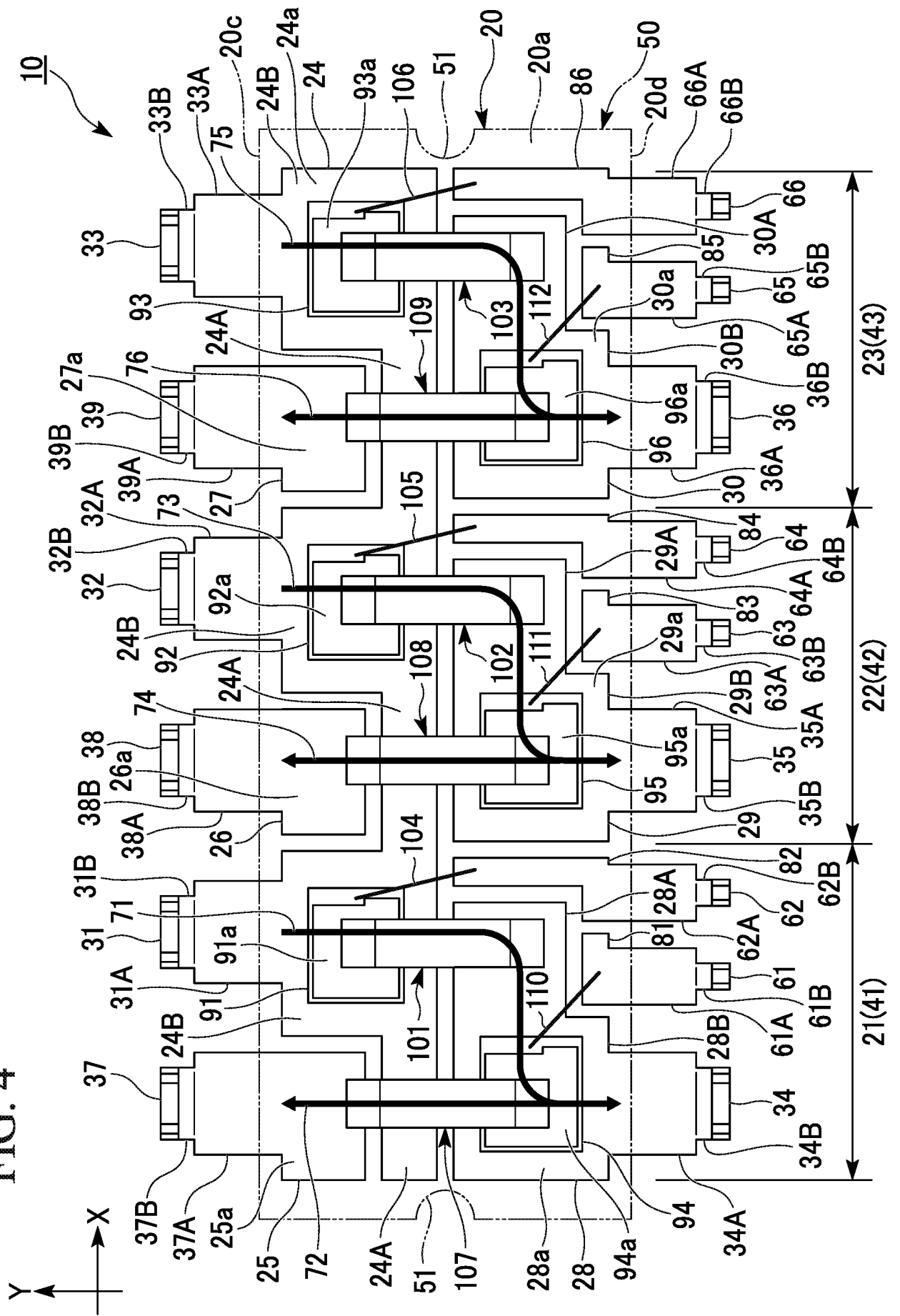


FIG. 5

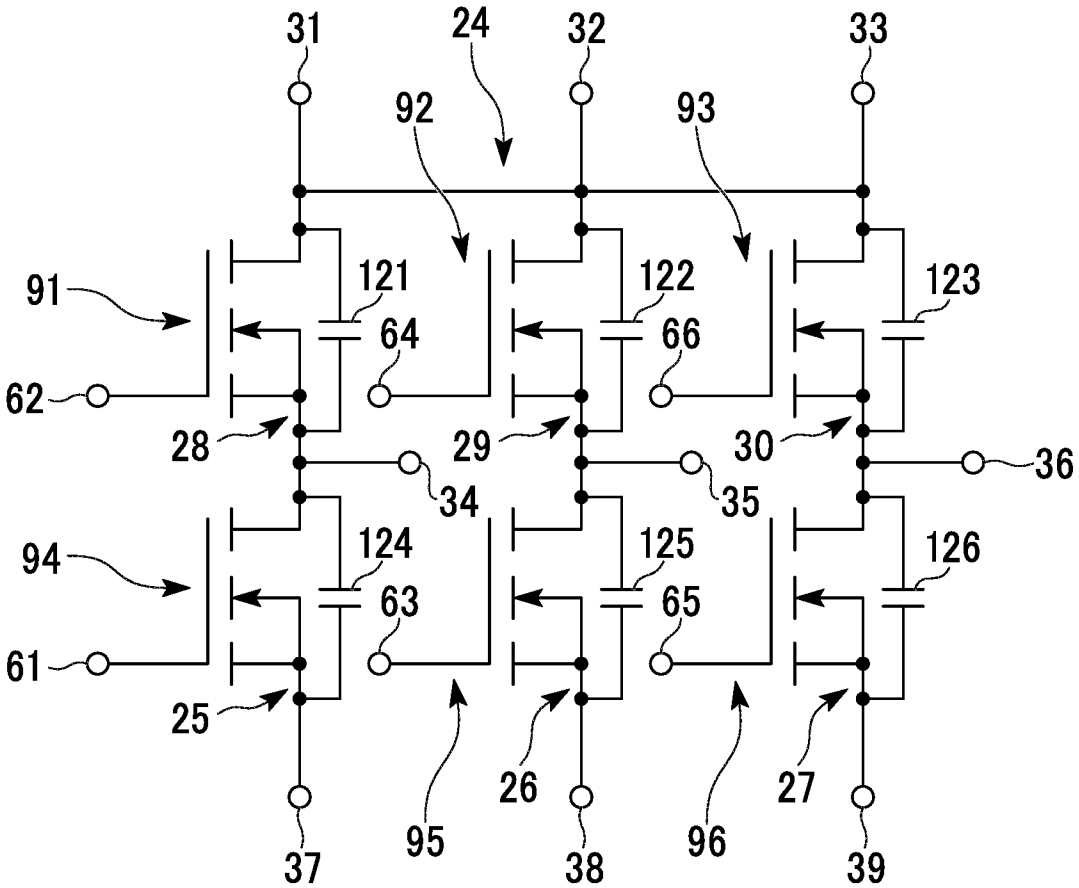
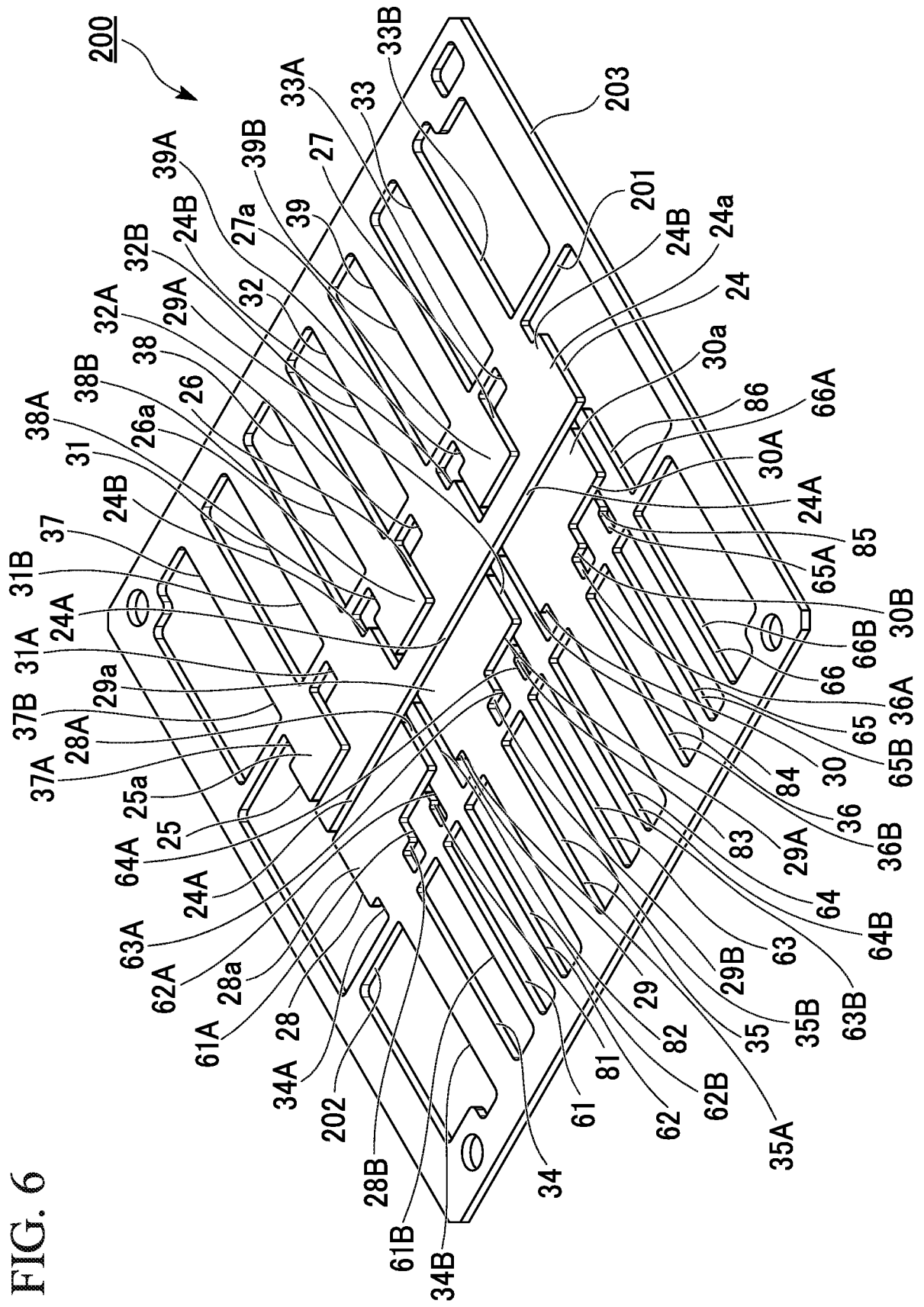


FIG. 6



ABSTRACT

A semiconductor device according to a first aspect of the present invention includes a device main body, a single power supply wiring board, a plurality of output wiring boards, and a plurality of semiconductor elements. In a long-side direction of the device main body, the narrow portion of one of any two adjacent wiring boards faces the wide portion of another one of the any two adjacent wiring boards. In a short-side direction of the device main body, the narrow portion and the wide portion of each of the output wiring boards respectively face the wide portion and the narrow portion, in a single pair, of the power supply wiring board. In the long-side direction of the device main body a width of each of the output wiring boards is smaller than a sum of widths of the narrow portion and the wide portion, in a single pair, of the power supply wiring board.

FIG. 1



Rijksdienst voor Ondernemend
Nederland

OCTROOIAANVRAAG NR.:
NO 139793
NL 2018487

ONDERZOEKSRAPPORT

BETREFFENDE HET RESULTAAT VAN HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK

RELEVANTE LITERATUUR			
Categorie ¹	Literatuur met, voor zover nodig, aanduiding van speciaal van belang zijnde tekstgedeelten of figuren	Van belang voor conclusie(s) nr.	Classificatie (IPC)
A, D	US 2013/221516 A1 (ASADA SHINSUKE [JP] ET AL) 29 augustus 2013 (2013-08-29) * figuren 1,2 *	1,15	INV. H01L25/07 H01L23/495
A	US 2013/020687 A1 (KIM KWANG SOO [KR] ET AL) 24 januari 2013 (2013-01-24) * figuur 1 *	1	
			Onderzochte gebieden van de techniek
			H01L
Indien gewijzigde conclusies zijn ingediend, heeft dit rapport betrekking op de conclusies ingediend op:			
Plaats van onderzoek:		Datum waarop het onderzoek werd voltooid:	Bevoegd ambtenaar:
's-Gravenhage		25 augustus 2017	Gélébart, Jacques
¹ CATEGORIE VAN DE VERMEDELDE LITERATUUR			
X: de conclusie wordt als niet nieuw of niet inventief beschouwd ten opzichte van deze literatuur Y: de conclusie wordt als niet inventief beschouwd ten opzichte van de combinatie van deze literatuur met andere geciteerde literatuur van dezelfde categorie, waarbij de combinatie voor de vakman voor de hand liggend wordt geacht A: niet tot de categorie X of Y behorende literatuur die de stand van de techniek beschrijft O: niet-schriftelijke stand van de techniek P: tussen de voorrangsdatum en de indieningsdatum gepubliceerde literatuur T: na de indieningsdatum of de voorrangsdatum gepubliceerde literatuur die niet bezwarend is voor de octrooiaanvraag, maar wordt vermeld ter verheldering van de theorie of het principe dat ten grondslag ligt aan de uitvinding E: eerdere octrooi(aanvraag), gepubliceerd op of na de indieningsdatum, waarin dezelfde uitvinding wordt beschreven D: in de octrooiaanvraag vermeld L: om andere redenen vermelde literatuur S: lid van dezelfde octrooifamilie of overeenkomstige octrooipublicatie			

**AANHANGSEL BEHORENDE BIJ HET RAPPORT BETREFFENDE
HET ONDERZOEK NAAR DE STAND VAN DE TECHNIEK,
UITGEVOERD IN DE OCTROOIAANVRAGE NR.**

NO 139793
NL 2018487

Het aanhangsel bevat een opgave van elders gepubliceerde octrooiaanvragen of octrooien (zogenaamde leden van dezelfde octroofamilie), die overeenkomen met octrooischriften genoemd in het rapport.

De opgave is samengesteld aan de hand van gegevens uit het computerbestand van het Europees Octrooibureau per
De juistheid en volledigheid van deze opgave wordt noch door het Europees Octrooibureau, noch door het Bureau voor de Industriële eigendom gegarandeerd; de gegevens worden verstrekt voor informatiedoeleinden.

25-08-2017

In het rapport genoemd octrooigeschrift	Datum van publicatie	Overeenkomend(e) geschrift(en)	Datum van publicatie
US 2013221516 A1	29-08-2013	CN 103339724 A	02-10-2013
		EP 2674973 A1	18-12-2013
		JP 5669866 B2	18-02-2015
		JP WO2012108011 A1	03-07-2014
		US 2013221516 A1	29-08-2013
		WO 2012108011 A1	16-08-2012

US 2013020687 A1	24-01-2013	KR 20130011149 A	30-01-2013
		US 2013020687 A1	24-01-2013
		US 2013337613 A1	19-12-2013

SCHRIFTELIJKE OPINIE

DOSSIER NUMMER NO139793	INDIENINGSDATUM 09.03.2017	VOORRANGSDATUM 11.03.2016	AANVRAAGNUMMER NL2018487
CLASSIFICATIE INV. H01L25/07 H01L23/495			
AANVRAGER Shindengen Electric Manufacturing Co., Ltd.			

Deze schriftelijke opinie bevat een toelichting op de volgende onderdelen:

- ☒ Onderdeel I Basis van de schriftelijke opinie
- ☐ Onderdeel II Voorrang
- ☐ Onderdeel III Vaststelling nieuwheid, inventiviteit en industriële toepasbaarheid niet mogelijk
- ☐ Onderdeel IV De aanvraag heeft betrekking op meer dan één uitvinding
- ☒ Onderdeel V Gemotiveerde verklaring ten aanzien van nieuwheid, inventiviteit en industriële toepasbaarheid
- ☐ Onderdeel VI Andere geciteerde documenten
- ☐ Onderdeel VII Overige gebreken
- ☐ Onderdeel VIII Overige opmerkingen

	DE BEVOEGDE AMBTENAAR Gélébart, Jacques
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SCHRIFTELIJKE OPINIE

Aanvraag nr.:
NL2018487

Onderdeel I Basis van de Schriftelijke Opinie

1. Deze schriftelijke opinie is opgesteld op basis van de meest recente conclusies ingediend voor aanvang van het onderzoek.
2. Met betrekking tot **nucleotide en/of aminozuur sequenties** die genoemd worden in de aanvraag en relevant zijn voor de uitvinding zoals beschreven in de conclusies, is dit onderzoek gedaan op basis van:
 - a. type materiaal:
 - ☐ sequentie opsomming
 - ☐ tabel met betrekking tot de sequentie lijst
 - b. vorm van het materiaal:
 - ☐ op papier
 - ☐ in elektronische vorm
 - c. moment van indiening/aanlevering:
 - ☐ opgenomen in de aanvraag zoals ingediend
 - ☐ samen met de aanvraag elektronisch ingediend
 - ☐ later aangeleverd voor het onderzoek
3. ☐ In geval er meer dan één versie of kopie van een sequentie opsomming of tabel met betrekking op een sequentie is ingediend of aangeleverd, zijn de benodigde verklaringen ingediend dat de informatie in de latere of additionele kopieën identiek is aan de aanvraag zoals ingediend of niet meer informatie bevatten dan de aanvraag zoals oorspronkelijk werd ingediend.
4. Overige opmerkingen:

SCHRIFTELIJKE OPINIE

Aanvraag nr.:
NL2018487

Onderdeel V Gemotiveerde verklaring ten aanzien van nieuwheid, inventiviteit en industriële toepasbaarheid

1. Verklaring

Nieuwheid	Ja: Conclusies 1-15 Nee: Conclusies
Inventiviteit	Ja: Conclusies 1-15 Nee: Conclusies
Industriële toepasbaarheid	Ja: Conclusies 1-15 Nee: Conclusies

2. Citaties en toelichting:

Zie aparte bladzijde

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

Reference is made to the following document:

D1 US 2013/221516 A1 (ASADA SHINSUKE [JP] ET AL) 29 augustus 2013
(2013-08-29)

D1 is regarded as being the prior art closest to the subject-matter of claim 1, and discloses

a resin packaged power module using a lead frame which is exposed at the bottom of the package.

The subject-matter of claim 1 therefore differs from this known package in that the power leads and the output leads both have broad and narrow regions arranged to cover the back surface of the package as much as possible, and is therefore new.

The problem to be solved by the present invention may be regarded as increasing the heat distribution area while securing a sufficient pitch between adjacent terminal leads, see paragraph 5.

The solution to this problem proposed in claim 1 of the present application is considered as involving an inventive step because such an elaborated construction is not disclosed in the prior art.

Claims 2-14 are dependent on claim 1 and as such also meet the requirements of novelty and inventive step.

The lead frame of claim 15, by virtue of its dependency from claim 1, also has the elaborated construction mentioned above. Consequently, claim 15 is also new and inventive.