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(71) Applicant: **MOTOROLA, INC., A CORPORATION OF THE STATE OF DELAWARE** [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(72) Inventors: **MOSNA, Jr., Frank, J.**; 6903 S. Lakeshore Dr., Temp, AZ 85283 (US). **ELLIOT, Alexander, J.**; 1936 E. Vinedo Lane, Tempe, AZ 85284 (US). **STROM, William, M.**; 2667 Gila Lane, Chandler, AZ 85224 (US).

(74) Agents: **WUAMETT, Jennifer, B.** et al.; SPS PATENT OPERATION MANAGER - ON BEHALF OF MOTOROLA, INC., Corporate Law Department, Intellectual Property Section, 7700 West Parmer Lane (US).

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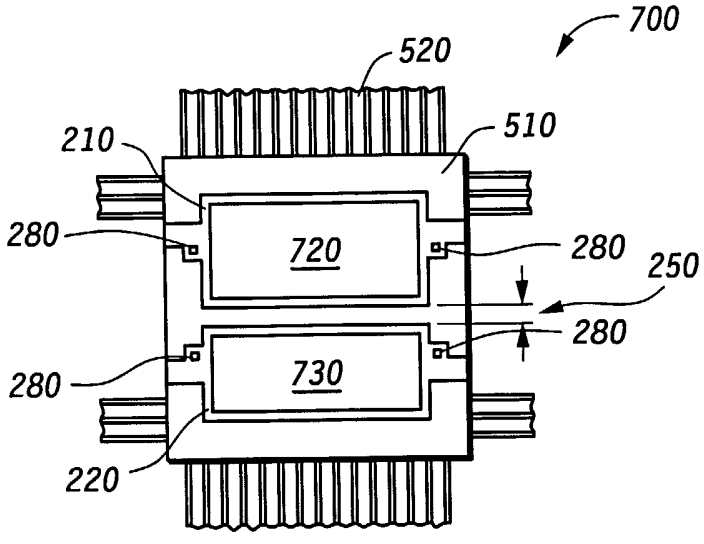
(54) Title: MOUNTING SURFACES FOR ELECTRONIC DEVICES



(57) Abstract: A mount, packaged device, and method of making the same are provided. In one embodiment, a method for making a mount for at least two electronic devices comprises forming a first mounting surface (210) from a material (240), and forming a second mounting surface (220) from the material (240). The first mounting surface (210) is connected to, but spaced from, the second mounting surface (220) by a mounting surface distance (250). The method further comprises reducing the mounting surface distance (250).

WO 2004/012485 A2

MOUNTING SURFACES FOR ELECTRONIC DEVICES

BACKGROUND OF THE INVENTION:

The present invention relates generally to mounting electronic devices.

FIG. 1 illustrates aspects of a conventional multi-die package. The package has a power die 110 and a control die 120, both of which are secured to a mounting surface (commonly called a "flag" 130).

In many applications, the power die 110 and the control die 120 must be electrically isolated. One conventional method is to attach at least one die (such as the control die 120) to the flag 130 with a non-conductive epoxy compound (not seen). Typically, the epoxy compound is applied by placing dots of epoxy compound on the flag 130 and then using pressure to push the control die 120 onto the flag 130. The epoxy compound is squeezed out evenly under the control die 120. If the epoxy compound layer is too thin, however, there is not enough electrical isolation. This may cause the control die 120 or the power die 110 to short.

To electrically isolate the control die 110 and the power die 120 by physically isolating the mounting surfaces of the control die 110 and the power die 120 has proven to be difficult or costly. First, to simply create two separate mounting surfaces and then attach each of those mounting surfaces to another leadframe (not illustrated), requires more components than a single flag 130. This increases cost and forces a larger package size.

Furthermore, stamping two mounting surfaces out of a single material is constrained because stamping causes the stamped material to become bent or

deformed. This deformation interferes with the assembly and operation of the electronic package. Thus, the thicker the material to be stamped, the greater the required physical isolation of the two mounting surfaces. This drives up the total size of the package.

5

BRIEF DESCRIPTIONS OF THE FIGURES:

FIG. 1 shows a control die and a power die attached to a flag in accordance with the prior art.

FIG. 2 shows the result of forming a plurality of mounting surfaces in accordance with the present invention.

FIG. 3 shows a reduced gap between two mounting surfaces in accordance with the present invention.

FIG. 4 shows two singulated mounting surfaces in accordance with the present invention.

FIG. 5 shows two mounting surfaces attached to the leadframe in accordance with the present invention.

FIG. 6 shows two mounting surfaces with the gap filled in accordance with the present invention.

FIG. 7 shows an electronic device package with two electronic devices mounted on two mounting surfaces in accordance with the present invention.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS OF THE PRESENT INVENTION:

FIG. 2 illustrates various aspects of an example embodiment of the present invention. In one example embodiment, a method of making a mount for at least two electronic devices is provided. The method comprises stamping a first mounting surface 210 from a material 240 and stamping a second mounting surface 220 from the material 240. Commonly, the material 240 comprises oxygen-free high-conductive copper alloy, but in alternate embodiments, any suitable material is substituted for copper alloy. Depending on manufacturing conditions, in some embodiments, many first mounting surfaces 210 and second mounting surfaces 220 are stamped out of the same material 240 wherein the second stamped surface 220 is mechanically connected with the first surface 210.

In the illustrated embodiment, the mounting surfaces 210 and 220 are stamped by progressive stamping with a standard stamping tool, which stamps out the shape to be formed by making many individual stamps. The hatched region indicates the areas of the material 240 that are removed.

The first mounting surface 210 and the second mounting surface 220 are, in some embodiments, stamped with a collapsible connection 230 on either side of the first mounting surface 210 and second mounting surface 220. Between the first mounting surface 210 and the second mounting surface 220 is a gap 250. Attachment holes 280 are formed on either side of the first mounting surface 210 and the second mounting surface 220. The function of these attachment holes 280 is explained below.

Conventional stamping cannot stamp the gap 250 between the first mounting surface 210 and the second mounting surface 220 less than about 1.5

times the thickness of the material 240 (for most materials and stamping methods). In no case is it believed a material suitable for electronics can be stamped closer than about 1.2 times the thickness. Therefore, the first mounting surface 210 and the second mounting surface 220 are stamped with a gap 250, which is at least 1.2 times the thickness of the material 240; and, many times, is greater than 1.5 times the thickness of material 240. However, for many applications, the thickness of the material 240 causes the gap 250 to be too large. Therefore, it is desirable for the gap 250 to be reduced.

FIG. 3 illustrates an example embodiment of the first mounting surface 210 and the second mounting surface 220 with the gap 250 reduced. In example embodiments of the invention, various methods are used to reduce the gap 250 to below the 1.5 or 1.2 times material thickness limit. Generally, a force is used to deform the collapsible connection 230 and bring the first mounting surface 210 and the second mounting surface 220 closer together. For example, applying a force on the outside 274 of the first mounting surface 210 and the outside 275 of the second mounting surface 220 deforms the collapsible connection 230. In another example, force is applied to the outsides 272 and 273 of the collapsible connection 230. In alternate embodiments, the force is applied with a conventional tool or a tool specifically designed for reducing the gap 250. Examples of conventional tools include stamping tools, clamps, presses, and crimpers to name only a few. In one embodiment, a specifically designed tool (not illustrated) uses a V-shape. The open end of the "V" is pressed downward on the outsides 274 and 275 to provide a narrowing surface against which the first and second mounting surfaces 210 and 220 are pressed.

Although the illustrated example shows a curved shape (here in the specific form of an "S") for the collapsible connection 230, any deformable connection suffices. For example, the collapsible connection 230 is not limited to the type of deforming associated with a curved shape. In still a further embodiment, a straight connection having a weak area (for example, a thinner cross-section than surrounding portions of material 240) bends upon application of pressure. In still a further embodiment, a straight link with no designed-in weakened area is used. An important function of the collapsible connection 230, in any event, is that it comprises a deformable means for holding the mounting surfaces 210 and 220 at the distance at which they are formed while being pliable enough to reduce the gap 250 to a distance desired for use in a package upon application (directly or indirectly) of some force to the connection 230.

In a further embodiment, once the gap 250 is reduced to a desired distance, the first mounting surface 210, the second mounting surface 220, and the collapsible connections 230 are "singulated" by, for example, cutting them from the outer edges 260 (sometimes called "rails") and the rest of the material 240. FIG. 4 illustrates a singulated first mounting surface 210 and second mounting surface 220, with attachment holes 280, and two collapsible connections 230.

In still a further embodiment, as illustrated in FIG. 5, the singulated first mounting surface 210 and second mounting surface 220 are mounted onto a leadframe 510. The leadframe 510 includes a plurality of leads 520, which are used to provide electrical communication to electronic devices to be mounted on first and second mounting surfaces 210 and 220. The leadframe 510 comprises holes (not seen), which correspond to the attachment holes 280 on either side of the

first mounting surface 210 and the second mounting surface 220. The first mounting surface 210 and second mounting surface 220 are staked to the leadframe 510 by staking a pin or rivet through the attachment holes 280 on either side of the first mounting surface 210 and second mounting surface 220 and the leadframe 510. The edges of the pin or rivet are deformed, securing the mounting surfaces 210 and 220 to the leadframe 510. In various alternate embodiments, the mounting surfaces 210 and 220 are attached to the leadframe 510 by soldering, gluing, or any other method of attaching.

In a further embodiment, illustrated in FIG. 6, once the first mounting surface 210 and the second mounting surface 220 are attached to the leadframe 510, the collapsible connections 230 are removed (e.g., by cutting). By removing the collapsible connections 230, the first mounting surface 210 and the second mounting surface 220 are physically and electrically isolated.

As seen in FIG. 7, with the first mounting surface 210 and the second mounting surface 220 electrically isolated and attached to the leadframe 510, electronic components 720 and 730 are attached to the first and second mounting surfaces 210 and 220 (for example, by soldering, gluing, or any other method of attaching electronic components) creating a circuit 700.

In still a further embodiment, after electronic components 720 and 730 are mounted on the mounting surfaces 210 and 220, an encapsulant is applied and surrounds the circuit 700 and fills the gap 250. Filling the gap 250 further electrically isolates the first mounting surface 210 and the second mounting surface 220. In various embodiments, the encapsulant comprises plastic, rubber, or any other encapsulant used in semiconductor technology.

In some embodiments, one side of each of the mounting surfaces 210 and 220 is not encapsulated. Instead, the mounting surfaces 210 and 220 are left exposed to dissipate heat. In some embodiments (for example, power packages), the material of the first electronic component mounting surface 210 and the second electronic component mounting surface 220 is thicker than the material of the leadframe 510, which also provides heat dissipation.

The example embodiments of the present invention have been described with a certain degree of particularity; however, many changes may be made in the details without departing from the scope of the invention. It is understood that the invention is not limited to the embodiments set forth herein, but is to be limited only by the scope of the attached claims, including the full range of equivalency to which each is entitled.

We claim:

1. A method of making a mount for at least two electronic devices, the method comprising:

stamping a first mounting surface (210) from a material (240);

stamping a second mounting surface (220) from the material, wherein the first mounting surface is connected to, but spaced from, the second mounting surface by a mounting surface gap (250); and

reducing the mounting surface gap.

2. The method of claim 1, wherein the reducing comprises reducing the mounting surface gap to less than about 1.5 times the thickness of the material.

3. The method of claim 1, wherein the stamping a second mounting surface comprises forming a collapsible connection (230) that connects the first mounting surface and the second mounting surface, and reducing comprises deforming the collapsible connection.

4. The method of claim 1, further comprising electrically isolating the first mounting surface and the second mounting surface.

5. The method of claim 4, further comprising encapsulating the first mounting surface and the second mounting surface within a same plastic package.

6. The method of claim 1, wherein the first mounting surface and the second mounting surface are stamped essentially concurrently.

7. A packaged electronic device comprising:

a first stamped mounting surface (210) and a second stamped mounting surface (220), wherein the first stamped mounting surface and the second stamped mounting surface comprise the same material;

a gap (250) between the first stamped mounting surface and the second stamped mounting surface;

a first electronic device (720) mounted on the first stamped mounting surface; and

a second electronic device (730) mounted on the second stamped mounting surface;

wherein the gap is less than about 1.5 times a thickness of the first stamped mounting surface.

8. The package of claim 7, further comprising an encapsulant covering at least a portion of the first stamped mounting surface.

9. The package of claim 20, wherein the encapsulant substantially fills the gap.

10. The package of claim 7 wherein the first electronic device and the second electronic device are electrically isolated.

11. A mount for at least two electronic components, the mount comprising:

a first mounting surface (210);

a second mounting surface (220); and

a deformable means (230) for holding the first mounting surface and the second mounting surface.

12. A mount as in claim 11, wherein the deformable means comprises a substantially straight link.

13. A mount as in claim 11, wherein the deformable means comprises a curved shape.

14. A mount as in claim 13, wherein the deformable means comprises a S shape.

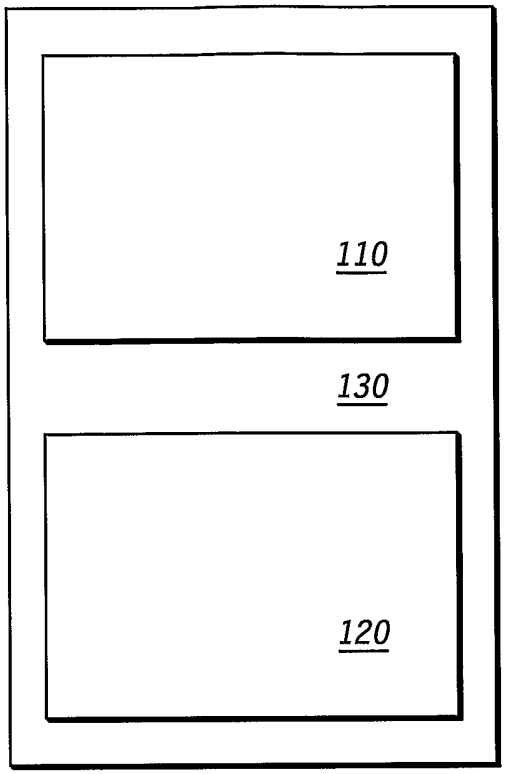

110
130
120

FIG.1

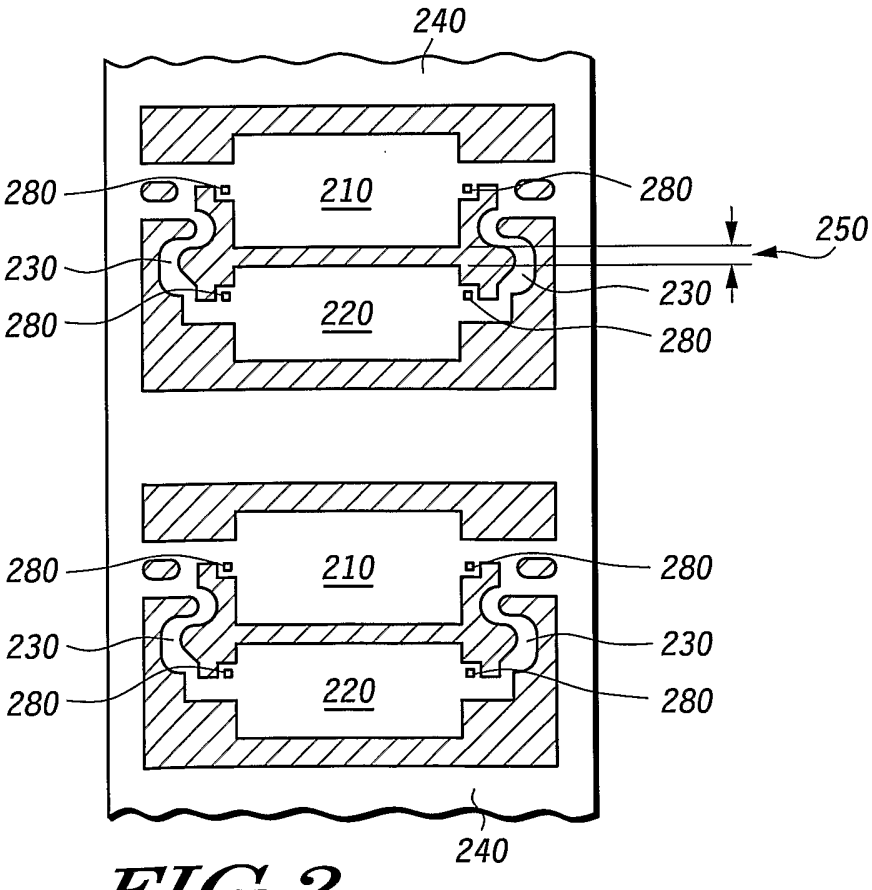

240
210
280
280
250
230
230
220
280
280
210
280
280
230
230
220
280
240

FIG.2

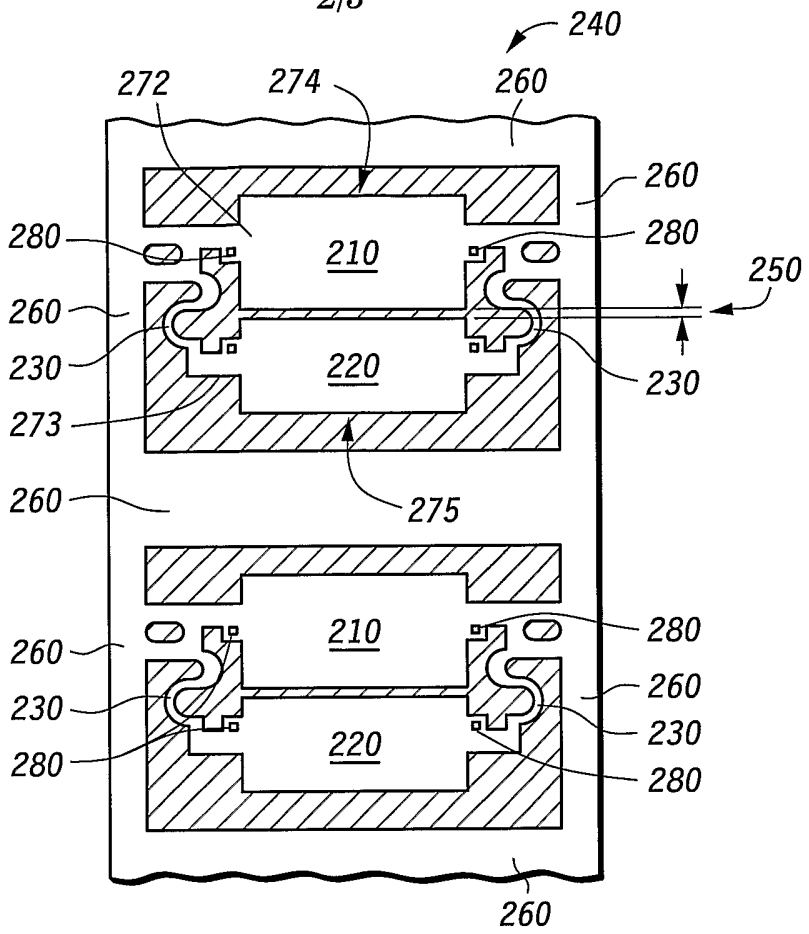


FIG.3

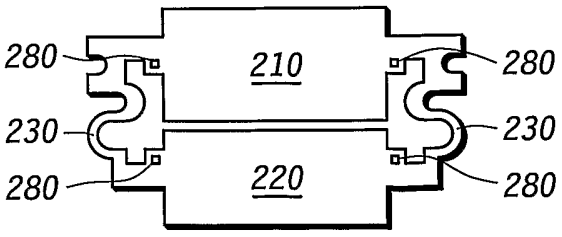


FIG.4

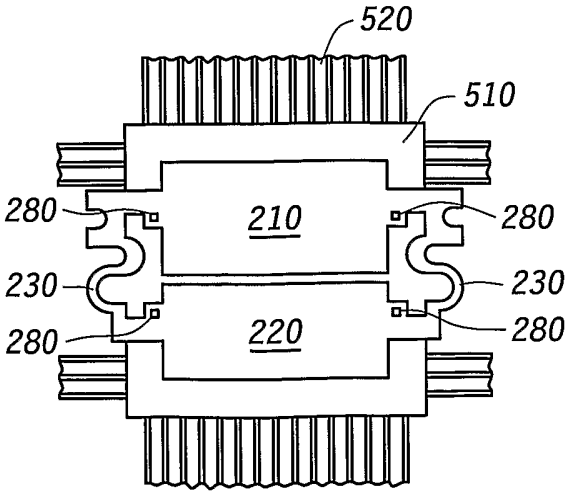


FIG.5

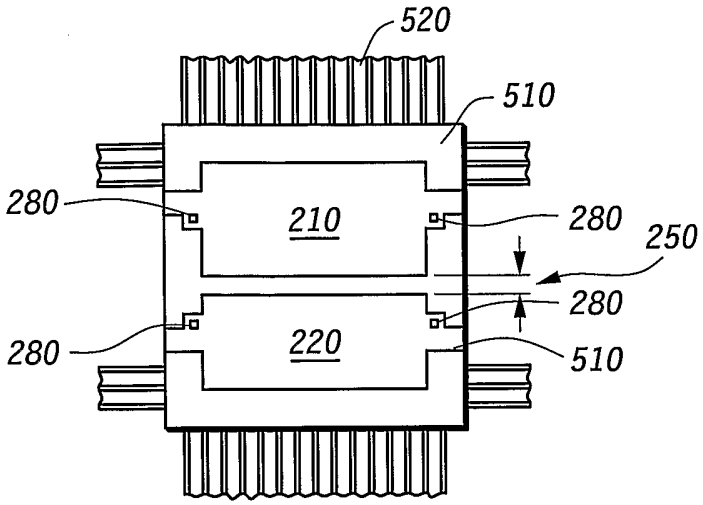

520
510
280
210
280
250
280
220
280
510

FIG. 6

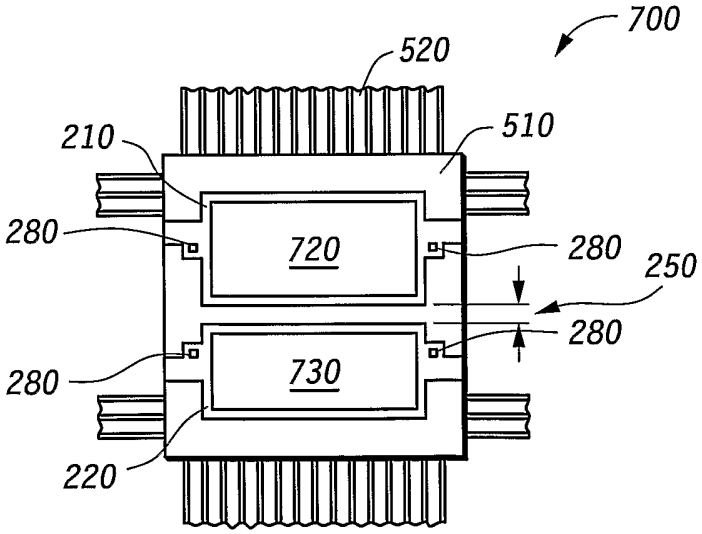

700
520
210
510
280
720
280
250
280
730
280
220

FIG. 7