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Gerrish et al.

(54) **HERMETICALLY-SEALED ELECTRICAL CIRCUIT APPARATUS**

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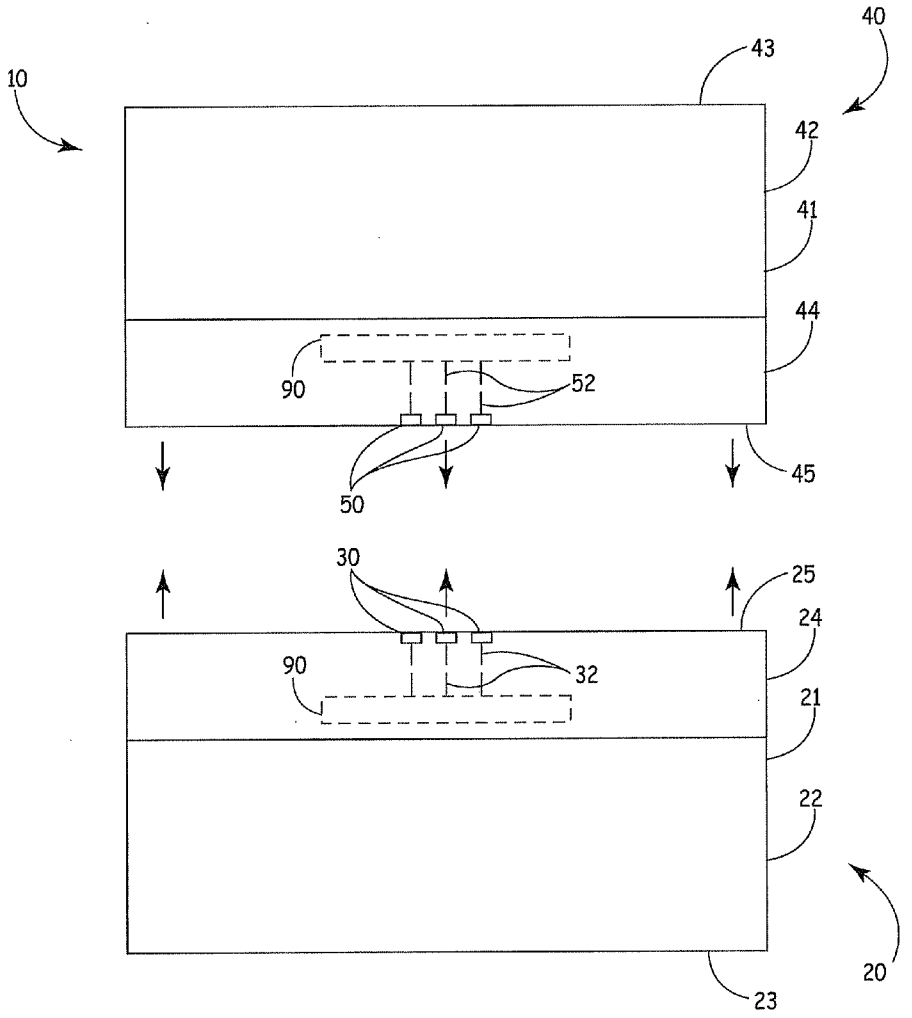
(57) **ABSTRACT**

Hermetically-sealed electrical circuit apparatus and methods for constructing such apparatus using one or more seal portions.



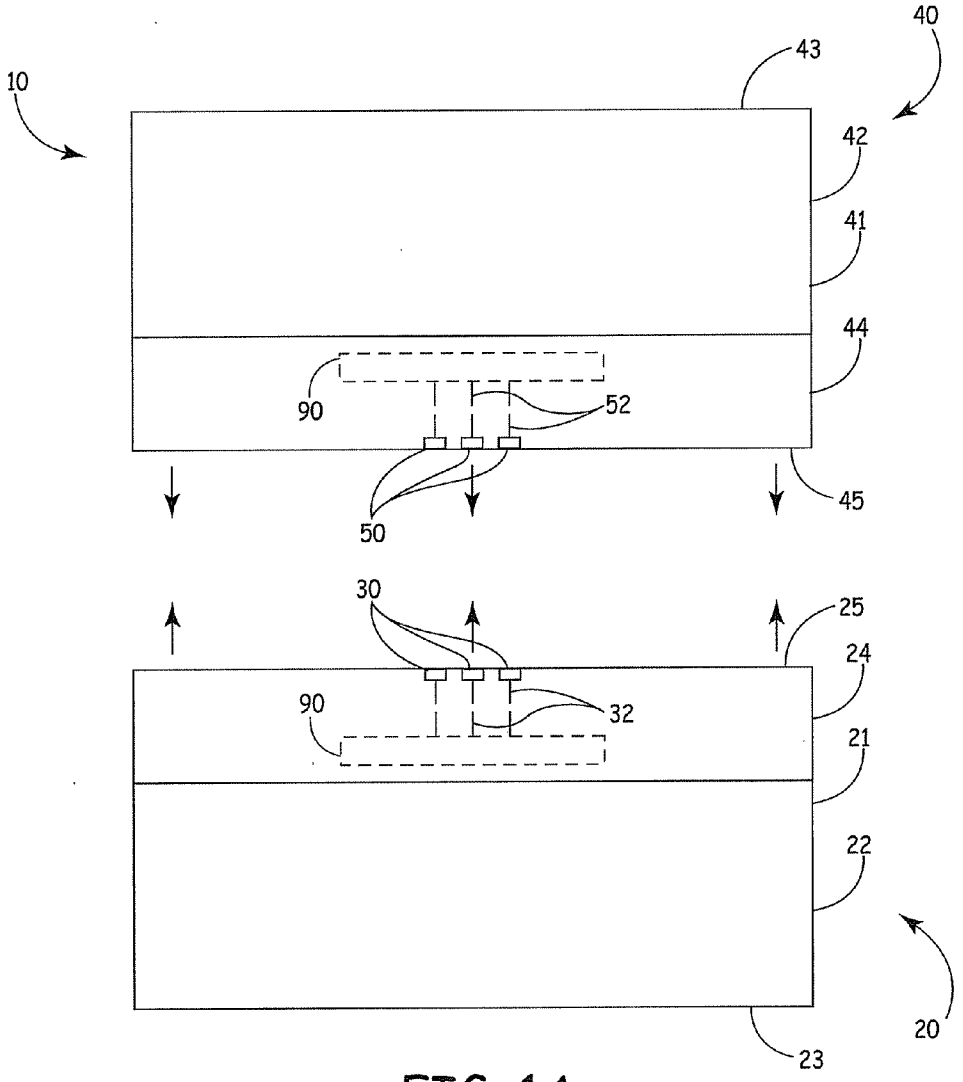


FIG. 1A

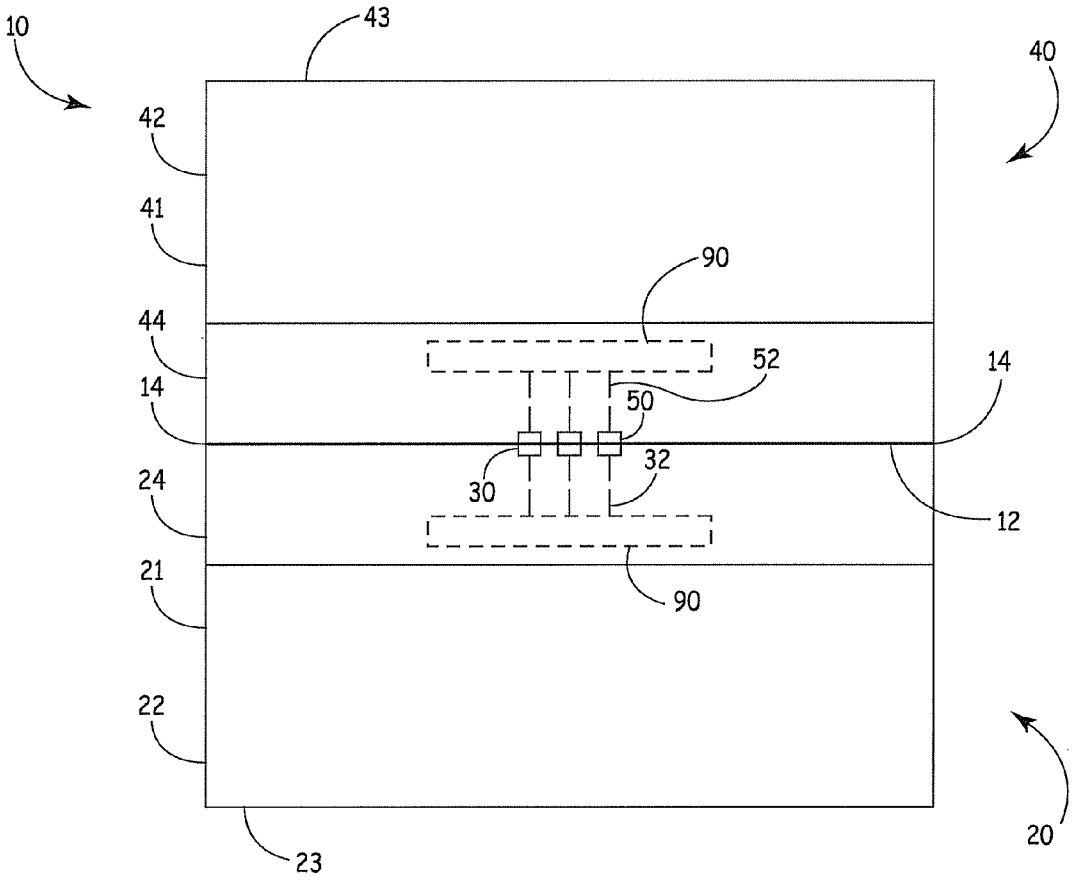


FIG. 1B

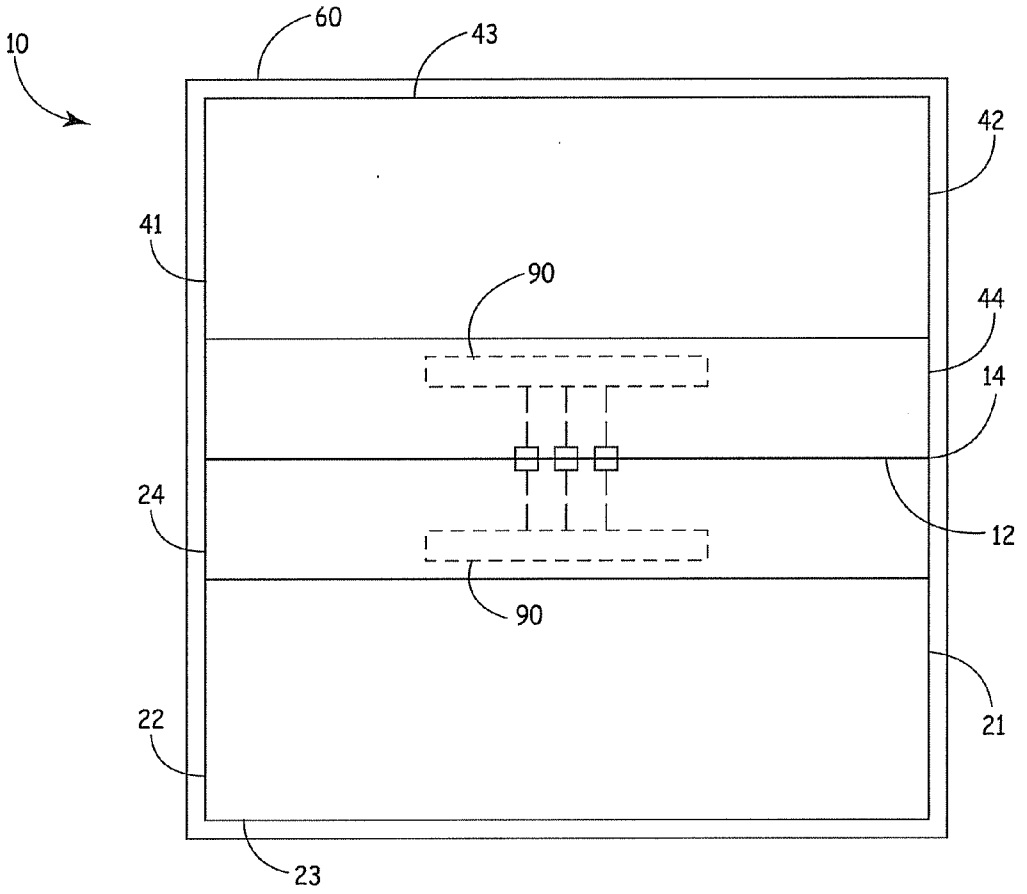


FIG. 1C

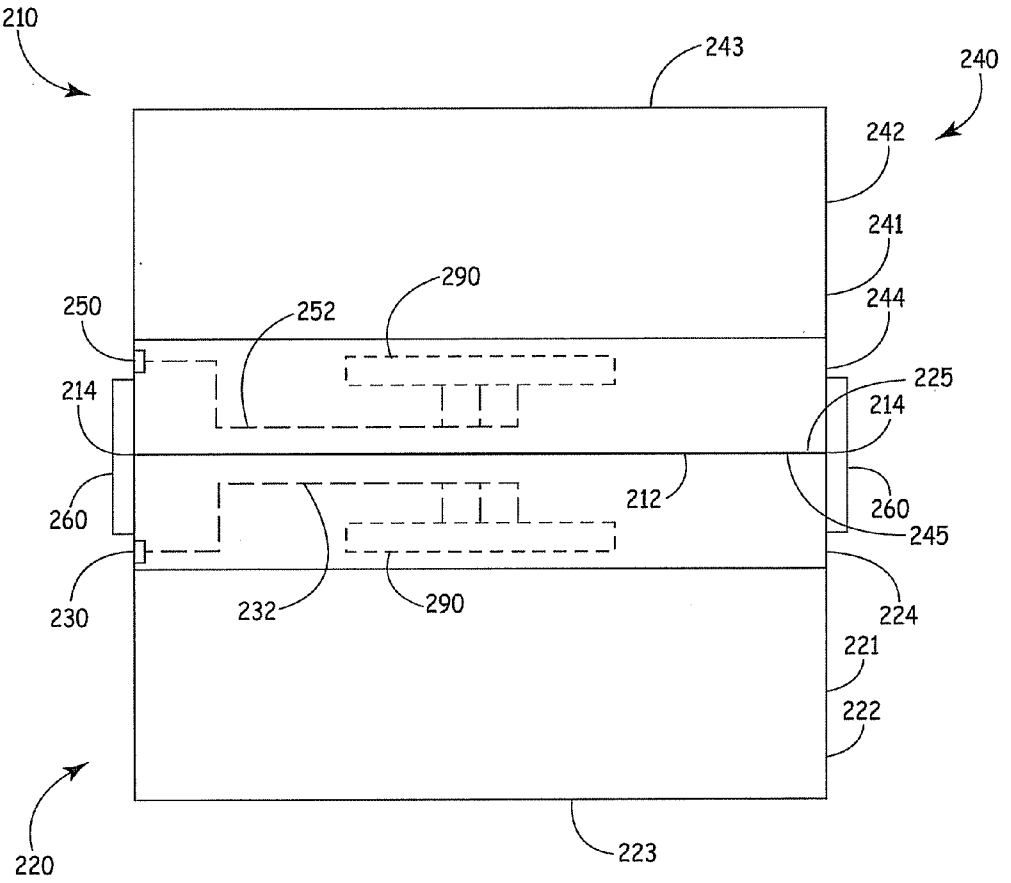

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FIG. 2A

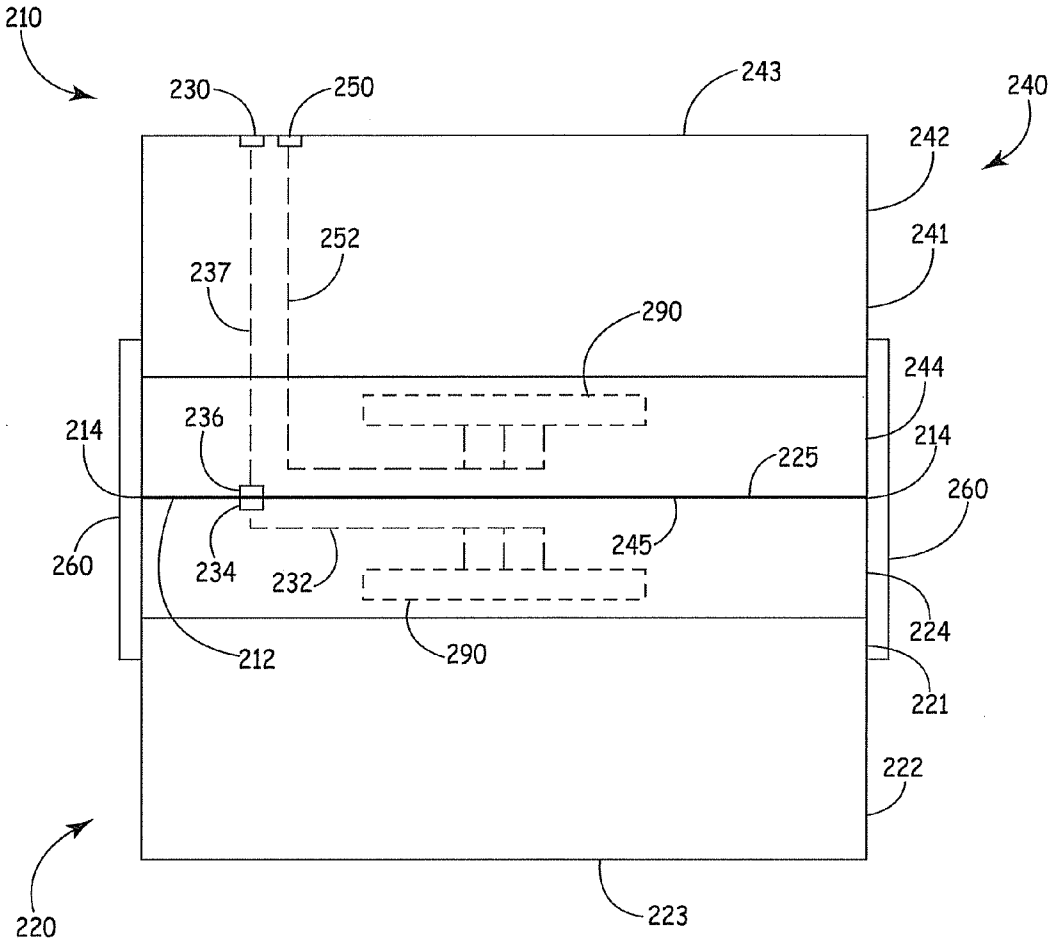
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FIG. 2B

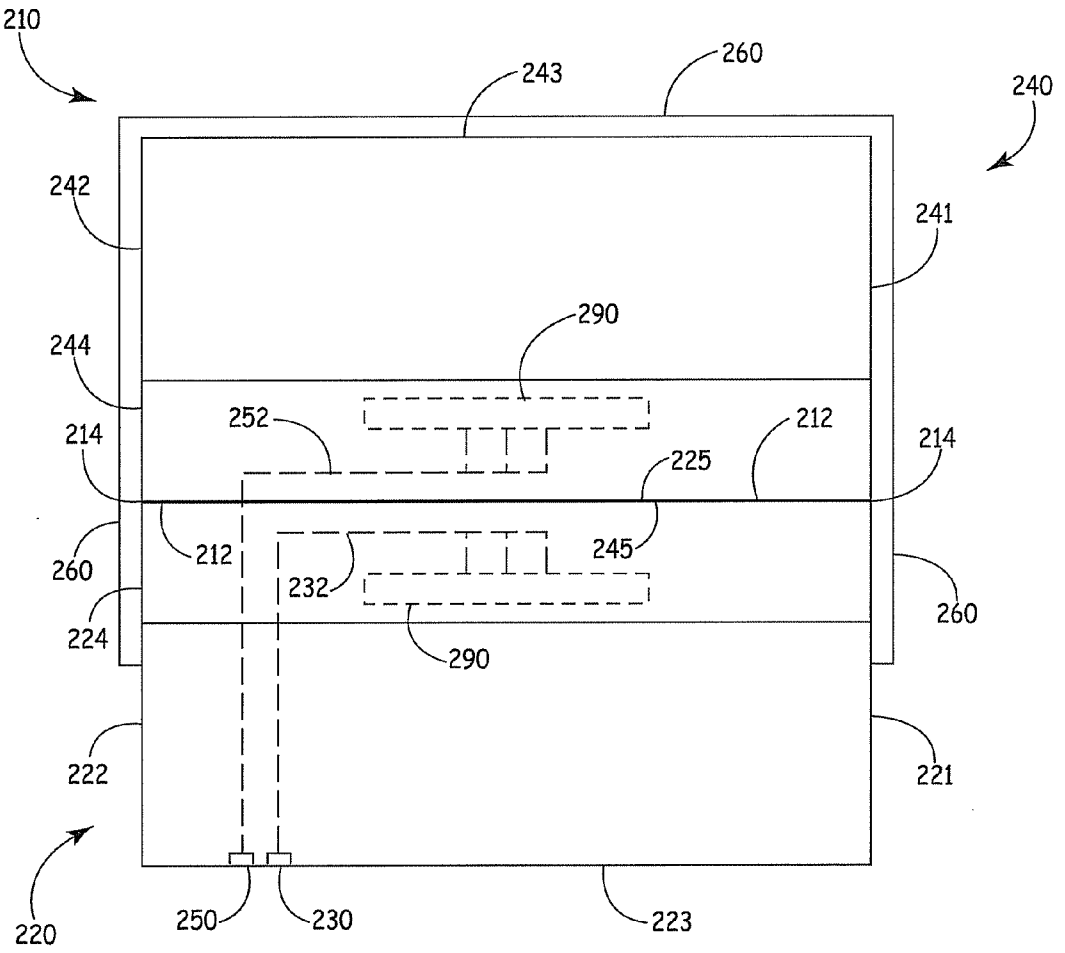
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FIG. 2C

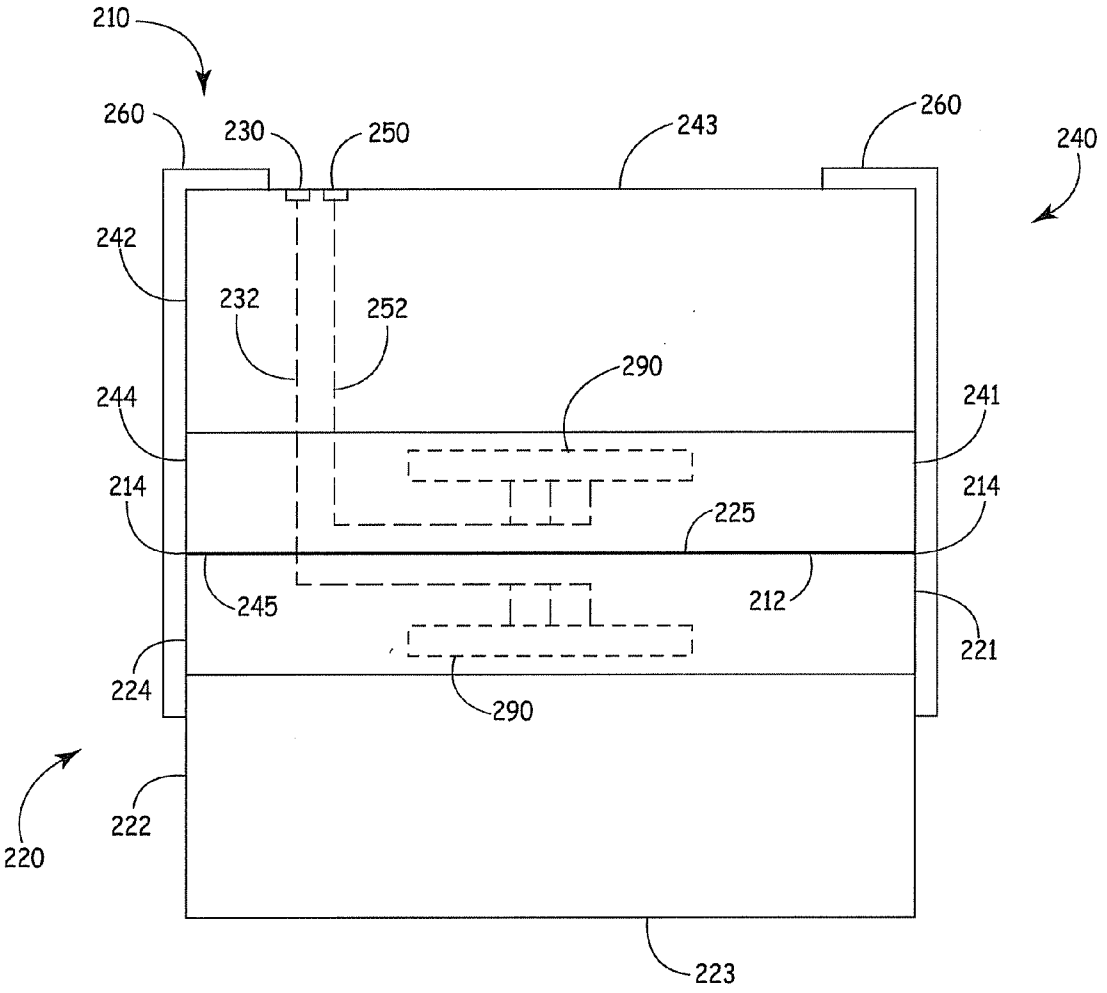
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FIG. 2D

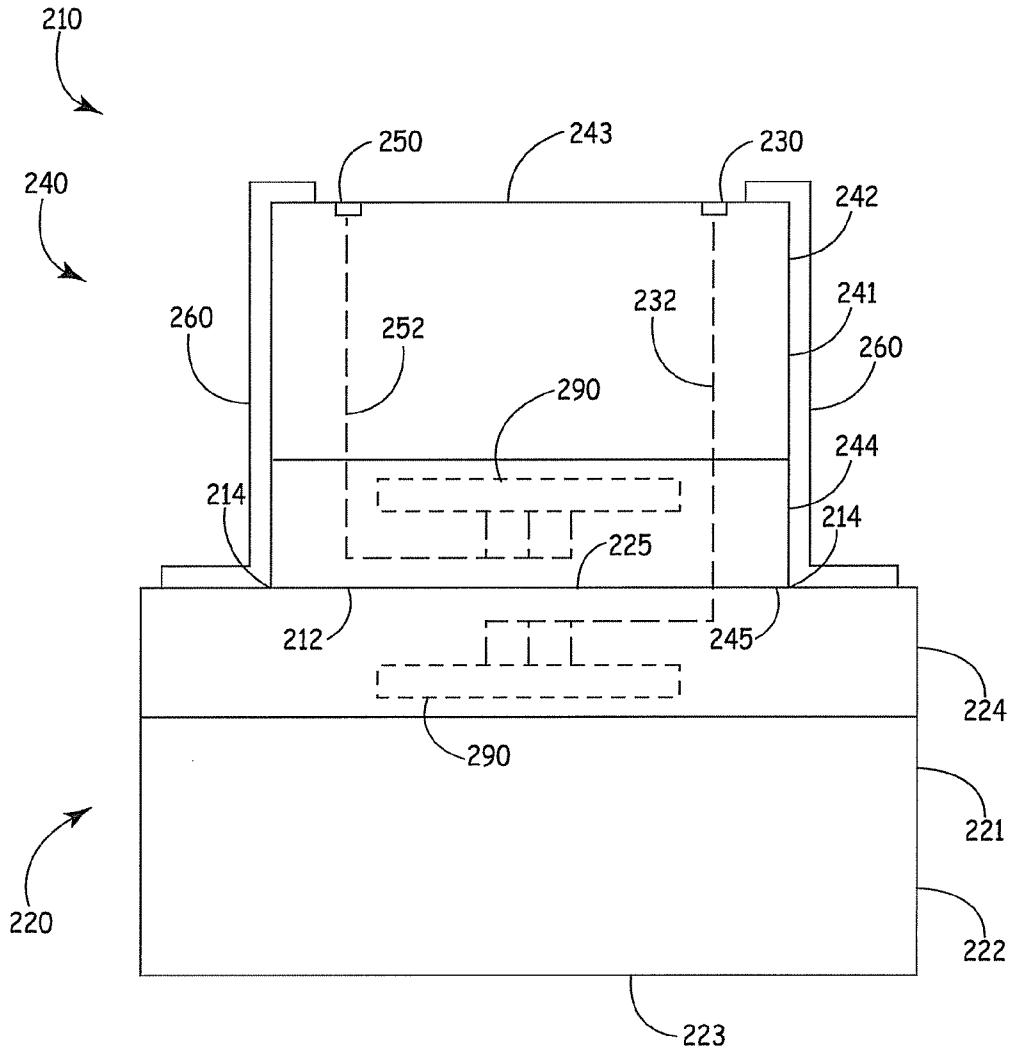
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FIG. 3A

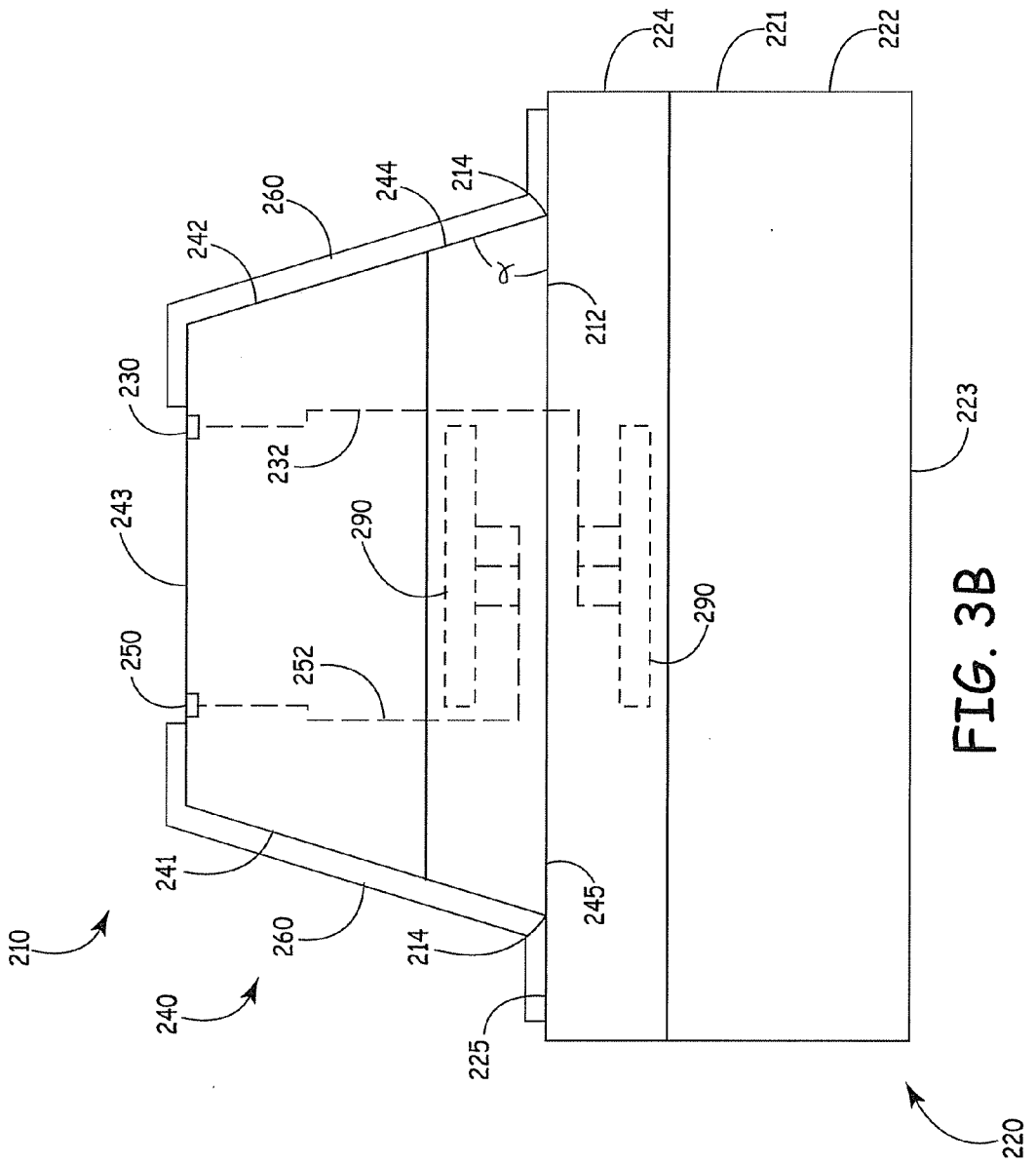
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FIG. 3B

HERMETICALLY-SEALED ELECTRICAL CIRCUIT APPARATUS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application Ser. No. 61/185,881 filed 10 Jun. 2009, entitled "FARADAY CAGE FOR CIRCUITRY USING SUBSTRATES," U.S. Provisional Application Ser. No. 61/229,867 filed 30 Jul. 2009, entitled "APPARATUS FOR RESTRICTING MOISTURE INGRESS," U.S. Provisional Application Ser. No. 61/229,869 filed 30 Jul. 2009, entitled "HERMETICITY TESTING," and U.S. Provisional Application Ser. No. 61/235,745 filed 21 Aug. 2009, entitled "HERMETICALLY-SEALED ELECTRICAL CIRCUIT APPARATUS," all of which are incorporated herein by reference in their respective entireties.

BACKGROUND

[0002] The disclosure herein relates to hermetically-sealed electrical circuit apparatus, and further to fabrication methods for constructing such apparatus.

[0003] Electrical circuits (e.g., integrated circuits) include many types of active and passive devices (e.g., transistors, capacitors, resistors, etc.) that may be subject to damage from moisture (e.g., corrosion and functional changes to the system). For example, moisture may affect the operation and performance of circuitry, such as sensitive circuits used in implantable medical devices (e.g., sensor circuitry, pacing circuitry, timing circuitry, etc.).

[0004] Various attempts have previously been made to seal the interior of semiconductor device dies from moisture ingress. The bottom substrate in many semiconductor devices (e.g., silicon) effectively blocks moisture from entering the interior of the die from the bottom, but materials commonly employed in fabricating further layers above the substrate provide a path for moisture to enter from the top and/or sides of the die, e.g., after die separation. For example, certain commonly employed insulator materials such as silicon dioxide (SiO_2) may be penetrated by moisture.

SUMMARY

[0005] The disclosure herein relates generally to hermetically-sealed electrical circuit apparatus, and methods of fabrication of such apparatus. For example, as described in one or more embodiments herein, semiconductor substrates and semiconductor fabrication techniques may be used to provide a hermetic enclosure around a circuit device (e.g., a die that includes circuitry).

[0006] One exemplary apparatus disclosed herein includes an electrical circuit apparatus. The electrical circuit apparatus includes a first portion, a second portion, at least one circuit, and one or more seal portions. The first portion includes a planar connection surface, a substrate provided from a wafer (e.g., the substrate includes a substrate surface opposite the planar connection surface) and at least one side surface extending between the substrate surface and the planar connection surface. The second portion includes a planar connection surface, a substrate provided from a wafer (e.g., the substrate comprises a substrate surface opposite the planar connection surface), and at least one side surface extending between the substrate surface and the planar connection surface. The planar connection surface of the first portion is bonded to the planar connection surface of the second portion to form an interface defining at least one interface edge about the perimeter of the interface between the planar connection surfaces of the first portion and the second portion. The at least one circuit device includes electrical circuitry. Further, the at least one circuit device is encompassed by at least portions of the first portion and the second portion. The one or more seal portions cover at least the at least one interface edge of the interface to restrict moisture from ingressing into the apparatus.

[0007] One exemplary method disclosed herein includes providing at least one electrical circuit apparatus. The method includes providing a first portion, providing a second portion, and providing at least one circuit device comprising electrical circuitry. The first portion includes a planar connection surface, a substrate provided from a wafer (e.g., the substrate comprises a substrate surface opposite the planar connection surface), and at least one side surface extending between the substrate surface and the planar connection surface. The second portion includes a planar connection surface, a substrate provided from a wafer (e.g., the substrate comprises a substrate surface opposite the planar connection surface), and at least one side surface extending between the substrate surface and the planar connection surface. The method further includes coupling the planar connection surface of the first portion to the planar connection surface of the second portion to form an interface defining at least one interface edge about the perimeter of the interface between the planar connection surfaces of the first portion and the second portion. After such coupling, the at least one circuit device is encompassed by at least portions of the first portion and the second portion. The method further includes providing one or more seal portions covering at least the at least one interface edge of the interface to restrict moisture from ingressing into the apparatus.

[0008] The above summary is not intended to describe each embodiment or every implementation of the present disclosure. A more complete understanding will become apparent and appreciated by referring to the following detailed description and claims taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIGS. **1**A-**1**C are illustrative cross-sectional side views generally depicting a method for fabricating one exemplary embodiment of a hermetically-sealed electrical circuit apparatus.

[0010] FIG. **2**A is an illustrative cross-sectional view of one exemplary embodiment of an electrical circuit apparatus such as generally shown in FIGS. **1**A-**1**C.

[0011] FIG. **2**B is an illustrative cross-sectional view of another exemplary embodiment of an electrical circuit apparatus such as generally shown in FIGS. **1**A-**1**C.

[0012] FIG. **2**C is an illustrative cross-sectional view of still another exemplary embodiment of an electrical circuit apparatus such as generally shown in FIGS. **1**A-**1**C.

[0013] FIG. **2**D is an illustrative cross-sectional view of yet still another exemplary embodiment of an electrical circuit apparatus such as generally shown in FIGS. **1**A-**1**C.

[0014] FIG. **3**A is an illustrative cross-sectional view of one exemplary embodiment of an electrical circuit apparatus, such as generally shown in FIGS. **1**A-**1**C, including first and second portions having different sizes.

[0015] FIG. **3**B is an illustrative cross-sectional view of another exemplary embodiment of an electrical circuit apparatus, such as generally shown in FIGS. **1**A-**1**C, including first and second portions having different sizes.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0016] In the following detailed description of illustrative embodiments, reference is made to the accompanying figures of the thawing which form a part hereof, and in which are shown, by way of illustration, specific embodiments which may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from (e.g., still falling within) the scope of the disclosure presented hereby.

[0017] Exemplary apparatus, and methods of constructing such apparatus, shall be described with reference to FIGS. **1-3**. It will be apparent to one skilled in the art that elements from one embodiment may be used in combination with elements of the other embodiments, and that the possible embodiments of such apparatus using combinations of features set forth herein is not limited to the specific embodiments shown in the Figures and/or described herein. Further, it will be recognized that the embodiments described herein may include many elements that are not necessarily shown to scale. Still further, it will be recognized that the size and shape of various elements herein may be modified but still fall within the scope of the present disclosure, although one or more shapes and/or sizes, or types of elements, may be advantageous over others.

[0018] FIGS. **1A-1C** show illustrative cross-sectional views generally depicting a method for fabricating one exemplary embodiment of a hermetically-sealed electrical circuit apparatus **10** (see FIG. **1C**) including at least one circuit device **90**. The method may include providing a first portion **20** and a second portion **40**.

[0019] Wafer scale fabrication techniques may be used to provide each of the first and second portions **20**, **40**. In one or more embodiments, each of the first portion **20** and the second portion **40** includes a substrate **22**, **42**, respectively, provided from or as a part of a wafer (e.g., a portion of any size and shape of substrate usable in wafer scale fabrication processes, such as a circular silicon wafer, a glass substrate, a plastic substrate, etc.). In other words, multiple portions may be fabricated on a wafer (e.g., the first portions on a first wafer and the second portions on a second wafer). As such, the fabrication of each of the portions may be initiated with use of a wafer substrate (e.g., a semiconductor, conductor, or insulator substrate wafer). In one or more embodiments, the wafer substrate is a doped semiconductor wafer substrate (e.g., doped to either a bulk n-type or p-type wafer), such as those used as the base substrate for microelectronic devices (e.g., substrates built in and over using one or more microfabrication process steps such as doping, ion implantation, etching, deposition of various materials, and photolithographic patterning processes). In one or more embodiments, the wafer is a silicon wafer. However, other available types of semiconductor wafers may be used, such as, for example, a gallium arsenide wafer, a germanium wafer, a silicon on insulator (SOI) wafer, etc. Further, for example, in one or more embodiments, the substrate may be formed of one or more materials other than semiconductor material, such as a glass substrate, wherein the substrate includes a metal film. In other words, for example, the first portion **20** may include a substrate **22** provided from or as a part of a wafer and the second portion **40** may include a substrate **42** provided from or as a part of a wafer.

[0020] As shown in FIGS. **1A-1C**, the substrate **22** may include a substrate surface **23** located opposite a connection surface **25** of the first portion **20**. The first portion **20** further includes one or more layers **24** formed on the substrate **22** terminating at the connection surface **25** (e.g., a planar connection surface, a connection surface orthogonal to the at least one side surface **21**, etc.). Also, the first portion **20** includes at least one side surface **21** (e.g., one side surface, four side surfaces, etc.) extending between the substrate surface **23** and the connection surface **25** (e.g., defined by the substrate **22** and the one or more layers **24**).

[0021] At least in one embodiment, the second portion **40** may only include a substrate (e.g., substrate **42**). In the embodiment depicted, the second portion **40** is substantially similar to the first portion **20**. For example, the substrate **42** may include a substrate surface **43** located opposite a connection surface **45** of the second portion **40**. The second portion **40** may further include one or more layers **44** formed on the substrate **42** terminating at the connection surface **45** (e.g., a planar connection surface, a connection surface orthogonal to the at least one side surface **41**). Also, the second portion **40** may include at least one side surface **41** (e.g., one side surface, four side surfaces, etc.) extending between the substrate surface **43** and the connection surface **45** (e.g., defined by the substrate **42** and the one or more layers **44**).

[0022] At least in one embodiment, the connection surfaces **25**, **45**, which may be defined at least partly by one or more layers; may include oxide material. For example, such oxide material may be oxide material formed, deposited or grown as part of one or more processing steps (e.g., oxides such as borophosphosilicate glass, silicon dioxide, native oxide, etc.).

[0023] The apparatus **10** may include one or more circuit devices **90** (e.g., at least one circuit device **90**) encompassed by (e.g., within, surrounded by, etc.) at least portions of the first and the second portions **20**, **40**. In at least one embodiment (as shown in FIGS. **1A-1C**), the first portion **20** and/or the second portion **40** may be processed to form one or more circuit devices **90** by fabricating (e.g., using any known fabrication processes including deposition, patterning, and/or etching) the one or more circuit device **90** within the one or more layers **24**, **44** fowled on the substrates **22**, **42**. In other words, the one or more circuit devices **90** may be formed as part of the one or more layers **24**, **44** of the first and second portions **20**, **40**, respectively.

[0024] The first and second portions **20**, **40** may further include one or more contact pads **30**, **50**, respectively, electrically coupled to the one or more circuit devices **90** using one or more interconnects **32**, **52** (represented schematically with dashed lines) and located at the connection surfaces **25**, **45**. When the first portion **20** is assembled (e.g., bonded) with the second portion **40**, the contact pads **30**, **50** are electrically coupled to each other such that the one or more circuit devices **90** are electrically coupled to each other. Further, although not depicted, the apparatus **10** (e.g., the first portion **20** and/or the second portion **40**) may include one or more additional interconnects extending between the circuit devices **90** and any other surface (e.g., outside surface) or any other location of the apparatus **10** for any purpose.

[0025] Further, although not depicted, one or both of the first and second portions **20**, **40** (e.g., the one or more layers **24**, **44**) may define a cavity and at least one of the one or more circuit devices **90** may be located within the cavity. As used herein, the one or more circuit devices **90** may be any device or devices that include electrical circuitry that performs one

or more functions (e.g., die containing circuitry). In such embodiments, the one or more circuit devices **90** may be directly electrically coupled to the one or more contacts pads **30**, **50** without the use of interconnects (e.g., interconnects **32**, **52**). For example, at least in one embodiment, the second portion **40** defines a cavity extending into the connection surface **45**. A circuit device **90** may be located within the cavity and electrically coupled to the contact pads **30** of the first portion **20**.

[0026] The one or more circuit devices **90**, the one or more interconnects **32**, **52**, and the one or more contact pads **30**, **50** may be formed using standard microelectronic fabrication processing techniques (e.g., such as etching of materials, deposition of materials, and photolithographic patterning process steps, etc.). Further, various portions of first and second portions **20**, **40** may be formed during the same or different processing steps. The present disclosure is not limited to any particular processing, or timing or order, of such process steps. However, some types of processing and order thereof may be beneficial over other types.

[0027] The method further includes bonding (e.g., oxide bonding, plasma-enhanced direct wafer bonding, etc.) the first portion **20** to the second portion **40** to form an interface **12** defining at least one interface edge **14** about the perimeter of the interface **12** (e.g., the interface **12** between the planar connection surfaces **25**, **45** of the first and the second portions **20**, **40**) (see FIG. **1**B). The interface **12** between the connection surfaces **25**, **45**, of the first portion **20** and the second portion **40** may be hermetic. As used herein, an interface that is hermetic is an interface that restricts (e.g., substantially limits, slows, prevents, etc.) moisture from passing, diffusing, pervading, infiltrating, and/or leaking through itself (e.g., the interface **12** may restrict moisture from passing, diffusing, pervading, infiltrating, and/or leaking through itself). As used herein, "moisture" may be defined as any material capable of ingressing into semiconductor devices. For example, moisture may include water, biological liquids, vapors, gases, etc.

[0028] In one or more embodiments, bonding the first and second portions **20**, **40** together to assemble the apparatus **10** may be implemented using any wafer or die bonding process (e.g., bonding a wafer including the first portions with a wafer including the second portions, which also refers to the bonding of an individual die to a full wafer, an individual die to another individual die, etc.), such as chemical bonding processes (e.g., those using adhesion promoters, high temperature bonding processes, hydrogen bonding processes, plasma-enhanced bonding processes, oxide bonding processes, etc.). For example, use of plasma-enhanced bonding permits oxide surfaces (e.g., portions of the connection surfaces **25**, **45** of the first and second portions **20**, **40** including a dioxide material, such as silicon oxide or native oxide) to be bonded together.

[0029] Further, for example, in one or more embodiments, the connection surfaces **25**, **45** may be each etched, polished, or planarized (e.g., using a chemical mechanical planarization or polishing) to expose any conductive portions thereof (e.g., the contact pads **30**, **50** at connection surfaces **25**, **45**) to be exposed. For example, when the oxide portions and the conductive portions (e.g., contact pads **30**) located at the connection surface **25** (e.g., a planar surface) are aligned with the oxide portions and the conductive portions (e.g., contact pads **50**) located at the connection surface **45** (e.g., a planar surface), plasma-enhanced bonding may be performed. Further, plasma-enhanced bonding processes may form a bond between oxide portions of the connection surfaces **25**, **45** of the first and second portions **20**, **40** without the need for adhesives or other intermediate layers. For example, at least in one embodiment, the bonding at the interface **12** may be formed by driving off any existing water present between the connection surfaces **25**, **45** and forming silicon-oxygen bonds throughout the structure such that a covalent bond is formed.

[0030] The method further includes providing one or more seal portions **60** at least covering the at least one interface edge **14** that, e.g., restricts moisture from entering the interface between the connection surfaces **25**, **45** (e.g., planar connection surfaces) of the first and second portions **20**, **40**, respectively. As shown in FIG. **1**C, the one or more seal portions **60** include a layer covering the entire exterior surface (e.g., the substrates surfaces **23**, **43**, the at least one side surfaces **41**, **21**, the interface **14**, etc.). In at least one embodiment, the one or more seals portions **60** only cover a portion of the exterior surface of the apparatus **10** (e.g., one or more portions of one or both of the at least one side surface **21**, **41** defined by either or both of the one or more layers **24**, **44** of the first and the second portions **20**, **40**; one or more portions of one or both of the at least one side surface **21**, **41** defined by either or both of the substrates **22**, **42** of the first and the second portions **20**, **40**; one or more portions of the substrate surfaces **23**, **43** of the first and the second portions **20**, **40**; etc.).

[0031] The one or more seal portions **60** may be provided by forming or depositing (e.g., physical deposition, chemical deposition, etc.) the one or more seal portions **60** as part of one or more processing steps (e.g., masking and depositing). For example, in at least one embodiment, the one or more seal portions **60** are provided by sputtering metals or polysilicon. Further, for example, in at least one embodiment, the one or more seal portions **60** are provided by chemical-vapor deposition.

[0032] The one or more seal portions **60** may include various materials such as, e.g., oxide materials, semiconductor materials, conductor materials, insulator materials, polysilicon, metals, phosphosilicate glass, borophosphosilicate glass, silicon nitride, tetraethyl orthosilicate, silox, etc. Further, such material of the one or more seal portions **60** may be biocompatible (e.g., such as for use in implantable medical devices). The one or more seal portions **60** may have a thickness of about 1 angstrom. Further, the one or more seal portions **60** may have a thickness of about 1 angstrom or more (in other words, at least about 1 angstrom), about 2 angstroms or more, about 5 angstroms or more, about 10 angstroms or more, about 50 angstroms or less, about 25 angstroms or less, about 10 angstroms or less, about 7 angstroms or less, about 5 angstroms or less, about 2 angstroms or less, or about 1 angstroms or less, etc. In at least one embodiment, the one or more seal portions **60** have a thickness that is thicker than the thickness of any material that may naturally form or grow on the first and second portions **20**, **40** (e.g., native oxide).

[0033] In at least one embodiment, the one or more seal portions **60** may include one or more layers of the same or various materials formed in the same or different process. Further, each layer of the one or more layers forming the one or more seal portions **60** may have a thickness of at least about 1 angstrom. For example, the one or more seal portions **60** may include atomic layer deposition of dielectrics, sputtering of metals, chemical-vapor deposition of silicon nitride, etc

[0034] The apparatus **10** as shown in FIG. **1**C may be utilized as a standalone package (e.g., apparatus **10** may not need any additional integrated circuit packaging or encapsulation). In at least one embodiment, however, one or more barrier layers (not shown) may be provided (e.g., formed) over the apparatus **10** after the one or more seal portions **60** have formed thereon. For example, the apparatus **10** may be encapsulated in silicone, medical adhesive, titanium, etc.

[0035] The process flow presented in FIGS. **1**A-**1**C is only an exemplary method that may be used to implement the apparatus described herein and is not to be taken as limiting to the scope of the disclosure provided herein. Various modifications to the process and/or timing or order of the process steps may be made to the method while still providing the benefits of apparatus described herein.

[0036] Although not limited thereto, in one or more embodiments, the apparatus **10** is beneficial circuitry for packaging used in implantable medical devices. For example, the one or more circuit devices **90** of the apparatus **10** may be a part of an implantable medical device. Further, the apparatus **10** may be biocompatible. For example, the implantable medical device may be a device implantable in a body near a human heart. For example, the implanted medical device may be any implantable cardiac pacemaker, defibrillator, cardioverter-defibrillator, or pacemaker-cardioverter-defibrillator (PCD). Further, for example, the implantable medical device may be an implantable nerve stimulator or muscle stimulator, an implantable monitoring device (e.g., a hemodynamic monitoring device), a brain stimulator, a gastric stimulator, a drug pump, or any other implantable device that would benefit from moisture protection. Therefore, the apparatus **10** may find wide application in any form of implantable medical device. As such, any description herein making reference to any particular medical device is not to be taken as a limitation of the type of medical device which can benefit from and which can employ apparatus **10** as described herein.

[0037] Further, although the apparatus **10** may be beneficial for implantable medical devices, such structure is in no manner limited to such applications. For example, such testing structure may be beneficial for many different types of circuitry (e.g., whether for medical use or not, whether for an implantable medical device or not). For example, one or more types of circuits that may benefit from such testing structure may include circuits such as sensor circuits, pacing circuits, timing circuits, telemetry circuits, etc.

[0038] FIGS. **2**A-**2**D and **3**A-**3**B are illustrative cross-sectional views of exemplary embodiments of electrical circuit apparatus such as generally shown in FIGS. **1**A-**1**C. Each embodiment depicted in each of FIGS. **2**A-**2**D and **3**A-**3**B utilizes many of the same components/portions, and as such, utilizes the same reference numbers in the description provided herein. However, each embodiment depicted in each of FIGS. **2**A-**2**D and **3**A-**3**B is constructed in different configurations.

[0039] The electrical circuit apparatus **210** may be similar to the electrical circuit apparatus **10** and components thereof described herein with reference to FIGS. **1**A-**1**C. For example, electrical circuit apparatus **210** includes a first portion **220** (e.g., including a substrate **222**, a substrate surface **223**, one or more layers **224**, a connection surface **225**, at least one side surface **221**, a circuit device **290**, contact pads **230**, and interconnects **232** (represented schematically with dashed lines)), a second portion **240** (e.g., including a substrate **242**, a substrate surface **243**, one or more layers **244**, a connection surface **245**, at least one side surface **241**, a circuit device **290**, contact pads **250**, and interconnects **252** (represented schematically with dashed lines)), an interface **212** defining at least one interface edge **214** about the perimeter of the interface **212**, and a one or more seal portions **260**. As such, for simplicity, further description on some of the details of the electrical circuit apparatus **210** shall not be provided.

[0040] The one or more seal portions **260** are located in various locations on the exemplary electrical circuit apparatus **210** depicted in FIGS. **2**A-**2**D. For example, the one or more seal portions **260** cover a portion of the at least one side surface **221** of the first portion **220** and at least a portion of the at least one side surface **241** of the second portion **240** of the electrical circuit apparatus **210** in FIG. **2**A. More specifically, the at least one interface edge **214** and portions of the side surfaces **221**, **241** defined by portions of both of the one or more layers **224**, **244** are covered by the one or more seal portions **260** such that the one or more seal portions **260** restrict moisture ingress (e.g., movement of moisture) into the electrical circuit device **290** (e.g., through the interface **212**), e.g., to protect the circuit devices **290**. The one or more seal portions **260** may extend around the entire interface edge **214** or one or more portions of interface edge **214** (e.g., one or more sides so as to restrict moisture ingress from particular directions).

[0041] Further, the apparatus **210** depicted in FIG. **2**A includes interconnects **232**, **252** extending within the one or more layers **224**, **244**, respectively, between the circuit devices **290** and the contact pads **230**, **250**. The contact pads **230**, **250** are located within the one or more layers **224**, **244** proximate the respective side surfaces **221**, **241** without being covered by the one or more seal portions **260** such that, e.g., they may electrically connected to any other device. Although only two contact pads **230**, **250** and two interconnects **232**, **252** are depicted in FIG. **2**A, the electrical circuit apparatus **210** may include more or less than two contact pads and two interconnects electrically coupled to the circuit devices **290**. As a result of interconnects **232**, **252** and contact pads **230**, **250**, the circuit devices **290** may be in electrical communication with a device located outside of the electrical circuit apparatus **210** by electrically coupling such device to the contact pads **230**, **250**. Further, the circuit devices **290** of the first and second portions **220**, **240** may be electrically coupled to each other by the use of interconnects (not shown) similar to the electrical circuit devices **90** depicted in FIGS. **1**A-**1**C.

[0042] The formation of interconnects **232**, **252** and the contact pads **230**, **250** may be formed using standard microelectronic fabrication processing techniques (e.g., such as etching of materials, deposition of materials, photolithographic patterning process steps, etc.). Further, interconnects **232**, **252** may be formed of various structures including, e.g., stacked vias, through-silicon vias, metal layers, etc. Various portions of first and second portions **220**, **240** may be formed during the same or different processing steps. For example, a portion of an interconnect **232** may be formed within a layer of the one or more layers **224** during formation of device **290**. Still further, for example, process steps to form interconnects **232**, **252** may be completely separate therefrom, such as in the formation of a through-silicon via after other layer processing is completed. The present disclosure is not limited to any particular processing, or timing or order, of such process steps. However, some types of processing and order thereof may be beneficial over other types.

[0043] Still further, in one or more embodiments, the first and second portions **220**, **240** may not include interconnects or vias connecting the circuit devices to contact pads on the outside of the apparatus **210**. For example, in at least one embodiment, the apparatus **210** may include various apparatus and/or structures to wirelessly communicate to other devices/apparatus outside of apparatus **210**.

[0044] One or more seal portions **260** cover a larger portion of the side surfaces **221**, **241** of the electrical circuit apparatus **210** in FIG. **2**B than in FIG. **2**A. More specifically, the interface edge **214**, portions of side surfaces **221**, **241** defined by the one or more layers **224**, **244**, and a portion of the substrates **222**, **242** are covered by the one or more seal portions **260** such that one or more seal portions **260** restrict moisture ingress (e.g., movement of moisture) into the electrical circuit apparatus **210** (e.g., through the interface **212**, one or more layers **224**, **244**, etc.), e.g., to protect the circuit devices **290**.

[0045] The apparatus **210** depicted in FIG. **2**B includes interconnects **232**, **237**, **252** extending between the circuit devices **290** and the contact pads **230**, **250**. In this embodiment, the contact pads **230**, **250** are located proximate the substrate surface **243** of the second portion **240**. The interconnect **232** extends through the one or more layers **224** of the first portion **220** to a contact pad **234**. The contact pad **234** is electrically coupled to contact pad **236** when the first portion **220** is coupled to the second portion **240**. The contact pad **236** is electrically coupled to interconnect **237**, which extends through the second portion **240** (e.g., the one or more layers **244** and the substrate **242**) to the contact pad **230** thereby electrically coupling the contact pad **230** and the circuit device **290** of the first portion **220**. The interconnects described herein may also use a similar connection (using contact pads, etc.) between the one or more layers and substrate of a respective portion. Further, interconnect **252** extends through the one or more layers **244** and the substrate **242** and is electrically coupled to contact pad **250**. Although only contact pads **230**, **250** and interconnects **232**, **237**, **252** are depicted in FIG. **2**B, the electrical circuit apparatus **210** may include more than two contact pads and/or more than three interconnects electrically coupled to the circuit devices **290**.

[0046] Further, for example, one or more seal portions **260** may cover the substrate surface **243** of the second portion **240** and a portion of the side surfaces **221**, **241** of the electrical circuit apparatus **210** as shown in FIG. **2**C. More specifically, the interface edge **214**, the side surface **221** defined by the substrate **242**, the side surfaces **221**, **241** defined by the one or more layers **244**, the side surface **221** defined by a portion of the substrate **222**, and the substrate surface **243** are covered by the one or more seal portion **260** such that one or more seal portions **260** restrict moisture ingress (e.g., movement of moisture) into the electrical circuit apparatus **210** (e.g., through the interface **212**, through the one or more layers **224**, **244**, etc.) to, e.g., protect the circuit devices **290**.

[0047] The apparatus **210** depicted in FIG. **2**C includes interconnects **232**, **252** extending between the circuit devices **290** and the contact pads **230**, **250**. In this embodiment, the contact pads **230**, **250** are located proximate the substrate surface **223** of the first portion **220**. The interconnect **252** extends through the one or more layers **244** of the second portion **240** and through the one or more layers **224** and substrate **222** of the first portion **220** to the contact pad **250** (e.g., electrically coupled to the contact pad **250**). Although not depicted in FIG. **2**C, the interconnect **252** may include multiple portions and/or contact pads (e.g., contact pads located proximate each of the connection surfaces **225**, **245** so as to complete the interconnect **252** when the first portion **220** is bonded to the second portion **240** similar to contact pads **234**, **236** shown in FIG. **2**B). Further, interconnect **232** extends through the one or more layers **224** and the substrate **222** to contact pad **230** (e.g., electrically coupled to the contact pad **230**). Although only contact pads **230**, **250** and interconnects **232**, **252** are depicted in FIG. **2**C, the electrical circuit apparatus **210** may include more than two contact pads and/or more than two interconnects electrically coupled to the circuit devices **290**.

[0048] Still further, for example, one or more seal portions **260** may cover at least a portion of the substrate surface **243** of the second portion **240** and a portion of the side surfaces **221**, **241** of the electrical circuit apparatus **210** as shown in FIG. **2**D. More specifically, the interface edge **214**, the side surfaces **221**, **241** defined by the one or more layers **224**, **244**, the side surface **221** defined by least a portion of the substrate **222**, the surface **241** defined by the substrate **242**, and at least a portion of the substrate surface **243** are covered such that one or more seal portions **260** restrict moisture ingress (e.g., movement of moisture) into the electrical circuit apparatus **210** (e.g., through the interface **212**, through one or more layers **224**, **244**, etc.), e.g., to protect the circuit devices **290**.

[0049] The apparatus **210** depicted in FIG. **2**D includes interconnects **232**, **252** extending between the circuit devices **290** and the contact pads **230**, **250** in a similar manner to that shown in FIG. **2**C but to surface **243** instead of to surface **223**.

[0050] The apparatus **210** depicted in FIGS. **3**A-**3**B includes first portions **220** that are larger than the second portions **240** (e.g., the connection surface **225** of the first portion **220** defines a larger area than the connection surface **245** of the second portion **240**). In at least one embodiment, the second portion **240** when bonded to the first portion **220** is centered within the area defined by the connection surface **225** of the first portion **220**. The first portion **220** and the second portion **240** may be any size relative to each other so as to provide suitable functionality to the apparatus **210** (e.g., to provide contact pads on various locations of the apparatus **210** for electrically coupling the apparatus **210** to various devices, to reduce the size and/or shape of the apparatus **210**, to reduce the amount of material used to form the apparatus **210**, etc.).

[0051] The apparatus **210** depicted in FIGS. **3**A-**3**B, however, differ from each other in that at least the angle and/or shape of their respective side surfaces **241** of the second portions **240** differ. For example, the second portion **240** depicted in FIG. **3**A includes at least one side surface **241** that is substantially perpendicular to the connection surface **245** such that the area of the substrate surface **243** is about equal to the area of the connection surface **245**. The second portion **240** depicted in FIG. **3**B includes at least one side surface **241** that is not perpendicular but rather is less than 90 degrees (e.g., the angle alpha between the at least one side surface **241** and the connection surface **254** may be about 89 degrees, 85 degrees, 80 degrees, 70 degrees, 60 degrees, 50 degrees, 45 degrees, 40 degrees, 30 degrees, etc.) to the connection surface **245** such that the area of the substrate surface **243** is smaller than the area of the connection surface **245**.

[0052] The one or more seal portions **260** are located in substantially the same locations on the exemplary electrical circuit apparatus **210** depicted in FIGS. **3**A-**3**B. For example, the one or more seal portions **260** cover the at least one side

surface **241** defined by the one or more layers **244** and substrate **242** of the second portion **240**, at least a portion of the substrate surface **243** of the second portion **240**, and at least a portion of the connection surface **225** of the first portion **220** of the electrical circuit apparatus **210**. Further, the at least one interface edge **214** between the connection surface **225** of the first portion **220** and the connection surface **245** of the second portion **240** is covered such that the one or more seal portions **260** restrict moisture ingress (e.g., movement of moisture) into the electrical circuit device **290** (e.g., through the interface **212**, through the one or more layers **224**, **244**, etc.), e.g., to protect the circuit devices **290**.

[0053] Further, the apparatus **210** depicted in FIGS. **3**A-**3**B includes interconnects **232**, **252** extending between the circuit devices **290** and the contact pads **230**, **250**. The contact pads **230**, **250** are located proximate the substrate surface **243** of the second portion and are not covered by the one or more seal portions **260** such that, e.g., they may be electrically connected to any other device. Interconnect **232** extends through the one or more layers **224** of the first portion **220** and the one or more layers **244** and substrate **242** of the second portion **240**. Further, interconnect **252** extends through the one or more layers **244** and substrate **242** of the second portion **240**. Although not depicted in FIGS. **3**A-**3**B, the interconnect **232** may include multiple portions and/or contact pads (e.g., contact pads located proximate each of the connection surfaces **225**, **245** so as to complete the interconnect **232** when the first portion **220** is bonded to the second portion **240** similar to contact pads **234**, **236** shown in FIG. **2**B). Further, although only two contact pads **230**, **250** and two interconnects **232**, **252** are depicted in FIGS. **3**A-**3**B, the electrical circuit apparatus **210** may include more than two contact pads and/or interconnects electrically coupled to the circuit devices **290**. As a result of these contact pads and interconnects, the circuit devices **290** may be in electrical communication with a device located outside of the electrical circuit apparatus **210** by connecting such device to the contact pads **230**, **250**. Further, the circuit devices **290** of the first and second portions **220**, **240** may be electrically coupled to each other by the use of interconnects (not shown) similar to the electrical circuit device **10** depicted in FIGS. **1**A-**1**C.

[0054] Any features, components, and/or properties of any of the embodiments described herein may be incorporated into any other embodiment(s) described herein.

[0055] All patents, patent documents, and references cited herein are incorporated in their entirety as if each were incorporated separately. This disclosure has been provided with reference to illustrative embodiments and is not meant to be construed in a limiting sense. As described previously, one skilled in the art will recognize that other various illustrative applications may use the techniques as described herein to take advantage of the beneficial characteristics of the apparatus and methods described herein. Various modifications of the illustrative embodiments, as well as additional embodiments of the disclosure, will be apparent upon reference to this description.

1. An electrical circuit apparatus comprising:

a first portion comprising:

a planar connection surface,

a substrate provided from a wafer, wherein the substrate comprises a substrate surface opposite the planar connection surface, and

at least one side surface extending between the substrate surface and the planar connection surface;

a second portion comprising:

a planar connection surface,

a substrate provided from a wafer, wherein the substrate comprises a substrate surface opposite the planar connection surface, and

at least one side surface extending between the substrate surface and the planar connection surface, wherein the planar connection surface of the first portion is bonded to the planar connection surface of the second portion to foam an interface defining at least one interface edge about the perimeter of the interface between the planar connection surfaces of the first portion and the second portion;

at least one circuit device comprising electrical circuitry, wherein the at least one circuit device is encompassed by at least portions of the first portion and the second portion; and

one or more seal portions covering at least the at least one interface edge of the interface to restrict moisture from ingressing into the apparatus.

2. The apparatus of claim **1**, wherein the one or more seal portions comprise deposited material.

3. The apparatus of claim **1**, wherein the one or more seal portions comprise a thickness of at least about 1 angstrom.

4. The apparatus of claim **1**, wherein the one or more seal portions comprise oxide material.

5. The apparatus of claim **1**, wherein the one or more seal portions cover at least a portion of the at least one side surface of the first portion and the at least one side surface of the second portion to restrict moisture from ingressing into the apparatus.

6. The apparatus of claim **1**, wherein at least one of the first portion and the second portion further comprises one or more layers formed on the substrate thereof terminating at the connection surface thereof and defining a portion of the at least one side surface thereof, wherein the one or more seal portions cover the portion of the at least one side surface defined by the one or more layers to restrict moisture from ingressing into the apparatus.

7. The apparatus of claim **1**, wherein the one or more seal portions at least partially cover the substrate surface of the first portion, the substrate surface of the second portion, the at least one side surface of the first portion, and the at least one side surface of the second portion to restrict moisture from ingressing into the apparatus.

8. The apparatus of claim **1**, wherein the connection surface of the first portion defines a larger area than the connection surface of the second portion.

9. The apparatus of claim **1**, wherein the substrate of the first portion and the substrate of the second portion each comprise semiconductor substrates.

10. The apparatus of claim **1**, wherein the at least one circuit device forms a part of an implantable medical device.

11. The apparatus of claim **1**, wherein the first portion further comprises one or more layers formed on the substrate terminating at the connection surface, wherein the one or more layers of the first portion comprise a circuit device of the at least one circuit device.

12. The apparatus of claim **11**, wherein the one or more layers of the first portion further comprise contact pads electrically coupled to the circuit device and located at the connection surface, and wherein second portion further comprises one or more layers formed on the substrate terminating at the connection surface, wherein the one or more layers of

the second portion further comprise a circuit device of the at least one circuit device and contact pads electrically coupled to the circuit device and located at the connection surface, wherein the contact pads of the first portion are electrically coupled to the contact pads of the second portion to electrically couple the circuit device of the first portion to the circuit device of the second portion.

13. The apparatus of claim **1**, wherein at least one of the first portion and the second portion defines a cavity, wherein a circuit device of the at least one circuit device is located within the cavity.

14. The apparatus of claim **1**, wherein the apparatus further comprises:

one or more interconnect vias formed in at least one of the first portion and the second portion and terminating at one or more surface contacts at the substrate surface, the connection surface, or the at least one side surface of at least one of the first and second portions; and

at least one electrical interconnect extending from the at least one circuit device to at least one of the one or more interconnect vias.

15. The apparatus of claim **1**, wherein the connection surface of the first portion is plasma-enhanced bonded to the connection surface of the second portion.

16. A method of providing at least one electrical circuit apparatus, wherein the method comprises:

providing a first portion, wherein the first portion comprises:

a planar connection surface,

a substrate provided from a wafer, wherein the substrate comprises a substrate surface opposite the planar connection surface, and

at least one side surface extending between the substrate surface and the planar connection surface,

providing a second portion, wherein the second portion comprises:

a planar connection surface,

a substrate provided from a wafer, wherein the substrate comprises a substrate surface opposite the planar connection surface, and

at least one side surface extending between the substrate surface and the planar connection surface,

providing at least one circuit device comprising electrical circuitry;

coupling the planar connection surface of the first portion to the planar connection surface of the second portion to form an interface defining at least one interface edge about the perimeter of the interface between the planar connection surfaces of the first portion and the second portion, wherein the at least one circuit device is encompassed by at least portions of the first portion and the second portion; and

providing one or more seal portions covering at least the at least one interface edge of the interface to restrict moisture from ingressing into the apparatus.

17. The method of claim **16**, wherein providing one or more seal portions comprising depositing one or more seal portions.

18. The method of claim **16**, wherein the one or more seal portions comprise a thickness of at least about 1 angstrom.

19. The method of claim **16**, wherein the one or more seal portions comprise oxide material.

20. The method of claim **16**, wherein coupling the planar connection surface of the first portion to the planar connection surface of the second portion comprises oxide bonding the planar connection surface of the first portion to the planar connection surface of the second portion.

21. The method of claim **16**, wherein coupling the planar connection surface of the first portion to the planar connection surface of the second portion comprises plasma-enhanced bonding the planar connection surface of the first portion to the planar connection surface of the second portion.

22. The method of claim **16**, providing the first portion comprises providing one or more layers formed on the substrate thereof terminating at the connection surface thereof and defining a portion of the at least one side surface thereof, wherein the one or more seal portions cover at least the portion of the at least one side surface defined by the one or more layers to restrict moisture from ingressing into the apparatus to restrict moisture from ingressing into the apparatus.

23. The method of claim **22**, providing at least one circuit device comprises forming the at least one circuit within the one or more layers formed on the substrate of the first portion.

24. The method of claim **16**, wherein the one or more seal portions at least partially cover each of the substrate surfaces and completely cover the at least one side surfaces of the first portion and the second portion to restrict moisture from ingressing into the apparatus.

25. The method of claim **16**, wherein the substrate of the first portion and the substrate of the second portion each comprise semiconductor substrates.

26. The method of claim **16**, wherein the at least one circuit device forms a part of an implantable medical device.

27. The method of claim **16**, wherein at least one of the first portion and the second portion defines a cavity, wherein a circuit device of the at least one circuit device is located within the cavity.

28. The method of claim **16**, wherein the apparatus further comprises:

one or more interconnect vias formed in at least one of the first portion and the second portion and terminating at one or more surface contacts at the substrate surface, the connection surface, or the at least one side surface of at least one of the first and second portions; and

at least one electrical interconnect extending from the at least one circuit device to at least one of the one or more interconnect vias.

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