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(54) SEMICONDUCTOR DEVICE HAVING A PASSIVATED SURFACE

(71) We, PHILIPS ELECTRONIC AND ASSOCIATED INDUSTRIES LIMITED of Abacus House, 33 Gutter Lane, London, EC2V 8AH a British Company, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

The invention relates to a semiconductor device having a semiconductor body comprising a *p-n* junction terminating at a surface of the body, the surface being covered at least at the area of the *p-n* junction with a passivating layer of semiconductor material. Such a semiconductor device is known, for example, from "Electronics", June 26, 1975, pages 5E and 6E.

The expression "passivating layer" is to be understood to mean herein a layer which physically and chemically protects the semiconductor surface covered by said layer and in addition makes the semiconductor layer electrically independent of external charges which might impede the operation of the device.

It is known that generally the active surface of a semiconductor device should be passivated at least at the area of the *p-n* junction or junctions so as to stabilise the electrical properties of the *p-n* junctions. The passivation should be carried out very carefully when it concerns devices which are to operate at high voltages.

The most frequently used solution to passivate a semiconductor device is the provision on an active surface of the device of a silicon dioxide layer which covers the active surface entirely or partly. Polymers of silicone lacquers are also used for passivating purposes. However, the drawback of these materials is either that they are not very effective or that the provision thereof is difficult.

Silicon dioxide itself has several drawbacks. Firstly, it resistivity is very high. Consequently positive or negative electrical charges may occur on the surface exposed to the atmosphere, which charges may be the result of impurities in the surrounding atmosphere or may be the result of various electrical fields. It is difficult for these charges to flow away to the mass of the underlying substrate and so they move over the surface in a very irregular manner. The result of this is that the said charges may give rise to variations of the characteristics of the semiconductor devices; in particular the breakdown voltages of the *p-n* junctions may vary between very wide limits. It is also known that charges may be stored in the silicon dioxide itself, for example as a result of the presence of sodium ions. These charges may also move and give rise to undesired electrical effects at the semiconductor surface covered by the silicon dioxide.

In addition it is known that silicon dioxide is permeable to moisture or other gaseous constituents. This "permeability" also results in the irregular operation of the semiconductor device.

Attempts have been made to replace silicon dioxide as a passivating agent by other materials, for example, silicon nitride. The use of silicon nitride, however, remains an exception because the temperature necessary for the growth of silicon nitride is high and in addition silicon nitride is often not sufficiently electrically passive.

A recently proposed improvement is the use of oxygen-doped polycrystalline silicon as a passivating layer. The insulating and passivating properties of polycrystalline silicon, either in the undoped condition or doped with, for example, arsenic, were known and already used before. It has been found that the passivating properties of oxygen-doped polycrystalline silicon are exceptionally good. The advantages of the use thereof are described elaborately in the article "Polysilicon layer doped with oxygen

improves devices" in "Electronics", pages 5E and 6E, June 26, 1975. This article deals with the passivation of semiconductor devices by providing one single surface layer of oxygen-doped polycrystalline silicon.

The particular advantage of the use of polycrystalline silicon resides in its electrical neutrality which is not disturbed by the presence of foreign ions in the layer, for example sodium ions which occur in silicon dioxide. As a result of this the provision of the polycrystalline silicon on the surface of a semiconductor device does not form a source of irregularities in the operation of the device. The oxygen-doped polycrystalline silicon is also suitable for covering mesa-junctions due to the fact that the growth temperature (between 650°C and 850°C) is sufficiently low to cause no damage to the *p-n* junctions already formed. It has been found in addition that polycrystalline silicon is impervious to moisture.

The use of polycrystalline silicon as described in the said article, that is the use of a single homogeneous layer of oxygen-doped polycrystalline silicon covered, if desired, with a silicon dioxide layer so as to reduce the influence of leakage currents, however, has an important drawback. The resistivity of oxygen-doped polycrystalline silicon is very high as a matter of fact, namely in the order of 10^{10}ohm cm. As a result of this, parasitic charges on the surface exposed to the atmosphere can only flow away to the underlying substrate with difficulty as in the case of silicon dioxide. The result of this is that the characteristics of the semiconductor devices passivated in this manner and the breakdown voltages of their *p-n* junctions are influenced in an undesired manner.

According to the invention there is provided a semiconductor device having a semiconductor body comprising at least a *p-n* junction terminating at a surface of the body, the surface being covered at least at the area of the *p-n* junction with a passivating layer which comprises a first semiconductor layer situated on said surface and having a resistivity of at least 10^{10}ohm. cm. and a second semiconductor layer on said first layer and having a resistivity of at most 10^{8}ohm. cm.

A device in accordance with the invention has a passivating layer composed of a first semiconductor layer of a very high resistivity and a second semiconductor layer of a comparatively lower, although still high, resistivity. As a result of this charges of different densities and polarities on the surface of the second semiconductor layer can flow away *via* said semiconductor layer, for example, to a neutral zone or to a zone having a fixed potential, for example to earth. Consequently the manufactured device has stable electrical characteristics. In addition, due to the absence of charges on and in the passivating layer, the field lines at the level of the *p-n* junction are regularly distributed, which ensures readily defined breakdown voltages which are higher than those of analogous devices passivated using known methods.

Advantageously, the first and second layers may be provided one after the other in one uninterrupted process step.

The semiconductor material may be a single element, for example germanium or silicon. Alternatively, a semiconductor compound, for example a III-V compound, for example GaAs, may be used.

Advantageously, polycrystalline silicon is selected as a semiconductor material. The polycrystalline silicon may be doped with oxygen so that the first and second semiconductor layers have the desired resistivities.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a diagrammatic cross-sectional view of a first device in accordance with the invention having a diode which is obtained according to the mesa technology, the active surface of which is covered with a passivating layer, and

Figure 2 is a diagrammatic cross-sectional view of another device in accordance with the invention having a transistor obtained according to the planar technology.

The device shown in Figure 1 comprises a semiconductor substrate 1 of a first conductivity type, for example *n*-type. On the surface of the substrate layer is provided a layer 2 of the opposite conductivity type, so in this example of the *p*-type. It will be obvious that the conductivity types may be reversed so that the substrate 1 may be of the *p*-type and the layer 2 of the *n*-type. The regions 1 and 2 form a *p-n* junction 3. According to the usual mesa technology a groove 4 is provided which extends down into the substrate 1. In this manner a mesa diode D of known structure is obtained. The electrodes of the diode D are formed by metal layers 6 and 7 of which the layer 6 is provided on the free surface of the layer 2 and the layer 7 is provided on the rear surface of the substrate 1.

It will be obvious that the *p-n* junction 3 is exposed at the place 3a where it terminates at the groove 4. Especially at this area the diode should be protected physically, electrically and chemically by an electrically neutral and impervious layer. Although the passivation is of particuar importance on the place 3*a* where the *p-n* junction 3 terminates at the groove 4 it should not be neglected in the other exposed regions of the diode. Therefore, the active surface of the

device is preferably covered entirely by a passivating layer except for the electrode 6.

In accordance with the invention the passivating layer is in the form of a layer 8 which comprises two semiconductor layers lying one above the other, namely a first layer 8*a* the resistivity of which is at least 10^{10}ohm. cm., and an upper second layer 8*b* the resistivity of which is at most 10^{8}ohm. cm.

The simultaneous presence of the layers 8*a* and 8*b* ensures a correct electrical insulation in both directions between the diode elements, namely the direction which is parallel to the surface of the said semiconductor layers and the direction normal thereto. In most cases this insulation is sufficient, even for diodes which are to operate at voltages of at least 1000 to 2000 Volts.

Due to the presence of a second layer 8*b*, the resistivity of which is large, although smaller than that of the layer 8*a*, it is possible to cause charges which may be present at the surface exposed to the atmosphere to flow away to regions which are situated farther away from the *p-n* junction 3. In this manner these charges cannot adversely influence the *p-n* junction 3, in particular in the most sensitive region 3*a* of the *p-n* junction. Consequently the device is electrically stable and has a high and readily defined breakdown voltage.

It is advantageous that the passivating layer 8 consists of polycrystalline silicon which is doped with oxygen so that the first layer 8*a* has a resistivity of at least 10^{10} and at most 10^{11}ohm. cm. and the second layer 8*b* is not or is only slightly doped with oxygen. The thickness of the first layer 8*a* is at least 0.5 micron and at most 1 micron and that of the second layer 8*b* is at least 0.2 micron and at most 0.3 micron.

Figure 2 shows a part of a second embodiment of a semiconductor device in accordance with the invention, which device comprises a transistor manufactured according to the planar technology. In Figure 2 a substrate 20 is shown having a transistor T with a diffused base 21 and with a diffused emitter 22. The necessary contacts to the collector 20, the base 21 and the emitter are realized *via* metal layers 23, 24 and 25.

The whole active surface 20A of the device except the contact zones below the layers 24 and 25 is covered with a passivating layer 28 analogous or identical to the layer 8 of Figure 2. The layer 28 comprises a first layer 28*a* having a resistivity of at least 10^{10}ohm. cm. and a second layer 28*b* the resistivity of which is lower than that of the layer 28 and is at most 10^{8}ohm. cm. The passivating layer 28 covers in particular the zones where the collector-base junction 26 and the base-emitter junction 27 terminate at the active surface 20A. These zones which are sensitive to the influence of parasitic surface charges are passivated in this manner.

Although in the example the second semiconductor layer is exposed to the atmosphere, one or more dielectric layers may be provided on said layer, if desired, in as far as at least said dielectric layers or their surfaces comprise no electric charges.

It will be obvious that for the manufacture of devices described with reference to Figures 1 and 2 the insulation layers which were provided on the active surface of the device in the form of etching masks or diffusion masks and which may still be present, have to be removed prior to providing the passivating layers 28 and 8. Otherwise it is necessary to selectively etch the passivating layers 8 and 28 so as to provide therein the apertures necessary for providing the contacts. In the case of passivating layers of polycrystalline silicon, this is done by conventional methods by a chemical etching treatment.

The method of providing a passivating layer in accordance with the invention in which polycrystalline silicon is used as the material of the passivating layer has the advantage that the first and second semiconductor layers may be obtained in one single uninterrupted process step.

The growth of the passivating layer is carried out by decomposition of silane (SiH_4) and of nitrous oxide (N_2O) in the presence of nitrogen in a vacuum or in an open tube, in a furnace at a temperature of at least 650°C and at most 850°C (the preferred temperature is at least 740°C and at most 760°C).

In a first phase which corresponds to the growth of the first layer (8*a* or 28*a*) the quantity of silane is equal to at least 0.1 and at most 0.3 per cent by volume of the quantity of nitrogen, while the quantity of nitrous oxide is at least 1 and at most 10 per cent by volume of the quantity of nitrogen (in accordance with the desired doping concentration and the resulting resistivity of the said layers). In these circumstances the thickness growth per minute is 0.03 to 0.06 micron, which means a time of 8 to 15 minutes for providing a layer whose thickness is 0.5 micron.

In a second phase necessary to form the upper second layer 8*b* or 28*b*, only one variation is carried out. The above-stated quantity of N_2O is made smaller than in the formation of the first layers 8*a* and 28*a*, respectively. It is known that the resistivity of polycrystalline silicon decreases with the oxygen concentration. When no nitrous oxide is used, or when the quantity of nitrous oxide is only equal to at most 1% by volume of the quantity of nitrogen, a thickness

growth of 0.05 to 0.01 micron per minute is realised. This means that the provision of a layer 8*b* or 28*b* whose thickness is 0.2 micron requires a time of 2 to 3 minutes.

It will be obvious that the above-stated values are not absolute values and that they are specific for a method of providing the passivating layer in a given reactor. The method of providing the passivating layer is very flexible, since only one process step is necessary to form the two layers of the structure, in which only the quantity of N_2O is varied.

The above-described manner of provision enables the manufacture of, for example, mesa devices of silicon which are protected by a passivating double layer of polycrystalline silicon, in which the first oxygen-doped layer has a resistivity of 10^{10} to 10^{11} ohm. cm., and the second layer which is doped only comparatively weakly with oxygen has a resistivity of 10^6 to 10^8 ohm. cm., while the breakdown voltages of the resulting *p-n* junctions are approximately 1000 volts, and this in a reproduceable manner. The invention is not restricted to the examples described and notably the semiconductor material of the passivating layer, as well as the doping thereof, and the semiconductor material of the passivated silicon body and of the material and dopants mentioned in the examples may differ.

WHAT WE CLAIM IS:—

1. A semiconductor device having a semiconductor body comprising at least a *p-n* junction terminating at a surface of the body, the surface being covered at least at the area of the *p-n* junction with a passivating layer which comprises a first semiconductor layer situated on said surface and having a resistivity of at least 10^{10} ohm. cm. and a second semiconductor layer on said first layer and having a resistivity of at most 10^8 ohm. cm.

2. A semiconductor device as claimed in Claim 1, in which each of the semiconductor layers consists of a single semiconductor element.

3. A semiconductor device as claimed in Claim 1, in which each of the semiconductor layers consists of a semiconductor compound.

4. A semiconductor device as claimed in Claim 2, in which both the semiconductor layers consist of polycrystalline silicon.

5. A semiconductor device as claimed in Claim 4, in which at least the first semiconductor layer of polycrystalline silicon is doped with oxygen.

6. A semiconductor device as claimed in Claim 4 or 5, in which the second semiconductor layer of polycrystalline silicon is not doped with oxygen.

7. A semiconductor device as claimed in Claim 5, in which the first semiconductor layer has a thickness of at least 0.5 micron and at most 1 micron and a resistivity of at least 10^{10} and at most 10^{11} ohm. cm., and that the second semiconductor layer has a thickness of at least 0.2 micron and at most 0.3 micron, and a resistivity of at least 10^6 ohm. cm. and at most 10^8 ohm. cm.

8. A method of manufacturing a semiconductor device as claimed in Claim 5, in which the passivating layer is provided by decomposing a gas current containing silane (SiH_4), nitrous oxide (N_2O) and nitrogen at a temperature of at least 650°C and at most 850°C.

9. A method as claimed in Claim 8, in which the said temperature is at least 740°C and at most 760°C.

10. A method as claimed in Claim 8 or 9, in which the growth of the entire passivating layer takes place in a continuous process.

11. A method as claimed in Claim 10, in which during the growth of the first semiconductor layer the quantity of silane (SiH_4) is at least 0.1% by volume and at most 0.3% by volume of the quantity of nitrogen, and the quantity of nitrous oxide (N_2O) is at least 1% by volume and at most 10% by volume of the quantity of nitrogen, and that during the growth of the second semiconductor layer, in otherwise equivalent conditions, the quantity of nitrous oxide is reduced to at most 1% by volume of the quantity of nitrogen.

12. A method as claimed in Claim 11, in which during the growth of the second semiconductor layer no nitrous oxide (N_2O) is present so that the second semiconductor layer is not doped with oxygen.

13. A semiconductor device substantially as herein described with reference to Figure 1 or Figure 2 of the accompanying drawings.

14. A method of manufacturing a semiconductor device substantially as herein described with reference to Figure 1 or Figure 2 of the accompanying drawings.

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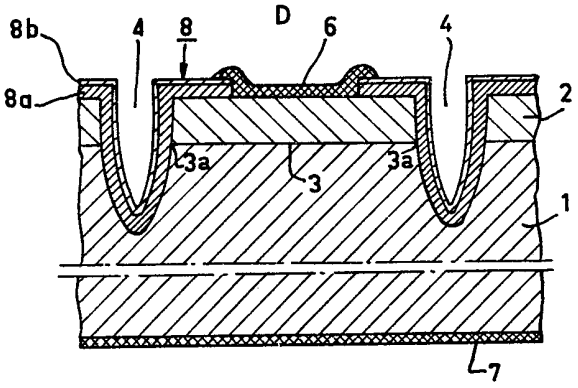


FIG.1

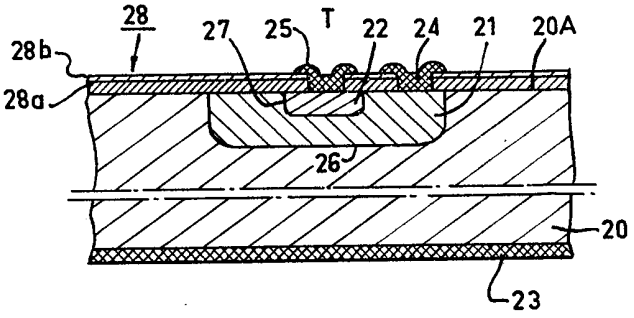


FIG.2