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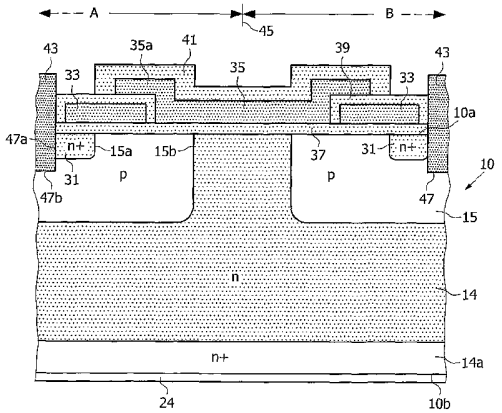

(57) Abstract: A semiconductor device includes a channel-accommodating region (15) extending from a first major surface (10a) of its semiconductor body and separating source and drain regions. The channel-accommodating region defines junctions (15a, 15b) with the source and drain drift regions at the first major surface. First and second gates (33, 35) extend laterally over the first major surface (10a) which are isolated from each other so as to be independently operable. The first gate (33) extends part way across the channel-accommodating region (15) from over said source region junction (15a) towards said drain drift region junction (15b), and the second gate (35) extends over the channel-accommodating region (15) from adjacent to the first gate (33) to over said drain drift region junction (15b) such that the first and second gates are operable to form a conduction channel in the channelaccommodating region between the source and drain regions. In use of the device, a modulating potential is applied to the first gate (33), and a fixed potential is applied to the second gate (35). The device is therefore turned on by application of a sufficient bias potential to the first gate, in combination with a sufficient fixed potential at the second gate. The controlling first gate is spaced from the drain drift region (14) by the associated insulating layer and also a portion of the channelaccommodating region (15). The gate-drain capacitance of the device is therefore negligible, providing a substantial reduction in switching losses.

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DESCRIPTION

POWER SEMICONDUCTOR DEVICES

The present invention relates to power semiconductor devices and to circuit arrangements including such devices.

Vertical insulated gate field effect power transistor semiconductor devices are known which comprise a semiconductor body having an active area with a plurality of electrically parallel transistor cells. Each transistor cell has a source region and a drain region of a first conductivity type, which are separated by a channel-accommodating body region of a second, opposite, conductivity type which extends adjacent to an insulated gate structure.

A desirable property for power transistors is to have good switching performance, that is fast switching and low switching losses when the device is turned on and off. This is particularly important where the power transistor is to be used in the output stage of the power supply, for example a voltage regulation module (VRM) for a PC motherboard, where it is continuously turned on and off at very high frequency.

WO-A-2004/032243 (Applicants' reference PHGB020239) discloses a vertical insulated gate field effect power transistor in which the gate structure comprises first and second gates isolated from each other so as to be independently operable. The first gate is a trench-gate, and the second gate is a planar gate. Simultaneous operation of the first and second gates forms a conduction channel between source and drain regions of the device.

The present invention provides a semiconductor device including: a semiconductor body defining opposed first and second major surfaces; a drain region of a first conductivity type comprising a drain drift region and a drain contact region, with the drain drift region extending to part of the first major surface, and the drain contact region being more highly doped than the drain drift region and extending to the second major surface; a source region of the first conductivity type

extending from the first major surface; a channel-accommodating region of a second, opposite conductivity type extending from the first major surface and separating the source and drain regions and defining junctions with the source and drain drift regions at the first major surface; first and second gates extending laterally over the first major surface which are isolated from each other so as to be independently operable, the first gate extending part way across the channel-accommodating region from over said source region junction towards said drain drift region junction, and the second gate extending over the channel-accommodating region from adjacent to the first gate to over said drain drift region junction, such that the first and second gates are operable to form a conduction channel in the channel-accommodating region between the source and drain regions.

Typically, in use of the device, a modulating potential is applied to the first gate, and a fixed potential is applied to the second gate. The device is therefore turned on by application of a sufficient bias potential to the first gate, in combination with a sufficient fixed potential at the second gate. If no bias potential is applied to the first gate, the net current flow through the conduction channel of the device will be zero.

The controlling first gate is spaced from the drain drift region by the associated insulating layer and also a portion of the channel-accommodating region. The gate-drain capacitance of the device is therefore negligible, providing a substantial reduction in switching losses. The device structure of the present invention is more cost effective to manufacture than that of WO-A-2004/032243. Its fabrication may only require one more photolithographic stage than the manufacture of a known planar VDMOS (vertical double-diffused metal oxide semiconductor) device.

Preferably, the second gate extends between two adjacent transistor cells, and extends over the junction of the first major surface between the drain drift region and the channel-accommodating region in each of the two adjacent cells.

In a preferred embodiment, one of the first and second gates extends part way over the other gate. This serves to minimise the gap between the gates where there will be reduced field effect. If both gates are formed in the same layer and defined in the same photolithographic step, the minimum gap would typically be

about 0.5 micron (or at least the same as the minimum etched dimension for a particular toolset). Overlapping the gates reduces this gap to the thickness of the intervening insulating layer (typically about 50 nm).

Overlapping the gates may also give greater flexibility in cell design, more readily facilitating the fabrication of square or hexagonal arrays, as well as stripe cell geometries.

In a further preferred embodiment, the source and channel-accommodating regions are contacted by a source electrode at the surface of a trench which extends into the semiconductor body from the first major surface. This reduces the area required to achieve these contacts, making the structure more compact.

The first and second gates may be connected to first and second gate terminals for connection to respective control potentials. In particular, the first gate terminal may be connected to a gate driver circuit for applying a modulating potential, and the second gate terminal connected in use to a fixed, bias potential.

The invention further provides a circuit arrangement including a device as described herein, wherein the device is a power transistor connected in series with a second power transistor for supplying a regulated voltage to an output via a switch node connection between the power transistors, the gate driver circuit being included in a control circuit for alternately switching the power transistors on and off.

The present invention also provides a circuit arrangement including a device as described herein, wherein the device is a switch for supplying current to a load connected to one of a source electrode and a drain electrode of the device. In a preferred circuit arrangement embodiment, the second gate terminal of the device is connected to a supply voltage rail of the circuit.

A prior art device and embodiments of the invention will now be described by way of example and with reference to the accompanying schematic drawings, wherein:

Figure 1 shows a cross-sectional side view of the active area of a semiconductor body of a prior art device;

Figure 2 shows a cross-sectional side view of the active area of the semiconductor body of a semiconductor device according to an embodiment of the present invention;

Figures 3 and 4 are graphs showing plots of switching energy loss during turn-on and turn-off, respectively, against time, generated by simulation of a prior art device and a device embodying the invention;

Figure 5 is a graph showing plots of on-resistance and switching energy loss per cycle at turn-on and turn-off generated by simulation of a device embodying the invention;

Figure 6 is a graph showing plots of switching energy figure of merit per cycle at turn-on and turn-off generated by a simulation of the device embodying the invention;

Figure 7 is a graph showing plots of drain current against drain voltage generated by simulation of a prior art device and a device embodying the present invention;

Figure 8 shows a voltage regulation module circuit arrangement including a device embodying the invention connected as a high side power transistor in series with a low side power transistor via a switch node; and

Figure 9 shows a circuit arrangement including a device embodying the invention connected as a low side switch for supplying current to a load and including a protection circuit.

It should be noted that Figures 1 and 2 are diagrammatic and not drawn to scale. Relative dimensions and proportions of parts of these Figures have been shown exaggerated or reduced in size, for the sake of clarity and convenience in the drawings.

Figure 1 illustrates a device of the form disclosed in WO-A-2004/032243. It comprises a monocrystaline silicon semiconductor body 10 having a top major surface 10a opposed to a bottom major surface 10b.

The semiconductor body 10 comprises a relatively highly doped substrate 14a of n-type conductivity which forms the drain contact region of the device. A lower doped semiconductor region 14 of n-type conductivity is provided over the

drain contact region 14a and forms a drain drift region 14. A p-type channel-accommodating region 15 extends between the top surface 10a and the drain drift region 14.

The source region 13 is contacted by a source electrode 23 at the top major surface 10a of the device body. The drain contact region 14a is contacted at the bottom major surface 10b of the semiconductor body by a drain electrode 24.

The gate structure of the device shown in Figure 1 comprises first and second gates 17 and 19 respectively, which are isolated from each other so as to be independently operable. The second gate 19 is provided in a trench which extends from the top major surface 10a, through the channel-accommodating region 15, to the drain drift region 14. The first gate 17 is a planar gate formed over and extending to the side of the second gate. The first gate enables a first, lateral channel portion to be formed in the channel-accommodating region when a gate potential is applied to the first gate. The second gate 19 enables a second, vertical channel portion to be formed in the channel-accommodating region when a gate potential is applied thereto.

Typically, a modulating gate potential is connected to the first gate, and a fixed gate potential is connected to the second gate. Near zero Cgd and Qgd values result from the second gate 19 shielding the first gate 17 from the drain drift region, reducing the gate-drain periphery of the second gate to zero.

Figure 2 illustrates an exemplary embodiment of a power semiconductor device according to the invention. The drain drift region 14 extends to part of the first major surface 10a. Channel-accommodating region 15 extends from the first major surface 10a and separates the source and drain regions, 31 and 14, 14a respectively. It defines a junction 15a with the source region and a junction 15b with the drain drift region adjacent to the first major surface 10a.

A first gate 33, in the form of a planar gate, extends laterally over the first major surface 10a and extends from over the source region, across the junction 15a between the source region and the channel-accommodating region, and part way across the channel-accommodating region 15 towards the junction 15b. The second gate 35 extends from a location adjacent to the first gate, over the channel-

accommodating region 15, and over the junction 15b between the channel-accommodating region and the drain drift region 14.

A portion 35a of the second gate 35 extends partway over the first gate 33. The first and second gates are insulated from the semiconductor body by an insulating layer 37. The thickness of the insulating layer 37 under the second gate 35 may be greater than that under the first gate 33. An insulating layer 39 is provided over the first gate 33, isolating it from the second gate. This layer is typically 20-60 nm thick and may be formed of silicon dioxide or silicon nitride, for example. A further insulating layer 41 is formed over the second gate 35.

In the embodiment illustrated in Figure 2, the source region is contacted by a source electrode 43. This electrode 43 is provided in a trench 47 which extends through source region 31 and into the channel-accommodating region 15. This enables the source electrode to contact both the source region and the channel-accommodating region without the need to provide an area of the top major surface 10a where the channel-accommodating region is to be connected to, thereby making the structure more compact. The source region extends to the sidewall of the trench 47a, and the channel accommodating region extends to its base 47b.

The device of Figure 2 is operable in a similar manner to that of Figure 1. Typically, a fixed gate potential is applied to the second gate 35, and a modulating gate potential applied to the first gate 33. Cgd and Qgd of the device shown in Figure 2 are essentially zero, with the first gate being shielded from the drain drift region, and having zero gate-drain periphery.

It will be appreciated that devices embodying the present invention may be manufactured using techniques well known to those skilled in the art. In particular, the device may be manufactured using processes associated with DMOS or VDMOS technology. Once the first gate 33 has been formed, a short oxidation or deposition process may be carried out to form the insulating layer 39 between the first and second gates. The second gate may then be formed by depositing a layer of polysilicon and using photolithography to pattern this layer to form the second gate 35 and its bond pad. Further oxidation (or deposition) may then be performed to form the insulating layer 41 over the second gate 35.

No plan view of the cellular geometry is shown in the drawings, as the device according to the invention may be fabricated using quite different, known cell geometries. Thus, for example, the cells may have a square geometry as illustrated in Figure 14 of US-A-5378655, or they may have a close-packed hexagonal geometry, or an elongate stripe geometry. In each case, the second gate 35 extends around the boundary of each cell. Figure 2 shows half of each of two adjacent cells A and B, which meet at a boundary having a lateral location indicated by numeral 45 in Figure 2. It will be appreciated that typically a device will comprise many hundreds of parallel cells between the electrodes 43 and 24.

The active cellular area of the device may be bounded around the periphery of the body 10 by various known peripheral termination schemes (also not shown). Such schemes normally show the formation of a thick field-oxide layer at the peripheral area of the first major surface 10a, before the transistor cell fabrication steps. Furthermore, various known circuits (such as gate control circuits) may be integrated with the device in an area of the body 10, between the active cellular area and the peripheral termination scheme. Typically the circuit elements may be fabricated with their own layout in this circuit area using some of the same masking and doping steps as are used for the transistor cells.

The applicants have simulated a device embodying the present invention, to demonstrate its improved performance relative to a simulation of a known device having a typical three terminal trench-gate configuration. In the simulated example, the device embodying the invention had the following characteristics:

Cell pitch	3.5 microns
Drain drift region doping concentration	2.71×10^{16} atoms/cm^3 (25 V silicon)
Drain drift region thickness	4.6 microns
Thickness of insulating layer 37	38 nm
Thickness of insulating layer 39	58 nm
Distance between adjacent channel-accommodating regions	1.1 microns

Source electrode trench depth	0.5 micron
Source electrode trench width	0.8 micron

To demonstrate the relatively low switching losses of the simulated device embodying the invention, Figures 3 and 4 show plots of switching energy loss against time at turn-on and turn-off, respectively, for one cycle. In plots 51 and 51', (plotted using square data points), a constant bias of 5 volts was applied to second gate 35, and in plots 53 and 53' (plotted using triangular data points) a constant bias of 10 volts was applied to second gate 35. Plots 55 and 55' (circular data points) show the performance of the simulated known trench-gate device.

Figure 5 shows simulated measurements of on-resistance (Ron) at a first gate voltage of 10 V (plot 61 with square data points); and switching energy loss per cycle at turn-on (plot 63, triangular data points) and turn-off (plot 65, circular data points) for a device having an active area of 10 mm^2, whilst the bias applied to the second gate is varied from 5 V to 10 V.

It can be seen that increasing the second gate voltage from 5 V to 10 V reduces the Ron of the device. At turn-off, the switching energy loss increases linearly for a second gate bias greater than around 6 V. The turn-off loss is also greater than the turn-on switching loss. The gate resistance used in the simulation was 1.8 Ohm. Reducing the value of the gate resistance will reduce the turn-off loss further. In the embodiment simulated, it can be seen that it is preferable for the second gate to be biased at around 6 V or less.

Figure 6 shows plots of the simulated turn-on, turn-off and "total switching energy figure of merit" (plots 71, 73 and 75 respectively). This figure of merit is the switching energy per cycle (mJ) multiplied by the Ron (mOhm) of the device at a first gate voltage of 10 V. Again the plots are over a range of second gate bias voltages from 5 V to 10 V. Like Figure 5, Figure 6 suggests that a preferred value for the voltage power supply to the second gate is around 6 V or less. With a second gate bias of 5 V the total switching energy figure of merit for the simulated device embodying the invention was found to be around 60% lower than that for the simulated known trench-gate structure.

Figure 7 shows the reverse characteristics of the device embodying the invention (plot 81) and the known trench-gate device (plot 83). In this example, a bias voltage of 5 V was applied to the second gate. It can be seen that the device embodying the invention supports a significantly greater reverse voltage than the known device using the same drain drift region doping concentration.

Figure 8 shows a voltage regulation module (VRM) circuit arrangement 150 including a power transistor 113 embodying the present invention connected as a high side power transistor in series with a low side power transistor 116 for supplying a regulated voltage to an output 151 via a switch node connection 152 between the transistors 113 and 116.

The circuit 150 may be, for example, a synchronous DC-DC buck converter used to convert an input voltage supply (e.g. 12 V) to a lower output voltage supply (e.g. 5 V). The input voltage is applied between an input line voltage terminal 153 and a ground terminal 154. The high side transistor 113 is next to the input terminal 153 and is known as the control FET. The low side transistor 116 is connected to the ground terminal 154 and is known as the synchronous FET (syncFET). The switch node connection 152 feeds through an inductor 155 and across a capacitor 156 to the output line voltage terminal 151.

A control circuit 157 has a control portion 171 with one input on a control terminal 158 and another input fed from the output 151 via a feedback path 159. The controller portion 171 supplies control signals to a gate driver circuit 173 for the high side transistor 113 and to a gate driver circuit 176 for the low side transistor 116. These control signals are alternating signals which cause the control and sync FETs 113, 116 to conduct alternately. The mark-space ratio, that is the ratio of the time for which the control FET 113 conducts to the time the sync FET 116 conducts is varied to achieve the desired voltage on the ouput 151.

The second gates 35 of the cells of the transistor 113 are connected to a second gate terminal 111 which is connected to terminal means Vcc for connecting a supply to a fixed gate potential to the second gate terminal 111. As shown in Figure 8, the terminal Vcc to which the gate terminal 111 is connected is the terminal which supplies a 12 V line voltage to the gate driver circuit 173.

Alternatively, the gate terminal 111 could be connected to the 12 V input line voltage terminal 153 or to the 5 V output line voltage terminal 151.

The first gates 33 of the cells of the transistor 113 are connected to a first gate terminal 121 which is connected to the gate drive circuit 173 for applying a modulating potential to the gate terminal 121.

The power transistor of the invention described herein is particularly advantageous for use as the high side control FET because low switching losses are a primary consideration for this transistor. Low switching losses are less important for the low side syncFET 116 for which a low on-state resistance is important. A trench gate MOSFET power transistor may therefore be preferable for use as the syncFET 116.

Figure 9 shows a circuit arrangement 160 including a power transistor embodying the present invention connected as a low side power transistor in series with a load L between a voltage supply line terminal 163 and a ground terminal 164. The power transistor 113 acts as a switch for supplying current to the load L when its drain electrode is connected to the load L via the terminal 162 of the circuit 160. A control circuit 167 has a control portion 171 connected to a control input terminal 168. The control portion 171 supplies control signals to a gate driver circuit 173 for the transistor 113.

The second gates 35 of the cells of the transistor 113 are connected to a second gate terminal 111 which is connected to terminal means V_F for connecting a supplied fixed gate potential to the gate terminal 111. The first gates 33 of the cells of the transistor 113 are connected to a first gate terminal 121 which is connected to the gate driver circuit 173 for applying a modulating potential to the gate terminal 121.

The control circuit 167 includes protection circuit means 174 for the power transistor switch 113. The protection circuit means 174 is not shown connected in Figure 9, since its connections to the other circuit elements shown within the circuit arrangement 160 depend on whether it is adapted and arranged for one or more of the functions of voltage overload protection, current overload protection, and temperature overload protection.

The embodiment shown in Figure 2 is a MOSFET device. However, it will be appreciated that the drain contact region 14a may be of opposite conductivity type to region 14 to provide a vertical IGBT.

The particular example described in relation to Figure 2 is an n-channel device. By using opposite conductivity type dopants to those shown in Figure 2, a p-channel device can be provided. In that case, the regions 31, 14 and 14a are of p-type conductivity, the region 15 is of n-type, and a hole inversion channel is induced in the region 15 by the first and second gates 33 and 35.

A vertical discrete device has been described with reference to Figure 2. However, an integrated device is also possible in accordance with the invention. In this case, the region 14a may be a doped buried layer between a device substrate and the epitaxial low-doped drain drift region 14. This buried layer 14a may be contacted by an electrode 24 at the front of the major surface 10a, via a doped peripheral contact region which extends from the surface 10a to the depth of the buried layer.

From reading the present disclosure, other variations and modifications will be apparent to persons skilled in the art. Such variations and modifications may involve equivalent and other features which are already known in the art, and which may be used instead of or in addition to features already described herein.

Although Claims have been formulated in this Application to particular combinations of features, it should be understood that the scope of the disclosure of the present invention also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any Claim and whether or not it mitigates any or all of the same technical problems as does the present invention.

Features which are described in the context of separate embodiments may also be provided in combination in a single embodiment. Conversely, various features which are, for brevity, described in the context of a single embodiment, may also be provided separately or in any suitable subcombination. The Applicants hereby give notice that new Claims may be formulated to such features and/or combinations of

such features during the prosecution of the present Application or of any further Application derived therefrom.

CLAIMS

1. A semiconductor device including: a semiconductor body (10) defining opposed first and second major surfaces (10a, 10b); a drain region of a first conductivity type comprising a drain drift region (14) and a drain contact region (14a), with the drain drift region extending to part of the first major surface (10a), and the drain contact region being more highly doped than the drain drift region and extending to the second major surface (10b); a source region (31) of the first conductivity type extending from the first major surface; a channel-accommodating region (15) of a second, opposite conductivity type extending from the first major surface (10a) and separating the source and drain regions and defining junctions (15a, 15b) with the source and drain drift regions at the first major surface; first and second gates (33, 35) extending laterally over the first major surface (10a) which are isolated from each other so as to be independently operable, the first gate (33) extending part way across the channel-accommodating region (15) from over said source region junction (15a) towards said drain drift region junction (15b), and the second gate (35) extending over the channel-accommodating region (15) from adjacent to the first gate (33) to over said drain drift region junction (15b), such that the first and second gates are operable to form a conduction channel in the channel-accommodating region between the source and drain regions.

2. A device of claim 1, wherein the semiconductor body (10) has an active area comprising a plurality of electrically parallel transistor cells (A, B), the second gate extending between two adjacent transistor cells and over the junction (15b) at the first major surface (10a) between the drain drift region (14) and the channel-accommodating region (15) of each of the two adjacent cells.

3. A device of claim 1 or claim 2 wherein one of the first and second gates (33 or 35) extends part way over the other gate (35 or 33).

4. A device of any preceding claim wherein the source and channel accommodating regions (31, 15) are contacted by a source electrode (43) at the

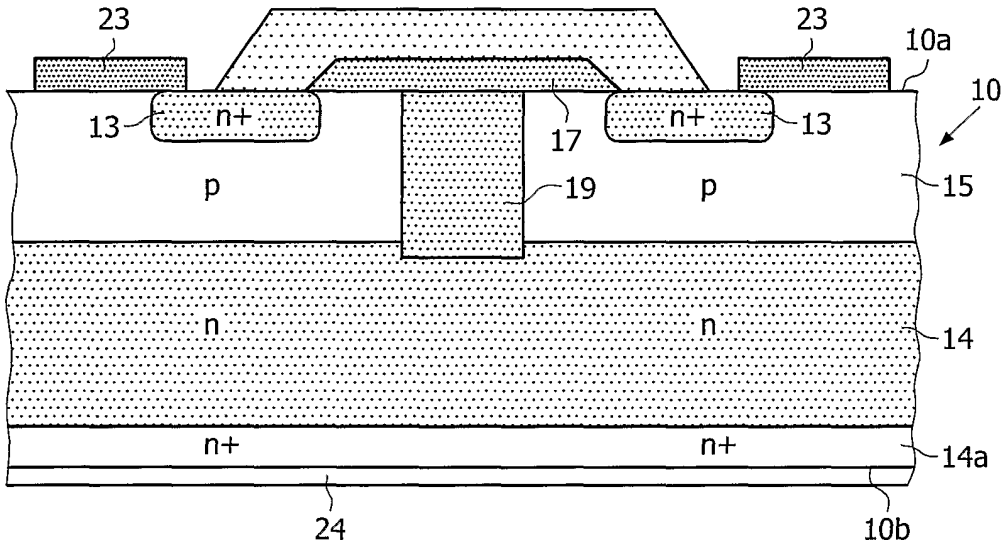
surface of a trench (47) which extends into the semiconductor body (10) from the first major surface (10a).

5. A device of any preceding claim, wherein the first and second gates (33, 35) are connected to first and second gate terminals (121, 111) for connection to respective control potentials.

6. A circuit arrangement including a device of claim 5, wherein the first gate terminal (121) is connected to a gate driver circuit (173) for applying a modulating potential, and the second gate terminal (111) is connected in use to a fixed potential (Vcc).

7. A circuit arrangement of claim 6, wherein the device is a power transistor (113) connected in series with a second power transistor (116) for supplying a regulated voltage to an output (151) via a switch node connection (152) between the power transistors, the gate driver circuit (173) being included in a control circuit (157) for alternately switching the power transistors on and off.

8. A circuit arrangement of claim 6, wherein the device is a switch (113) for supplying current to a load (L) connected to one of a source electrode and a drain electrode of the device.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10b

FIG. 1

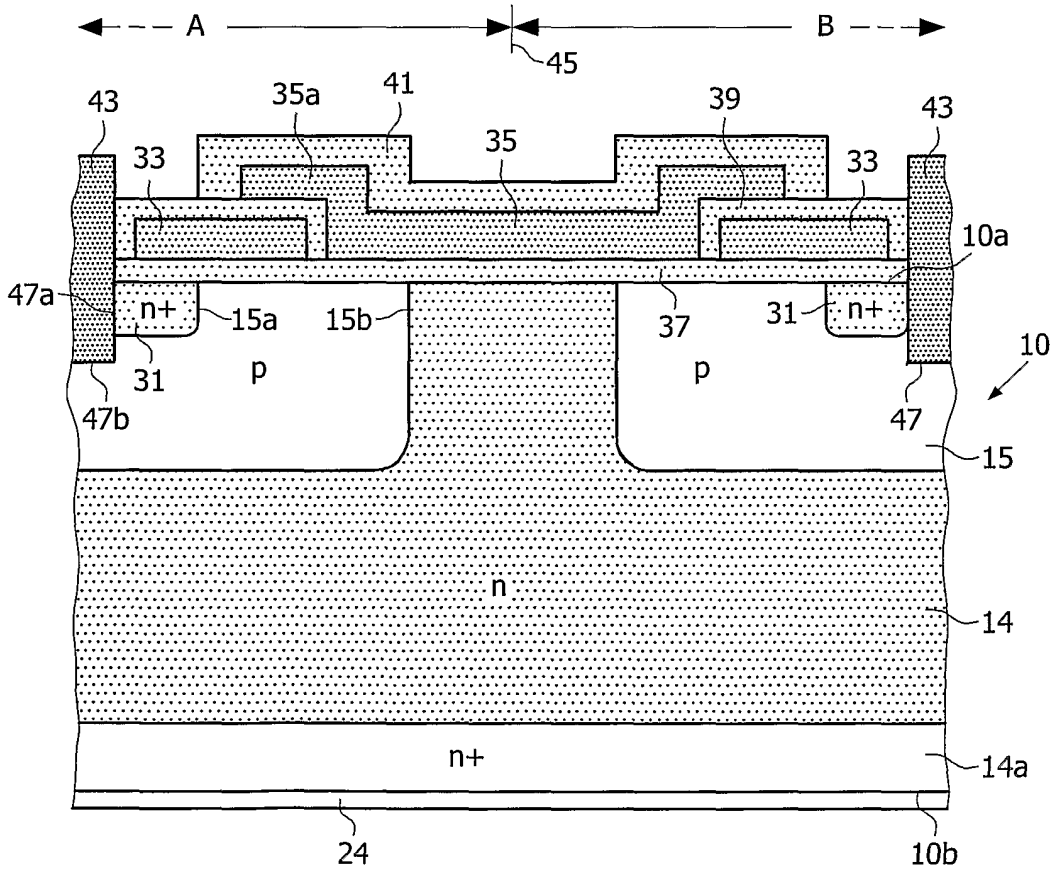
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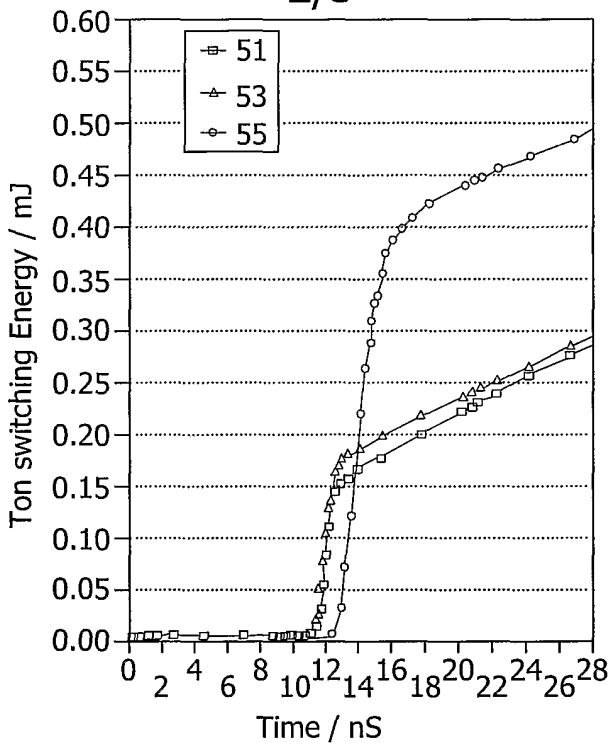
FIG. 2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51
53
55
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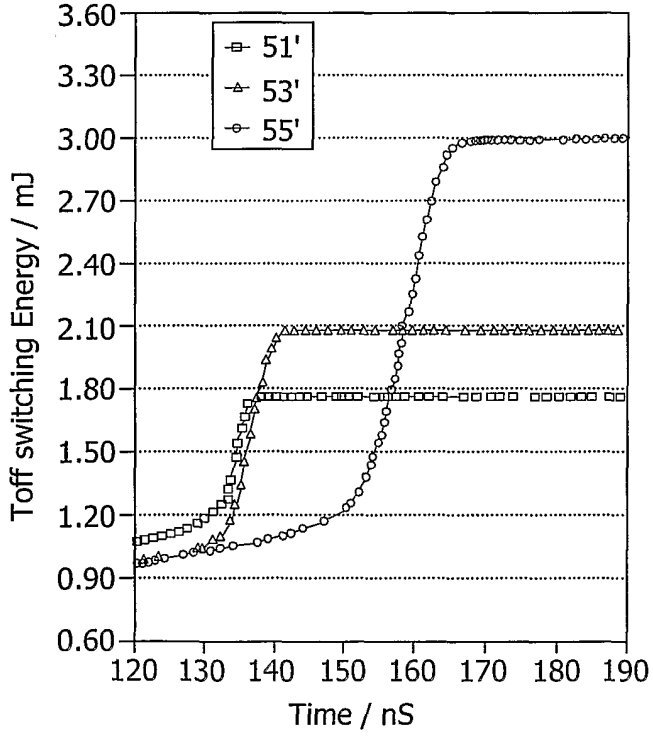
Time / nS

FIG. 3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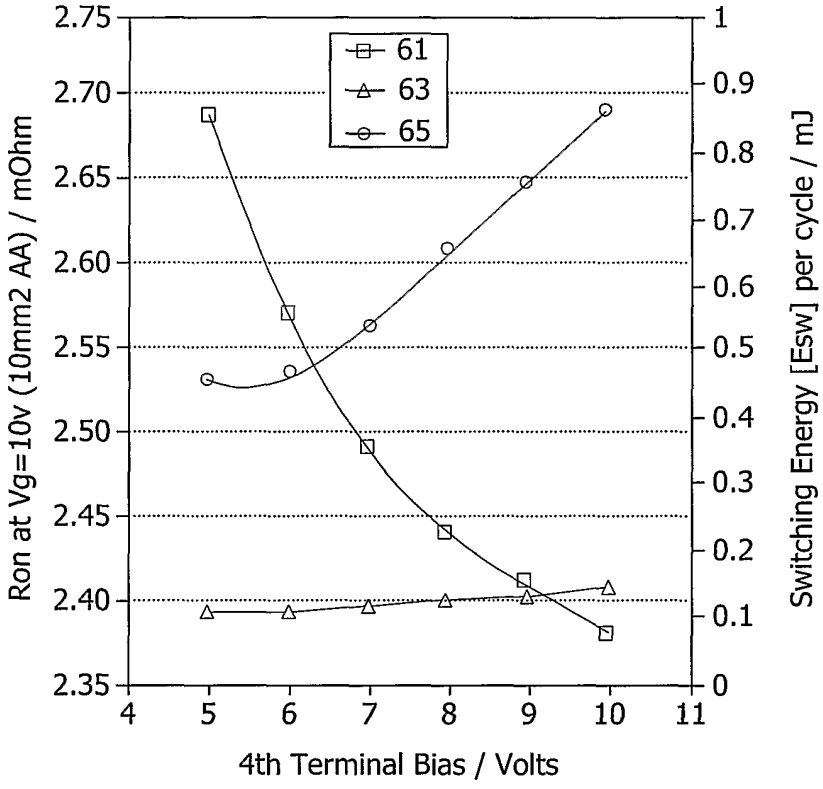
Time / nS

FIG. 4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2.40
2.35
Ron at Vg=10v (10mm2 AA) / mOhm
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Switching Energy [Esw] per cycle / mJ
61
63
65
4
5
6
7
8
9
10
11
4th Terminal Bias / Volts

FIG. 5

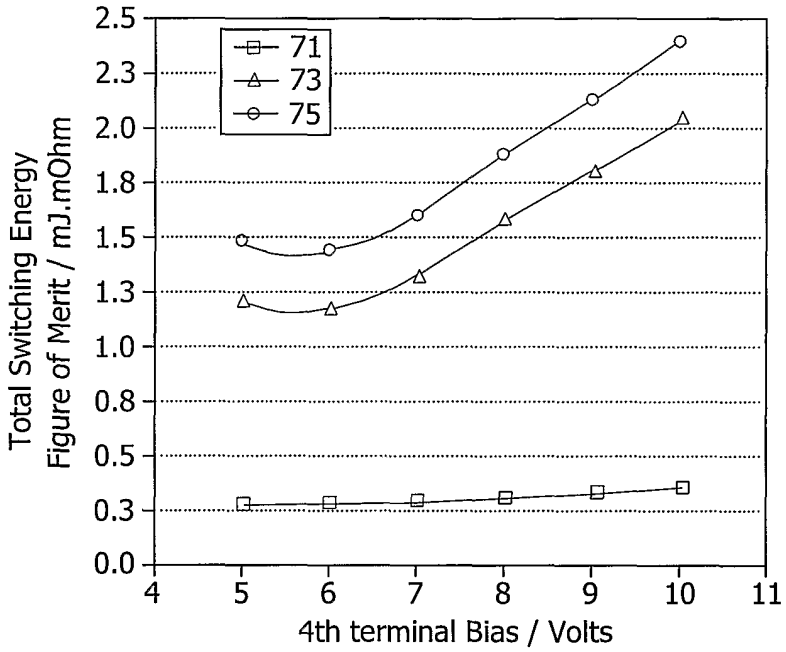
Total Switching Energy
Figure of Merit / mJ.mOhm
2.5
2.3
2.0
1.8
1.5
1.3
1.0
0.8
0.5
0.3
0.0
71
73
75
4
5
6
7
8
9
10
11
4th terminal Bias / Volts

FIG. 6

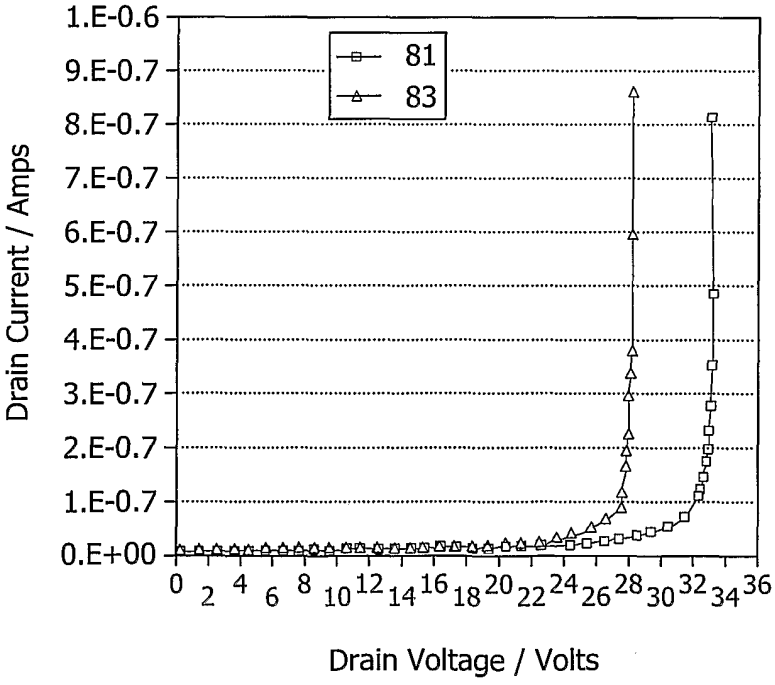
Drain Current / Amps
1.E-0.6
9.E-0.7
8.E-0.7
7.E-0.7
6.E-0.7
5.E-0.7
4.E-0.7
3.E-0.7
2.E-0.7
1.E-0.7
0.E+00
81
83
0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36
Drain Voltage / Volts

FIG. 7

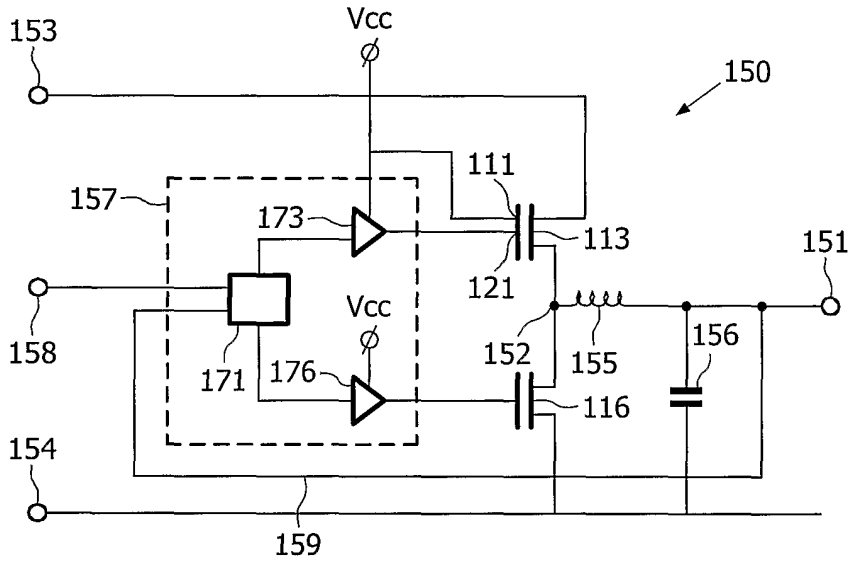
153
Vcc
150
111
157
173
113
151
121
158
Vcc
152
155
156
171
176
116
154
159

FIG. 8

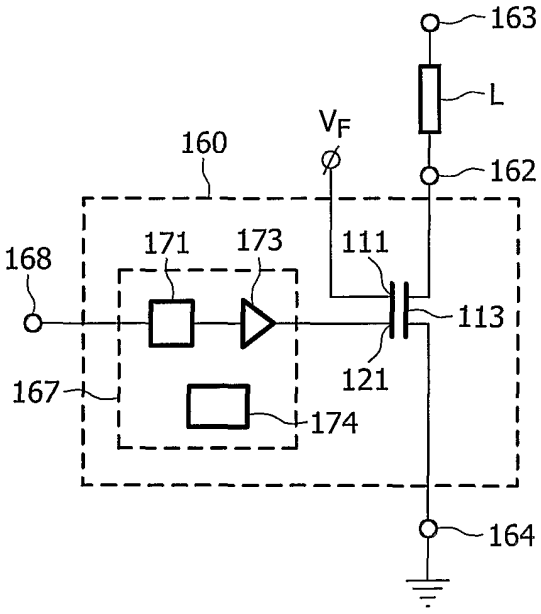
163
L
V_F
160
162
171
173
111
168
113
121
167
174
164

FIG. 9