May 6, 1969 C. T. ALTFATHER 3,443,159

FREQUENCY SHIFT RELAYING APPARATUS

Filed May 6, 1966 Sheet 1 of 2

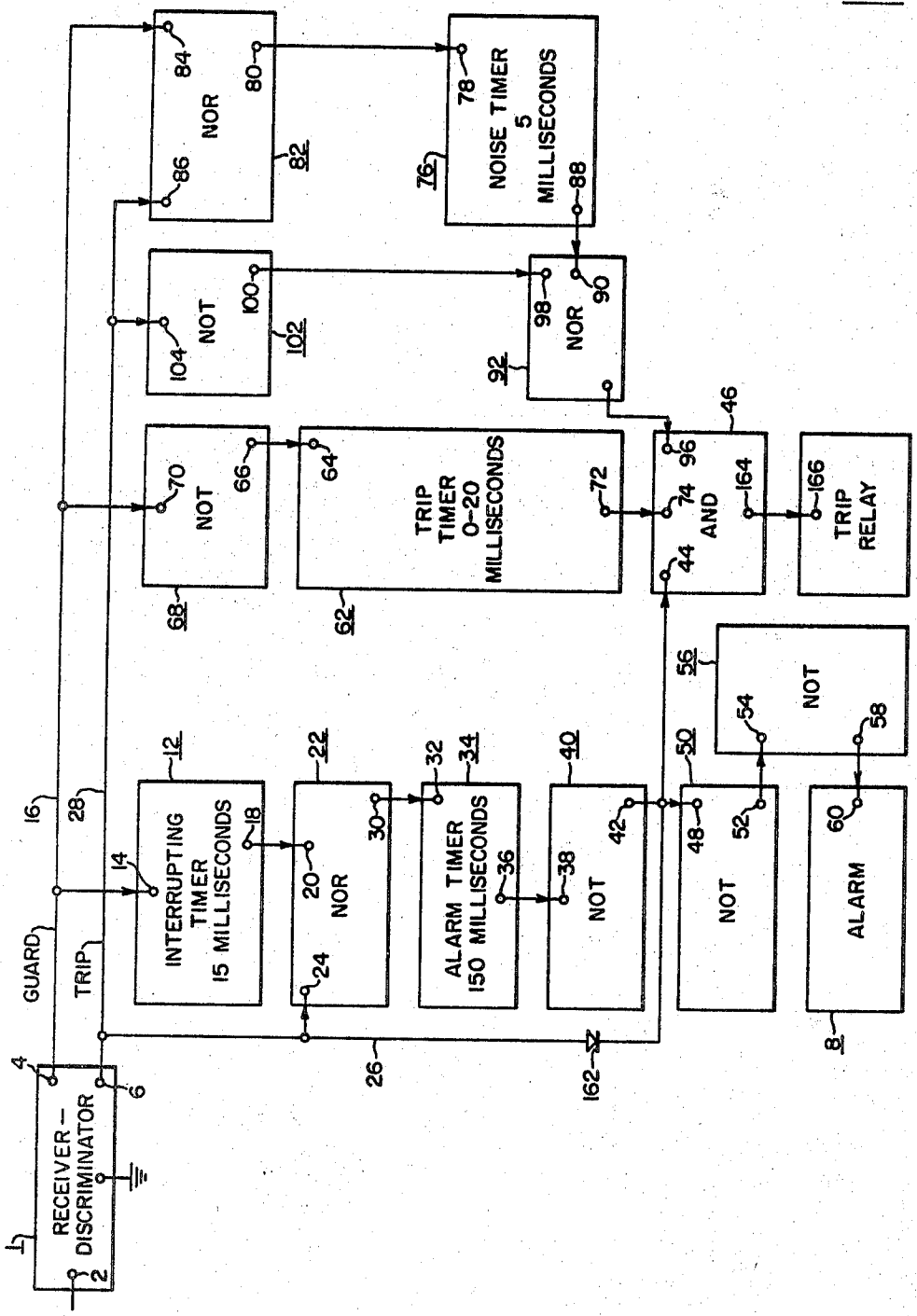

FIG. 1.

WITNESSES

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FREQUENCY SHIFT RELAYING APPARATUS

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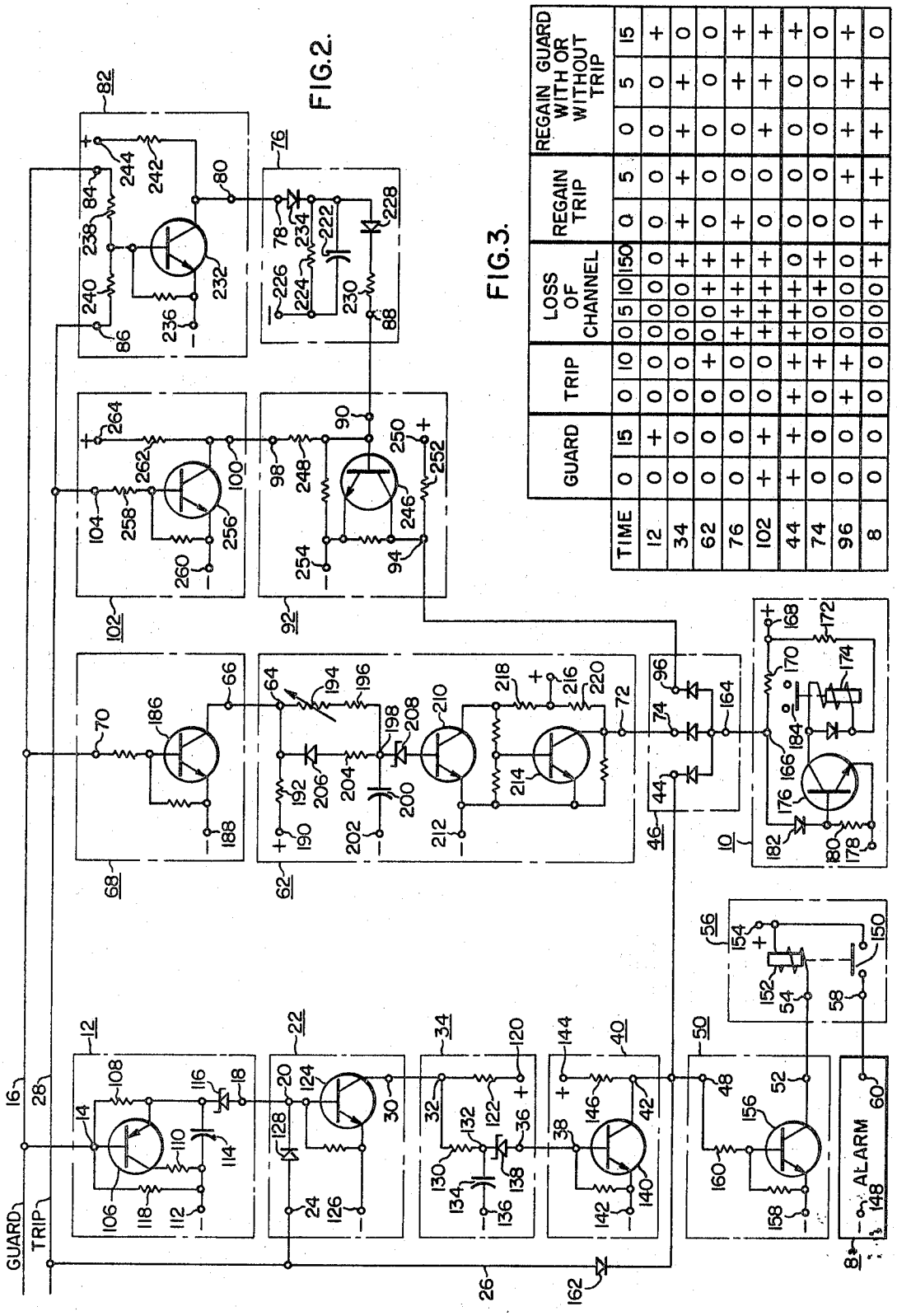

FIG. 2.

FIG. 3.

TIME	GUARD		TRIP		LOSS OF CHANNEL			REGAIN TRIP		REGAIN GUARD WITH OR WITHOUT TRIP		
	0	15	0	10	0	5	10	0	5	0	5	15
12	0	+	0	0	0	0	0	0	0	0	0	+
34	0	0	0	0	0	0	+	+	+	+	+	0
62	0	0	0	+	0	+	+	0	0	0	0	0
76	0	0	0	0	+	+	+	+	0	0	+	+
102	+	+	0	0	+	+	+	0	0	+	+	+
44	+	+	+	+	+	+	0	0	0	0	0	+
74	0	0	0	+	0	+	+	0	0	0	0	0
96	0	0	+	+	0	0	0	0	+	+	+	+
8	0	0	0	0	0	0	+	+	+	+	+	0

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FREQUENCY SHIFT RELAYING APPARATUS

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U.S. Cl. 317—36 11 Claims

This application relates generally to relaying apparatus and more particularly to relaying apparatus actuated in response to a shift in the output frequency of a remotely located transmitter.

In the application of frequency-shift carrier to the control of protective relaying apparatus, it has been customary to employ two relays, one energized when guard frequency is being transmitted and the other energized when trip frequency is being transmitted. The breaker trip coil in such apparatus is connected in series with a normally-open contact of the trip relay and normally-closed contact of the guard relay so that the breaker will not be tripped until the guard frequency is absent and the trip frequency is present. Additionally, a time delay may be introduced between the drop-out of the guard relay and the pickup of the trip relay in order to reduce the possibility of incorrect tripping due to spurious frequencies in a noise burst. To further minimize the possibility of incorrect tripping due to noise, an intermediate frequency filter with a narrow pass band and steep skirts may be used in the receiver. To reduce the intensity of the noise generated frequencies on the trip side of the receiver output, the intermediate frequency filter response is adjusted to have its peak response on the guard side of the channel. However, this involves critical adjustments that are sensitive to frequency drift in the crystals and the filter response and incorrect performance may result.

This invention is directed to circuitry by which the guard relay and the narrow intermediate filter are eliminated. Tripping for a true fault condition is accomplished more reliably and with minimum delay and greater security against incorrect tripping by transient conditions. Furthermore, solid state components are used throughout the logic circuitry.

An object of this invention is to provide a positively operated apparatus actuated by a frequency shift of the input signal.

A further object of this invention is to provide such an apparatus which is not affected by a noise.

Another object of this invention is to provide a positive actuated alarm signal for indicating the loss of the transmitted signal.

Another object is to provide an apparatus for preventing false tripping as a consequence of a prolonged severe noise.

Another object of this invention is to provide means for resetting a time delay apparatus in the event that the noise frequency shifts momentarily into the guard range.

Other objects of the invention will appear from the appended claims, the description and the drawings, in which:

FIGURE 1 is a block-diagram representation of a frequency shift actuated relaying apparatus embodying the invention;

FIG. 2 is a similar view showing the schematic circuitry which may be used in carrying out the invention; and,

FIG. 3 is a tabulation helpful in the understanding of the invention.

Referring to the drawings by characters of reference, the numeral 1 indicates generally a receiver-discriminator having an input 2 and a pair of output terminals 4 and 6. An input signal is applied between the input terminal

2 and ground and the output guard signal will appear between the output terminal 4 and ground while the trip output signal will appear between the output terminal 6 and ground. Normally, the signal supplied to the receiver discriminator 1 will be of such a frequency that the receiver discriminator will maintain the guard output terminal 4 energized and the trip output terminal 6 deenergized whereby an alarm 8 and a trip relay 10 will remain in their deenergized conditions.

The trip relay 10 is designed to be operated only in response to a condition in which guard output energization is eliminated and trip output energization is applied substantially immediately and when the trip output energization is maintained for a predetermined time interval. The alarm 8 is arranged to be energized to sound an alarm solely after both of the output terminals 4 and 6 have been deenergized for a predetermined time period to indicate along both the guard and trip signals or loss of channel.

More specifically, an alarm timer interrupting timer 12 has its input connection 14 connected to guard output bus 16 which is connected to and energized by the output terminal 4. The timer output 18 is connected to one input terminal 20 of a NOR network 22. A second input terminal 24 of the NOR network 22 is connected by means of a bus 26 to a trip output bus 28 which bus is in turn connected to and energized by the output terminal 6 of the receiver-discriminator 1.

The output terminal 30 of the NOR network 22 is connected to the input terminal 32 of a second or alarm timer 34 which has its output terminal 36 connected to input terminal 38 of a NOT network 40. The output terminal 42 of the NOT network is connected to a first input terminal 44 of an AND network 46 and to input terminal 48 of a NOT network 50. The output terminal 52 of the NOT network is connected to input terminal 54 of a second NOT network 56 which has its output terminal 58 connected to input terminal 60 of the alarm 8. The bus 26, in addition to being connected to the input terminal 24 of the NOR network 22, is connected to the output terminal 42 of the NOT network 40. A third or trip timer 62 has its input terminal 64 connected to output terminal 66 of a NOT network 68, the input terminal 70 of which is connected to the guard bus 16. The output terminal 72 of the timer 62 is connected to the second input terminal 74 of the AND network 46.

A fourth or noise timer 76 has its input terminal 78 connected to output terminal 80 of a NOR network 82. The NOR network 82 is provided with a first input terminal 84 which is connected to the guard bus 16 and a second input terminal 86 which is connected to the trip bus 28. The output terminal 88 of the timer 76 is connected to a first input terminal 90 of a NOR network 92, the output terminal 94 of which is connected to the third input terminal 96 of the AND network 46. The second input terminal 98 of the NOR network 92 is connected to the output terminal 100 of a NOT network 102, the input terminal 104 of which is connected to the trip output bus 28.

Typical examples of the time delays imposed by the timers are illustrated in FIG. 1 and are as follows: the interrupting timer 12 has a 15 millisecond timing interval; the alarm timer 34 has a 150 millisecond timing interval; the trip timer 62 has a 2 to 20 millisecond timing interval; and the timer 76 has a 5 millisecond timing interval. The actual time of the timer 76 will depend upon the noise characteristics of the network and 5 milliseconds has been chosen for explanations. For purposes of the tabulation of FIG. 3, it has been assumed that the trip timer 62 is adjusted to provide a 10 millisecond timing interval.

Referring more specifically to FIG. 2, it will be ob-

served that the interrupting timer **12** includes a transistor **106** having its base connected to its input terminal **14** and its emitter connected through a resistor **108** to the input terminal **14**. The collector of the transistor **106** is connected through a resistor **110** to a grounded terminal **112** to which one terminal of a capacitor **114** is connected. The other terminal of the capacitor **114** is connected to the emitter of the transistor **106** and to one terminal of a Zener diode **116** which has its other terminal connected to the output terminal **18**. When the guard bus **16** is energized, the base of the transistor **106** can never become negative with respect to the emitter and the transistor **106** is held blocked. Under these conditions, charging current for capacitor **114** will flow from the input terminal **14** through resistor **108** to the ground terminal **112**. The charging of the capacitor **114** will be at a rate determined by the magnitude of the resistor **108**. The time interval for charging the capacitor **114** to the breakover voltage of the Zener diode **116** may be, as indicated above, 15 milliseconds.

When the guard bus **16** becomes deenergized, base current flows through resistor **118** and the transistor **106** becomes conducting. The resistor **110** is of a relatively low value whereby the capacitor **114** rapidly discharges through the emitter collector circuit of the transistor **106**. This insures that the capacitor **114** becomes substantially completely discharged each time the guard bus **16** is deenergized.

The alarm timer **34** is provided with a positive potential input terminal **120** which is connected to the timer input terminal **32** through a resistor **122**. This terminal **32** is connected through terminal **30** to the collector of a transistor **124** (in the NOR network **22**) which has its emitter connected to a grounded terminal **126** whereby the terminals **30** and **32** are maintained substantially at ground potential during the conductive intervals of the transistor **124**. The base of the transistor **124** is connected to the first input terminal **20** of the NOR circuit **22** and through a diode **128** to the second input terminal **24**. It will be appreciated that whenever the terminal **24** or terminal **20** is energized, base current will flow through the transistor **124** to maintain it conductive and the potential of the timer terminal **32** will be held substantially at ground potential. The input terminal **32** is connected through a resistor **130** to one terminal **132** of a capacitor **134**, the other terminal of which is connected to a grounded terminal **136**. The capacitor terminal **132** is connected through a Zener diode **138** to output terminal **36** of the timer **34**.

It will be appreciated that when the terminal **32** of the timer **34** is maintained at ground potential, no charging current can flow through the resistor **130** to charge the capacitor **134** and any charge in the capacitor **134** at the time that the terminal **132** is brought to ground potential will discharge through the resistor **130** and the transistor **124**. When, however, the transistor **124** is rendered non-conducting charging current for the capacitor **134** will flow through the resistors **122** and **130** at a rate determined primarily by the magnitude of the resistance of the resistor **122**. At the end of a predetermined timing interval, which as suggested above may be 150 milliseconds, the potential of the terminal **132** of the capacitor **134** will be raised to such a potential that the Zener diode **138** will breakover and raise the potential of the output terminal **36** of the timer.

The NOT circuit **40** comprises a transistor **140** having its base connected to its input terminal **38** and its emitter connected to a grounded terminal **142**. The NOT circuit is further provided with a potential supplying terminal **144** which is connected through a resistor **146** to the output terminal **42** and to the collector of the transistor **140**. When the potential of the input terminal **38** of the NOT network **40** is raised above ground, base current flows through the transistor **140** which will then conduct and maintain the potential of the output terminal **42** at ground potential. When, however, no input potential is supplied to the input terminal **38** the transistor **140** will become non-conducting and the potential of the output terminal **42** will be raised due to the connection thereof to the positive potential input terminal **140** through the resistor **146**.

The alarm **8** can take any desired form such as a visual or audio device connected between a grounded terminal **148** and its input terminal **60**. The input terminal **60** is connected through normally closed contacts **150** of a relay **152** to a positive potential input terminal **154**. The winding of the relay **152** is connected between the positive potential input terminal **154** and the output terminal **54**. This output terminal **54** is connected through input terminal **52** of NOT network **50** and the collector and emitter of a transistor **156** to a grounded terminal **158**. The base of the transistor **156** is connected through a resistor **160** to input terminal **48** of the NOT network **50**.

The AND network **46** comprises three diodes having their anodes connected together to an output terminal **164** and their cathodes connected individually to the three input terminals **44, 74** and **96**. The output terminal **164** is connected to input terminal **166** of the trip relay **10**.

The trip relay **10** includes a positive potential input terminal **168** which is connected through a first resistor **170** to the input terminal **166** and a second resistor **172**, the winding of a relay **174**, the collector emitter circuit of a transistor **176** to a grounded terminal **178**. The base of the transistor **176** is connected through a resistor **180** to the grounded terminal **178** and through a diode **182** to the input terminal **166**. The impedance to forward current flow through the diode **182** is sufficient so that insufficient base current will flow through the transistor **176** if any one of the input terminals **44, 74** and **96** are connected to ground as will be set forth below. Unless current flows through the diode **182**, the transistor **176** will remain non-conducting and the relay **174** will remain deenergized to maintain its normally open contacts **184** open.

The third or trip timer **62** has its input terminal **64** connected to output terminal **66** of NOT network **68**. When the transistor **186** conducts it connects the terminals **64** and **66** to ground through a grounded terminal **188**. The base of the transistor **186** is connected through a current limiting resistor to the guard bus **16** through the input terminal **70**. The timer **62** is provided with a positive potential input terminal **190** which is connected through a resistor **192**, the input terminal **64**, a variable resistor **194** and a fixed resistor **196** to one terminal **198** of a capacitor **200** having its other terminal connected to a grounded terminal **202**. The capacitor **200** may discharge through a circuit provided by the resistor **204** and diode **206** which are connected in shunt with the timing resistors **194** and **196**.

The capacitor terminal **198** is connected through a Zener diode **208** to the base of a transistor **210** the emitter of which is connected to a grounded terminal **212** and the collector of which is connected to the base of a second transistor **214** through a current limiting resistor and to a positive potential input terminal **216** through a voltage dropping resistor **218**. The terminal **216** is connected through a resistor **220** to the collector of the transistor **214** and to the output terminal **72**. The emitter of the transistor **214** is connected to the grounded terminal **212**.

It will be appreciated that upon interruption of current flow through the transistor **186** of the NOT network **68**, the input terminal **64** of the trip timer **62** will be disconnected from the grounded terminal **188** and charging current will flow to the capacitor **200** from the positive potential terminal **190** through the resistors **192, 194** and **196**. At the end of a predetermined timing interval, the potential of the capacitor terminal **198** will be elevated sufficiently to cause the Zener diode **208**

to breakover and supply base current to the transistor 210 which thereupon conducts to remove the base drive current from the transistor 214. This drive current previously flowed from the positive potential input terminal 216 through resistor 218, a current limiting resistor, and from base to emitter of the transistor 214 to grounded terminal 212. When transistor 214 becomes non-conducting, the potential of the output terminal 72 of the timer is elevated to apply a blocking potential to the diode of the AND circuit connected to its second input terminal 74.

The third input terminal 96 of the AND network 46 is controlled by means of a network which comprises the NOR networks 82 and 92, the NOT network 102 and the noise timer 76. The noise timer 76 comprises a capacitor 222 shunt connected with a resistor 224. One common terminal of the capacitor 222 and resistor 224 is connected to a grounded terminal 26 and the other common terminal is connected to the input terminal 78 through a diode 234 and connected to the output terminal 88 through a diode 228 and a resistor 230.

The timer 76 is controlled by the conductive condition of a transistor 232 of the NOR network 82. For this purpose, the collector of the transistor 232 is connected through output terminal 80 to the input terminal 78 of the timer 76. The transistor 232 has its emitter connected to a grounded terminal 236 and its base connected through resistors 238 and 240 to the first and second inputs terminal 84 and 86. The collector of transistor 232 is connected through a resistor 242 to a positive potential input terminal 244.

The NOR network 92 comprises a transistor 246 which has its base connected directly to the first input terminal 90 and through a resistor 248 to its second input terminal 98. The NOR network 92 further includes a positive potential input terminal 250 which is connected through a resistor 252 and output terminal 94 to the collector of the transistor 246. The emitter of the transistor 246 is connected to a grounded terminal 245.

The potential of the second input terminal 98 is controlled as a consequence of the conductive condition of a transistor 256 of the NOT network 102. The base of the transistor 256 is connected through a current limiting resistor 258 and the NOT input terminal 104 to the trip bus 28. The emitter of the transistor 256 is connected to a grounded terminal 260 while the collector of the transistor 256 is connected through the output terminal 100 and a voltage dropping resistor 262 to a positive potential input terminal 264.

A reference to FIG. 3 will indicate that the alarm 8 is energized only when the alarm timer 34 has timed out. The trip relay 10 may be energized solely upon the timing out of the trip timer 62 provided; however, that this time out occurs in response to the termination of the energization of the guard bus 16 followed by the energization of the trip bus 28.

It is believed that any remaining details of construction may best be understood by description of the operation which is as follows: Under normal conditions a remote signal source energizes the receiver-discriminator 1 with a signal such that the output terminal 4 is energized and the output terminal 6 is deenergized. Upon initial energization of the guard bus 16, the input terminal 14 of timer 12 is energized thereby terminating conduction of the transistor 106 and initiating or timing interval of the timer. The capacitor 114 charges at a rate as determined by the magnitude of the resistance of the resistor 108 and at the end of a predetermined time interval (in this instance assumed to be 15 milliseconds), the Zener diode breaks over and energizes output terminal 18. The base drive thereby provided for the transistor 124 of the NOR network 22 causes the transistor 124 to conduct and discharge the capacitor 134 of the second or alarm timer 34. This removes any output potential which might have existed at its output terminal 36.

When no potential is present at the output terminal 36, the transistor 140 of the NOT network 40 becomes non-conducting and the potential of its output terminal 42 is raised to provide a blocking potential at the first input terminal 44 of the AND network 46. The increase in potential of the output terminal 42 also is applied to the input terminal 48 of the NOT network 50 which renders transistor 156 conducting to energize the winding of the relay 152 which thereupon opens its normally closed contacts 150 to interrupt any energization of the alarm 8.

Energization of the guard bus 16 also energizes the input terminal 70 of the NOT network 68 whereby its transistor 186 conducts and grounds its output terminal 66. This results in the discharge of the capacitor 200 of the trip timer 62 and to insure that the transistor 210 is held blocked. When the transistor 210 is blocked, base current flows in the transistor 214 whereby the potential of the timer output terminal 72 maintained at ground potential as indicated by O in FIG. 3. This in turn connects the second input terminal of the AND circuit 74 to ground potential so that current flowing in the trip relay 10 from the positive potential input terminal through the resistor 170 will flow through transistor 214 and not through the transistor 176.

Energization of the guard bus 16 also results in energization of the second input terminal 84 of the NOR circuit 82 to cause the transistor 232 to conduct and connect its output terminal 80 to ground. This prevents any current flow from the positive potential input terminal 244 to the noise timer 76 so that the capacitor 222 thereof will discharge primarily through resistor 230, the base of the transistor 246 and the interconnected negative terminals 254 and 226. A lesser amount may discharge through the timing resistor 224.

Typically, resistor 242 has an ohmic value of 6.8K, resistor 224 has an ohmic value of 470K, and resistor 230 has an ohmic value of 82K. Consequently capacitor 222 will be charged to approximately 90% of the supply voltage if both guard and trip discriminator output are absent for about 8 milliseconds. After the discriminator regains either guard or trip output, the charge on capacitor 222 will keep transistor 246 conductive for approximately 40 to 50 milliseconds. The time depends upon component tolerances and the gain of the individual transistor, i.e., the amount of base current needed to keep it fully conducting. Consequently, the delay introduced by noise timer 76 can vary widely, depending upon how frequently and for how long it forces the discriminator to have zero output.

When the transmitter is keyed from guard to trip, it is desired that the interval during which there is no output from the discriminator should not permit sufficient charge to build up on capacitor 222 to keep transistor 246 conducting for any longer than the minimum delay of the timer 62. This permits a user who has no appreciable noise problem to keep his overall trip time to a minimum. The purpose of resistor 224 is to drain off any residual charge on capacitor 222, so that its charge will have to build up from substantially zero voltage. Resistors 230 and 242 primarily control the charge and discharge time of the capacitor 222.

At the end of the timing period of the timer 76, its output terminal 88 will go to ground potential. At this time, the trip bus 28 is not energized, the transistor 256 of the NOT circuit will be blocked and base drive current for the transistor 246 will flow from the positive terminal of the NOT circuit through resistors 262 and 248 base to emitter in the transistor 246 whereby transistor 246 conducts and maintains the potential of the third input terminal 96 of the AND circuit 46 substantially at ground potential. The maintenance of the terminals 74 and 96 substantially at ground potential is insurance that the transistor 176 will not conduct.

In the even of the existence of a fault in a transmission network (not shown) protected by the trip relay **10**, a signal will be supplied to the input terminal **2** of the receiver-discriminator **1** which will cause the output terminal **4** to become deenergized and the output terminal **6** to become energized. This reversal of energization of the buses **16** and **28** occurs a short interval that is much shorter than the timing period of the alarm timer **34**.

Deenergization of the guard bus **16** results in a substantially instantaneous reduction of the output potential at the output terminal **18** of the timer **12**. This may cause a short period of blocking of the transistor **124** and a partial timing of the alarm timer **34**. As soon, however as the trip bus **28** is energized, the transistor **124** will again become conducting due to base current flow from the trip bus **28** through diode **128** to the ground terminal **126**. This results in the input terminal **32** of the alarm timer **34** being again lowered to ground potential and the discharge of any charge which may have accumulated on the capacitor **134** during the time interval subsequent to the deenergization of the guard bus and the energization of the trip bus. This rendering of the NOR circuit **22** actuated to deenergize its output terminal **30** insures that the timer **34** cannot time out and energize the alarm **8**. This can only be done in the absence of deenergization of both the guard bus **16** and the trip bus **28** and then only when this absence is for the full timing period of the alarm timer **34**. Under all other operating conditions as for example the energization of the guard bus, the timer **12** times out to prevent timing out of the timer **34** or the energization of the trip bus **28** actuates the NOR circuit **22** to ensure that the timer **34** does not time out.

Deenergization of the guard bus **16** causes the transistor **186** to become non-conducting whereby the input potential of the input terminal **64** of the timer **62** is disconnected from ground and the timing capacitor **200** of the timer **62** begins to be charged at a rate determined primarily by the setting of the resistor **194**. Assuming that the timing interval of the timer **62** is set at 10 milliseconds, as indicated in FIG. 3, and that the trip bus is energized for this 10 millisecond period, the potential of the capacitor terminal **198** reaches a sufficient potential to cause the Zener diode **208** to breakover and the transistor **210** to conduct. Conduction of the transistor **210** shunts the base drive current for the transistor **214** which thereupon ceases to conduct and the potential of the output terminal **72** of the timer is elevated due to its energization from the positive potential input terminal **16** through the resistor **220**. This places a positive potential on the second input terminal **74** of the AND circuit **46** to back-bias the diode connected thereto.

Energization of the trip bus **28** will re-establish conduction through the transistor **232** which would otherwise be interrupted due to deenergization of the guard bus **16** whereby the timer **76** will be prevented from increasing the potential of the output terminal **80** thereof.

Energization of the trip bus **28** causes base current to flow in the transistor **256** of the NOT circuit **102** to ground the input terminal **98** of the NOR circuit **92**. Since at this time there is no input to the NOR input terminal **90** from the timer **76** and no input to the NOR input terminal **98** from the NOT terminal **100**, the transistor **246** of the NOR network **92** ceases to conduct. This results in the third input terminal **96** of the AND network **46** being positively biased due to its connection to the positive input terminal **250** through the resistor **252**.

As described above when all of the diodes of the AND network **46** are positively biased, base current from the transistor **176** is no longer shunted through the AND network **46** and instead flows through the diode **182** in the base circuit of the transistor **176** which thereupon conducts to establish a circuit extending from the positive potential input terminal **168** through resistor **172**, the energizing winding of the relay **184** and transistor **176** to the grounded terminal **178**. This current flow results in energization of the relay **174** and closure of its normally open contacts **184** which control, through circuitry not illustrated, the trip mechanism of a circuit breaker or other circuit opening device of the network being protected by the relay system.

Under some conditions of operation, however, due to noise or other failures of the channel supplying the receiver-discriminator **1**, the guard bus **16** as well as the trip bus **28** may be deenergized. The absence of the trip signal holds the transistor **256** of the NOT network **68** blocked and the potential of the second input terminal **98** of the NOR circuit **92** is elevated sufficiently to insure that the transistor **246** will continue in its conducting conditions to maintain the potential of the third input terminal of the AND network **46** substantially at ground potential. This prevents any base current flow to the transistor **176** and a consequent operation of the trip relay **10**.

Immediately upon loss of the guard signal, the transistor **232** of the NOR network **82** became non-conducting and elevated the potential of output terminal **80** of the timer **76**. This elevation in the potential of output terminal **80** caused the capacitor **222** to become fully charged substantially instantaneously to place the timer **76** into its set-to-time condition.

Under conditions in which both buses **16** and **28** are deenergized the timer **34** begins to timeout. At the end of the timing interval of the alarm timer **34** the timer **34** times out and renders the transistor **140** of the NOT network **40** conducting to terminate base current flow through the transistor **156** of the NOT network **50** whereby the relay **152** of the network **56** is deenergized and closes its normally closed contacts **150**. This closure of the contacts **150** energizes the input terminal **60** and the alarm **8** provides its signal as indicated by the plus mark in FIG. 3.

Should the trip output bus be energized without a subsequent reenergization of the guard bus **16** to reset the alarm timer **34**, the connection of the bus **26** to ground through the diode **162** and transistor **140** of the NOT network **40** will prevent any re-establishment of base current flow through the transistor **124** of the NOT circuit **22** and any resetting of the alarm timer **34**. Unless alarm timer **34** is reset, the transistor **140** of the NOT circuit will continue to conduct and prevent any energization of the relay **152** to open the alarm circuit and discontinue signal alarm. As indicated in FIG. 3, this condition of continued energization of the alarm will remain.

In the event that the guard signal is retured to the guard bus with or without the return of a trip signal, the alarm **8** at the end of the time out period of the interrupting timer **12** will be deenergized. Such an operation in which the trip bus **28** is energized as well as the guard bus **16** will not be a normal operation for actuation of the trip relay and if it does occur may occur as for example due to noise on the input circuit to the receiver-discriminator **1**. As indicated in FIG. 3 as long as the guard signal is present, the trip timer relay **62** cannot time out. As long as the trip timer **62** does not time out, the potential of the second input terminal to the AND network **46** cannot be elevated sufficiently to block current flow through the diode connected thereto. This is one of the requisites for establishing base current flow to the trip transistor **176**.

As indicated in FIG. 3, the sole result of the establishment of guard potential or the unlikely occurrence of both guard potential and trip potential will be to cause further operation of the alarm at the end of the timing interval of the timer **12** but not to cause tripping and operation of the tripping relay **10** which can only be actuated, after loss of channel, by a return of the energization of the guard bus **16** followed by a deenergization thereof.

In the event of a momentary energization of the guard bus **16**, caused as for example by noise, the noise timer **76** will maintain the transistor **246** conducting. In gen-

eral effect the noise timer differentiate between a false and a true energization of the guard bus **16**.

Since numerous changes may be made in the above described apparatus and different embodiments of the invention may be made without departing from the spirit thereof, it is intended that all matter contained in the foregoing description or shown in the accompanying drawings, shall be interpreted as illustrative and not in a limiting sense.

What is claimed and is desired to be secured by United States Letters Patent is as follows:

1. In a relaying network, first and second signal actuated input means, a first output means, a plurality of timers, each said timer being operable to time out a time interval, a first control network interconnecting both of said input means and said first output means and including a first and a second of said timers, said first timer having a lesser time interval than said second timer, said first control network being effective to place said first output means in a first condition solely when upon the expiration of said time interval of said second timer, said first control network including first circuit means interconnecting said first timer to said first input means and to said second timer, said circuit means being responsive to the expiration of said time interval of said first timer for preventing the timing out of said time interval of said second timer, said circuit means being responsive to a first energized condition of said first input means to initiate the timing of said time interval of said first timer, said network including second circuit means interconnecting said second timer to said second input means, said second circuit means being responsive to a first energized condition of said second input means to prevent the timing out of said time interval of said second timer, said first control network being effective to place said first output means in its said first condition solely upon the expiration of a concurrent time interval that both of said input means have been removed from their said first conditions, said concurrent interval being at least equal to said time interval of said second timer.

2. The combination of claim **1** in which there is provided a second output means, a second control network interconnecting a third of said timers and one of said input means and responsive to the removal of said input means from its said one condition to initiate the timing out of the said time interval of said third timer, a third control network interconnecting said second and said third timers to said second output means, said third control network being effective to place said second output means in a first condition solely when said third timer has timed out its said time interval and said second timer has not timed out its said time interval.

3. The combination of claim **2** in which there is provided a fourth control network, including means connecting a fourth of said timers to both of said input means, said fourth control network being responsive to the rendering of a certain of said input means in its said first condition to initiate the timing out of said time interval of said fourth timer, said fourth control network being connected to said third control network and including circuit means interconnecting said fourth timer to said third control network, said third control network being effective to place said second output means in its said first condition solely when said third and fourth timers have timed out their said time intervals and said second timer has not timed out its said time interval.

4. The combination of claim **3** in which said fourth control network includes a third circuit means connected in bypass relation with said fourth timer between one of said input means and said third network, said third circuit means being responsive to the absence of said first condition in the one of said input means to which said third circuit means is connected to maintain said third control network ineffective to place said second output means in its said first condition irrespective of the timing out of said time interval of said fourth timer.

5. In a relaying network, first and second input means, each of said means having a first and a second condition, a plurality of timers, each said timer having a set and a timed out condition and operable to time out a time interval as a consequence of changing from its set to its timed out condition, a first output means, a first control network connecting a first of said timers to said first input means and a second of said timers to said first timer and to said second input means, a second control network connecting a third of said timers to one of said input means, a third control network connecting said second and said third timers to said first output means and effective to place said first output means in a first condition solely when said third timer is in its said timed out condition and said second timer has not been placed in its said timed out condition.

6. The combination of claim **5** in which said third control network is effective when said second timer is in its said timed out condition to prevent the placing of said first output means in its said first condition irrespective of the condition of said third timer.

7. The combination of claim **6** in which a fourth control network connects a fourth of said timers between at least a certain of said input means and said third control network, said third control network being effective to place said first output means in its said first condition solely when said third and said fourth timers are in their said timed out conditions and said second timer is not in its said timed out condition.

8. The combination of claim **7** in which a fifth control network connects said input means to said third control network, said fifth control network being responsive to a said cnodition of the one of said input means to which said fifth control network is connected to prevent said third control network from placing said first output means in its said first condition even though said fourth timer is in its said timed out condition.

9. In a relaying network, a guard input means, a trip input means, a trip output means, a plurality of timers, each said timer having a timed-out condition and a non-timed-out condition including an initial state, each said timer being effective to time out a determined time period as it goes from its said initial state to its said timed-out condition, and AND network having a plurality of input connections and having an output connection connected to said trip output means for controlling the energized condition thereof, first means connecting a first of said timers between said guard means and a second of said timers, second means connecting said second timer to said trip input means, third means connecting said second timer to a first of said input connections of said AND network, fourth means connecting a third of said timers between said guard means and a second of said input connections of said AND network, a fifth means connecting a fourth of said timers between at least one of said input means and a third of said input connections of said AND network, said first means being effective to cause said first timer to time out its said time period as a consequence of the presence of a critical potential at said guard input means for a time interval at least equal to said time period of said first timer, said first means being effective to actuate said first timer into its said initial state as a consequence of the absence of said critical potential at said guard input means, said first means being effective to prevent the timing out of the timing interval of said second timer when said first timer is in its said timed-out condition, said second means being effective to maintain said second timer in its said non-timed-out condition in the presence of a critical potential at said trip input means, said AND network being effective to place said trip output means in a first energized condition solely when a critical signal is present at all of its said input connections, said third means being ineffective to supply to said first input connection of said AND network its said critical signal when said second timer

is in its said timed-out conditions, said fourth means being effective to prevent the timing out of said third timer when said gurad input means is at its critical potential, said fourth means further being effective to supply to said second input connections of said AND network its said critical signal solely when said third timer is in its said timed-out condition, said fifth means being effective to place said fourth timer in its said initial state as a consequence of the absence of said critical potential of the said input means to which it is connected, and said fifth means further being effective to cause said fourth timer to time out its said determined time period as a consequence of the return of said critical potential of the said input means to which said fifth circuit is connected for a time period not less than said time interval of said fourth timer.

10. The combination of claim **9** in which said second means is connected to said third means, said third means being effective when said second timer is in its said timed-out condition to render said second means ineffective to actuate said second timer into its said non-timed-out condition.

11. The combination of claim **10** in which said first energized condition of said trip output means actuates a disconnect device, an alarm device, and sixth means connecting said second timer to said alarm device, said sixth means being effective solely when said second timer is in its said timed-out condition to actuate said alarm device to provide an alarm signal.

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