



(51) International Patent Classification:
H01L 33/36 (2010.01)

(21) International Application Number:

PCT/KR2013/011914

(22) International Filing Date:

20 December 2013 (20.12.2013)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

10-2012-0150388

21 December 2012 (21.12.2012)

KR

10-2013-0029136 19 March 2013 (19.03.2013)

KR

10-2013-0032481 27 March 2013 (27.03.2013)

KR

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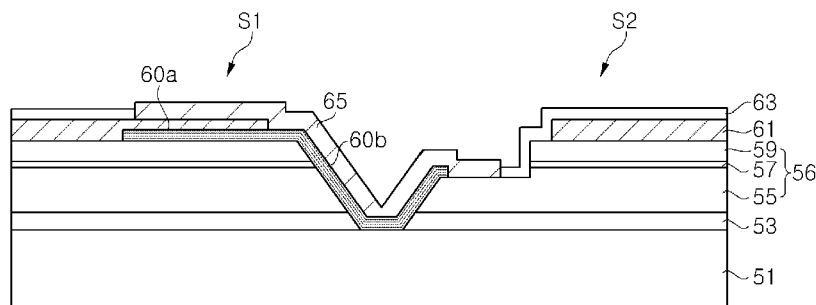
(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: LIGHT EMITTING DIODE AND METHOD OF FABRICATING THE SAME



(57) Abstract: Exemplary embodiments of the present invention provide a light emitting diode including a first light emitting cell and a second light emitting cell disposed on a substrate and spaced apart from each other, a first transparent electrode layer disposed on the first light emitting cell and electrically connected to the first light emitting cell, a current blocking layer disposed between a portion of the first light emitting cell and the first transparent electrode layer, an interconnection electrically connecting the first light emitting cell and the second light emitting cell, and an insulation layer disposed between the interconnection and a side surface of the first light emitting cell. The current blocking layer and the insulation layer are connected to each other.

Description

Title of Invention: LIGHT EMITTING DIODE AND METHOD OF FABRICATING THE SAME

Technical Field

- [1] The present invention relates to a light emitting diode and a method of fabricating the same, and more particularly, to a light emitting diode including a plurality of light emitting cells connected to each other via interconnections on a single substrate, and a method of fabricating the same.

Background Art

- [2] Gallium nitride (GaN) based light emitting diodes (LEDs) have been used in a wide range of applications including full color LED displays, LED traffic sign boards, white LEDs, etc. In recent years, with higher luminous efficacy than existing fluorescent lamps, white light emitting diodes are expected to overtake existing fluorescent lamps in the field of general lighting.
- [3] A light emitting diode may be driven to emit light by forward current and require a supply of direct current. Thus, when the light emitting diode is directly connected to an alternating current (AC) source, the light emitting diode repeats on/off operation dependent upon a direction of electric current, and cannot continuously emit light and may be easily damaged by reverse current.
- [4] To solve such problems of a light emitting diode, WO 2004/023568 (A1) of Sakai et. al., entitled "LIGHT-EMITTING DEVICE HAVING LIGHT-EMITTING ELEMENTS", discloses a light emitting diode which can be used through direct connection to a high voltage AC source.
- [5] The AC light emitting diode of WO 2004/023568(A1) includes a plurality of light emitting elements connected to each other via an air bridge interconnection to be driven by an AC source. Such an air-bridge interconnection may be easily broken by external force and may cause short circuit due to deformation by external force.
- [6] To solve such a drawback of the air bridge interconnection, AC light emitting diodes are disclosed in Korean Patent Nos. 10-069023 and 10-1186684, for example.
- [7] Figure 1 is a schematic plan view of a typical light emitting diode including a plurality of light emitting cells, and Figure 2 and Figure 3 are sectional views taken along line A-A of Figure 1.
- [8] Referring to Figure 1 and Figure 2, the light emitting diode includes a substrate 21, a plurality of light emitting cells 26 including S1, S2, a transparent electrode layer 31, an insulation layer 33, and an interconnection 35. In addition, each of the light emitting cells 26 includes a lower semiconductor layer 25, an active layer 27, and an upper

semiconductor layer 29, and a buffer layer 23 may be interposed between the substrate 21 and the light emitting cells 26.

- [9] The light emitting cells 26 are formed by patterning the lower semiconductor layer 25, active layer 27, and upper semiconductor layer 29 grown on the substrate 21, and the transparent electrode layer 31 is formed on each of the light emitting cells S1, S2. In each of the light emitting cells 26, an upper surface of the lower semiconductor layer 25 is partially exposed by partially removing the active layer 27 and the upper semiconductor layer 29 for connection to the interconnection 35.
- [10] Next, the insulation layer 33 is formed to cover the light emitting cells 26. The insulation layer 33 includes a side insulation layer 33a covering side surfaces of the light emitting cells 26 and an insulation protective layer 33b covering the transparent electrode layer 31. The insulation layer 33 is formed with an opening through which a portion of the transparent electrode layer 31 is exposed and an opening through which the lower semiconductor layer 25 is exposed. Then, the interconnection 35 is formed on the insulation layer 33, in which a first connection section 35p of the interconnection 35 is connected to the transparent electrode layer 31 of one light emitting cell S1 through the opening of the insulation layer 33, and a second connection section 35n of the interconnection 35 is connected to the lower semiconductor layer 25 of another light emitting cell S2 adjacent the one light emitting cell S1 through the other opening of the insulation layer 33. The second connection section 35n is connected to an upper surface of the lower semiconductor layer 25, which is exposed by partially removing the active layer 27 and the upper semiconductor layer 29.
- [11] In a conventional technique, the interconnection 35 is formed on the insulation layer 33 and thus may be prevented from deformation by external force. In addition, since the interconnection 35 is separated from the light emitting cells 26 by the side insulation layer 33a, it is possible to prevent short circuit of the light emitting cells 26 by the interconnection 35.
- [12] However, such a conventional light emitting diode may have a limit in current spreading in areas of the light emitting cells 26. Specifically, electric current may be concentrated under one end of the interconnection 35 connected to the transparent electrode layer 31 instead of being evenly spread in the areas of the light emitting cells 26. Current crowding may become severe with increasing current density.
- [13] Moreover, such a conventional light emitting diode may have problems in that some of the light generated in the active layer 27 may be absorbed and lost by the interconnection 35, and the thickness of the insulation layer 33 may need to be increased to prevent formation of defects such as pin-holes and the like.
- [14] Furthermore, since a portion of the upper surface of the lower semiconductor layer 25 is exposed for electric connection of the second connection section 35n, the active

layer 27 and the upper semiconductor layer 29 are partially removed, and may thereby reduce an effective light emitting area.

[15] In order to prevent current crowding, a current blocking layer 30 may be disposed between the transparent electrode layer 31 and the light emitting cells 26 to prevent current crowding under the connection end of the interconnection 35.

[16] Figure 3 is a sectional view of a light emitting diode including a current blocking layer 30 in the related art.

[17] Referring to Figure 1 and Figure 3, the current blocking layer 30 is disposed under the connection end of the interconnection 35, and may thereby prevent current crowding under the connection end of the interconnection 35. In addition, the current blocking layer 30 may be formed as a reflector such as a distributed Bragg reflector, and may thereby prevent light generated in the active layer 27 from being absorbed into the connection end of the interconnection 35.

[18] However, when the current blocking layer 30 is additionally formed as shown in Figure 3, a photolithography process for forming the current blocking layer 30 is added, and may thereby increase manufacturing costs.

[19] Moreover, as in the light emitting diode of Figure 2, the light emitting diode of Figure 3 may also have problems, such as optical loss due to absorption of light generated in the active layer 27 by the interconnection 35, reduction in effective light emitting area, and increase in thickness of the insulation layer 33 to prevent defects such as pinholes in the insulation layer 33.

Disclosure of Invention

Technical Problem

[20] Exemplary embodiments of the present invention provide a light emitting diode, which may employ a current blocking layer while preventing increase in the number of photolithography processes, and a method of fabricating the same.

[21] Exemplary embodiments of the present invention also provide a light emitting diode capable of reducing absorption of light by an interconnection, and a method of fabricating the same.

[22] Exemplary embodiments of the present invention also provide a light emitting diode, which includes a plurality of light emitting cells each having an increased effective light emitting area, and a method of fabricating the same.

[23] Additional features of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention.

Solution to Problem

[24] An exemplary embodiment of the present invention provides a light emitting diode,

the light emitting diode including a first light emitting cell and a second light emitting cell disposed on a substrate and spaced apart from each other, a first transparent electrode layer disposed on the first light emitting cell and electrically connected to the first light emitting cell, a current blocking layer disposed between a portion of the first light emitting cell and the first transparent electrode layer, an interconnection electrically connecting the first light emitting cell and the second light emitting cell, and an insulation layer disposed between the interconnection and a side surface of the first light emitting cell. The current blocking layer and the insulation layer are connected to each other.

- [25] Thus, the insulation layer separating the interconnection from the side surface of the light emitting cell may be formed together with the current blocking layer by the same process. Since the insulation layer is formed together with the current blocking layer, there may be no need for formation of the insulation layer together with an insulation protective layer as in the related art, thereby allowing the insulation protective layer and the interconnection to be formed using the same mask.
- [26] In addition, the current blocking layer and the insulation layer may include distributed Bragg reflectors. Thus, the light emitting diode may significantly reduce an amount of light absorbed by the interconnection. Further, the insulation layer is formed as a distributed Bragg reflector formed of multiple layers, thereby efficiently preventing formation of defects such as pinholes.
- [27] Further, the current blocking layer and the insulation layer may be disposed between the first light emitting cell and the interconnection over an entire overlapping area between the first light emitting cell and the interconnection.
- [28] Further, the insulation layer may be disposed between the interconnection and the side surface of the second light emitting cell.
- [29] The light emitting diode may further include an insulation protective layer disposed on the first light emitting cell and the second light emitting cell. The insulation protective layer is disposed outside an area in which the interconnection is formed. In addition, a side surface of the insulation protective layer may face a side surface of the interconnection on a coplanar surface. The side surface of the insulation protective layer may contact the side surface of the interconnection. The side surface of the insulation protective layer may be spaced apart from the side surface of the interconnection.
- [30] In some embodiments, the light emitting diode may further include a first transparent conductive layer disposed between the insulation layer and the interconnection. In addition, the first transparent conductive layer may be connected to the first transparent electrode layer. Further, the first transparent conductive layer may be formed of the same material as that of the first transparent electrode layer.

- [31] Each of the first and second light emitting cells may include a lower semiconductor layer, an upper semiconductor layer, and an active layer disposed between the lower semiconductor layer and the upper semiconductor layer. The first transparent electrode layer is electrically connected to the upper semiconductor layer, and the interconnection is electrically connected at one end thereof to the first transparent electrode layer and at the other end thereof to the lower semiconductor layer of the second light emitting cell. Here, each of the lower semiconductor layer, active layer and upper semiconductor layer may include a gallium nitride-based semiconductor layer. The lower semiconductor layer and the upper semiconductor layer may be n-type and p-type semiconductor layers, respectively, or vice versa.
- [32] The interconnection may be directly connected to the first transparent electrode layer over an entire overlapping area therebetween. Accordingly, as compared with techniques in the related art, the light emitting diode according to the present invention may increase a connection area between the interconnection and the first transparent electrode layer, or may decrease an area of the interconnection disposed on the first transparent electrode layer.
- [33] The current blocking layer may be disposed at least under the connection area between the first transparent electrode layer and the interconnection. As a result, it is possible to prevent current crowding under the connection area of the interconnection.
- [34] In addition, the first light emitting cell and the second light emitting cell may have the same structure.
- [35] An exemplary embodiment of the present invention provides a light emitting diode, the light emitting diode including a first light emitting cell and a second light emitting cell disposed on a substrate and spaced apart from each other, a first transparent electrode layer disposed on the first light emitting cell and electrically connected to the first light emitting cell, a current blocking layer disposed between a portion of the first light emitting cell and the first transparent electrode layer, an interconnection electrically connecting the first light emitting cell to the second light emitting cell, and an insulation layer spaced apart from the interconnection from a side surface of the first light emitting cell. The current blocking layer and the insulation layer include distributed Bragg reflectors having the same structure and formed of the same material. Thus, the current blocking layer and the insulation layer may be simultaneously formed by the same process.
- [36] In addition, the interconnection may be directly connected to the first transparent electrode layer over an entire overlapping area therebetween.
- [37] The distributed Bragg reflectors may be disposed under the interconnection over the entire area of the interconnection.
- [38] The light emitting diode may further include an insulation protective layer disposed

outside an area in which the interconnection is formed.

[39] In some embodiments, the light emitting diode may further include a first transparent conductive layer disposed between the insulation layer and the interconnection. In addition, the first transparent conductive layer may be connected to the first transparent electrode layer. Further, the first transparent conductive layer may electrically connect the first transparent electrode layer to the second light emitting cell.

[40] An exemplary embodiment of the present invention provides a method of fabricating a light emitting diode, the method including: forming a first light emitting cell and a second light emitting cell separated from each other on a substrate; forming a current blocking layer covering a partial area of an upper portion of the first light emitting cell together with an insulation layer covering a partial area of a side surface of the first light emitting cell; forming a first transparent electrode layer electrically connected to the first light emitting cell such that a portion of the first transparent electrode layer is formed on the current blocking layer; and forming an interconnection electrically connecting the first light emitting cell to the second light emitting cell. Here, one end of the interconnection is electrically connected to the first transparent electrode layer.

[41] According to this embodiment, the current blocking layer and the insulation layer may be formed by the same process. Thus, it is possible to prevent increase in the number of exposure processes by forming the current blocking layer.

[42] The one end of the interconnection may be connected to the first transparent electrode layer in an upper area of the current blocking layer. Accordingly, it is possible to achieve current spreading by the current blocking layer.

[43] The method of fabricating a light emitting diode may further include forming an insulation protective layer before forming the interconnection. The insulation protective layer is formed with an opening through which an area allocated for formation of the interconnection is exposed.

[44] In addition, formation of the insulation protective layer may include forming an insulation material layer covering the first light emitting cell and the second light emitting cell, forming a mask pattern having an opening on the area allocated for formation of the insulation material layer, and etching the insulation material layer using the mask pattern as an etching mask.

[45] The method of fabricating a light emitting diode may further include forming a first transparent conductive layer disposed on the insulation layer. The first transparent conductive layer may be formed together with the first transparent electrode layer. The first transparent conductive layer prevents damage of the insulation layer during formation of the insulation protective layer. The first transparent conductive layer may be connected to the first transparent electrode layer, and the first transparent conductive layer may electrically connect the first transparent electrode layer to the

second light emitting cell.

- [46] Further, the interconnection may be formed by a lift-off process using the mask pattern after the insulation protective layer is formed. Thus, the insulation protective layer and the interconnection may be formed using the same mask pattern, thereby reducing the number of exposure processes.
- [47] Each of the first and second light emitting cells may include a lower semiconductor layer, an upper semiconductor layer, and an active layer disposed between the lower semiconductor layer and the upper semiconductor layer. Here, the other end of the interconnection is electrically connected to the lower semiconductor layer of the second light emitting cell.
- [48] In addition, the insulation layer may extend to partially cover a side surface of the lower semiconductor layer of the second light emitting cell. Further, the interconnection may be disposed within an upper area of the current blocking layer and the insulation layer except for a portion of the interconnection electrically connected to the lower semiconductor layer of the second light emitting cell. Accordingly, it is possible to minimize absorption of light by the interconnection.
- [49] The current blocking layer may be connected to the insulation layer, and the current blocking layer and the insulation layer may include distributed Bragg reflectors, respectively.
- [50] An exemplary embodiment of the present invention provides a light emitting diode including a first light emitting cell and a second light emitting cell disposed on a substrate and spaced apart from each other, a first transparent electrode layer disposed on the first light emitting cell and electrically connected to the first light emitting cell, a current blocking layer disposed between a portion of the first light emitting cell and the first transparent electrode layer, an interconnection electrically connecting the first light emitting cell to the second light emitting cell, and an insulation layer separating the interconnection from a side surface of the first light emitting cell. In addition, the second light emitting cell has an inclined side surface, the interconnection includes a first connection section connected to the first light emitting cell and a second connection section connected to the second light emitting cell, in which the first connection section contacts the first transparent electrode layer within an upper area of the current blocking layer and the second connection section contacts the inclined side surface of the second light emitting cell.
- [51] Since the second connection section contacts the inclined side surface of the second light emitting cell, there is no need for partial removal of the active layer in order to expose an area for contacting the second connection section, thereby increasing an effective light emitting area of the second light emitting cell.
- [52] The second connection section may contact the inclined side surface of the second

light emitting cell along a periphery of the second light emitting cell. Thus, the light emitting diode according to the present invention can increase a contact area of the second connection section without decreasing the effective light emitting area, whereby the contact resistance of the second connection section can be lowered, thereby enabling reduction in forward voltage of the light emitting diode.

- [53] Each of the first and second light emitting cells includes a lower semiconductor layer, an upper semiconductor layer and an active layer disposed between the lower semiconductor layer and the upper semiconductor layer. The overall upper surface of the lower semiconductor layer may be covered by the active layer, and the second connection section is connected to a side surface of the lower semiconductor layer.
- [54] The current blocking layer may be connected to the insulation layer. Thus, the insulation layer separating the interconnection from the side surface of the light emitting cell may be formed together with the current blocking layer by the same process.
- [55] In addition, the current blocking layer and the insulation layer may include distributed Bragg reflectors. Thus, the light emitting diode may significantly reduce an amount of light absorbed by the interconnection. Further, the insulation layer is formed as a distributed Bragg reflector formed of multiple layers, thereby efficiently preventing formation of defects such as pinholes.
- [56] Further, the current blocking layer and the insulation layer may be disposed between the first light emitting cell and the interconnection over an entire overlapping area between the first light emitting cell and the interconnection.
- [57] The light emitting diode may further include an insulation protective layer covering the first light emitting cell and the second light emitting cell. The insulation protective layer is disposed outside an area in which the interconnection is formed. In addition, a side surface of the insulation protective layer may face a side surface of the interconnection on a coplanar surface. The side surface of the insulation protective layer may contact the side surface of the interconnection. However, the present invention is not limited thereto, and the side surface of the insulation protective layer may be separated from the side surface of the interconnection.
- [58] In some embodiments, the light emitting diode may further include a first transparent conductive layer disposed between the insulation layer and the interconnection. In addition, the first transparent conductive layer may be connected to the first transparent electrode layer. Further, the first transparent conductive layer may be formed of the same material as that of the first transparent electrode layer.
- [59] The interconnection may be directly connected to the first transparent electrode layer over an entire overlapping area therebetween without an insulation material interposed therebetween. Accordingly, as compared with techniques in the related art, the light emitting diode according to the present invention may increase a connection area

between the interconnection and the first transparent electrode layer, or may decrease an area of the interconnection disposed on the first transparent electrode layer.

[60] The current blocking layer may be disposed at least under the connection area between the first transparent electrode layer and the interconnection. As a result, it is possible to prevent current crowding under the connection area of the interconnection.

[61] In addition, the first light emitting cell and the second light emitting cell may have the same structure.

[62] An exemplary embodiment of the present invention provides a method of fabricating a light emitting diode, the method including: forming a first light emitting cell and a second light emitting cell separated from each other on a substrate and each including an inclined side surface; forming a current blocking layer covering a partial area of an upper portion of the first light emitting cell; forming a first transparent electrode layer electrically connected to the first light emitting cell such that a portion of the first transparent electrode layer is formed on the current blocking layer; and forming an interconnection electrically connecting the first light emitting cell to the second light emitting cell. In addition, the interconnection includes a first connection section for electrical connection to the first light emitting cell and a second connection section for electrical connection to the second light emitting cell, in which the first connection section contacts the first transparent electrode layer within an upper area of the current blocking layer and the second connection section contacts the inclined side surface of the second light emitting cell.

[63] Since the second connection section contacts the inclined side surface of the second light emitting cell, the method according to the present invention may increase an effective light emitting area as compared with a conventional method.

[64] The method of fabricating a light emitting diode may further include forming an insulation layer partially covering a side surface of the first light emitting cell. In addition, the insulation layer may be formed together with the current blocking layer. Thus, the current blocking layer and the insulation layer may be formed by the same process.

[65] Further, the current blocking layer may be connected to the insulation layer, and each of the current blocking layer and the insulation layer may include a distributed Bragg reflector.

[66] The method of fabricating a light emitting diode may further include forming an insulation protective layer before forming the interconnection. The insulation protective layer is formed with an opening through which an area allocated for formation of the interconnection is exposed.

[67] In addition, formation of the insulation protective layer may include forming an insulation material layer covering the first light emitting cell and the second light

emitting cell, forming a mask pattern having an opening on the area allocated for formation of the insulation material layer, and etching the insulation material layer using the mask pattern as an etching mask.

- [68] The method of fabricating a light emitting diode may further include forming a first transparent conductive layer disposed on the insulation layer. The first transparent conductive layer may be formed together with the first transparent electrode layer. The first transparent conductive layer prevents damage of the insulation layer during formation of the insulation protective layer. The first transparent conductive layer may be connected to the first transparent electrode layer.
- [69] Further, the interconnection may be formed by a lift-off process using the mask pattern after the insulation protective layer is formed. Thus, the insulation protective layer and the interconnection are formed using the same mask pattern, thereby reducing the number of exposure processes.
- [70] Each of the first and second light emitting cells may include a lower semiconductor layer, an upper semiconductor layer, and an active layer disposed between the lower semiconductor layer and the upper semiconductor layer. Here, the second connection section of the interconnection is electrically connected to the lower semiconductor layer of the second light emitting cell.
- [71] Exemplary embodiments of the invention provide a light emitting diode which allows a current blocking layer and a side insulation layer to be formed by the same process. Since the current blocking layer and the side insulation layer are formed by the same process, it is possible to prevent addition of an exposure process even in the case of adopting the current blocking layer. In addition, the current blocking layer and the insulation layer are formed as the distributed Bragg reflectors, thereby minimizing absorption of light by the interconnection.
- [72] Further, one of the connection sections of the interconnection is electrically connected to an inclined side surface of the light emitting cell, whereby an effective light emitting area of the light emitting cell can be increased. In addition, since the current blocking layer and the side insulation layer are formed by the same process, it is possible to prevent addition of an exposure process even in the case of adopting the current blocking layer. Further, the current blocking layer and the insulation layer are formed as the distributed Bragg reflectors, thereby minimizing absorption of light by the interconnection.
- [73] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

Brief Description of Drawings

- [74] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention, and together with the description serve to explain the principles of the invention.
- [75] Figure 1 is a schematic plan view of a light emitting diode in the related art.
- [76] Figure 2 and Figure 3 are schematic sectional views taken along line A-A of Figure 1.
- [77] Figure 4 is a schematic sectional view of a light emitting diode according to an exemplary embodiment of the present invention.
- [78] Figure 5 to Figure 11 are schematic sectional views illustrating a method of fabricating a light emitting diode according to the exemplary embodiment of Figure 4.
- [79] Figure 12 is a schematic sectional view of a light emitting diode according to an exemplary embodiment of the present invention.
- [80] Figure 13 to Figure 16 are schematic sectional views illustrating a method of fabricating a light emitting diode according to the exemplary embodiment of Figure 12.
- [81] Figure 17 is a schematic plan view of a light emitting diode according to an exemplary embodiment of the present invention.
- [82] Figure 18 is a schematic sectional view taken along line B-B of Figure 17.
- [83] Figure 19 to Figure 25 are schematic sectional views illustrating a method of fabricating a light emitting diode according to the exemplary embodiment of Figure 18.
- [84] Figure 26 is a schematic plan view of a light emitting diode according to an exemplary embodiment of the present invention.
- [85] Figure 27 to Figure 30 are schematic sectional views illustrating a method of fabricating a light emitting diode according to the exemplary embodiment of Figure 26.

Best Mode for Carrying out the Invention

- [86] The invention is described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure is thorough, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the size and relative sizes of layers and regions may be exaggerated for clarity. Like reference numerals in the drawings denote like elements.
- [87] It will be understood that when an element or layer is referred to as being "on" or "connected to" another element or layer, it can be directly on or directly connected to the other element or layer, or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on" or "directly connected

to" another element or layer, there are no intervening elements or layers present. It will be understood that for the purposes of this disclosure, "at least one of X, Y, and Z" can be construed as X only, Y only, Z only, or any combination of two or more items X, Y, and Z (e.g., XYZ, XYY, YZ, ZZ).

[88] Spatially relative terms, such as "beneath", "below", "lower", "above", "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary term "below" can encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

[89] Figure 4 is a schematic sectional view of a light emitting diode according to an exemplary embodiment of the present invention.

[90] Referring to Figure 4, a light emitting diode according to one embodiment of the invention includes a substrate 51, light emitting cells S1, S2, a transparent electrode layer 61, a current blocking layer 60a, an insulation layer 60b, an insulation protective layer 63, and an interconnection 65. The light emitting diode may further include a buffer layer 53.

[91] The substrate 51 may be an insulating or conductive substrate. For example, the substrate 51 may be a sapphire substrate, a gallium nitride substrate, a silicon carbide (SiC) substrate, or a silicon substrate. On a single substrate 51, the first light emitting cell S1 and the second light emitting cell S2 are separated from each other. Each of the first and second light emitting cells S1, S2 has a stack structure 56, which includes a lower semiconductor layer 55, an upper semiconductor layer 59 disposed on one area of the lower semiconductor layer, and an active layer 57 interposed between the lower semiconductor layer and the upper semiconductor layer. Here, the upper and lower semiconductor layers may be p-type and n-type semiconductor layers, respectively, or vice versa.

[92] Each of the lower semiconductor layer 55, the active layer 57 and the upper semiconductor layer 59 may be formed of a gallium nitride-based material, for example, (Al, In, Ga)N. The active layer 57 may be formed of a material having a composition capable of emitting light in a desired wavelength range, for example, UV or blue light, and the lower and upper semiconductor layers 55, 59 are formed of a material having a wider band gap than that of the active layer 57.

- [93] As shown, the lower semiconductor layer 55 and/or the upper semiconductor layer 59 may be formed of a single layer or multiple layers. In addition, the active layer 57 may have a single quantum-well structure or a multi-quantum well structure.
- [94] Each of the first and second light emitting cells S1, S2 may have an inclined side surface, an inclined angle of which ranges from 15 to 80 with respect to an upper surface of the substrate 51. Although not shown, the lower semiconductor layer 55 may have a stepped portion formed along a sidewall thereof.
- [95] The active layer 57 and the upper semiconductor layer 59 are disposed on some area of the lower semiconductor layer 55, and the other area of the lower semiconductor layer 55 is exposed as shown in Figure 4. Although the side surfaces of the active layer 57 and upper semiconductor layer 59 are shown as being vertical side surfaces in Figure 4, it should be understood that these side surfaces may also be inclined.
- [96] In Figure 4, the first light emitting cell S1 and the second light emitting cell S2 are partially shown. However, it should be noted that the first light emitting cell S1 and the second light emitting cell S2 have a similar or the same structure. Specifically, the first and second light emitting cells S1, S2 have the same stack structure, and some area of the lower semiconductor layer 55 of the first light emitting cell S1 is exposed as in some area of the lower semiconductor layer 55 of the second light emitting cell S2.
- [97] The buffer layer 53 may be interposed between the light emitting cells S1, S2 and the substrate 51. The buffer layer 53 is used to relieve lattice mismatch between the substrate 51 and the lower semiconductor layer 55 when the substrate 51 is a growth substrate.
- [98] The transparent electrode layer 61 is disposed on each of the light emitting cells S1, S2. Specifically, a first transparent electrode layer 61 is disposed on the first light emitting cell S1, and a second transparent electrode layer 61 is disposed on the second light emitting cell S2. The transparent electrode layer 61 may be disposed on an upper surface of the upper semiconductor layer 59 to be connected to the upper semiconductor layer 59, and may have a smaller area than that of the upper semiconductor layer 59. In other words, the transparent electrode layer 61 may be recessed from an edge of the upper semiconductor layer 59. Thus, the light emitting diode according to this embodiment may prevent current crowding at the edge of the transparent electrode layer 61 through the sidewalls of the light emitting cells S1, S2.
- [99] The current blocking layer 60a may be disposed on each of the light emitting cells S1, S2 between the transparent electrode layer 61 and each of the light emitting cells S1, S2. Particularly, the current blocking layer 60a is disposed near one edge of the first light emitting cell S1, and a portion of the transparent electrode layer 61 is disposed on the current blocking layer 60a. The current blocking layer 60a is formed of an insulation material, and particularly, may include a distributed Bragg reflector

formed by alternately stacking layers having different indices of refraction.

- [100] The insulation layer 60b covers a portion of the side surface of the first light emitting cell S1. As shown in Figure 4, the insulation layer 60b extends to cover a portion of a side surface of the lower semiconductor layer 55 of the second light emitting cell S2. The insulation layer 60b has the same structure as that of the current blocking layer 60a and is formed of the same material as that of the current blocking layer 60a, and may include a distributed Bragg reflector. When the insulation layer 60b includes the distributed Bragg reflector formed of multiple layers, it is possible to efficiently suppress formation of defects such as pinholes in the insulation layer 60b. Alternatively, the insulation layer 60b may be separated from the current blocking layer 60a.
- [101] The interconnection 65 electrically connects the first light emitting cell S1 to the second light emitting cell S2. The interconnection 65 is electrically connected at one end thereof to the transparent electrode layer 61 on the first light emitting cell S1 and at the other end thereof to the lower semiconductor layer 55 of the second light emitting cell S2, whereby the first light emitting cell S1 can be directly connected in series to the second light emitting cell S2.
- [102] The interconnection 65 may contact the transparent electrode layer 61 over an entire overlapping area between the interconnection 65 and the transparent electrode layer 61. In the related art, a portion of the insulation layer 33 is disposed between the transparent electrode layer 31 and the interconnection 35. However, in this embodiment, the interconnection 65 directly contacts the transparent electrode layer 61 without any insulating material interposed therebetween.
- [103] Further, the current blocking layer 60a may be disposed over an entire overlapping area between the interconnection 65 and the transparent electrode layer 61, and the current blocking layer 60a and the insulation layer 60b may be disposed over an entire overlapping area between the interconnection 65 and the first light emitting cell S1. In addition, the insulation layer 60b may be disposed between the second light emitting cell S2 and the interconnection 65 except for a connection area between the interconnection 65 and the second light emitting cell S2.
- [104] When the current blocking layer 60a and the insulation layer 60b have reflective characteristics like distributed Bragg reflectors, the current blocking layer 60a and the insulation layer 60b may be substantially within the same area as that of the interconnection 65 in an area two times or less than that of the interconnection 65. The current blocking layer 60a and the insulation layer 60b prevent absorption of light by the interconnection 65 when light is emitted from the active layer 57. However, when the current blocking layer 60a and the insulation layer 60b occupy an excessively large area, there is a possibility of blocking discharge of light. Thus, it may be necessary to

limit the area of the current blocking layer 60a and the insulation layer 60b.

- [105] The insulation protective layer 63 may be disposed outside the area of the interconnection 65. The insulation protective layer 63 covers the first and second light emitting cells S1, S2 outside the area of the interconnection 65. The insulation protective layer 63 may be formed of a silicon oxide layer (SiO_2) or a silicon nitride layer. The insulation protective layer 63 is formed with an opening through which the transparent electrode layer 61 on the first light emitting cell S1 and the lower semiconductor layer of the second light emitting cell S2 are exposed, and the interconnection 65 may be disposed within this opening.
- [106] A side surface of the insulation protective layer 63 and a side surface of the interconnection 65 may be disposed to face each other, or to contact each other. Alternatively, the side surface of the insulation protective layer 63 may be separated from the side surface of the interconnection 65 to face each other.
- [107] According to this embodiment, the current blocking layer 60a and the insulation layer 60b may be formed of the same material and have the same structure, and thus may be formed by the same process. In addition, since the interconnection 65 is disposed within the opening of the insulation protective layer 63, the insulation protective layer 63 and the interconnection 65 may be formed using the same mask pattern.
- [108] In this embodiment, the light emitting diode is illustrated as including two light emitting cells, that is, the first light emitting cell S1 and the second light emitting cell S2. However, the present invention is not limited to the two light emitting cells, and more light emitting cells may be electrically connected to each other by interconnections 65. For example, the interconnections 65 may electrically connect the lower semiconductor layers 55 of adjacent light emitting cells to the transparent electrode layers 61 thereof to form a series array of the light emitting cells. The light emitting diode according to this embodiment may include a plurality of such arrays, which is connected to each other in reverse parallel and connected to an AC source. In addition, the light emitting diode may be provided with a bridge rectifier (not shown) connected to the series array of light emitting cells, such that the light emitting cells can be driven by an AC source. The bridge rectifier may be formed by connecting the light emitting cells having the same structure as that of the light emitting cells S1, S2 using the interconnections 65.
- [109] Figure 5 to Figure 11 are sectional views illustrating a method of fabricating a light emitting diode according to one embodiment of the present invention.
- [110] Referring to Figure 5, a semiconductor stack structure 56 is formed on a substrate 51, and includes a lower semiconductor layer 55, an active layer 57 and an upper semiconductor layer 59. In addition, before formation of the lower semiconductor layer 55,

a buffer layer 53 may be formed on the substrate 51.

- [111] The substrate 51 may be a sapphire (Al_2O_3) substrate, a silicon carbide (SiC) substrate, a zinc oxide (ZnO) substrate, a silicon (Si) substrate, a gallium arsenide (GaAs), a gallium phosphide (GaP) substrate, a lithium alumina (LiAl_2O_3) substrate, a boron nitride (BN) substrate, an aluminum nitride (AlN) substrate, or a gallium nitride (GaN) substrate, without being limited thereto. That is, the substrate 51 may be selected from among various materials dependent upon materials of semiconductor layers to be formed thereon.
- [112] The buffer layer 53 is formed to relieve lattice mismatch between the substrate 51 and the semiconductor layer 55 formed thereon, and may be formed of, for example, gallium nitride (GaN) or aluminium nitride (AlN). When the substrate 51 is a conductive substrate, the buffer layer 53 may be formed as an insulation layer or a semi-insulation layer, for example, AlN or semi-insulation GaN.
- [113] Each of the lower semiconductor layer 55, the active layer 57 and the upper semiconductor layer 59 may be formed of a gallium nitride-based semiconductor material, for example, (Al, In, Ga)N. The lower and upper semiconductor layers 55, 59 and the active layer 57 may be discontinuously or continuously formed by metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy, hydride vapor phase epitaxy (HVPE), and the like.
- [114] Here, the lower and upper semiconductor layers are n-type and p-type semiconductor layers, respectively, or vice versa. The n-type semiconductor layer is formed by doping a gallium nitride-based compound semiconductor layer with, for example, silicon (Si) impurities, and the p-type semiconductor layer is formed by doping the gallium nitride-based compound semiconductor layer with, for example, magnesium (Mg) impurities.
- [115] Referring to Figure 6, a plurality of light emitting cells S1, S2 is formed to be separated from each other by photolithography and etching. Each of the light emitting cells S1, S2 has an inclined side surface, and the lower semiconductor layer 55 of each of the light emitting cells S1, S2 is partially exposed.
- [116] In each of the light emitting cells S1, S2, the lower semiconductor layer 55 is first exposed by mesa-etching, and the light emitting cells are separated from each other by a cell isolation process. Alternatively, the light emitting cells S1, S2 may be first separated from each other by the cell isolation process, and then are subjected to mesa etching to expose the lower semiconductor layers 55 thereof.
- [117] Referring to Figure 7, a current blocking layer 60a covering a partial area of the first light emitting cell S1 is formed together with an insulation layer 60b covering a partial area of a side surface of the first light emitting cell S1. The insulation layer 60b may also extend to cover a portion of a side surface of the lower semiconductor layer 55 of the second light emitting cell S2.

- [118] The current blocking layer 60a and the insulation layer 60b may be formed by depositing an insulation material layer, followed by patterning the insulation material layer through photolithography and etching. Alternatively, the current blocking layer 60a and the insulation layer 60b may be formed of an insulation material through a lift-off process. In particular, the current blocking layer 60a and the insulation layer 60b may be formed as distributed Bragg reflectors by alternately stacking layers having different indices of refraction, for example, a SiO_2 layer and a TiO_2 layer. When the insulation layer 60b is a distributed Bragg reflector formed of multiple layers, it is possible to prevent formation of defects such as pinholes in the insulation layer 60b, whereby the insulation layer 60b may be formed to be relatively thin as compared with conventional techniques.
- [119] As shown in Figure 7, the current blocking layer 60a and the insulation layer 60b may be connected to each other, without being limited thereto.
- [120] Next, a transparent electrode layer 61 is formed on the first and second light emitting cells S1, S2. The transparent electrode layer 61 may be formed of a conductive material such as indium tin oxide (ITO) or zinc oxide, or a metal layer such as Ni/Au. The transparent electrode layer 61 is connected to the upper semiconductor layer 59 and is partially disposed on the current blocking layer 60a. The transparent electrode layer 61 may be formed by a lift-off process, without being limited thereto. Alternatively, the transparent electrode layer 61 may be formed by photolithography and etching.
- [121] Referring to Figure 8, an insulation protective layer 63 is formed to cover the first and second light emitting cells S1, S2. The insulation protective layer 63 covers the transparent electrode layer 61 and the insulation layer 60b. In addition, the insulation protective layer 63 may cover an overall area of the first and second light emitting cells S1, S2. The insulation protective layer 63 may be formed as an insulation material layer such as a silicon oxide layer or a silicon nitride layer by chemical vapor deposition or the like.
- [122] Referring to Figure 9, a mask pattern 70 having an opening is formed on the insulation protective layer 63. The opening of the mask pattern 70 corresponds to an area of the interconnection. Next, some region of the insulation protective layer 63 is etched using the mask pattern 70 as a mask. As a result, an opening is formed in the insulation protective layer 63 to expose some of the transparent electrode layer 61 and the insulation layer 60b, and the lower semiconductor layer 55 of the second light emitting cell S2 therethrough.
- [123] Referring to Figure 10, with the mask pattern 70 remaining on the insulation protective layer 63, a conductive material is deposited to form an interconnection 65 in the opening of the mask pattern 70. At this point, a portion 65a of the conductive

material may be deposited on the mask pattern 70. The conductive material may be deposited by plating, electron-beam evaporation or sputtering.

[124] Referring to Figure 11, the mask pattern 70 is removed together with the portion 65a of the conductive material on the mask pattern 70. Accordingly, the interconnection 65 electrically connecting the first and second light emitting cells S1, S2 to each other is finally formed.

[125] Here, one end of the interconnection 65 is connected to the transparent electrode layer 61 of the first light emitting cell S1, and the other end thereof to the lower semiconductor layer 55 of the second light emitting cell S2. In addition, the one end of the interconnection 65 is connected to the transparent electrode layer 60a within an upper area of the current blocking layer 60a. The interconnection 65 is separated from the side surface of the first light emitting cell S1 and the side surface of the second light emitting cell S2 via the insulation layer 60b. Furthermore, the interconnection 65 is disposed within the upper area of the current blocking layer 60a and the insulation layer 60b except for a portion of the interconnection 65 electrically connected to the lower semiconductor layer 55 of the second light emitting cell S2.

[126] In this embodiment, the current blocking layer 60a and the insulation layer 60b are formed by the same process. Accordingly, the insulation protective layer 63 and the interconnection 65 may be formed using the same mask pattern 70, whereby the light emitting diode can be fabricated using the same number of exposure processes while adding the current blocking layer 60a.

[127] Figure 12 is a schematic sectional view of a light emitting diode according to an exemplary embodiment of the present invention.

[128] Referring to Figure 12, the light emitting diode according to this embodiment is generally similar to the light emitting diode described with reference to Figure 4, and further includes a transparent conductive layer 62.

[129] In the light emitting diode according to this embodiment, a substrate 51, light emitting cells S1, S2, a buffer layer 53, a transparent electrode layer 61, a current blocking layer 60a, an insulation layer 60b, an insulation protective layer 63 and an interconnection 65 are similar to those of the light emitting diode according to the above embodiment described with reference to Figure 4, and detailed descriptions thereof will be omitted.

[130] The transparent conductive layer 62 is disposed between the insulation layer 60b and the interconnection 65. The transparent conductive layer 62 has a narrower line width than the insulation layer 60b, thereby preventing short circuit of the upper semiconductor layer 59 and the lower semiconductor layer 55 due to the transparent conductive layer 62. That is, when the insulation layer 60b is thicker than the transparent conductive layer 62, the insulation layer 60b may prevent a short circuit.

- [131] On the other hand, the transparent conductive layer 62 is connected to the first transparent electrode layer 61, and may connect the first transparent electrode layer 61 to the second light emitting cell S2. For example, one end of the transparent conductive layer 62 may be electrically connected to the lower semiconductor layer 55 of the second light emitting cell. In addition, when two or more light emitting cells are connected to each other, a second transparent conductive layer 62 may extend from a second transparent electrode layer 61 on the second light emitting cell S2.
- [132] In this embodiment, since the transparent conductive layer 62 is disposed between the interconnection 65 and the insulation layer 60b, electric current can flow through the transparent conductive layer 62 even in the case where the interconnection 65 is disconnected, thereby improving electrical stability of the light emitting diode.
- [133] Figure 13 to Figure 16 are schematic sectional views illustrating a method of fabricating a light emitting diode according to the present exemplary embodiment.
- [134] Referring to Figure 13, as in the method described with reference to Figure 5 and Figure 6, a semiconductor stack structure 56 is formed on a substrate 51 and a plurality of light emitting cells S1, S2 is formed to be separated from each other via photolithography and etching. Then, as described with reference to Figure 7, a current blocking layer 60a covering a partial area of the first light emitting cell S1 is formed together with an insulation layer 60b covering a partial area of a side surface of the first light emitting cell S1. The insulation layer 60b may also extend to cover a portion of a side surface of the lower semiconductor layer 55 of the second light emitting cell S2.
- [135] As described with reference to Figure 7, the current blocking layer 60a and the insulation layer 60b may be formed as distributed Bragg reflectors by alternately stacking layers having different indices of refraction, for example, a SiO₂ layer and a TiO₂ layer. When the insulation layer 60b is a distributed Bragg reflector formed of multiple layers, it is possible to prevent formation of defects such as pinholes in the insulation layer 60b, whereby the insulation layer 60b may be formed to be relatively thin as compared with conventional techniques.
- [136] Next, a transparent electrode layer 61 is formed on the first and second light emitting cells S1, S2. As described with reference to Figure 7, the transparent electrode layer 61 may be formed of a conductive material such as indium tin oxide (ITO) or zinc oxide, or a metal layer such as Ni/Au. The transparent electrode layer 61 is connected to the upper semiconductor layer 59 and is partially disposed on the current blocking layer 60a. The transparent electrode layer 61 may be formed by a lift-off process, without being limited thereto. Alternatively, the transparent electrode layer 61 may be formed by photolithography and etching.
- [137] During formation of the transparent electrode layer 61, a transparent conductive layer

62 is also formed. The transparent conductive layer 62 may be formed of the same material as that of the transparent electrode layer 61 through the same process. The transparent conductive layer 62 is formed on the insulation layer 60b, and may be connected to the transparent electrode layer 61. Further, one end of the transparent conductive layer 62 may be electrically connected to the lower semiconductor layer 55 of the second light emitting cell S2.

- [138] Referring to Figure 14, an insulation protective layer 63 is formed to cover the first and second light emitting cells S1, S2. The insulation protective layer 63 covers the transparent electrode layer 61, the transparent conductive layer 62 and the insulation layer 60b. In addition, the insulation protective layer 63 may cover an overall area of the first and second light emitting cells S1, S2. The insulation protective layer 63 may be formed as an insulation material layer such as a silicon oxide layer or a silicon nitride layer by chemical vapor deposition or the like.
- [139] Referring to Figure 15, as described with reference to Figure 9, a mask pattern 70 having an opening is formed on the insulation protective layer 63. The opening of the mask pattern 70 corresponds to an area of the interconnection. Next, some region of the insulation protective layer 63 is etched using the mask pattern 70 as a mask. As a result, an opening is formed in the insulation protective layer 63 to expose some of the transparent electrode layer 61 and the transparent conductive layer 62, and the lower semiconductor layer 55 of the second light emitting cell S2 therethrough. Further, a portion of the insulation layer 60b is exposed through the opening.
- [140] Referring to Figure 16, as described with reference to Figure 10, with the mask pattern 70 remaining on the insulation protective layer 63, a conductive material is deposited to form an interconnection 65 in the opening of the mask pattern 70.
- [141] Next, as described with reference to Figure 11, the mask pattern 70 is removed together with a portion 65a of the conductive material on the mask pattern 70. Accordingly, the interconnection 65 electrically connecting the first and second light emitting cells S1, S2 to each other is finally formed.
- [142] In the embodiment described with reference to Figure 5 to Figure 11, the insulation layer 60b may be damaged during etching of the insulation protective layer 63. For example, when the insulation protective layer 63 is subjected to etching using an etching solution such as fluoric acid, the insulation layer 60b including an oxide layer may be damaged by the etching solution. Thus, the insulation layer 60b may not insulate the interconnection 65 from the first light emitting cell S1, thereby causing short circuit.
- [143] On the contrary, in the present exemplary embodiment, since the transparent conductive layer 62 is disposed on the insulation layer 60b, the insulation layer 60b under the transparent conductive layer 62 can be protected from etching damage. Thus,

it is possible to prevent short circuit due to the interconnection 65.

- [144] In the present exemplary embodiment, the transparent electrode layer 61 and the transparent conductive layer 62 may be formed by the same process. Thus, the light emitting diode can be fabricated using the same number of exposure processes while adding the transparent conductive layer 62.
- [145] Figure 17 is a schematic plan view of a light emitting diode according to an exemplary embodiment of the present invention, and Figure 18 is a schematic sectional view taken along line B-B of Figure 17.
- [146] Referring to Figure 17 and Figure 18, the light emitting diode includes a substrate 51, light emitting cells S1, S2, a transparent electrode layer 61, a current blocking layer 60a, an insulation layer 60b, an insulation protective layer 63, and an interconnection 65. The light emitting diode may further include a buffer layer 53.
- [147] The substrate 51 may be an insulating or conductive substrate. For example, the substrate 51 may be a sapphire substrate, a gallium nitride substrate, a silicon carbide (SiC) substrate, or a silicon substrate. In addition, the substrate 51 may be a substrate having a convex-concave pattern (not shown) on an upper surface thereof, such as a patterned sapphire substrate.
- [148] On a single substrate 51, the first light emitting cell S1 and the second light emitting cell S2 are separated from each other. Each of the first and second light emitting cells S1, S2 has a stack structure 56, which includes a lower semiconductor layer 55, an upper semiconductor layer 59 disposed on one area of the lower semiconductor layer, and an active layer 57 interposed between the lower semiconductor layer and the upper semiconductor layer. Here, the upper and lower semiconductor layers may be p-type and n-type semiconductor layers, respectively, or vice versa.
- [149] Each of the lower semiconductor layer 55, the active layer 57 and the upper semiconductor layer 59 may be formed of a gallium nitride-based material, for example, (Al, In, Ga)N. The active layer 57 may be formed of a material having a composition capable of emitting light in a desired wavelength range, for example, UV or blue light, and the lower and upper semiconductor layers 55, 59 are formed of a material having a wider band gap than that of the active layer 57.
- [150] As shown, the lower semiconductor layer 55 and/or the upper semiconductor layer 59 may be formed of a single layer or multiple layers. In addition, the active layer 57 may have a single quantum-well structure or a multi-quantum well structure.
- [151] Each of the first and second light emitting cells S1, S2 may have an inclined side surface, an inclined angle of which ranges from 15 to 80 with respect to an upper surface of the substrate 51.
- [152] The active layer 57 and the upper semiconductor layer 59 are disposed on the lower semiconductor layer 55. An upper surface of the lower semiconductor layer 55 may be

completely covered by the active layer 57 such that the side surface of the lower semiconductor layer 55 can be exposed.

[153] In Figure 18, the first light emitting cell S1 and the second light emitting cell S2 are partially shown. However, it should be noted that the first light emitting cell S1 and the second light emitting cell S2 have a similar or the same structure as shown in Figure 17. Specifically, the first and second light emitting cells S1, S2 have the same gallium nitride-based semiconductor stack structure, and may have inclined side surfaces of the same structure.

[154] The buffer layer 53 may be interposed between the light emitting cells S1, S2 and the substrate 51. The buffer layer 53 is used to relieve lattice mismatch between the substrate 51 and the lower semiconductor layer 55 formed thereon when the substrate 51 is a growth substrate.

[155] The transparent electrode layer 61 is disposed on each of the light emitting cells S1, S2. Specifically, a first transparent electrode layer 61 is disposed on the first light emitting cell S1, and a second transparent electrode layer 61 is disposed on the second light emitting cell S2. The transparent electrode layer 61 may be disposed on an upper surface of the upper semiconductor layer 59 to be connected to the upper semiconductor layer 59, and may have a smaller area than that of the upper semiconductor layer 59. In other words, the transparent electrode layer 61 may be recessed from an edge of the upper semiconductor layer 59. Thus, the light emitting diode according to this embodiment may prevent current crowding at the edge of the transparent electrode layer 61 through the sidewalls of the light emitting cells S1, S2.

[156] The current blocking layer 60a may be disposed on each of the light emitting cells S1, S2 between the transparent electrode layer 61 and each of the light emitting cells S1, S2. A portion of the transparent electrode layer 61 is disposed on the current blocking layer 60a. The current blocking layer 60a may be disposed near an edge of each of the light emitting cells S1, S2, without being limited thereto. Alternatively, the current blocking layer 60a may be disposed at a central region of each of the light emitting cells S1, S2. The current blocking layer 60a is formed of an insulation material, and particularly, may include a distributed Bragg reflector formed by alternately stacking layers having different indices of refraction.

[157] The insulation layer 60b covers a portion of the side surface of the first light emitting cell S1. As shown in Figure 17 and Figure 18, the insulation layer 60b may extend to an area between the first light emitting cell S1 and the second light emitting cell S2, and may cover a portion of the side surface of the lower semiconductor layer 55 of the second light emitting cell S2. The insulation layer 60b has the same structure as that of the current blocking layer 60a and is formed of the same material as that of the current blocking layer 60a, and may include a distributed Bragg reflector. The insulation layer

60b may be formed of a different process than that of the current blocking layer 60a. When the insulation layer 60b includes the distributed Bragg reflector formed of multiple layers, it is possible to efficiently suppress formation of defects such as pinholes in the insulation layer 60b. The insulation layer 60b may be directly connected to the current blocking layer 60a to be positioned adjacent thereto, but is not limited thereto. The insulation layer 60b may be separated from the current blocking layer 60a.

- [158] The interconnection 65 electrically connects the first light emitting cell S1 to the second light emitting cell S2. The interconnection 65 includes a first connection section 65p and a second connection section 65n. The first connection section 65p is electrically connected to the transparent electrode layer 61 on the first light emitting cell S1, and the second connection section 65n is electrically connected to the lower semiconductor layer 55 of the second light emitting cell S2. The first connection section 65p may be disposed near one edge of the first light emitting cell S1, without being limited thereto. Alternatively, the first connection section 65p may be disposed at the central region of the first light emitting cell S1.
- [159] The second connection section 65n may contact an inclined side surface of the second light emitting cell S2, particularly, an inclined side surface of the lower semiconductor layer 55 of the second light emitting cell S2. In addition, as shown in Figure 17, the second connection section 65n may extend in opposite directions along the periphery of the second light emitting cell S2 while electrically contacting the inclined side surface of the lower semiconductor layer 55. The first light emitting cell S1 is connected in series to the second light emitting cell S2 by the first and second connection sections 65p, 65n of the interconnection 65.
- [160] The interconnection 65 may contact the transparent electrode layer 61 over an entire overlapping area between the interconnection 65 and the transparent electrode layer 61. In the related art, a portion of the insulation layer 33 may be disposed between the transparent electrode layer 31 and the interconnection 35. However, in the present exemplary embodiment, the interconnection 65 directly contacts the transparent electrode layer 61 without any insulating material interposed therebetween.
- [161] Further, the current blocking layer 60a may be disposed over the entire overlapping area between the interconnection 65 and the transparent electrode layer 61, and the current blocking layer 60a and the insulation layer 60b may be disposed over an entire overlapping area between the interconnection 65 and the first light emitting cell S1. In addition, the insulation layer 60b may be disposed between the second light emitting cell S2 and the interconnection 65 except for a connection area between the interconnection 65 and the second light emitting cell S2.
- [162] Although the first connection section 65p and the second connection section 65n of

the interconnection 65 are illustrated as being connected to each other via two paths in Figure 17, the first connection section 65p and the second connection section 65n may be connected to each other via a single path.

- [163] When the current blocking layer 60a and the insulation layer 60b have reflective characteristics like distributed Bragg reflectors, the current blocking layer 60a and the insulation layer 60b may be substantially within the same area as that of the interconnection 65 in an area two times or less than that of the interconnection 65. The current blocking layer 60a and the insulation layer 60b prevent absorption of light by the interconnection 65 when light is emitted from the active layer 57. However, when the current blocking layer 60a and the insulation layer 60b occupy an excessively large area, there is a possibility of blocking discharge of light. Thus, it may be necessary to limit the area of the current blocking layer 60a and the insulation layer 60b.
- [164] The insulation protective layer 63 may be disposed outside the area of the interconnection 65. The insulation protective layer 63 covers the first and second light emitting cells S1, S2 outside the area of the interconnection 65. The insulation protective layer 63 may be formed of a silicon oxide layer (SiO_2) or a silicon nitride layer. The insulation protective layer 63 is formed with an opening through which the transparent electrode layer 61 on the first light emitting cell S1 and the lower semiconductor layer of the second light emitting cell S2 are exposed, and the interconnection 65 may be disposed within this opening
- [165] A side surface of the insulation protective layer 63 and a side surface of the interconnection 65 may be disposed to face each other, or to contact each other. Alternatively, the side surface of the insulation protective layer 63 may be separated from the side surface of the interconnection 65 to face each other.
- [166] According to this embodiment, since the second connection section 65n of the interconnection 65 electrically contacts the inclined side surface of the second light emitting cell S2, there is no need for exposure of an upper surface of the lower semiconductor layer 55 of the second light emitting cell S2. Thus, there is no need for partial removal of the second semiconductor layer 59 and the active layer 57, thereby increasing an effective light emitting area of the light emitting diode.
- [167] In addition, the current blocking layer 60a and the insulation layer 60b may be formed of the same material and have the same structure, and thus may be formed by the same process. Further, since the interconnection 65 is disposed within the opening of the insulation protective layer 63, the insulation protective layer 63 and the interconnection 65 may be formed using the same mask pattern.
- [168] In this embodiment, the light emitting diode is illustrated as including two light emitting cells, that is, the first light emitting cell S1 and the second light emitting cell S2. However, the present invention is not limited to the two light emitting cells, and

more light emitting cells may be electrically connected to each other by interconnections 65. For example, the interconnections 65 may electrically connect the lower semiconductor layers 55 of adjacent light emitting cells to the transparent electrode layers 61 thereof to form a series array of the light emitting cells. The light emitting diode according to this embodiment may include a plurality of such arrays, which is connected to each other in reverse parallel and connected to an AC source. In addition, the light emitting diode may be provided with a bridge rectifier (not shown) connected to the series array of light emitting cells, such that the light emitting cells can be driven by an AC source. The bridge rectifier may be formed by connecting the light emitting cells having the same structure as that of the light emitting cells S1, S2 using the interconnections 65.

- [169] Figure 19 to Figure 25 are sectional views illustrating a method of fabricating a light emitting diode according to one embodiment of the invention.
- [170] Referring to Figure 19, a semiconductor stack structure 56 is formed on a substrate 51, and includes a lower semiconductor layer 55, an active layer 57 and an upper semiconductor layer 59. In addition, before formation of the lower semiconductor layer 55, a buffer layer 53 may be formed on the substrate 51.
- [171] The substrate 51 may be a sapphire (Al_2O_3) substrate, a silicon carbide (SiC) substrate, a zinc oxide (ZnO) substrate, a silicon (Si) substrate, a gallium arsenide (GaAs), a gallium phosphide (GaP) substrate, a lithium alumina (LiAl_2O_3) substrate, a boron nitride (BN) substrate, an aluminum nitride (AlN) substrate, or a gallium nitride (GaN) substrate, without being limited thereto. That is, the substrate 51 may be selected from among various materials dependent upon materials of semiconductor layers to be formed thereon. In addition, the substrate 51 may be a substrate having a convex-concave pattern (not shown) on an upper surface thereof, such as a patterned sapphire substrate.
- [172] The buffer layer 53 is formed to relieve lattice mismatch between the substrate 51 and the semiconductor layer 55 formed thereon, and may be formed of, for example, gallium nitride (GaN) or aluminium nitride (AlN). When the substrate 51 is a conductive substrate, the buffer layer 53 may be formed as an insulation layer or a semi-insulation layer, for example, AlN or semi-insulation GaN .
- [173] Each of the lower semiconductor layer 55, the active layer 57 and the upper semiconductor layer 59 may be formed of a gallium nitride-based semiconductor material, for example, $(\text{Al}, \text{In}, \text{Ga})\text{N}$. The lower and upper semiconductor layers 55, 59 and the active layer 57 may be discontinuously or continuously formed by metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy, hydride vapor phase epitaxy (HVPE), and the like.
- [174] Here, the lower and upper semiconductor layers are n-type and p-type semiconductor

layers, respectively, or vice versa. The n-type semiconductor layer is formed by doping a gallium nitride-based compound semiconductor layer with, for example, silicon (Si) impurities, and the p-type semiconductor layer is formed by doping the gallium nitride-based compound semiconductor layer with, for example, magnesium (Mg) impurities.

- [175] Referring to Figure 20, a plurality of light emitting cells S1, S2 is formed to be separated from each other by photolithography and etching. Each of the light emitting cells S1, S2 has an inclined side surface. In a conventional method of fabricating a light emitting diode, photolithography and etching processes are added to expose a portion of an upper surface of the lower semiconductor layer 55 of each of the light emitting cells S1, S2. In this embodiment, however, the photolithography and etching processes for partially exposing the upper surface of the lower semiconductor layer 55 are omitted.
- [176] Referring to Figure 21, a current blocking layer 60a covering a partial area of the first light emitting cell S1 is formed together with an insulation layer 60b covering a partial area of a side surface of the first light emitting cell S1. The insulation layer 60b may also extend to cover an area between the first light emitting cell S1 and the second light emitting cell S2, and may cover a portion of the side surface of the lower semiconductor layer 55 of the second light emitting cell S2.
- [177] The current blocking layer 60a and the insulation layer 60b may be formed by depositing an insulation material layer, followed by patterning the insulation material layer through photolithography and etching. Alternatively, the current blocking layer 60a and the insulation layer 60b may be formed as insulation material layers through a lift-off process. In particular, the current blocking layer 60a and the insulation layer 60b may be formed as distributed Bragg reflectors by alternately stacking layers having different indices of refraction, for example, a SiO₂ layer and a TiO₂ layer. When the insulation layer 60b is a distributed Bragg reflector formed of multiple layers, it is possible to prevent formation of defects such as pinholes in the insulation layer 60b, whereby the insulation layer 60b may be formed to be relatively thin as compared with conventional techniques.
- [178] As shown in Figure 21, the current blocking layer 60a and the insulation layer 60b may be connected to each other, without being limited thereto.
- [179] Next, a transparent electrode layer 61 is formed on the first and second light emitting cells S1, S2. The transparent electrode layer 61 may be formed of a conductive material such as indium tin oxide (ITO) or zinc oxide, or a metal layer such as Ni/Au. The transparent electrode layer 61 is connected to the upper semiconductor layer 59 and is partially disposed on the current blocking layer 60a. The transparent electrode layer 61 may be formed by a lift-off process, without being limited thereto. Alternatively, the transparent electrode layer 61 may be formed by photolithography and

etching.

- [180] Referring to Figure 22, an insulation protective layer 63 is formed to cover the first and second light emitting cells S1, S2. The insulation protective layer 63 covers the transparent electrode layer 61 and the insulation layer 60b. In addition, the insulation protective layer 63 may cover an overall area of the first and second light emitting cells S1, S2. The insulation protective layer 63 may be formed as an insulation material layer such as a silicon oxide layer or a silicon nitride layer by chemical vapor deposition or the like.
- [181] Referring to Figure 23, a mask pattern 70 having an opening is formed on the insulation protective layer 63. The opening of the mask pattern 70 corresponds to an area of the interconnection. Next, some region of the insulation protective layer 63 is etched using the mask pattern 70 as a mask. As a result, an opening is formed in the insulation protective layer 63 to expose some of the transparent electrode layer 61 and the insulation layer 60b, and an inclined side surface of the lower semiconductor layer 55 of the second light emitting cell S2 therethrough.
- [182] Referring to Figure 24, with the mask pattern 70 remaining on the insulation protective layer 63, a conductive material is deposited to form an interconnection 65 in the opening of the mask pattern 70. At this point, a portion 65a of the conductive material may be deposited on the mask pattern 70. The conductive material may be deposited by plating, electron-beam evaporation or sputtering.
- [183] Referring to Figure 25, the mask pattern 70 is removed together with the portion 65a of the conductive material on the mask pattern 70. Accordingly, the interconnection 65 electrically connecting the first and second light emitting cells S1, S2 to each other is finally formed.
- [184] Here, a first connection section 65p of the interconnection 65 is connected to the transparent electrode layer 61 of the first light emitting cell S1, and a second connection section 65n of the interconnection 65 is connected to the inclined side surface of the lower semiconductor layer 55 of the second light emitting cell S2. The first connection section 65p of the interconnection 65 is connected to the transparent electrode layer 60a within an upper area of the current blocking layer 60a. The interconnection 65 is separated from the side surface of the first light emitting cell S1 by the insulation layer 60b.
- [185] In this embodiment, the current blocking layer 60a and the insulation layer 60b are formed by the same process. Accordingly, the insulation protective layer 63 and the interconnection 65 may be formed using the same mask pattern 70, whereby the light emitting diode can be fabricated using the same number of exposure processes while adding the current blocking layer 60a.
- [186] Figure 26 is a schematic sectional view of a light emitting diode according to an

exemplary embodiment of the present invention.

- [187] Referring to Figure 26, the light emitting diode according to the present exemplary embodiment is generally similar to the light emitting device described with reference to Figure 17 and Figure 18, and further includes a transparent conductive layer 62.
- [188] In the light emitting diode according to this embodiment, a substrate 51, light emitting cells S1, S2, a buffer layer 53, a transparent electrode layer 61, a current blocking layer 60a, an insulation layer 60b, an insulation protective layer 63 and an interconnection 65 are similar to those of the light emitting diode according to the above embodiment described with reference to Figure 17 and Figure 18, and detailed descriptions thereof will be omitted.
- [189] The transparent conductive layer 62 is disposed between the insulation layer 60b and the interconnection 65. The transparent conductive layer 62 has a narrower line width than the insulation layer 60b, thereby preventing short circuit of the upper semiconductor layer 59 and the lower semiconductor layer 55 due to the transparent conductive layer 62.
- [190] On the other hand, the transparent conductive layer 62 is connected to the first transparent electrode layer 61, and may connect the first transparent electrode layer 61 to the second light emitting cell S2. For example, one end of the transparent conductive layer 62 may be electrically connected to the lower semiconductor layer 55 of the second light emitting cell. In addition, when two or more light emitting cells are connected to each other, a second transparent conductive layer 62 may extend from a second transparent electrode layer 61 on the second light emitting cell S2.
- [191] In this embodiment, since the transparent conductive layer 62 is disposed between the interconnection 65 and the insulation layer 60b, electric current can flow through the transparent conductive layer 62 even in the case where the interconnection 65 is disconnected, thereby improving electric stability of the light emitting diode.
- [192] Figure 27 to Figure 30 are schematic sectional views illustrating a method of fabricating a light emitting diode according to the exemplary embodiment of Figure 26.
- [193] Referring to Figure 27, as in the method described with reference to Figure 19 and Figure 20, a semiconductor stack structure 56 is formed on a substrate 51 and a plurality of light emitting cells S1, S2 is formed to be separated from each other via photolithography and etching. Then, as described with reference to Figure 21, a current blocking layer 60a covering a partial area of the first light emitting cell S1 is formed together with an insulation layer 60b covering a partial area of a side surface of the first light emitting cell S1.
- [194] As described with reference to Figure 21, the current blocking layer 60a and the insulation layer 60b may be formed as distributed Bragg reflectors by alternately stacking layers having different indices of refraction, for example, a SiO₂ layer and a

TiO₂ layer. When the insulation layer 60b is a distributed Bragg reflector formed of multiple layers, it is possible to prevent formation of defects such as pinholes in the insulation layer 60b, whereby the insulation layer 60b may be formed to be relatively thin as compared with conventional techniques.

[195] Next, a transparent electrode layer 61 is formed on the first and second light emitting cells S1, S2. As described with reference to Figure 21, the transparent electrode layer 61 may be formed of a conductive material such as indium tin oxide (ITO) or zinc oxide, or a metal layer such as Ni/Au. The transparent electrode layer 61 is connected to the upper semiconductor layer 59 and is partially disposed on the current blocking layer 60a. The transparent electrode layer 61 may be formed by a lift-off process, without being limited thereto. Alternatively, the transparent electrode layer 61 may be formed by photolithography and etching.

[196] During formation of the transparent electrode layer 61, a transparent conductive layer 62 is also formed. The transparent conductive layer 62 may be formed of the same material as that of the transparent electrode layer 61 through the same process. The transparent conductive layer 62 is formed on the insulation layer 60b, and may be connected to the transparent electrode layer 61. Further, one end of the transparent conductive layer 62 may be electrically connected to an inclined side surface of the lower semiconductor layer 55 of the second light emitting cell S2.

[197] Referring to Figure 28, an insulation protective layer 63 is formed to cover the first and second light emitting cells S1, S2. The insulation protective layer 63 covers the transparent electrode layer 61, the transparent conductive layer 62 and the insulation layer 60b. In addition, the insulation protective layer 63 may cover an overall area of the first and second light emitting cells S1, S2. The insulation protective layer 63 may be formed as an insulation material layer such as a silicon oxide layer or a silicon nitride layer by chemical vapor deposition or the like.

[198] Referring to Figure 29, as described with reference to Figure 23, a mask pattern 70 having an opening is formed on the insulation protective layer 63. The opening of the mask pattern 70 corresponds to an area of the interconnection. Next, some region of the insulation protective layer 63 is etched using the mask pattern 70 as a mask. As a result, an opening is formed in the insulation protective layer 63 to expose some of the transparent electrode layer 61 and the transparent conductive layer 62, and the inclined side surface of the lower semiconductor layer 55 of the second light emitting cell S2 therethrough. A portion of the insulation layer 60b is exposed through the opening. Further, a portion of the insulation layer 60b is exposed through the opening.

[199] Referring to Figure 30, as described with reference to Figure 24, with the mask pattern 70 remaining on the insulation protective layer 63, a conductive material is deposited to form an interconnection 65 in the opening of the mask pattern 70.

- [200] Next, as described with reference to Figure 25, the mask pattern 70 is removed together with a portion 65a of the conductive material on the mask pattern 70. Accordingly, the interconnection 65 electrically connecting the first and second light emitting cells S1, S2 to each other is finally formed.
- [201] In the embodiment described with reference to Figure 19 to Figure 25, the insulation layer 60b may be damaged during etching of the insulation protective layer 63. For example, when the insulation protective layer 63 is subjected to etching using an etching solution such as fluoric acid, the insulation layer 60b including an oxide layer may be damaged by the etching solution. Thus, the insulation layer 60b may not insulate the interconnection 65 from the first light emitting cell S1, thereby causing short circuit.
- [202] In the present exemplary embodiment, since the transparent conductive layer 62 is disposed on the insulation layer 60b, the insulation layer 60b under the transparent conductive layer 62 can be protected from etching damage. Thus, it is possible to prevent short circuit due to the interconnection 65.
- [203] In this embodiment, the transparent electrode layer 61 and the transparent conductive layer 62 may be formed by the same process. Thus, the light emitting diode can be fabricated using the same number of exposure processes while adding the transparent conductive layer 62.
- [204] Although the invention has been illustrated with reference to some embodiments in conjunction with the drawings, it will be apparent to those skilled in the art that various modifications and changes can be made to the invention without departing from the spirit and scope of the invention. Further, it should be understood that some features of a certain embodiment may also be applied to other embodiments without departing from the spirit and scope of the invention. Therefore, it should be understood that the embodiments are provided by way of illustration only and are given to provide complete disclosure of the invention and to provide thorough understanding of the invention to those skilled in the art. Thus, it is intended that the invention cover the modifications and variations provided they fall within the scope of the appended claims and their equivalents.

Claims

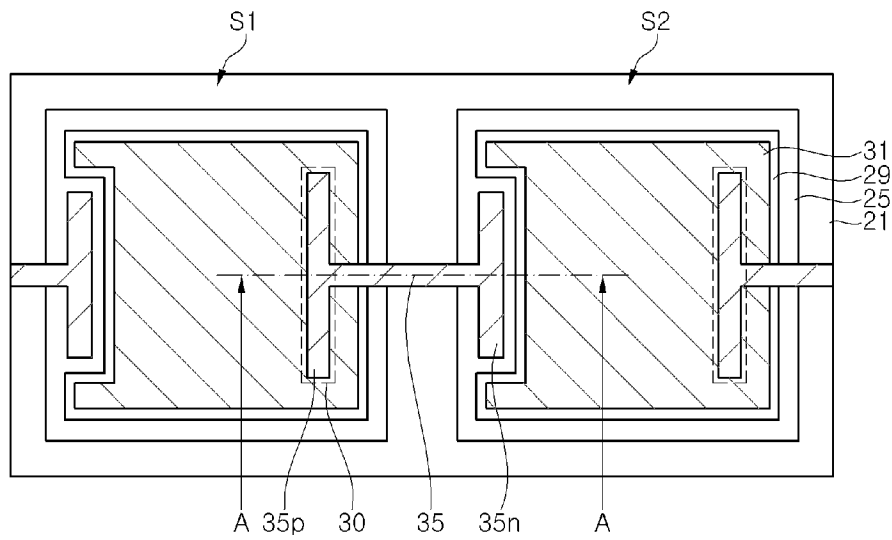
- [Claim 1] A light emitting diode, comprising:
a first light emitting cell and a second light emitting cell disposed on a substrate, the first light emitting cell and the second light emitting being spaced apart from each other;
a first transparent electrode layer disposed on the first light emitting cell, the first transparent electrode layer being electrically connected to the first light emitting cell;
a current blocking layer disposed between a portion of the first light emitting cell and the first transparent electrode layer;
an interconnection electrically connecting the first light emitting cell and the second light emitting cell; and
an insulation layer disposed between the interconnection and a side surface of the first light emitting cell,
wherein the current blocking layer and the insulation layer are connected to each other.
- [Claim 2] The light emitting diode of claim 1, wherein the current blocking layer and the insulation layer comprise distributed Bragg reflectors.
- [Claim 3] The light emitting diode of claim 2, wherein the current blocking layer and the insulation layer are disposed between the first light emitting cell and the interconnection in an entire overlapping area between the first light emitting cell and the interconnection.
- [Claim 4] The light emitting diode of claim 3, wherein the insulation layer is disposed between the interconnection and the side surface of the second light emitting cell.
- [Claim 5] The light emitting diode of claim 4, further comprising:
an insulation protective layer disposed on the first light emitting cell and the second light emitting cell, the insulation protective layer being disposed outside an area in which the interconnection is disposed.
- [Claim 6] The light emitting diode of claim 5, wherein a side surface of the insulation protective layer contacts a side surface of the interconnection on a coplanar surface.
- [Claim 7] The light emitting diode of claim 1, further comprising:
a first transparent conductive layer disposed between the insulation layer and the interconnection.
- [Claim 8] The light emitting diode of claim 7, wherein the first transparent conductive layer is connected to the first transparent electrode layer.

- [Claim 9] The light emitting diode of claim 1, wherein each of the first and second light emitting cells comprises a lower semiconductor layer, an upper semiconductor layer, and an active layer disposed between the lower semiconductor layer and the upper semiconductor layer, wherein the first transparent electrode layer is electrically connected to the upper semiconductor layer, and wherein the interconnection contacts the first transparent electrode layer at a first end thereof and the lower semiconductor layer of the second light emitting cell at a second end thereof.
- [Claim 10] The light emitting diode of claim 9, wherein the interconnection is directly connected to the first transparent electrode layer over an entire overlapping area therebetween.
- [Claim 11] The light emitting diode of claim 10, wherein the current blocking layer is disposed at least under the direct connection area between the first transparent electrode layer and the interconnection.
- [Claim 12] The light emitting diode of claim 9, wherein the first light emitting cell and the second light emitting cell comprise the same structure.
- [Claim 13] A light emitting diode, comprising:
a first light emitting cell and a second light emitting cell disposed on a substrate, the first light emitting cell and the second light emitting being spaced apart from each other;
a first transparent electrode layer disposed on the first light emitting cell, the first transparent electrode being electrically connected to the first light emitting cell;
a current blocking layer disposed between a portion of the first light emitting cell and the first transparent electrode layer;
an interconnection electrically connecting the first light emitting cell and the second light emitting cell; and
an insulation layer disposed between the interconnection and a side surface of the first light emitting cell,
wherein the current blocking layer and the insulation layer comprise distributed Bragg reflectors comprising the same structure, and comprise the same material.
- [Claim 14] The light emitting diode of claim 13, wherein the interconnection is directly connected to the first transparent electrode layer over an entire overlapping area therebetween.
- [Claim 15] The light emitting diode of claim 13, wherein the distributed Bragg reflectors are disposed under the interconnection over an entire area of

the interconnection.

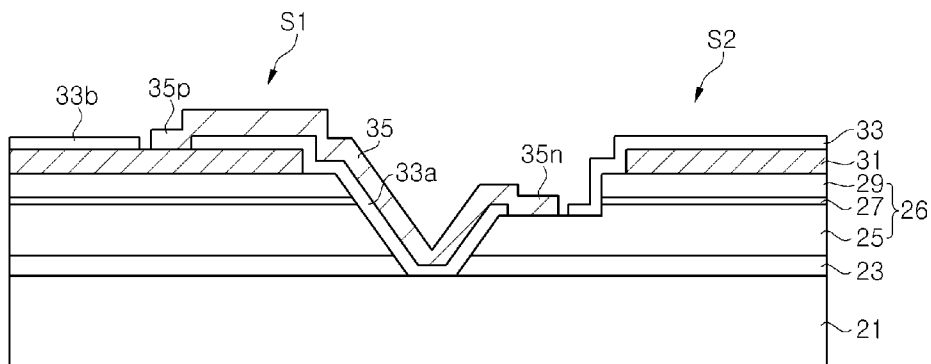
- [Claim 16] The light emitting diode of claim 13, further comprising:
a first transparent conductive layer disposed between the insulation layer and the interconnection.
- [Claim 17] The light emitting diode of claim 16, wherein the first transparent conductive layer is connected to the first transparent electrode layer.
- [Claim 18] The light emitting diode of claim 17, wherein the transparent conductive layer electrically connects the transparent electrode layer to the second light emitting cell.
- [Claim 19] The light emitting diode of claim 13, further comprising:
an insulation protective layer disposed outside an area in which the interconnection is disposed.
- [Claim 20] A light emitting diode, comprising:
a first light emitting cell and a second light emitting cell disposed on a substrate, the first light emitting cell and the second light emitting being spaced apart from each other;
a first transparent electrode layer disposed on the first light emitting cell, the first transparent electrode being electrically connected to the first light emitting cell;
a current blocking layer disposed between a portion of the first light emitting cell and the first transparent electrode layer;
an interconnection electrically connecting the first light emitting cell and the second light emitting cell; and
an insulation layer disposed between the interconnection from a side surface of the first light emitting cell,
wherein the second light emitting cell has an inclined side surface, and the interconnection comprises a first connection section connected to the first light emitting cell and a second connection section connected to the second light emitting cell, the first connection section contacting the first transparent electrode layer within an upper area of the current blocking layer, the second connection section contacting the inclined side surface of the second light emitting cell.

[Fig. 1]



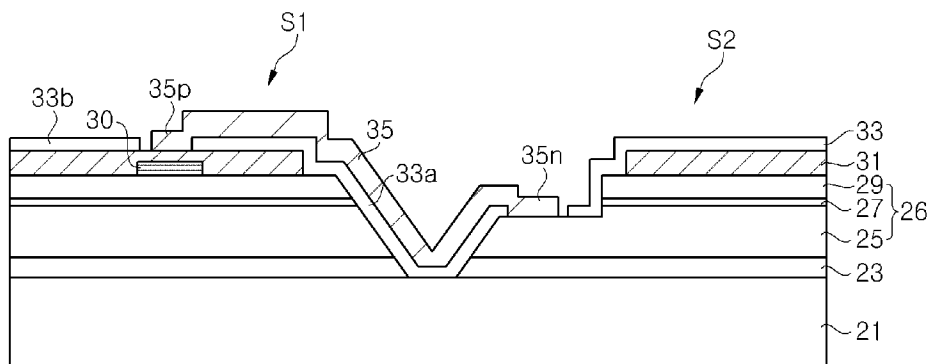
Prior Art

[Fig. 2]



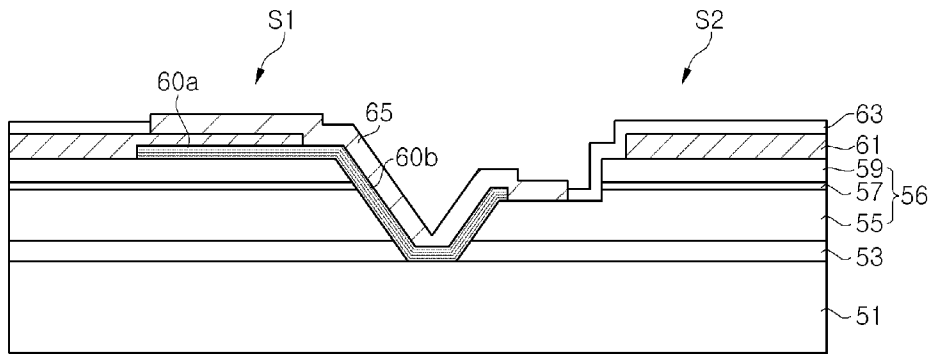
Prior Art

[Fig. 3]

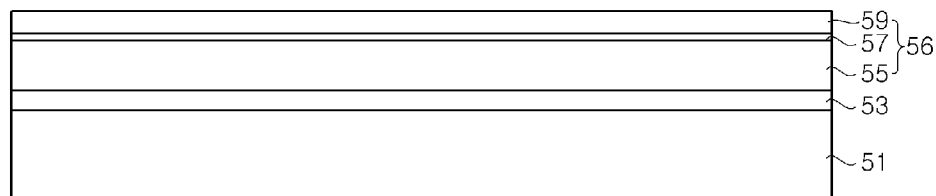


Prior Art

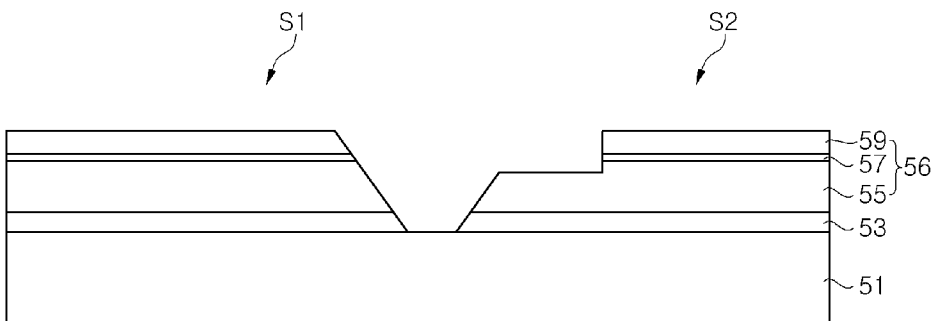
[Fig. 4]



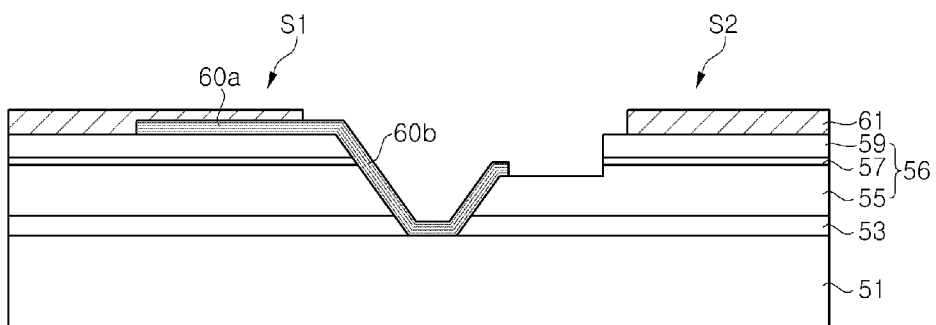
[Fig. 5]



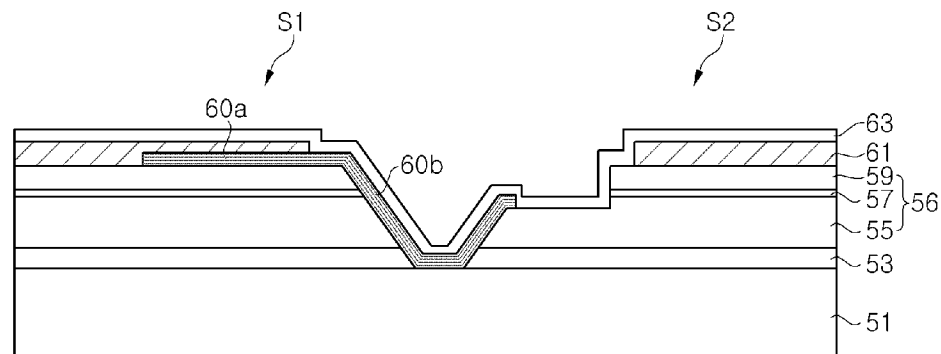
[Fig. 6]



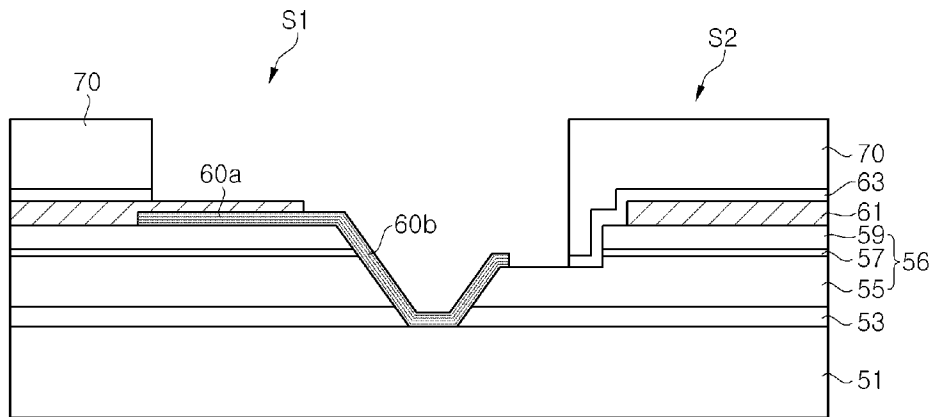
[Fig. 7]



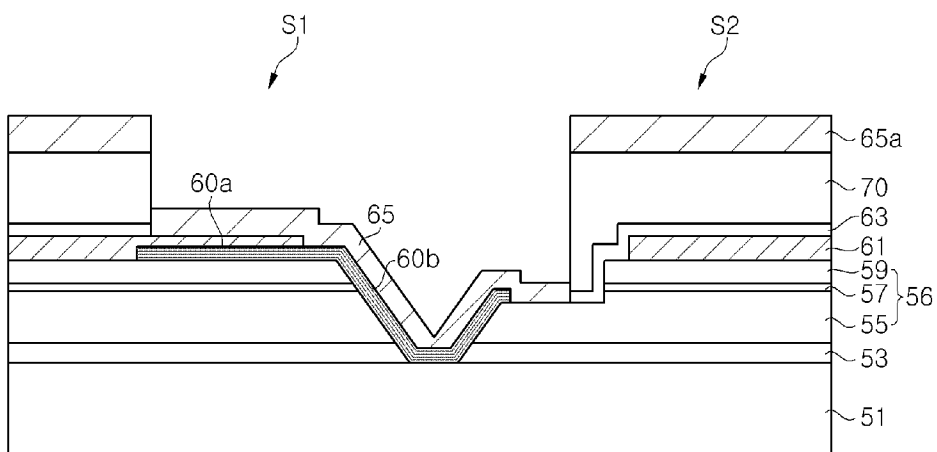
[Fig. 8]



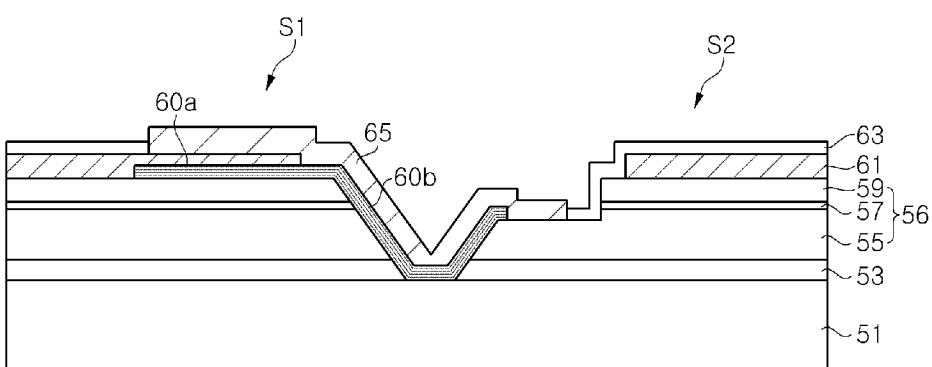
[Fig. 9]



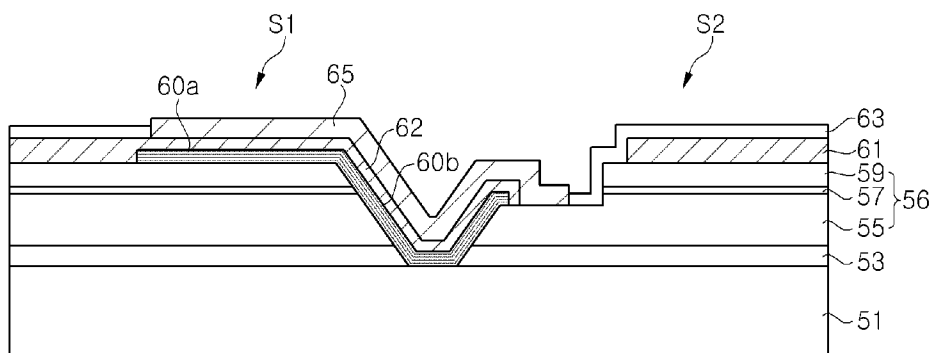
[Fig. 10]



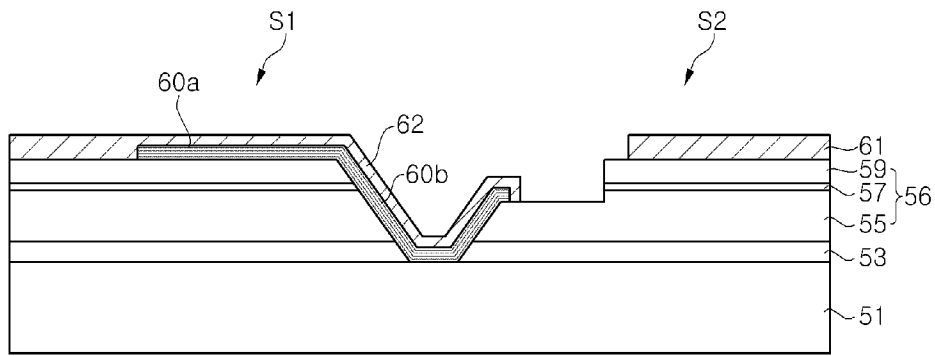
[Fig. 11]



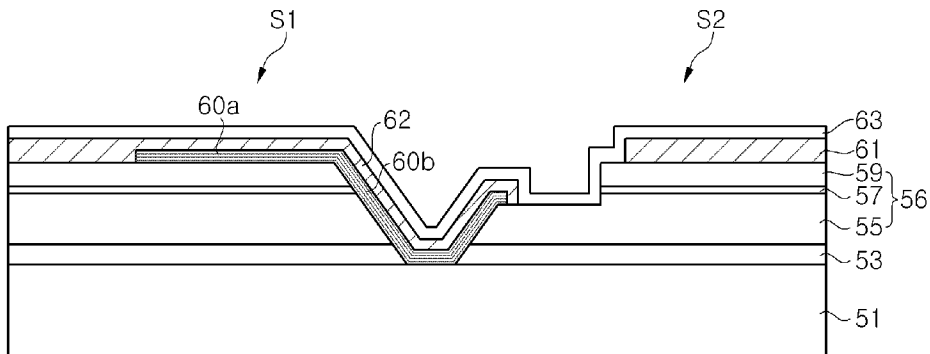
[Fig. 12]



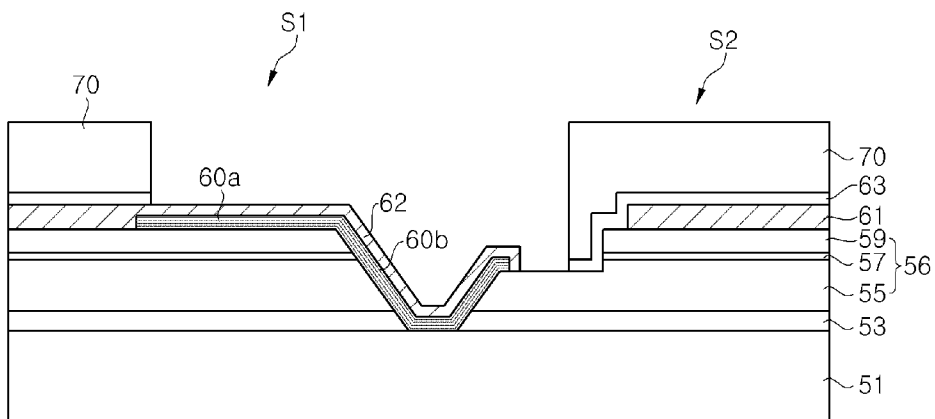
[Fig. 13]



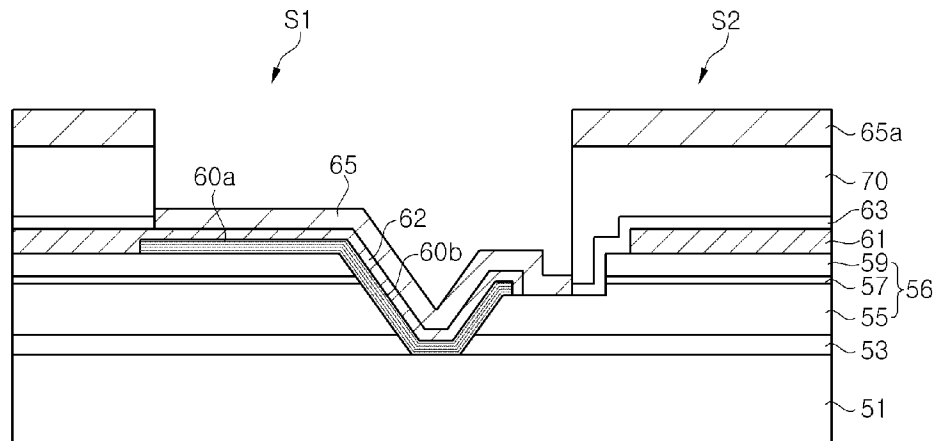
[Fig. 14]



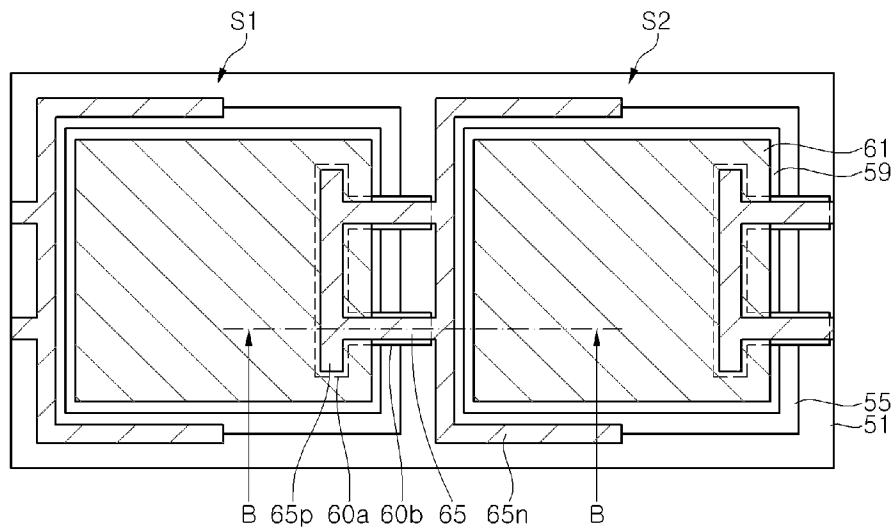
[Fig. 15]



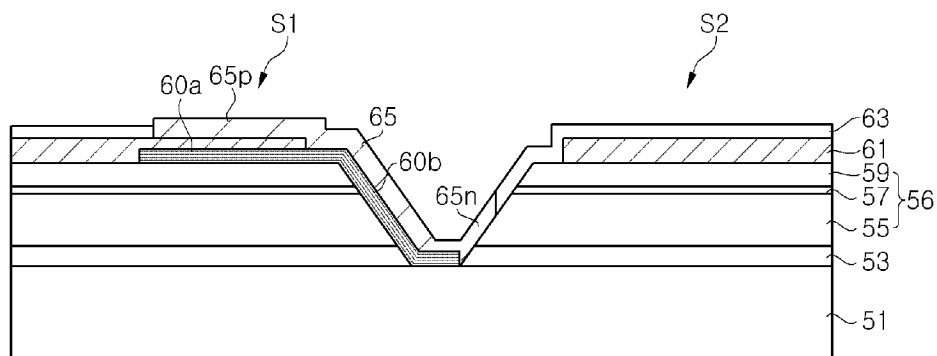
[Fig. 16]



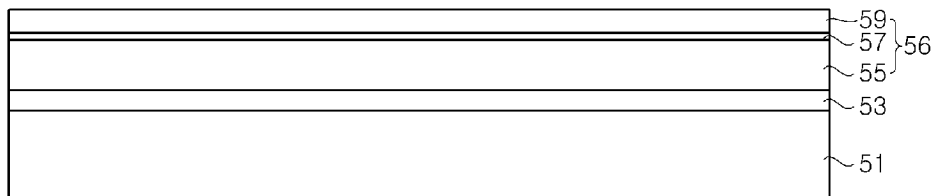
[Fig. 17]



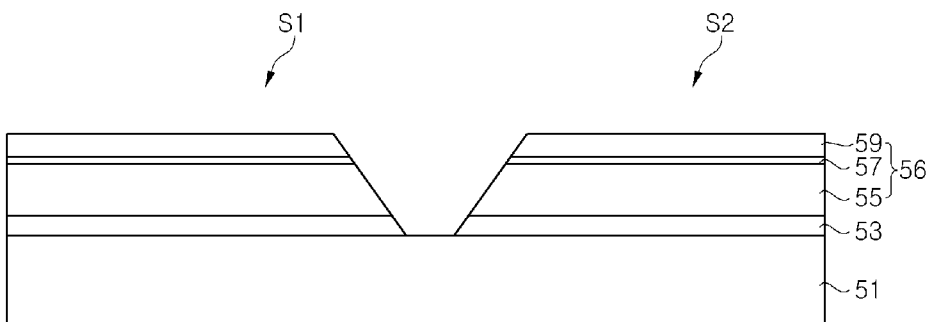
[Fig. 18]



[Fig. 19]

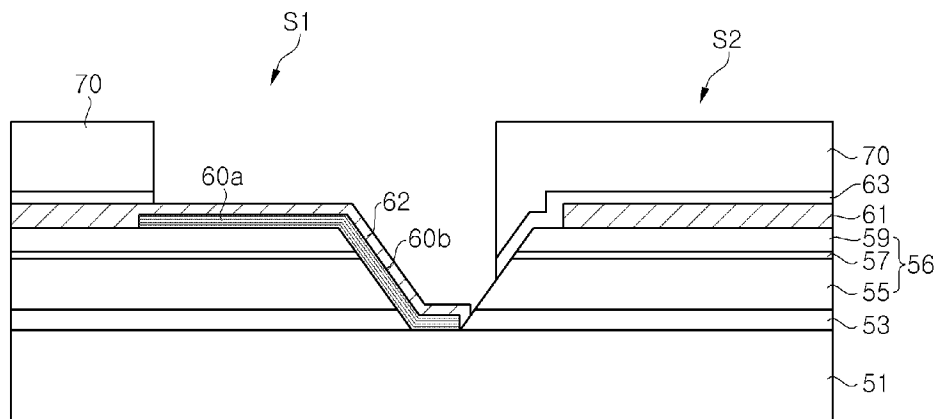


[Fig. 20]

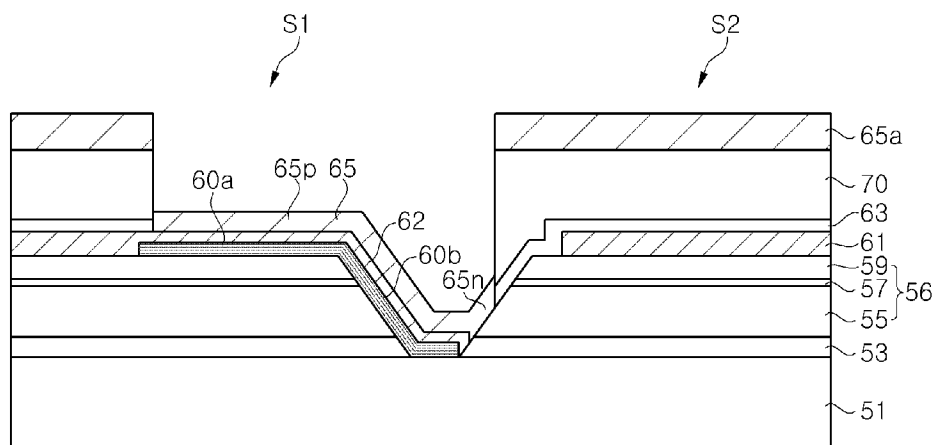


[illegible]

[Fig. 29]



[Fig. 30]



A. CLASSIFICATION OF SUBJECT MATTER**H01L 33/36(2010.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 33/36; H01L 33/20; H01L 33/46; H01L 33/10; H01L 33/00; H01L 33/08; H01L 33/42; H01L 33/38

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: LED, light emitting cell, current blocking layer, distributed Bragg reflector, sidewall

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2010-0059768 A1 (GHULAM HASNAIN) 11 March 2010 See abstract, paragraphs [0029]-[0032], [0044], claims 1-6 and figures 5-6, 11.	1,9-12
Y		20
A		2-8,13-19
Y	US 2011-0127549 A1 (SUM GEUN LEE et al.) 02 June 2011 See abstract, paragraphs [0060]-[0075], claim 1 and figure 7.	20
A		1-19
A	KR 10-2012-0044719 A (SEOUL OPTO DEVICE CO., LTD.) 08 May 2012 See abstract, paragraphs [0030]-[0040], claim 1 and figure 1.	1-20
A	JP 2010-045419 A (SEOUL OPTO DEVICE CO., LTD.) 25 February 2010 See paragraphs [0021]-[0034] and figure 1.	1-20
A	KR 10-0966372 B1 (SAMSUNG LED CO., LTD.) 28 June 2010 See paragraphs [0022]-[0026] and figure 1a.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search

26 March 2014 (26.03.2014)

Date of mailing of the international search report

27 March 2014 (27.03.2014)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2013/011914

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010-0059768 A1	11/03/2010	CN 102132429 A	20/07/2011
		EP 2338183 A2	29/06/2011
		EP 2338183 A4	27/03/2013
		JP 2012-507134 A	22/03/2012
		JP 2013-232677 A	14/11/2013
		KR 10-2011-0057152 A	31/05/2011
		TW 201027798 A	16/07/2010
		US 2011-0163347 A1	07/07/2011
		US 7939839 B2	10/05/2011
		US 8207543 B2	26/06/2012
		WO 2010-030482 A2	18/03/2010
		WO 2010-030482 A3	27/05/2010
US 2011-0127549 A1	02/06/2011	CN 102074622 A	25/05/2011
		EP 2362453 A2	31/08/2011
		JP 2011-109094 A	02/06/2011
		JP 2011-166146 A	25/08/2011
		KR 10-2011-0053064 A	19/05/2011
		KR 10-2011-0085961 A	27/07/2011
		KR 10-2011-0093587 A	18/08/2011
		TW 201130165 A	01/09/2011
		US 2011-0114969 A1	19/05/2011
		WO 2011-059173 A2	19/05/2011
		WO 2011-059173 A3	29/09/2011
		WO 2011-099771 A2	18/08/2011
		WO 2011-099771 A3	29/12/2011
KR 10-2012-0044719 A	08/05/2012	JP 2012-028749 A	09/02/2012
		KR 10-1158080 B1	22/06/2012
		KR 10-1272708 B1	10/06/2013
		US 2012-0187424 A1	26/07/2012
		US 8629471 B2	14/01/2014
		WO 2012-011749 A2	26/01/2012
		WO 2012-011749 A3	26/04/2012
JP 2010-045419 A	25/02/2010	CN 100580963 C	13/01/2010
		CN 101305477 A	12/11/2008
		CN 101305477 C0	12/11/2008
		CN 101820043 A	01/09/2010
		DE 112006002927 B4	02/06/2010
		DE 112006002927 T5	20/11/2008
		JP 2009-522803 A	11/06/2009
		JP 2011-187998 A	22/09/2011
		JP 4523670 B2	11/08/2010
		JP 4861437 B2	25/01/2012
		KR 10-0721515 B1	23/05/2007
		KR 10-0758542 B1	13/09/2007
		TW I322519 A	21/03/2010
		TW I322519 B	21/03/2010

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/KR2013/011914

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
KR 10-0966372 B1	28/06/2010	US 2010-0032694 A1	11/02/2010
		US 2010-0148190 A1	17/06/2010
		US 7700960 B2	20/04/2010
		US 7998761 B2	16/08/2011
		WO 2007-081092 A1	19/07/2007
		KR 10-2009-0053435 A	27/05/2009