Abstract

Disclosed is an improved method for fabricating an active matrix liquid crystal display device having enhanced pixel capacitance for improved display performance. The improved method provides for the use of fewer mask and etch steps, thus simplifying the manufacturing process. The inventive method also provides for protecting the channel region (40) of the thin film transistor switch at each picture element (38) from the harsh processing environment.
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PROCESS FOR MANUFACTURING AN ACTIVE MATRIX DISPLAY
FIELD OF THE INVENTION

The invention relates generally to the field of thin film transistor driven active matrix displays, and more particularly to the field of manufacturing processes for fabricating thin film transistor driven active matrix displays. The invention most particularly relates an improved process for fabricating thin film transistor driven active matrix liquid crystal display devices having a pixel capacitance in parallel to the pixel. The inventive process also provides enhanced protection to the channel region of the transistors, thus improving transistor performance.

BACKGROUND OF THE INVENTION

In the field of liquid crystal displays, and in particular in the field of active matrix liquid crystal displays, major international electronics companies have, for the last decade, expended hundreds of millions of dollars for the development of large area, high resolution displays. In addition to being large area, liquid crystal displays also must be able to display information at video speed rates, and be able to illustrate images in a wide variety of colors.

Fabricating a color LCD is a highly sophisticated endeavor, merging the sciences of chemistry, photography, microelectronic engineering and precision manufacturing techniques. These combined processes are as complex as producing a large scale semiconductor. The basic design principles of LCD’s are in fact closely coupled with semiconductor manufacturing technology.

The active matrix color LCD used in, for example, a "notebook" computer has an average of 307,200 picture elements ("pixels"). Each pixel contains red, green, and blue
elements. In order to address each element of each pixel at video rate speeds, a separate transistor must be provided at each element. That translates into 921,600 transistors. A comparable 14 inch diagonal LCD display would therefore require approximately 1,232,000 transistors. Essentially, each screen is a large microchip.

If a transistor fails or is defective, the pixel will not operate. It will be fused in either the "on" or "off" condition. As screen size increases, so does the probability of defective pixel transistors. Many manufacturers will reject any display in which more than 25 (out of 921,600) transistors malfunction. Depending upon the application for the display, failure rates of much fewer than 25 pixels may be necessary. Even at the level of 25 defects per display, world leaders in producing color LCD’s are achieving display manufacturing yields of less than 10%. These low production yields contribute to the high costs of displays.

The principal source of defects in the manufacturing of LCD’s is the fabrication of the switching element, or thin film transistor, disposed at every picture element. Fabrication of the thin film switching element typically requires 5 and up to 7 separate deposition-mask-etch steps in order to fabricate the transistor. As each layer of material is deposited, masked, and etched to create a new layer of structure, critical tolerances of less than 1 micron must be maintained in order to produce an operative device. As additional deposition-mask-etch steps are required, the likelihood of error increases, and hence, manufacturing yield of the display decreases.

Manufacturers have long sought a simpler method offabricating thin film transistors, particularly those for use in active matrix liquid crystal displays. An example of such efforts is disclosed in U.S. Patent No. 4,102,733, to Delamoneda, et al. for "INSULATED GATE FIELD EFFECT TRANSISTOR". While the ’733 patent does
realize cost savings due to reduced mask steps, and higher yields associated with area savings due to self-alignment, the '733 patent is directed to the fabrication of insulated gate field effect transistors. Moreover, there is no discussion of using such devices for fabricating the switching elements of active matrix liquid crystal displays. Moreover, the manufacturing process employed is different than that disclosed herein, and is not adapted for cooperatively fabricating all or part of an active matrix liquid crystal display.


These and other limitations inherent in the prior art are obviated by the instant invention.

OBJECTS OF THE INVENTION

It is a principal object of the instant invention to provide an effective method of fabricating a thin film field effect transistor.

It is a further object of the instant invention to provide a relatively inexpensive, highly reliable, active matrix liquid crystal display.
It is a further objective of the instant invention to provide a highly efficient, thin film transistor switching element for each pixel of an active matrix liquid crystal display.

It is yet another object of the instant invention to reduce the number of mask/etch steps necessary to fabricate such a transistor.

It is another objective of the instant invention to provide an active matrix liquid crystal display having a storage capacitor in parallel with the display pixel for improved pixel performance.

It is a further objective of the invention to provide a transistor switching device having a transistor channel region which is protected from the harsh active matrix display fabrication process.

It is yet another object of the invention to provide a transistor switching device having high mobility for enhanced switching performance.

It is a further objective of the instant invention to reduce the critical alignment between succeeding layers of material deposited during the fabrication of the thin film transistor.

These and other objects and advantages of the instant invention will become readily apparent to the reader upon perusing the Brief Description of the Invention, the Brief Description of the Drawings, the Detailed Description of the Preferred Embodiments, and the Claims, all which follow hereinafter.

**SUMMARY OF THE INVENTION**

There is disclosed herein, an improved method for fabricating field effect thin film transistor driven active matrix display device having parallel capacitance and a protected
channel transistor for improved performance, said transistor device also having gate
regions, source regions, and drain regions. The improved method comprises the steps
of providing a substrate member such as glass, plastic, quartz, and other known high
temperature substrate materials. Thereafter, a first layer of electrically conductive
material is disposed upon said substrate, which layer is patterned to form the gate
contacts of each TFT and first address means in electrical communication with said gate
contacts. The first address means typically includes a first address line adapted to be
electrically connected to electronic circuitry disposed about the peripheral edges of the
substrate.

The layer of electrically conductive material, which may be fabricated from
chromium, aluminum, molybdenum, tantalum, silver, tin, gold, and combinations thereof,
is then patterned using a first mask, and conventional photolithographic and etching
techniques to form said gate contacts and address means.

Thereafter, a layer of electrically insulating material, such as silicon oxide, silicon
nitride, or silicon carbide is disposed atop said patterned layer of electrically conductive
material. The layer, the gate insulating layer of electrically insulating material is
deposited to a thickness sufficient to assure that there are no defects or apertures formed
therein whereby there would be electrical communication between the first layer of
electrically conductive material and any subsequently deposited layers.

Disposed atop the layer of electrically insulating material is a body of
semiconductor material. The body of semiconductor material may be a single layer of
semiconductor material such as, for example, amorphous silicon, amorphous germanium
or combinations of silicon or germanium alloy materials. Alternatively, the body of
semiconductor material may be a multilayered structure in which each layer of
semiconductor material is either intrinsic or slightly p- or n-type doped. In a preferred embodiment of the instant invention, the body of semiconductor material is a two layer structure comprising a first layer of intrinsic amorphous silicon semiconductor material disposed immediately atop the layer of electrically insulating material. The second layer is a layer of slightly n-doped amorphous silicon deposited directly atop said layer of intrinsic amorphous silicon material.

Disposed atop the body of semiconductor material is a second layer of electrically conductive material. In a preferred embodiment of the instant invention, the second layer of electrically conductive material is a thin layer of metal such as chromium and/or aluminum. This second electrically conductive layer is then patterned using a second mask, and conventional photolithographic and etching techniques to form the second address line as well as the source and drain contact regions of the transistor. The source and drain contact regions are vertically disposed and electrically insulated from said gate region. This second layer also forms the contact of the pixel capacitor. This layer also serves to protect the semiconductor layer from the harsh environment of subsequent processing steps.

Thereafter, the patterned second electrically conductive layer is employed as the mask for the subsequent etching of the body of semiconductor material. Using conventional dry etch techniques, all semiconductor material not directly underlying said second layer of electrically conductive material are removed from the substrate. The result is the remaining structure thus includes only the body of semiconductor material underlying said second layer of electrically conductive material all of which is disposed atop the layer of electrically insulating material.
Thereafter, a layer of transparent conductive oxide, such as indium-tin-oxide is disposed atop the entire structure. The layer of indium-tin-oxide is patterned using a third mask, and conventional photolithographic and etching techniques to form a second conductive pathway atop such second address line as well as the source and drain regions of the thin film transistor device. The transparent conductive oxide layer is also patterned to be in electrical communication with the pixel capacitor. In the event that the thin film transistor device is in electrical communication with another device or component of a device, such as the first pixel electrode of an active matrix liquid crystal display, the layer of indium-tin-oxide may be further patterned so as to form that component.

Thereafter, employing the layer of transparent conductive material as a mask, it is possible to etch the remaining layer of electrically conductive material between the source and drain regions so as to assure that there is no direct electrical communication therebetween. By etching the so-called channel region between the source and drain of the transistor after all display processing is completed, the channel is protected from the harsh processing environment. Exposure to such conditions can degrade performance of the material comprising the channel region of the transistor.

**BRIEF DESCRIPTION OF THE DRAWINGS**

Figure 1 is a perspective, plan view of a transistor driven active matrix device, after a first deposition-mask-etch operation.

Figure 2a is a cross-sectional view, taken along line A-A of Figure 1, after the deposition of a insulating layer, a semiconductor body, and an electrically conductive layer.
Figure 2b is a cross-sectional view taken along line A-A of Figure 1, after a mask-etch operation on the electrically conductive layer illustrated in Figure 2a.

Figure 2c is a cross-sectional view, taken along line C-C of Figure 2d, after an etch operation on the semiconductor body; the patterned electrically conductive layer serving as the mask for etching the semiconductor body.

Figure 2d is a perspective plan view of the display device of Figure 2c.

Figure 3a is a cross-sectional view of the thin film transistor device after deposition and mask patterning of a layer of transparent conductive oxide material, said transparent conductive device adapted to be the first electrode of a liquid crystal picture element, electrically contacting a storage capacitor.

Figure 3b is a perspective plan view of the thin film transistor device and first pixel electrode of Figure 3a.

Figure 4 is a cross-sectional view of the device in Figure 3b, taken along line A-A thereof, after exposing the channel region of the transistor between the source region and the drain region, by an etch process.
DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Disclosed as part of the instant invention is an improved electronic display, such as a liquid crystal display, and more specifically, by way of example and not by way of limitation, an active matrix liquid crystal display. It is to be understood that while the improved method disclosed and claimed herein is of particular utility in the manufacture of active matrix liquid crystal displays, such process has great utility in other fields of electronics, including, for example, the fabrication of memory devices, microprocessor devices, and other computer circuitry.

Referring now to Figure 1, there is depicted therein a perspective plan view illustrating the first step of the improved process for fabricating an active matrix display plate having a storage capacitor in parallel. Specifically, illustrated in Figure 1 is a substrate 10 upon which the thin film transistor and any associated circuitry or other components are deposited. It is to be noted that in Figure 1, as well as the remaining figures, that while a single display picture element (pixel) and associated thin film transistor device is illustrated in a device having two rows of such devices, any number of similar devices may be disposed in any arrangement on a substrate 10 of any size. In the embodiment in which the thin film transistor is the switching element for a single picture element of an active matrix liquid crystal display, a single substrate may have several million such pixel and switching devices disposed thereon.

Returning to Figure 1, substrate 10 is typically a rigid member capable of withstanding the elevated temperatures necessary to fabricate active matrix display devices. Examples of preferred materials from which the substrate is fabricated include glass, plastic, quartz, and combinations thereof. In a particularly preferred embodiment
of the instant invention, the substrate 10 is fabricated from Corning Industry's "7059" glass.

Disposed upon said substrate 10 is a layer of electrically conductive material 12. The electrically conductive material is selected from the group of materials including chromium, aluminum, molybdenum, tantalum, silver, gold, tin, and combinations thereof. The electrically conductive material may be deposited by any number of known, conventional, deposition techniques. Examples of acceptable deposition techniques include sputtering, chemical vapor deposition ("CVD"), plasma enhanced chemical vapor deposition ("PECVD"), and evaporation. In a preferred embodiment of the instant invention, the electrically conductive material is a layer of chromium deposited, by a sputtering process, to a thickness of between 500 and 8000 angstroms, and most preferably between 1000 and 4000 angstroms.

A first mask is then used with conventional photolithographic and wet etching techniques to form a first address means 14a and gate region 16 of the thin film transistor device and first address means 14b of a second row of devices. The first address means 14a, 14b take the form of an address lines adapted to be connected to electronic circuitry which may be disposed at the periphery of the substrate 10. The first address line 14 is adapted to provide an electrical connection between the peripheral electronic circuitry and the gate region 16 whereby electrical impulses generated by the peripherally mounted circuitry are carried to the gate region.

Referring now to Figures 2a-2c, there is illustrated therein a cross-sectional side view taken along line A-A of Figure 1, and illustrating the deposition of subsequent layers of material forming the display pixel and thin film transistor device. Specifically, in Figure 2a, disposed atop said substrate 10, and said first address line 14 and gate
region 16 is a layer of electrically insulating material 18. Electrically insulating layer 18 may be fabricated from any of a number of electrically insulating materials including, for example, silicon nitride, silicon carbide, and silicon oxide. The layer of insulating material 18 may be deposited by any number of conventional deposition techniques including, CVD, PECVD, sputtering or evaporation. In a preferred embodiment of the instant invention, the electrically insulating layer 18 is a layer of silicon nitride deposited to a thickness of between 3000 and 6000 angstroms, by a PECVD process.

Thereafter, a body of semiconductor material is disposed atop the layer of electrically insulating material 18. The body of semiconductor material 20 may be either a single layer of a single conductivity type, or may be a multilayered structure including both intrinsic and doped layers of semiconductor material. The body of semiconductor material should be deposited to a thickness of between 1000 and 5000 angstroms, and be deposited by any of a number of known deposition techniques, including PECVD, CVD, evaporation, and sputtering. In a preferred embodiment, the semiconductor material used in fabricating said body of semiconductor material 20 include silicon, germanium, silicon: germanium alloys, germanium: silicon alloys, and combinations thereof. The body of semiconductor material 20 may also be fabricated of crystalline, polycrystalline, microcrystalline or amorphous semiconductor materials.

In a preferred embodiment of the instant invention, the body of silicon material 20 is a two-layer structure comprising a first layer of intrinsic amorphous silicon 20a and a slightly n-doped layer of amorphous silicon 20b. Layer 20a of amorphous silicon is deposited by PECVD over the entire layer of electrically insulating material 18 to a thickness of between 500 and 3000 angstroms. Thereafter, the layer of n-doped
amorphous silicon material 20b is disposed over the entire layer 20a by PECVD to a thickness of between 500 and 3000 angstroms.

Thereafter, a second layer of electrically conductive material 22 is disposed atop said body of semiconducting material 20. As with layer 12 of Figure 1, layer 22 may be fabricated from any of a number of electrically conducting materials including those discussed hereinabove with respect to layer 12. Moreover, those materials may be deposited by conventionally known techniques such as discussed hereinabove with respect to layer 12. In a preferred embodiment of the instant invention, layer 22 is a thin layer of metal, such as chromium and aluminum, wherein the chromium is deposited first, and the aluminum atop the chromium. This metal layer is deposited to a total thickness of between 1000 and 3000 angstroms by a sputtering technique.

Referring now to Figure 2b, the structure of deposited layers of materials described with respect to Figure 2a is modified to continue fabrication of the active matrix display pixel and associated thin film transistor device. In Figure 2b, electrically conductive layer 22, is patterned to form second address means 24, source contact region 26 and drain contact region 28 of the transistor device of Figure 2d, and metal contact region 25 of storage capacitor 39 of Figure 3b. Specifically, a second mask is used with conventional photolithographic and wet etching techniques to form said second address line 24 and contact regions 25, 26 and 28. As discussed hereinabove with respect to first electrically conductive layer 12, any number of conventionally known photolithographic and wet etching techniques may be used to pattern second electrically conductive layer 22.

Thereafter, the patterned layer of electrically conductive material 22 is used as a mask for the subsequent process of etching the body of semiconductor material.
Specifically, by using the patterned, second layer of electrically conductive material 22 as a mask during a subsequent etch step, only that semiconductor material underlying said layer of electrically conductive material 22 will remain after the etch process is completed.

In a preferred embodiment of the instant invention, the body of semiconductor material 20 is etched using a dry etching technique such as plasma or reactive ion etching ("RIE") technique, or conventional plasma etch. Figure 2c illustrates the results of employing a dry etch technique such as RIE to the structure of Figure 2b. The body of semiconductor material 20 remains only in those regions underlying the layer of electrically conductive material 22. The layer of electrically insulating material 18 is unaffected by the dry etch technique. Accordingly, the body of semiconductor material 20 and the second electrically conductive layer 22 are vertically disposed, and electrically insulated from the first address line 14 and the gate region 16. The configuration of the first and second address lines 14 and 24 respectively, as well as the gate region 16, source and drain contacts 26, 28, and storage capacitor 39 are illustrated in Figure 2d. For purposes of simplifying the illustration, electrically insulating layer 18, and semiconductor body 20 are not shown in Figure 2d. For purposes of illustration, the structure illustrated in Figure 2c is a cross-sectional side view taken along line C-C of Figure 2d.

Referring now to Figures 3a and 3b, the next step in the process of fabricating the thin film transistor involves the deposition of a layer of electrically conductive material atop layer 22. In a preferred embodiment of the instant invention, the layer of electrically conductive material 30 is a layer of a transparent conductive oxide material, which is deposited over the entire substrate member 10 so as to cover conductive layer 22 and insulating layer 18. Examples of transparent conductive materials suitable for this
purpose include indium tin oxide, tin oxide, indium oxide, cadmium stannate, and combinations thereof. The layer of transparent conductive material 30 may be deposited by any of a number of known conventional techniques including sputtering, evaporation, PECVD, and CVD. In a preferred embodiment of the instant invention, layer 30 is a layer of indium tin oxide deposited to a thickness of between 500 and 3000 angstroms by a sputtering process.

Thereafter, a third and final mask is used with conventional photolithographic and etching techniques to pattern the layer of transparent conductive material 30 to form a second conductive pathway 32, source region 34 and drain region 36 atop said second layer of electrically conductive material 22. In the embodiment in which the thin film transistor device is used as a switching element of an active matrix liquid crystal display, the layer of transparent conductive material may be further patterned to form a first pixel electrode 38 and contact a storage capacitor 39 in parallel with said first pixel electrode of said display. After patterning said layer of transparent conductive material 30, a conventional wet etch technique is used to form structures 32, 34, 36, 38 and 39 illustrated in Figure 3b.

The final step in the improved process of fabricating the thin film transistor device is accomplished by using the layer of transparent conductive material 30 and photoresist as above, as a mask for the subsequent process of wet etching the remaining electrically conductive material 22 and layer 20b in region 40 of Figure 3b between source 34 and drain 36. The area of material under region 40 is known as the channel of the transistor device. By protecting the channel region from the processing steps described above, the quality of the semiconductor material in the channel is improved. This means that fewer
defects are created in the material, and hence, the material performs better in terms of
having better values of mobility. In this way, it is possible to achieve a conventional,
TFT driven, display element having an associated storage capacitor, and a better
performing channel region, using fewer masks and processing steps than was known in
the prior art.

As may be readily appreciated by those skilled in the art, the present invention
can be practiced other than as specifically disclosed herein. Thus, while the instant
invention has been described with respect to certain preferred embodiments thereof, it
is to be understood that the foregoing and other modifications and variations may be
made without departing from the spirit or scope thereof.
CLAIMS:

1. A method of fabricating a subassembly for an active matrix liquid crystal display including at least a first pixel electrode, first and second address means, a storage capacitor and at least one thin film transistor including a gate region, a source region, and a drain region, said method including the steps of:

   providing a transparent substrate member having a first layer of electrically conductive material deposited thereon;

   patterning said layer of electrically conductive material to form said first address means and at least one of said gate regions;

   depositing a layer of electrically insulating material over said layer of electrically conductive material and said substrate;

   depositing a body of semiconductor material atop said layer of electrically insulating material;

   providing a second layer of electrically conductive material atop said body of semiconductor material, said second layer of electrically conductive material being photolithographically patterned and etched so as to form said second address means intersecting said first address means, source and drain contact regions above said gate region, and said storage capacitor atop said first address means;

   selectively removing areas of the body of semiconductor material not underlying said second layer of electrically conductive material;

   depositing a layer of transparent conductive material atop said electrically conductive material and said electrically insulating material, said transparent
conductive layer being photolithographically patterned and etched to cover said second address line and said source contact region, and forming said first pixel electrode and electrically communicating with said drain contact region and said storage capacitor; and

selectively removing the area of electrically conducting material between said source region and said drain region.

2. A method as recited in Claim 1, wherein the layer of transparent conductive material is a layer of indium tin oxide which functions as the mask for removing said layer of electrically conducting material between said source region and said drain region.

3. A method as recited in Claim 2, including the further step of depositing a layer of passivating material over said subassembly.

4. A method as recited in Claim 3, wherein said passivating material is selected from the group of materials consisting of silicon nitride, silicon oxide, and silicon carbide.

5. A method as recited in Claim 1, wherein said substrate is a transparent substrate selected from the group of materials consisting of glass, quartz, and plastic.

6. A method as recited in Claim 1, wherein said first and second layers of electrically conductive material are metallic materials selected from the group of materials consisting of aluminum, chromium, silver, tungsten, tantalum, molybdenum, and combinations thereof.

7. A method as recited in Claim 1, wherein said layer of electrically insulating material is selected from the group of materials consisting of silicon nitride, silicon carbide, silicon oxide, and combinations thereof.
8. A method as recited in Claim 1, wherein the step depositing the layer of semiconductor material includes the further steps:

   depositing a first layer of semiconductor material being an amorphous, intrinsic layer of silicon; and

   depositing a second layer of semiconductor material, the second layer comprising a layer of n-doped amorphous silicon material.

9. A method as recited in Claim 1, wherein said layer of transparent conductive material is a layer of transparent conductive oxide selected from the group of indium tin oxide, indium oxide, tin oxide, cadmium stannate, lead oxide, and combinations thereof.

10. A method of fabricating at least one field effect, thin film transistor device having a gate region, a source region, and a drain region, said method comprising the steps of:

    providing a substrate;

    depositing a first layer of electrically conducted material on said substrate, and patterning said layer to form said gate region;

    depositing a layer of electrically insulating material atop said gate region in said substrate;

    depositing a layer of semiconductor material atop said layer of electrically insulating material;

    depositing a second layer of electrically conducting material atop said layer of semiconductor material, and patterning said second layer to form a source contact and a drain contact above said gate region;
removing the areas of semiconductor material not lying beneath said
patterned, second layer of electrically conductive material;

providing a layer of transparent conductive material atop at least said
source contact and said drain contact to form said source region and said drain
region; and

removing the area of second electrically conductive material not underlying
said layer of transparent conductive material.

11. A method as recited in Claim 10, wherein said substrate is a transparent
substrate selected from the group of materials consisting of glass, quartz, and plastic.

12. A method as recited in Claim 10, wherein said first and second layers of
electrically conductive material are metallic materials selected from the group of
materials consisting of aluminum, chromium, silver, tungsten, tantalum, molybdenum, and
combinations thereof.

13. A method as recited in Claim 10, wherein said layer of electrically
insulating material is selected from the group of materials consisting of silicon nitride,
silicon carbide, silicon oxide, and combinations thereof.

14. A method as recited in Claim 10, wherein the step depositing the layer of
semiconductor material includes the further steps:

depositing a first layer of semiconductor material being an amorphous,
intrinsic layer of silicon; and

depositing a second layer of semiconductor material, the second layer
comprising a layer of n-doped amorphous silicon material.

15. A method as recited in Claim 10, wherein said layer of transparent
conductive material is a layer of transparent conductive oxide selected from the group
of indium tin oxide, indium oxide, tin oxide, cadmium stannate, lead oxide, and combinations thereof.
INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/03584

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H01L 21/336; 21/84; 29/784.
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 437/40, 47, 48, 59, 101; 909; 257/57; 359/59, 87

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

<table>
<thead>
<tr>
<th>Category</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
<th>Relevant to claim No.</th>
</tr>
</thead>
</table>

Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:
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Date of the actual completion of the international search
26 JULY 1993

Date of mailing of the international search report
19 AUG 1993

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Authorized officer
M. WILCZEWSKI

Telephone No. (703) 308-2771

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