



(51) International Patent Classification:
H04N 5/355 (2011.01)

(21) International Application Number:
PCT/EP2017/079751

(22) International Filing Date:
20 November 2017 (20.11.2017)

(25) Filing Language: English

(26) Publication Language: English

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(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: PIXEL SENSOR CELL FOR CMOS IMAGE SENSORS WITH ENHANCED CONVERSION GAIN AT HIGH DYNAMIC RANGE CAPABILITY

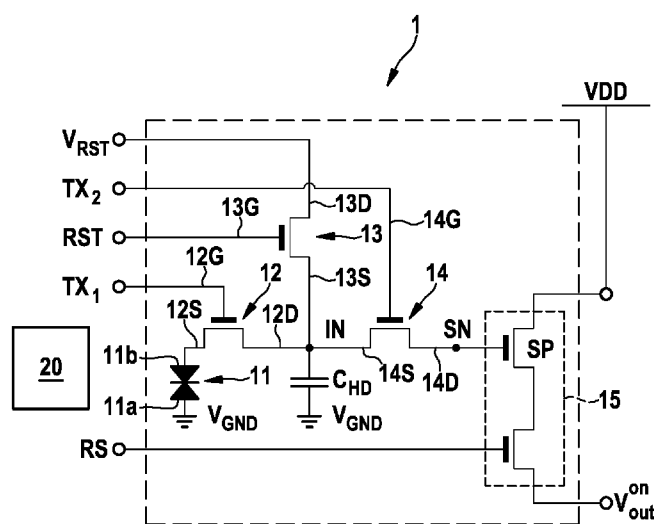


Fig. 1

(57) Abstract: The present invention relates to a pixel sensor cell (1) for a CMOS sensor device comprising: - a photodiode (11) for generating photoelectrons; - a first transfer transistor (12) coupling the photodiode (11) with an intermediate node (IN) and configured to be controlled by a first control signal (TX₁); - a gain reducing capacitance (C_{HD}) applied on the intermediate node (IN); - a second transfer transistor (14) coupling the intermediate node (IN) with a sense node (SN) and configured to be controlled by a second control signal (TX₂); - an output buffer (15) coupled with the sense node (SN) and configured to amplify a potential on the sense node (SN).

Published:

— *with international search report (Art. 21(3))*

Description

Pixel sensor cell for CMOS image sensors with enhanced conversion gain at high dynamic range capability

Technical field

The present invention relates to CMOS image sensors comprising a high number of pixels formed by pixel sensor cell having pinned photodiodes and CMOS integrated circuitry. Furthermore, the present invention relates to measures for readout noise reduction and increase of dynamic range of such CMOS image sensors.

Technical background

CMOS image sensors are widely applied in technical devices, such as mobile devices or digital cameras. While the development of the pinned photodiodes (buried photodiodes) dramatically increased noise performance of CMOS image sensors, the characteristics of conventional CMOS image sensors still have limitations with respect to sensitivity and dynamic range.

A conventional pixel sensor cell is exemplarily shown in document A. Boukhayma, A. Peizearat and C. Enz, "Noise Reduction Techniques and Scaling Effects towards Photon Counting CMOS Image Sensors", *Sensors* 2016, 16, 514, <http://www.mbp.com/thermal/sensors>. The conventional pixel sensor cell includes a pinned photodiode and generally four transistors which include a transfer transistor separating the pinned photodiode from a sense node, reset and row selection transistors and a source follower transistor that buffers the voltage level of the sense node.

The transfer transistor is used to control a potential barrier for charge carriers stored/generated in the pinned photodiode. When the gate voltage of the transfer transistor is low enough and the resulting potential in the channel of the transfer transistor is lower than the photo-generated voltage of the pinned photodiode, the integrated charge stored in the pinned photodiode is kept. When the gate voltage of the transfer transistor is set to a high voltage, a depletion in the channel of the transfer transistor is created so that the potential is higher than the charge potential of the pinned photodiode and also lower than a reset potential of the sense node. So, the electrons accumulated in the pinned photodiode during an integration phase flow towards the higher potential area of the sense node through the transfer transistor and the voltage level of the sense node drops from the reset potential depending on the transferred charge.

The voltage of the sense node is sensed by an adequate electronic circuit after resetting the sense node to the reset potential and after the charge of the photodiode has been allowed to flow onto the sense node. The sensed potentials are subtracted to obtain the signal level. This sensing method is called correlated double sampling and allows the reduction of noise that is correlated between the reset time and the transfer time.

While above architecture of the pixel sensor cell and the method of operation provide a good noise characteristic and a reasonable dynamic range, there is a further demand for CMOS image sensors with an even better sensitivity and a higher dynamic range.

Regarding an enhancement of the dynamic range, several techniques have been proposed in document K. Hara, H. Kubo, M. Kimura, F. Murao, and S. Komori, "A linear-logarithmic CMOS sensor with offset calibration using an injected charge signal" in ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005., Feb 2005, pp. 354–603 Vol. 1, in document M. Loose, K. Meier, and J. Schemmel, "A self-calibrating single-chip CMOS camera with logarithmic response," IEEE Journal of Solid-State Circuits, vol. 36, no. 4, pp. 586–596, Apr 2001 and in document J. S. et al., "A 1280 960 3.75 μ m pixel CMOS imager with triple exposure HDR," in International Image Sensors Workshop, 2009, Sept 2009, pp. 1–4 which have the disadvantage of not being linear or not having a single synchronous integration time. Further methods are disclosed in A.K.Kalgi et al., "Four concepts for synchronous, PSN limited, true CDS, HDR imaging", in International Image Sensors Workshop, 2015, Sept 2015, pp. 1–4. However, methods based on varying the integration time or using multiple different size photodiodes fail having photon-shot-noise

limited operation and methods based on acquiring and combining multiple frames at different gains fail to operate in synchronous shutter mode.

From documents EP 2 890 117 A1, US 7,408,210, US 7,719,590, and US2017/0148832, further approaches are known which allow a linear response and a low readout noise for all lighting conditions and have the possibility to operate in a synchronous shutter mode. These approaches are based on multiple ranges of linear gain so that a high gain is provided for low light signals to ensure a low noise performance, and a low gain is provided for high dynamic signal to avoid saturation. Hence, this method requires a varying sense node capacitance which is embodied by an additional capacitance to be coupled with the sense node by means of a transistor. So, for low-light conditions, the extra capacitance can be disconnected from the sense node to ensure the lowest sense mode capacitance. For high dynamic signals, the extra capacitor can be connected with the sense node in order to increase dramatically the sense node capacitance resulting in a much lower conversion gain and a much larger saturation level. A disadvantage of these approaches is that the additional transistor increases the sense node capacitance and therefore increases the noise floor which affects the overall sensitivity.

Summary of the invention

This object has been achieved by the pixel sensor cell according to claim 1, by the method of operating a pixel sensor cell and by the CMOS image sensor according to the further independent claims.

Further embodiments are indicated in the depending claims.

According to a first embodiment a pixel sensor cell for a CMOS sensor device is provided comprising:

- a photodiode for generating photoelectrons;
- a first transfer transistor coupling the photodiode with an intermediate node and configured to be controlled by a first control signal;
- a gain reducing capacitance applied on the intermediate node;
- a second transfer transistor coupling the intermediate node with a sense node and configured to be controlled by a second control signal;

- an output buffer coupled with the sense node and configured to amplify a potential on the sense node.

According to a further aspect, a method is provided for operating the above pixel sensor cell, comprising the steps of:

- accumulating photoelectrons in the photodiode during an integration time or allowing photoelectrons to accumulate in the photodiode during the integration time;
- in a first phase, coupling the intermediate node with the sense node by means of the second transfer transistor and providing a charge threshold for accumulated photoelectrons so that only excess photoelectrons (photoelectrons which contribute to a potential which allow an overflow over the charge threshold) are allowed to pass/flow to the intermediate node, wherein the potential generated by the excess photoelectrons is read out as an HDS sampling output signal;
- in a second phase, controlling the second transfer transistor to set a threshold of the second transfer transistor to a potential where the second transfer transistor forms an electrical isolation between the intermediate node and the sense node and which is substantially equal or higher than the potential of the intermediate node, coupling the intermediate node with the sense node and reading out the potential on the sense node as a LLS sampling output signal.

One idea of the above pixel sensor cell is to use a combination of a gain reducing capacitance and a first and second transfer transistors, particularly MOSFET transistors, to couple the preferably pinned photodiode with a sense node wherein the gain reducing capacitance may particularly be explicitly or intrinsically formed e.g. as a p+n junction and is separated from the sense node by the second transfer transistor. This allows the reduction of the noise by reducing the sense node capacitance by isolating it from the first transfer gate and the gain reducing capacitance.

Moreover, the saturation level of the pixel sensor cell is enhanced by providing an intermediate node with the gain reducing capacitance to be merged or isolated from the sense node by means of the second transfer transistor. Thereby, a high dynamic read-out can be performed by using the gain reducing capacitance. Further, a low-light sampling is also possible by having the integrated charge of the pinned photodiode directly flown into the sense node through the first and second transfer transistors. In difference to the state of the art high dynamic pixel sensor cells, the sense node is isolated from the first transfer

transistor and further components by means of the second transfer transistor. In other words, the second transfer transistor decouples the sense node from the rest of the circuitry which results in an important reduction of the sense node capacitance and a lower read-out noise.

By closing (herein understood as making conductive) the second transistor, the sense node is merged with the gain reducing capacitor, which increases the sense node capacitance, reduces the pixel conversion gain and increases the saturation level.

The above method of operating a pixel sensor cell exploits the fact that the transfer transistors can be operated with analogue inputs defining potential levels for the photoelectrons path starting in the photodiode, the first transfer transistor, the gain reducing capacitance and the second transfer transistor to the sense node during the read-out steps. The potential levels for thresholds which can be applied to beneficially implement a multi-step read-out scheme which allows the definition of several phases to interpret a photosignal.

For the first read-out step, the first transfer gate is controlled to provide a charge threshold for photoelectrons generated in the pinned photodiode. The charge threshold defines a saturation level and corresponds to an amount of photoelectrons for a low-light signal read-out. The second transfer transistor is controlled to be conductive, thereby merging the sense node with the intermediate node coupled with the gain reducing capacitor. Under low-light condition, the generated photoelectrons remain in the photodiode since the photodiode charge remains below the saturation level of the first transfer transistor, i.e. below the charge threshold formed thereby. Under high-dynamic conditions, photoelectrons are generated in the photodiode above saturation level, so that the generated photoelectrons overflow the charge threshold formed by the first transfer transistor into the merged intermediate and sense nodes which have been reset to a higher potential and lowers the node potential. The sense node then can be read out to obtain a first sampling output.

In a second read-out step for reading out a low-light signal, the generated photoelectrons cannot pass the potential barrier of the first transfer transistor so that in a second read-out step, the photoelectron charge stored within the photodiode needs to be measured.

The second read-out step requires a preparation of the sense node for the read-out of the low-light signal. This includes that the sense node is firstly isolated from the intermediate node by controlling the second transfer transistor to be opened (herein understood as making non-conductive) and that the intermediate node potential is reset to a level between the potential of the photodiode and the reset level of the sense node which has been reset before. Then, the second transfer transistor is controlled to adapt its charge threshold (saturation level) to be equal or slightly higher than the intermediate node potential. In this configuration, the sense node is still isolated from the intermediate node so that a reference potential of the sense node can be read out as a second sampling output.

In a third read-out step, the first transfer transistor is controlled to lower the threshold to a voltage between the pin voltage of the photodiode and the present intermediate node potential. The photoelectrons are then transferred directly to the sense node and reduce its node potential. The third sampling output can then be read out and differentiated with the reset sampling output taken before.

This multi-step read-out scheme allows a read-out for two different dynamic ranges, firstly a high-dynamic range and secondly a low-light range. The read-out steps came along with different conversion gains so that a wide dynamic range can be achieved by maintaining a low noise read-out for the low-light signal.

Furthermore, a reset transistor may be provided which is configured to receive a reset signal and to selectively couple a supplied reset voltage to the intermediate node.

According to an embodiment, a control unit may be provided to control operation of the pixel sensor cell by timely providing the first and second control signal.

Furthermore, the output buffer may be formed with a selectable source follower.

Regarding the method, a cell output may be determined depending on the LLS sampling output signal and the HDS sampling output signal.

It may be provided that after the first phase a first reset potential is loaded on the sense node and a second reset potential V_{RST2} which is in a range between a pin voltage V_{pin} of the photodiode 11 and the first reset potential.

After resetting the sense node and after the threshold of the second transfer transistor has been set to a potential where the second transfer transistor isolates the intermediate node and the sense node and which is substantially equal or higher than the potential of the intermediate node, a reference sampling output signal is read out, wherein the cell output is further determined depending on the reference sampling output signal.

Particularly, after reading out the potential on the sense node as an LLS sampling output signal, the second transfer transistor is controlled to electrically merge the intermediate node and the sense node, the intermediate and sense nodes are reset onto the first reset potential.

According to a further aspect, a CMOS image sensor including an array of multiple pixel sensor cells as described above is provided.

Brief description of the drawings

Embodiments are described in more detail in conjunction with the accompanying drawings in which:

Figure 1 shows a schematic of the pixel sensor cell;

Figure 2 a flowchart for illustrating the operating method for the pixel sensor cell of Figure 1;

Figure 3 shows a timing diagram of signals to control the operation of the pixel sensor cell of Figure 1;

Figures 4a to 4f show potential levels for the photoelectrons' path from the photodiode to the sense node during the read-out steps;

Figure 5 shows a diagram illustrating the conversion gate with two linear ranges; and

Figure 6 shows a block diagram of a low-noise, high-dynamic CMOS image sensor including the pixel sensor cells of Figure 1.

Description of embodiments

Figure 1 depicts a schematic of a pixel sensor cell 1 that has an increased dynamic range and a reduced read-out noise.

As shown in the exemplary circuit of Figure 1, there is a pinned photodiode 11 substantially formed by a reversely coupled pn junction, a ground terminal 11a of which is connected to a ground potential V_{GND} and a pin terminal 11b is coupled with a source terminal 12S of a first transfer transistor 12. A gate terminal 12G of the first transfer transistor 12 is applied with a first control signal TX_1 , and a drain terminal 12D is coupled to an intermediate node IN.

The intermediate node IN is coupled with a gain reducing capacitance C_{HD} which may be explicitly or intrinsically formed e.g. by an n+p junction layer. The intermediate node IN is further coupled with a source terminal 13S of a reset transistor 13. A drain terminal 13D of the reset transistor 13 is supplied by a reset voltage V_{RST} . The gate terminal 13G of the reset transistor 13 is coupled with a supplied reset signal RST.

The intermediate node IN is further coupled with a source terminal 14S of a second transfer transistor 14, while a drain terminal 14D of the second transfer transistor 14 is coupled with a sense node SN. The gate terminal 14G of the second transfer transistor 14 is supplied with a second control signal TX_2 .

Furthermore, the sense node SN is coupled with a read-out buffer 15 which is formed in the present embodiment by a selectable (can be enabled and disabled) source follower. The selectable source follower of the read-out buffer 15 may comprise a source follower transistor 16 and a row selection transistor 17 which may be controlled by a row select signal RS to enable the source follower. A drain terminal 16D of the source follower transistor 16 is coupled with a high supply potential VDD, while the source terminal 16S of the source follower transistor 16 is coupled with a drain terminal 17D of the selection transistor 17, while the source terminal 17S of the selection transistor 17 is coupled with an

output node ON for obtaining sampling outputs. The gate terminal 16G of the source follower transistor 16 is connected with the sense node SN.

The control signals TX_1 , TX_2 , RST, RS as well as the reset potential V_{RST} are provided by a control unit 20 which controls the read-out operation of the pixel sensor cell 1. The control unit 20 controls the operation of the pixel sensor cell 1 to obtain sampling outputs at the sampling node ON.

The operation of the pixel sensor cell 10 is described in detail with respect to the flowchart of Figure 2, the timing diagram of Figure 3 and the potential levels in the photoelectron's path of Figures 4a to 4f.

Initially, the intermediate node IN and the sense node SN had been reset to a well-defined potential. So, the potential of the intermediate and sense nodes IN, SN corresponds substantially to the reset potential V_{RST} .

In a step S1 which is also illustrated in Figure 4a, a threshold $TX1L$ (potential barrier) of the first transfer transistor 12 is set. This is achieved by setting the first control signal TX_1 to a low voltage that blocks charge flow from the photodiode 11 and allows filling the photodiode 11 with an amount of photoelectrons (pin potential V_{pin}) below the saturation level. In other words, the first transfer transistor 12 is controlled that it forms a potential barrier which isolates the photodiode 11 from the merged intermediate and sense nodes IN, SN when photoelectrons are generated in the photodiode 11. The charge threshold defined by the control of the first transfer transistor 12 by means of the first control signal TX_1 defines a saturation level of a low-light signal.

In step S2, the second transfer transistor 14 is made conductive, so that the intermediate node IN and the sense node SN are coupled/merged. This is achieved by setting the second control signal TX_2 to the highest voltage attracting electrons in the channel area of the second transfer transistor 14 and making the threshold level V_{TX2H} very low.

Under low light conditions, the integrated photoelectrons corresponding to (resulting from) the Low Light Signal (LLS) remain stored in the photodiode 11 as charge generation is too slow for the potential of the photodiode 11 to reach the saturation level. In other words, the gate voltage (of the first control signal TX_1) applied on the first transfer transistor 12 is set

to a potential where it prevents the photoelectrons to flow to the intermediate node IN as long as the accumulated charge in the photodiode 11 has not reached a saturation level defined by the potential of the first control signal TX₁.

Under high-light conditions, more photoelectrons are generated during integration time so that the charge in the photodiode 11 overflows as it reaches the saturation level and a part (the overflow) of the generated photoelectrons may pass through the first transfer transistor 12 to the higher potential of the intermediate node IN and the sense node SN which are merged via the conductive second transfer transistor 14.

In a step S3, the sense node SN potential is read-out by means of the output buffer 15 as a first sampling output signal V_{HDS}, when the row select signal RS activates the output buffer 15. The potential at the sense node SN results from the charge of the photoelectrons which could pass over the saturation level formed by the control of the first transfer transistor 12 in case of high-light conditions. Under low-light conditions, the first sampling output signal V_{HDS} has a potential associated with the reset potential on the sense node SN indicating the low light condition.

The high dynamic capacitance formed by the gain reducing capacitance C_{HD} is allowed for high light conditions as the shot noise dominates the read noise. Further a large capacitance is beneficial to ensure a high saturation level which is obtained by merging the gain reducing capacitor C_{HD} with the MOSFET capacitor of the second transfer transistor 14 and the sense node SN. In low light condition, the photodiode 11 is not completely filled with photoelectrons, and the integrated charge remains in the photodiode 11. In this case, the read noise is the dominating noise source, and a small capacitance at the sense node SN is required.

After the HDS sampling output signal V_{HDS} has been obtained, a second phase starts in case the light signal is a low light signal so that the amount of remaining charge carriers in the photodiode 11 has to be determined.

In step S4, as also shown in Figure 4b, by applying of the reset signal RST (high level) on the reset transistor 13 a first reset potential V_{RST1} is loaded on the merged intermediate node IN and sense node SN, so that the sense node SN has a predefined potential V_{RST1}.

After resetting the electrically merged intermediate and sense nodes IN, SN to the first reset potential V_{RST1} , in a next step S5, the sense node SN is isolated from the intermediate node IN by controlling the second transfer transistor 14 so that it forms a high threshold (high potential barrier) V_{TX2L} . The threshold V_{TX2L} is selected so that the intermediate node IN when charged with the photoelectrons of the photodiode 11 remains in the intermediate node IN as shown in Figure 4c. Substantially, the second control voltage TX_2 is therefore set to its lowest voltage level $TX2L$.

In step S6, the reset voltage V_{RST} is then set to a second reset potential V_{RST2} which is in a range between the pin voltage V_{pin} of the photodiode 11 and the stored first reset potential V_{RST1} of the sense node SN. The pin voltage V_{pin} of the photodiode 11 corresponds to a built-in potential like the one of a simple pn junction diode. The pin voltage V_{pin} is the voltage inside the photodiode 11 when it is completely emptied from electrons. It ranges between 0.6 and 1V and depends on the technology process.

After resetting, the reset transistor 13 is switched off in order to sample the achieved potential level at the intermediate node IN as shown in Figure 4d. The reset potentials in the intermediate node IN and sense node SN are set to be not equal to ensure that the two nodes are not electrically merged. In case of equal node potentials, the total capacitance of the sense node SN will be the sum of the capacitances of the two nodes SN, IN. With differing reset potentials in the nodes IN, SN the sense node capacitance can be kept as low as possible.

In step S7, the second control signal TX_2 is set to a potential $TX2I$ that makes the potential in the channel of the second transfer transistor 14 equal or slightly higher than the potential of the intermediate node IN as shown in Figure 4e. In this switching state, the potential of the intermediate node IN is still isolated from the sense node SN so that the higher charge V_{RST2} of the intermediate node IM can be prevented to flow to the sense node SN even before the first transfer transistor 12 is fully closed. Any charge leaking from the sense node SN during this step just changes slightly the voltage of the sense node SN from V_{RST1} to a slightly lower value $V1$. This does not affect the signal because the latter corresponds to the difference between that value $V1$ and the sense node voltage after the TX_1 is clocked high to remove the barrier between the photodiode 11 and the other nodes IN, SN. Also, by a simple calibration it is possible to obtain the exact voltage to apply on the TX_2 to have the voltage in the channel of the second transfer transistor 14 exactly equal to V_{RST2} .

In step S8, the potential of the sense node SN can be read out as a reference sampling output signal V_{Ref} which serves as a reference for analyzing a LLS sampling output V_{LLS} .

In a step S9, the first control signal TX_1 is controlled so that the threshold between the photodiode 11 and the intermediate node IN is lowered to a level between the pin voltage V_{pin} of the photodiode 11 and the potential of the intermediate node IN. The photoelectrons accumulated in the photodiode 11 transfer directly to the sense node SN and reduce its voltage as shown in Figure 4f. Substantially, this is achieved by increasing the potential of the first control signal TX_1 to TX_{1H} to a level that set the voltage in the channel to a value between the pin voltage V_{pin} of the photodiode 11 and the potential of the intermediate node IN. The photogenerated charges accumulated in the photodiode 11 transfer directly to sense node SN and reduce its voltage.

In step S10, the LLS sampling output signal V_{LLS} can be read-out.

In step S11, the pixel sensor cell 1 is reset by controlling the second transfer transistor 14 to electrically merge the intermediate node IN and the sense node SN, set the reset voltage V_{RST} to the first reset potential V_{RST1} and apply the reset signal RST to bring the intermediate and sense nodes IN, SN onto the first reset potential V_{RST1} to set the initial condition.

Hence, three sampling outputs, namely the HDS sampling output signal V_{HDS} , the reference sampling output signal V_{RST} , and the LLS sampling output signal V_{LLS} , can be obtained at the end of each read-out process. The HDS sampling output signal V_{HDS} corresponds to the high dynamic condition signal, the reference sampling output signal V_{ref} corresponds to the reset level and the LLS sampling output signal V_{LLS} corresponds to a low-light condition signal.

In step S12, the overall cell output can now be determined by the sum of the two components as

$$V_{out} = (V_{HDS} - V_{ref}) + \frac{A_{CD,HD}}{A_{CD,LL}} (V_{LLS} - V_{ref})$$

where $A_{CG,HD}$ and $A_{CG,LL}$ correspond to the pixel conversion gains for the high dynamic signal and low-light signal read-outs, respectively. The conversion gain is generally determined by

$$A_{CG} = \frac{\frac{1}{n}}{C_{SN} - \frac{2}{3n} C_{ox} WL}$$

wherein n is the slope factor of the read-out buffer 15, C_{SN} the sense node capacitance C_{ox} is the oxide capacitance per unit area, and W and L are its gate width and length (of the source follower transistor 16). As shown in the diagram of Figure 5, the sense node capacitance C_{SN} is much smaller during the low-light signal read-out so that $A_{CG,LL}$ is much larger than $A_{CG,HD}$.

The overall cell output is a representation of the amount of light detected by the pixel sensor cell 1 and can be further processed.

Figure 6 shows a configuration of a CMOS image sensor 100, having a plurality of pixel sensor cells 1 arranged in an array. The pixel sensor cells 1 are arranged in rows wherein each row is addressed by its first and second control signals $TX_{1\_1...n}$, $TX_{2\_1...n}$, reset signal $RST_{1...n}$ and row select signal $RS_{1...n}$, while each one of the pixel sensor cells 1 of each row have coupled its output nodes ON with a respective column line $CL_{1..m}$. A column line is coupled with a column level amplifier and the multiple sampling and ADC unit.

Claims

1. Pixel sensor cell (1) for a CMOS sensor device comprising:
 - a photodiode (11) for generating photoelectrons;
 - a first transfer transistor (12) coupling the photodiode (11) with an intermediate node (IN) and configured to be controlled by a first control signal (TX_1);
 - a gain reducing capacitance (C_{HD}) applied on the intermediate node (IN);
 - a second transfer transistor (14) coupling the intermediate node (IN) with a sense node (SN) and configured to be controlled by a second control signal (TX_2);
 - an output buffer (15) coupled with the sense node (SN) and configured to amplify a potential on the sense node (SN).
2. Pixel sensor cell (1) according to claim 1, wherein a reset transistor (13) is provided which is configured to receive a reset signal (RST) and to selectively couple a supplied reset voltage to the intermediate node (IN).
3. Pixel sensor cell (1) according to claim 1 or 2, wherein the intermediate node (IN) is provided with a gain reducing capacitance (C_{HD}) which particularly is formed as a p+n junction.
4. Pixel sensor cell (1) according to any of the preceding claims, wherein a control unit (20) is provided to control operation of the pixel sensor cell (1) by timely providing the first and second control signal (TX_1 , TX_2).
5. Pixel sensor cell (1) according to any of the preceding claims, wherein the photodiode (11) is formed as a pinned photodiode.
6. Pixel sensor cell (1) according to any of the preceding claims, wherein the transistors (12, 13, 14, 16, 17) are formed as MOSFET transistors.

7. Pixel sensor cell (1) according to any of the preceding claims, wherein the output buffer (15) is formed with a selectable source follower.
8. Method for operating a pixel sensor cell (1) according to any of the claims 1 to 7, comprising the steps of:
 - accumulating photoelectrons in the photodiode (11) during a predetermined integration time.
 - in a first phase, coupling the intermediate node (IN) with the sense node (SN) by means of the second transfer transistor (14) and providing a charge threshold for accumulated photoelectrons so that only excess photoelectrons are allowed to pass to the intermediate node (IN), wherein the potential generated by the excess photoelectrons is read out as an HDS sampling output signal (V_{HDS});
 - in a second phase, controlling the second transfer transistor (14) to set a threshold of the second transfer transistor to a potential where the second transfer transistor (14) isolates the intermediate node (IN) and the sense node (SN) and which is substantially equal or higher than the potential of the intermediate node (IN), coupling the intermediate node (IN) with the sense node (SN) and reading out the potential on the sense node (SN) as an LLS sampling output signal (V_{LLS}).
9. Method according to claim 8, wherein a cell output is determined depending on the LLS sampling output signal (V_{LLS}) and the HDS sampling output signal (V_{HDS}).
10. Method according to claim 9, wherein after the first phase a first reset potential ($VRST1$) is loaded on the sense node (SN) and a second reset potential V_{RST2} which is in a range between a pin voltage V_{pin} of the photodiode 11 and the first reset potential ($VRST1$).
11. Method according to claim 10, wherein after resetting the sense node (SN) and after the threshold of the second transfer transistor (14) has been set to a potential where the second transfer transistor (14) isolates the intermediate node (IN) and the sense node (SN) and which is substantially equal or higher than the potential of the intermediate node (IN), reading out a reference sampling output signal,

wherein the cell output is further determined depending on the reference sampling output signal.

12. Method according to claim 10 or 11, wherein after reading out the potential on the sense node (SN) as a LLS sampling output signal (V_{LLS}), the second transfer transistor (14) is controlled to electrically merge the intermediate node (IN) and the sense node (SN), reset the intermediate and sense nodes (IN, SN) onto the first reset potential (V_{RST1}).
13. CMOS image sensor (100) including an array of multiple pixel sensor cells (1) according to any of the claims 1 to 7.

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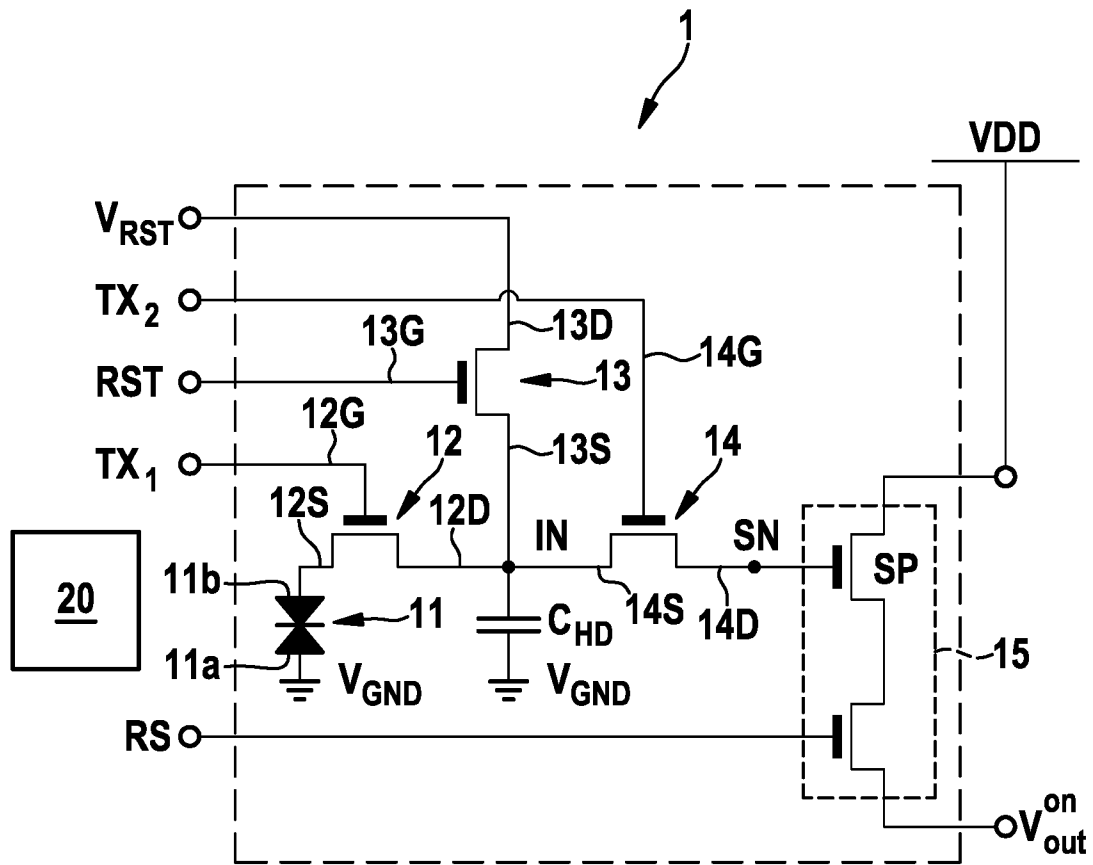


Fig. 1

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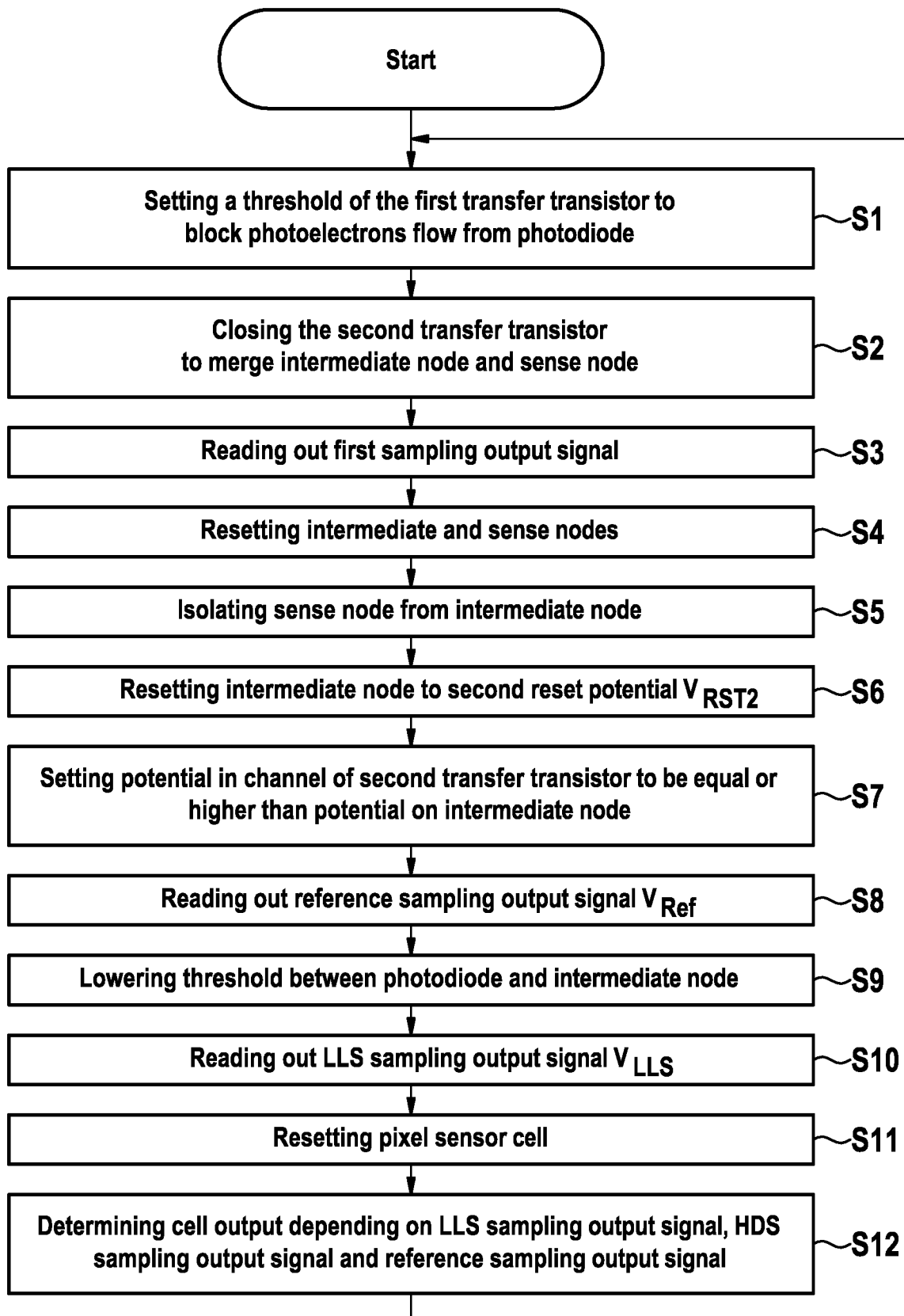


Fig. 2

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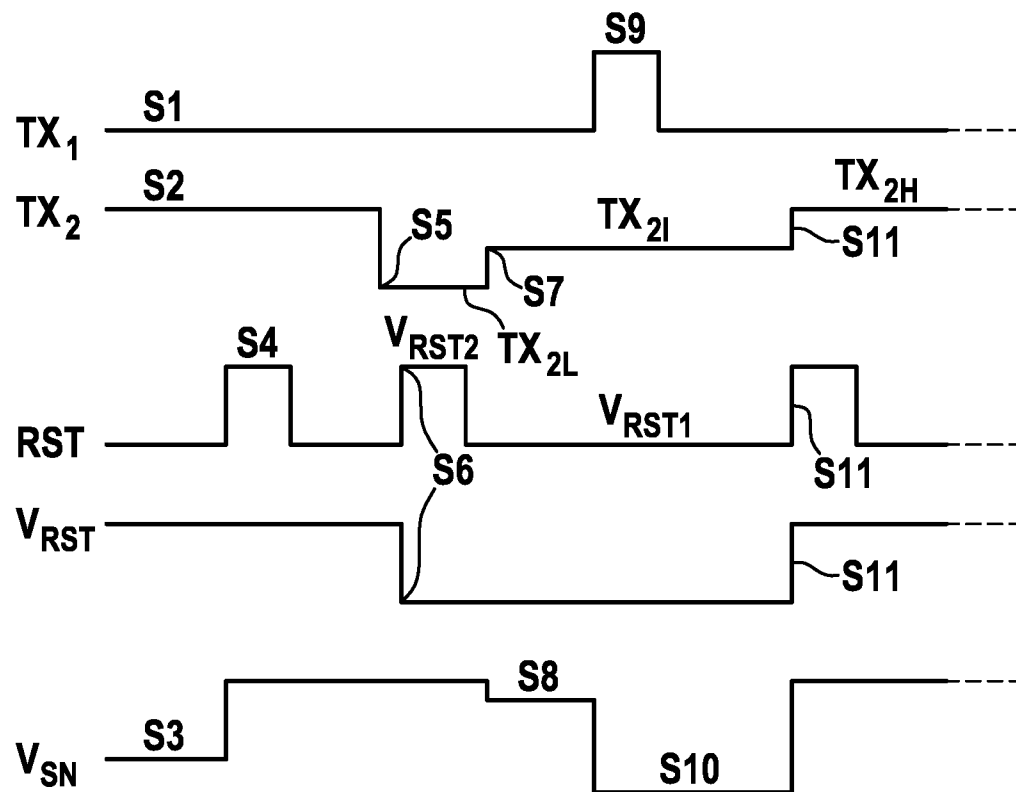


Fig. 3

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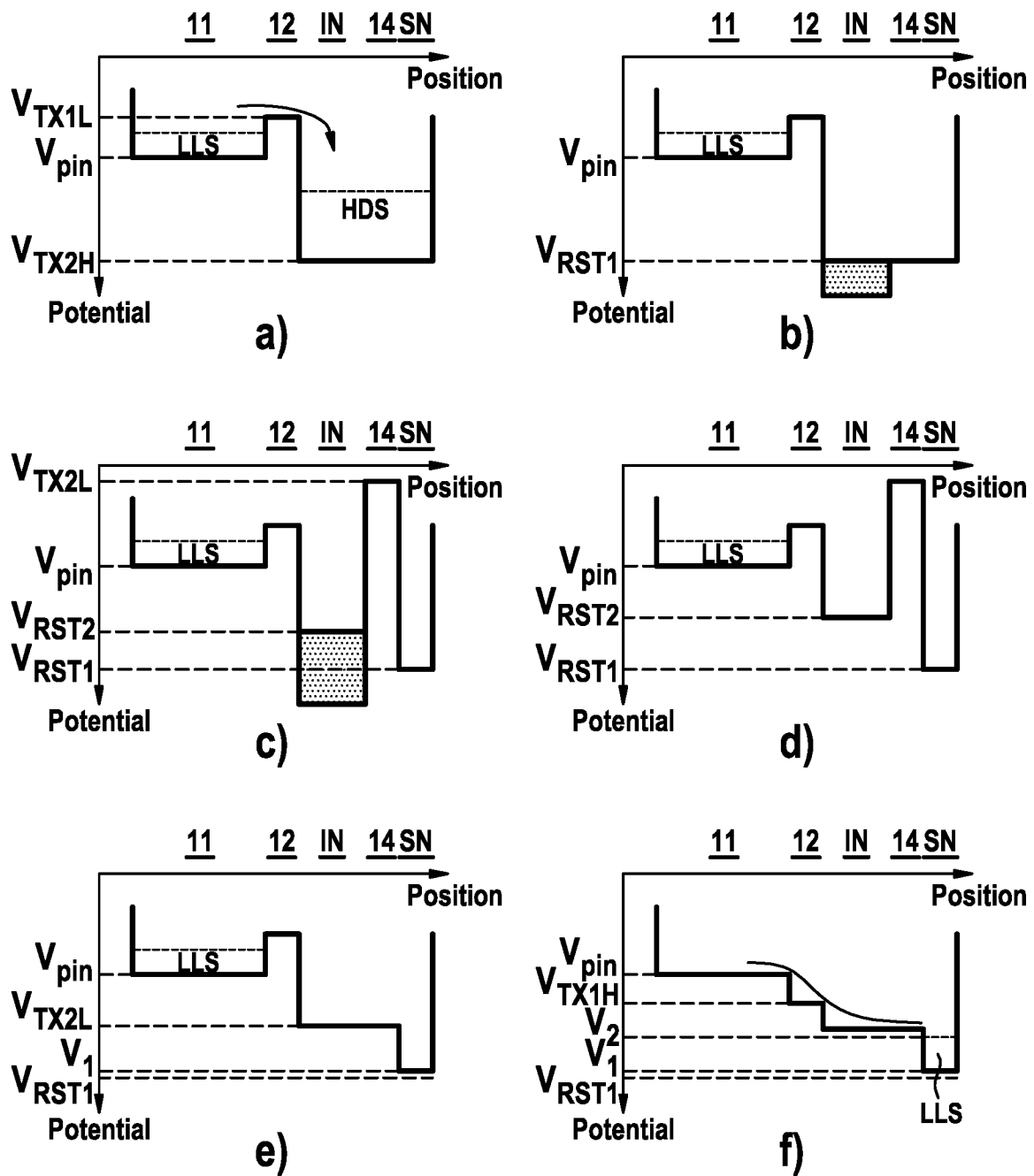


Fig. 4

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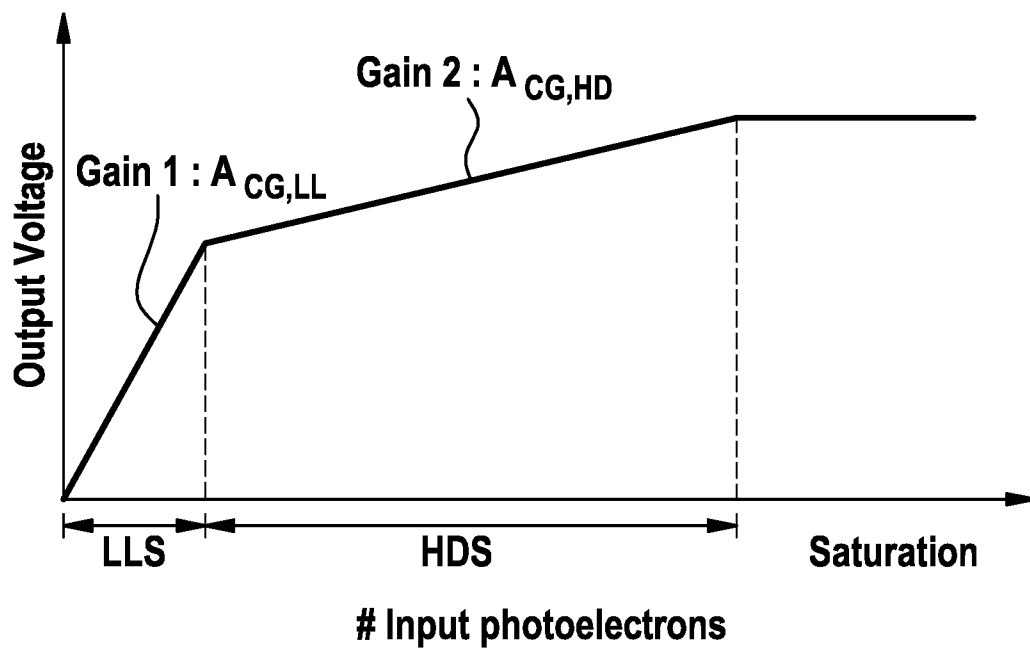


Fig. 5

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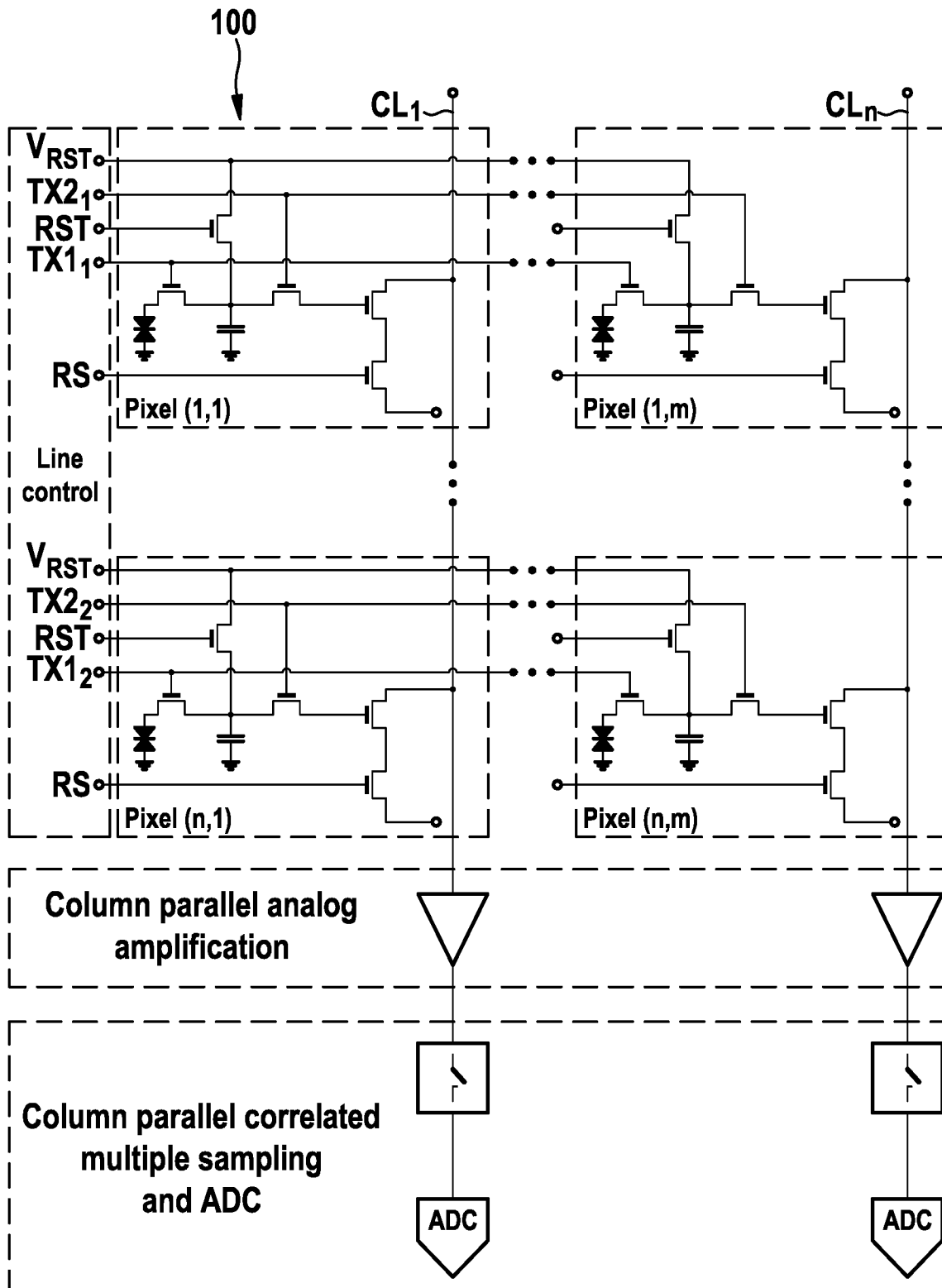


Fig. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/079751

A. CLASSIFICATION OF SUBJECT MATTER
INV. H04N5/355
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2006/124346 A1 (ALEXANDER KRYMSKI [US]) 23 November 2006 (2006-11-23)	1-7,13
Y	paragraph [0004] - paragraph [0005];	8-10
A	figure 1 paragraph [0023] - paragraph [0027]; figure 4	11,12

X	US 2006/219868 A1 (MORIMOTO TAKASHI [JP] ET AL) 5 October 2006 (2006-10-05)	1-7,13
Y	paragraph [0031] - paragraph [0032];	8-10
A	figure 1 paragraph [0037] - paragraph [0041]; figure 2	11,12

X	EP 2 919 457 A1 (CANON KK [JP]) 16 September 2015 (2015-09-16)	1-7,13
Y	paragraph [0021] - paragraph [0026];	8-10
A	figures 1,2	11,12

	-/--	



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

16 July 2018

Date of mailing of the international search report

23/07/2018

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INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2017/079751

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	A K KALGI ET AL: "Four Concepts for Synchronous, PSN limited, true CDS, HDR imaging", FOUR CONCEPTS FOR SYNCHRONOUS, PSN LIMITED, TRUE CDS, HDR IMAGING, 11 June 2015 (2015-06-11), XP055492432, cited in the application page 1, paragraph 1 - page 2, paragraph 11; figure 3 -----	8-10
Y	US 2016/148962 A1 (DUPONT BENOIT [BE]) 26 May 2016 (2016-05-26) paragraph [0058] - paragraph [0068]; figures 1-2 -----	8-10

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/EP2017/079751

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US 2016148962 A1	26-05-2016	NONE	