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(54) **DOUBLE-MASKING TECHNIQUE FOR INCREASING FABRICATION YIELD IN SUPERCONDUCTING ELECTRONICS**

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(57)   **ABSTRACT**

An improved microfabrication technique for Josephson junctions in superconducting integrated circuits, based on the use of a double-layer lithographic mask for partial anodization of the side-walls and base electrode of the junctions. The top layer of the mask is a resist material, and the bottom layer is a dielectric material chosen so to maximize adhesion between the resist and the underlying superconducting layer, be etch-compatible with the underlying superconducting layer, and be insoluble in the resist and anodization processing chemistries. The superconductor is preferably niobium, under a silicon dioxide layer, with a conventional photoresist or electron-beam resist as the top layer. This combination results in a substantial increase in the fabrication yield of high-density superconducting integrated circuits, increase in junction uniformity and reduction in defect density. A dry etch more compatible with microlithography may be employed.

Figure 1

SiO2

Nb

AlOx

Al

Nb

Figure 2

Figure 3

Photoresist

SiO2

Nb

AlOx

Al

Nb

Figure 4

Photoresist

SiO2

Nb

AlOx

Al

Nb

Figure 5

See Cross
Section of
Figure 6B

Photoresist

SiO2
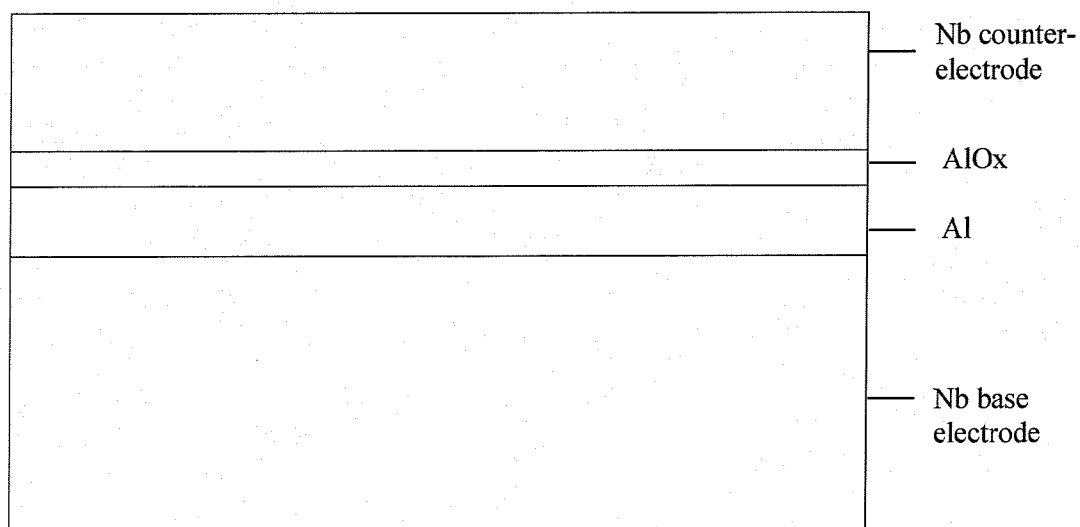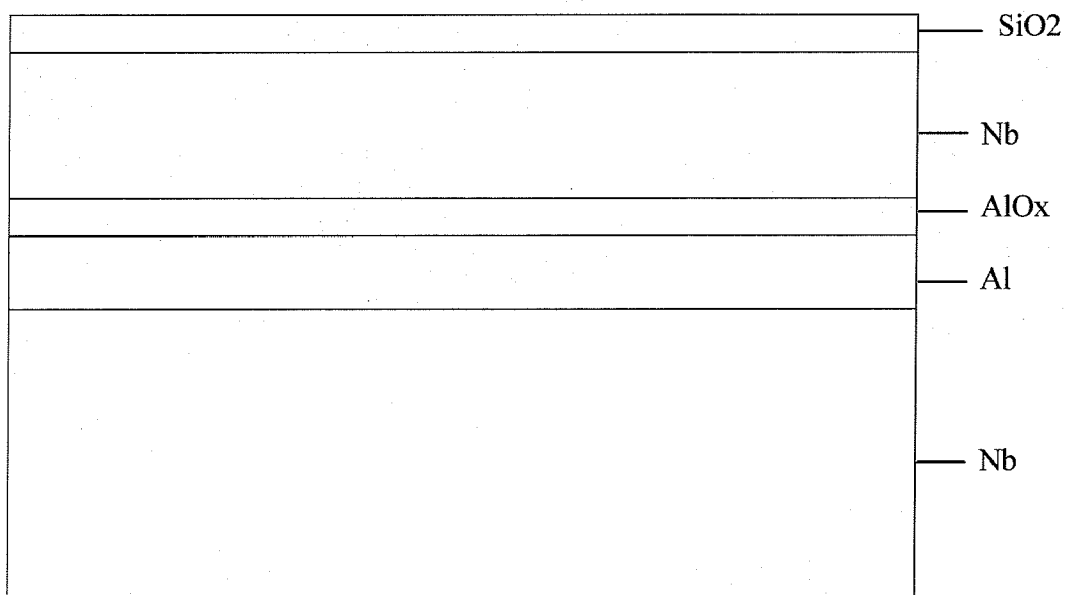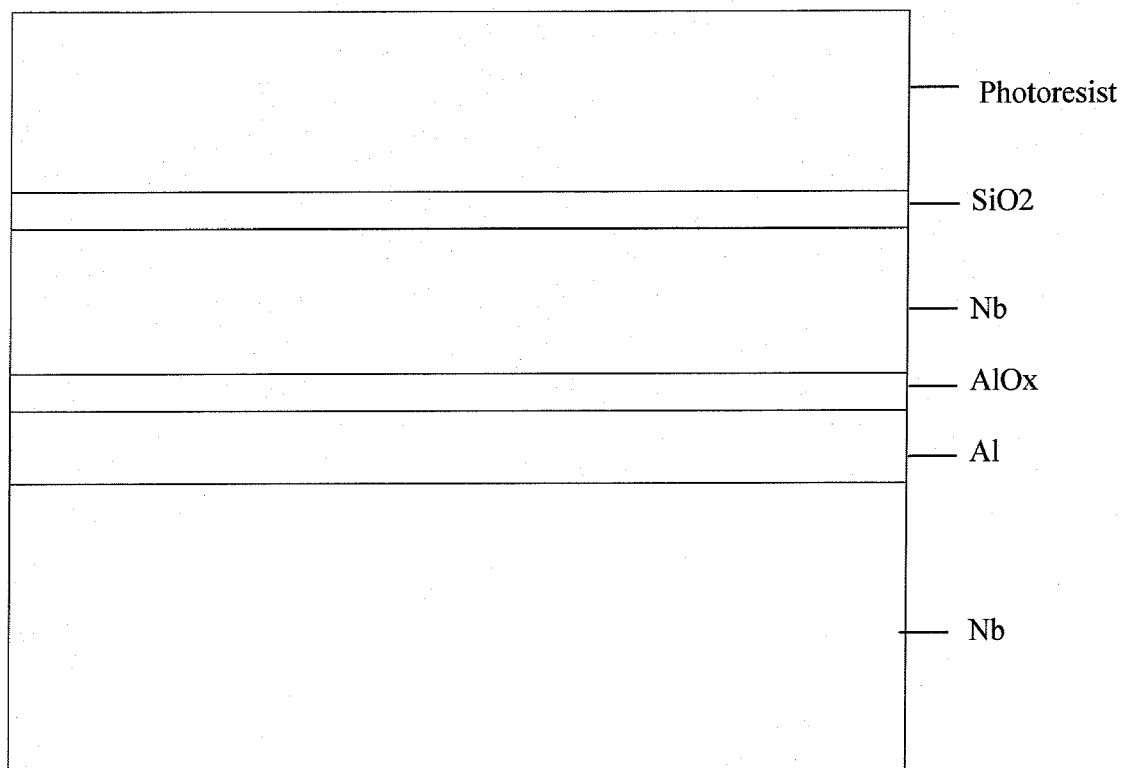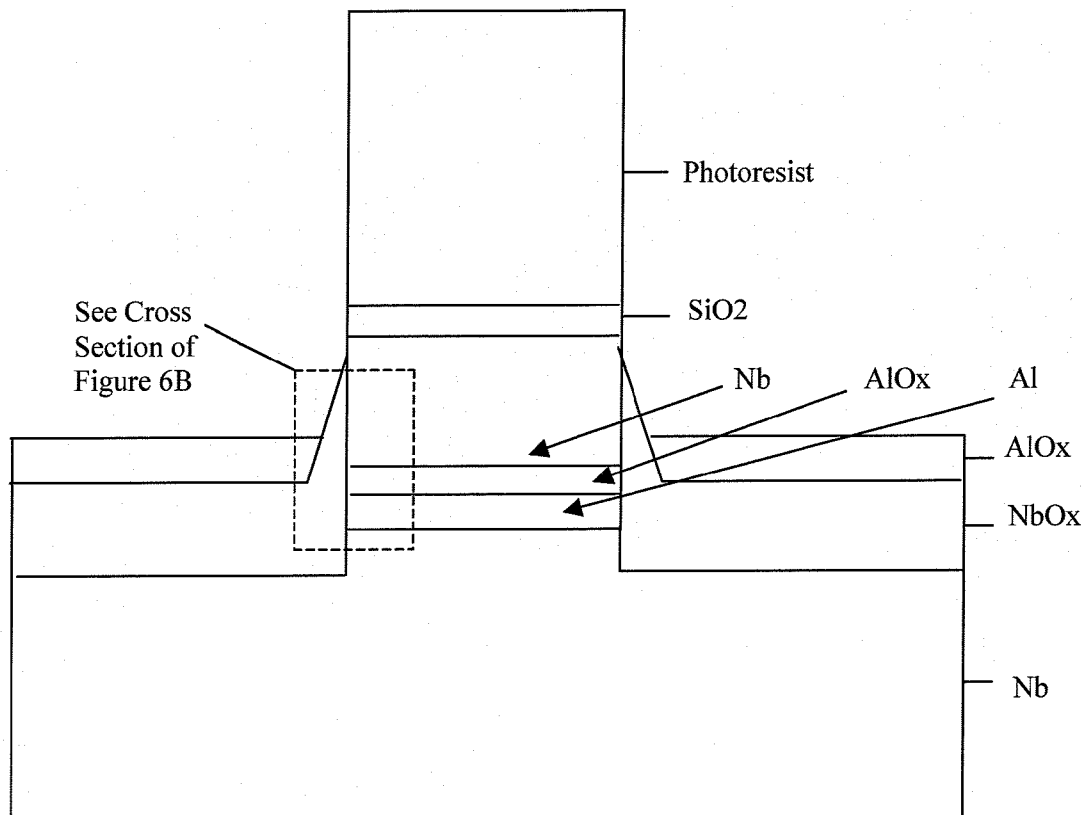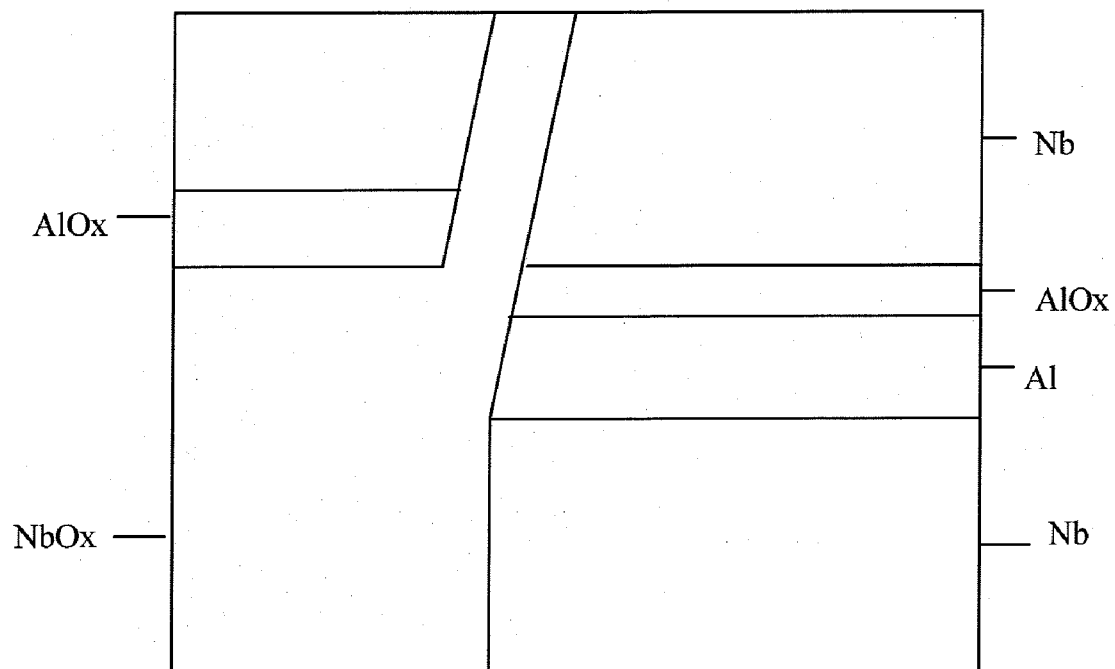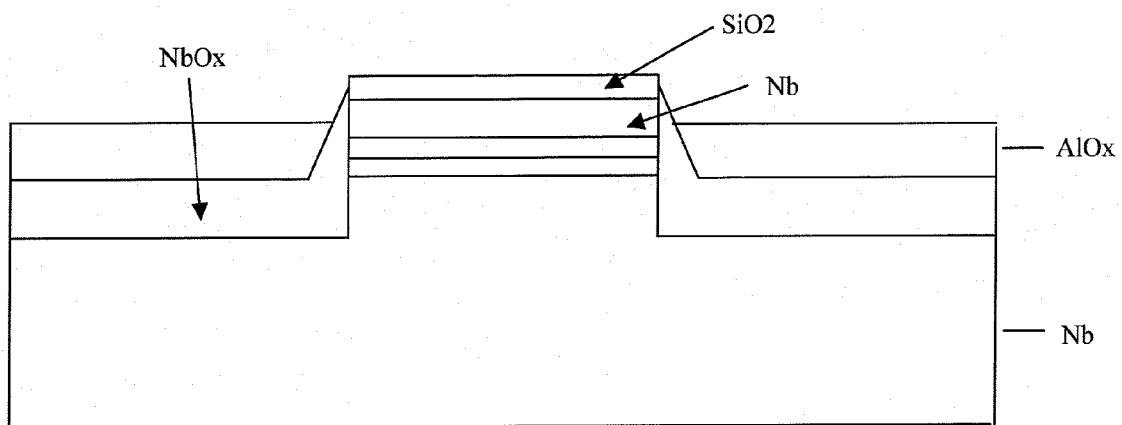
Nb   AlOx   Al

AlOx

NbOx

Nb

Figure 6A

AlOx

Nb

AlOx

Al

NbOx

Nb

Figure 6B

Figure 7

Figure 8

Figure 9

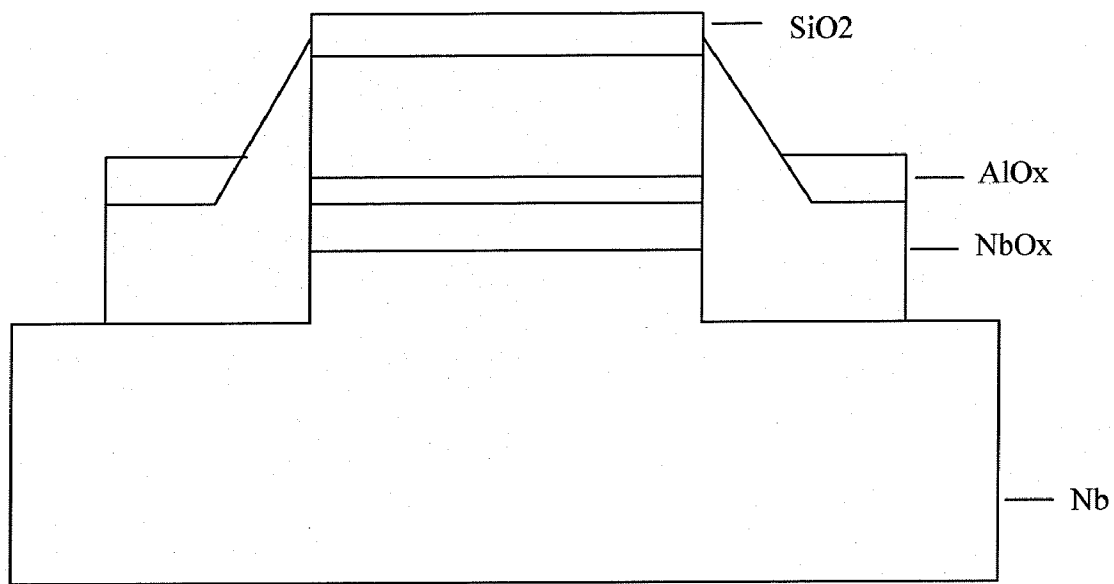SiO2

AlOx

NbOx

Nb

Figure 10

—— SiO2

—— Nb

Figure 11
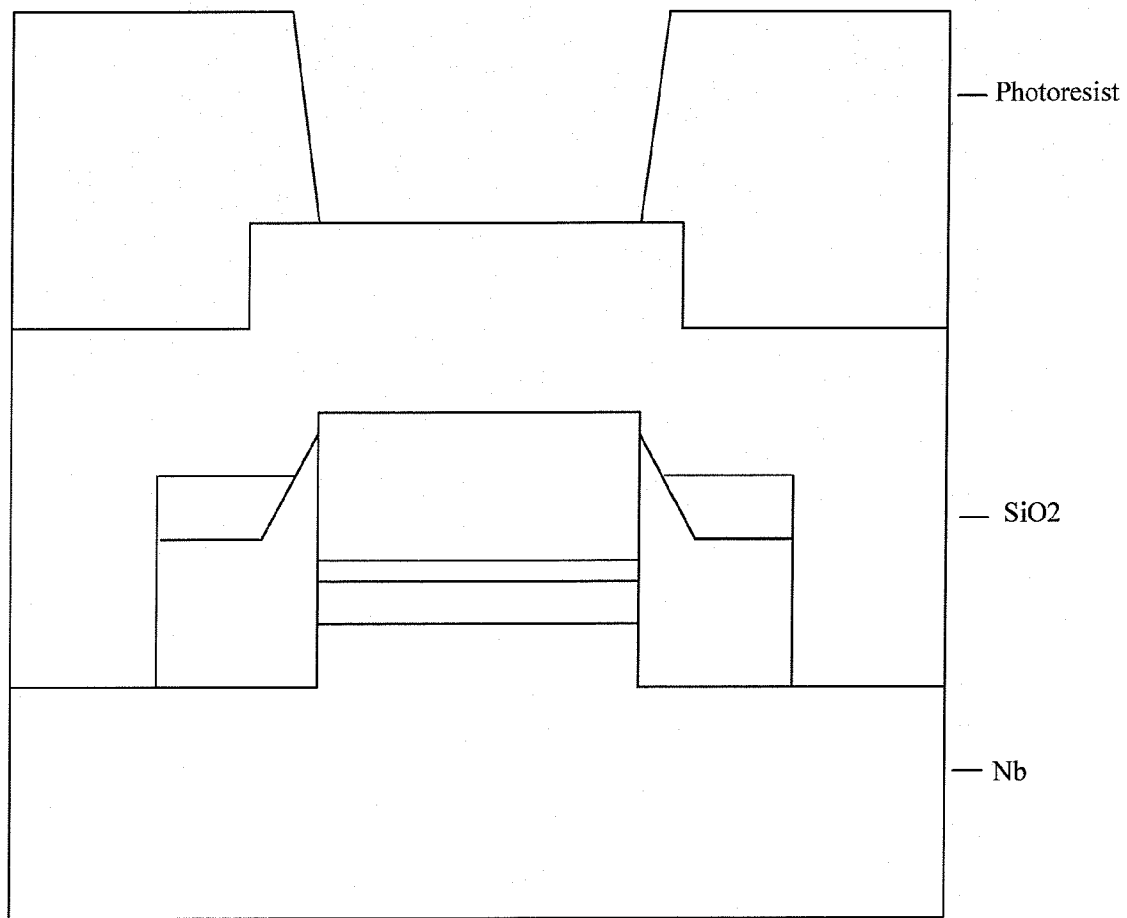
— Photoresist

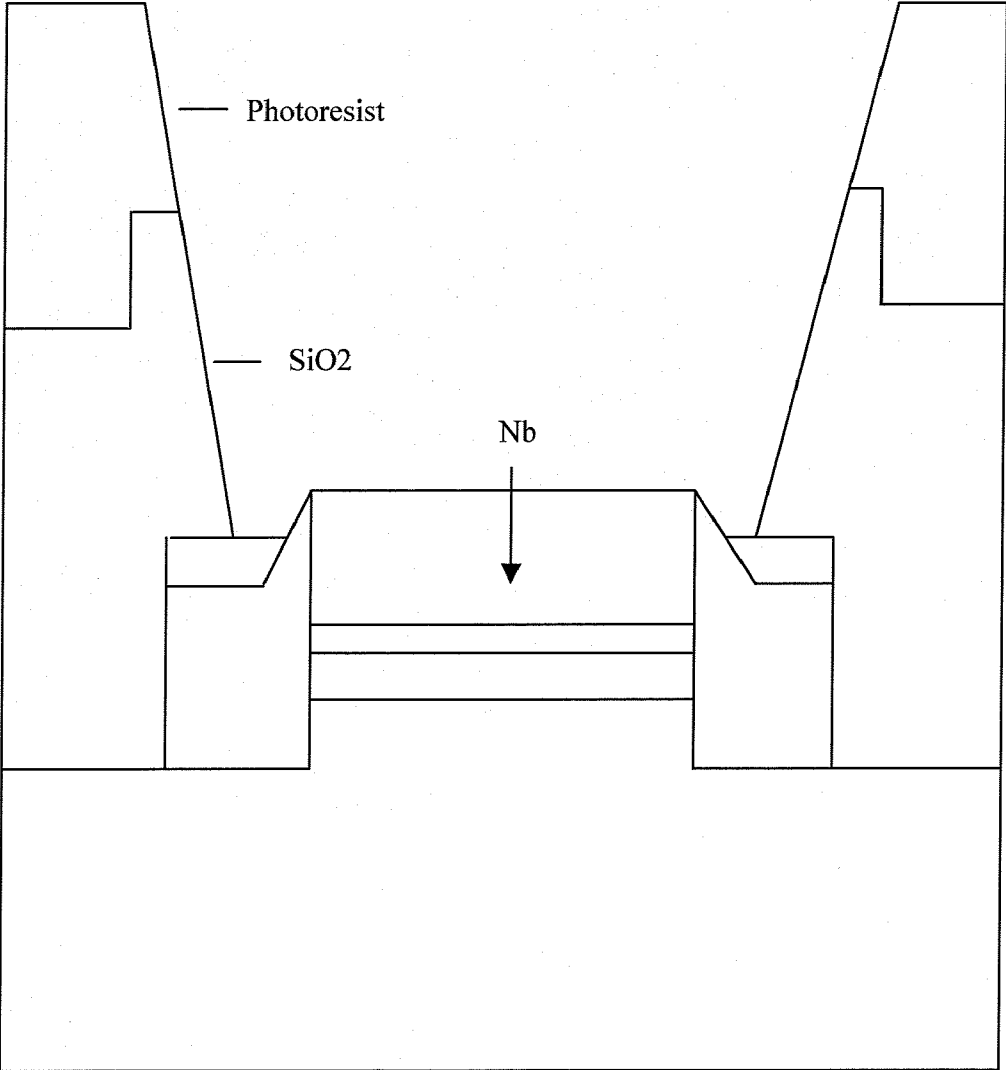— SiO2

— Nb

Figure 12

Photoresist
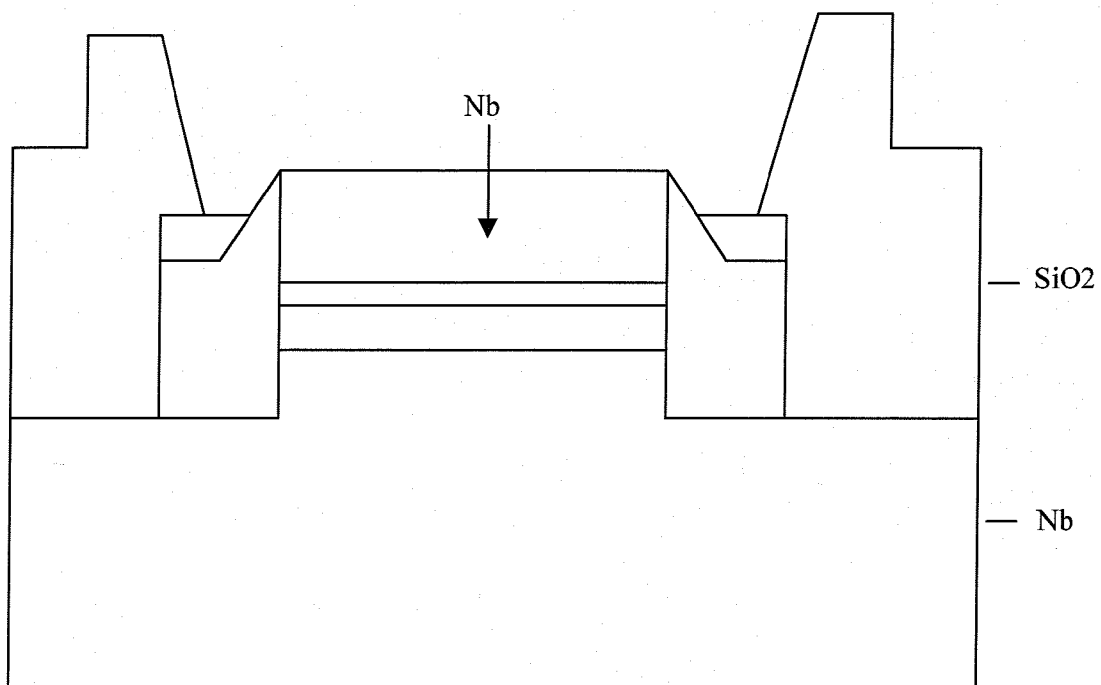
SiO2

Nb
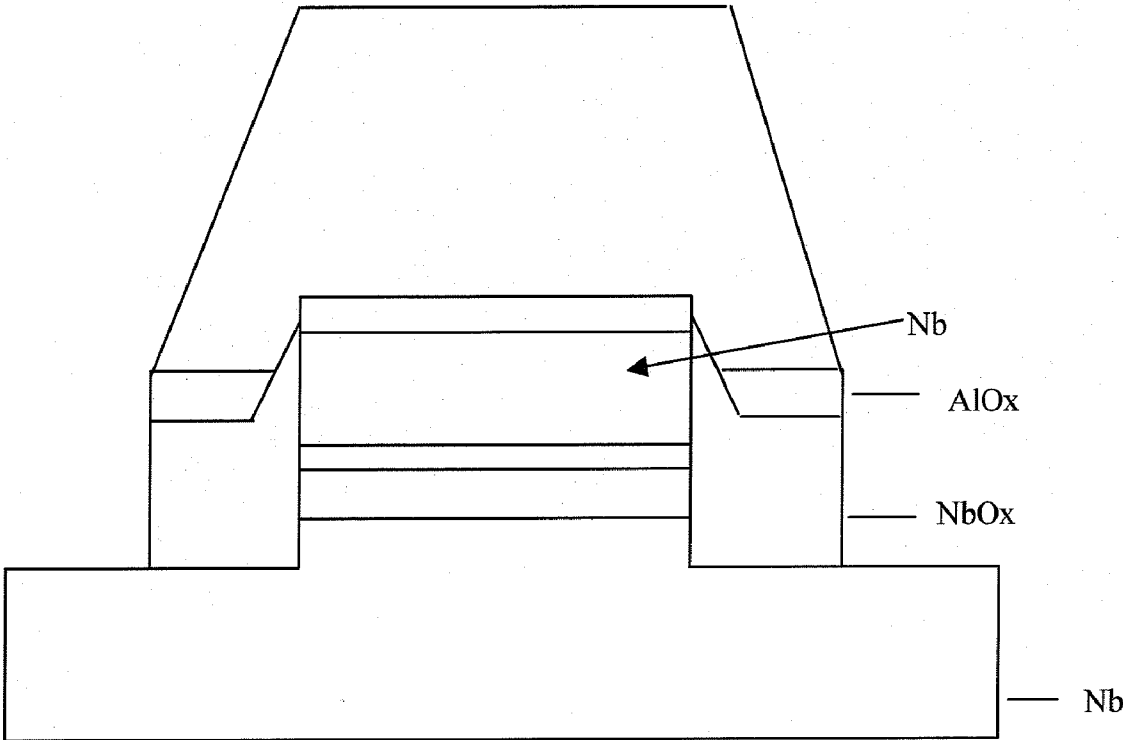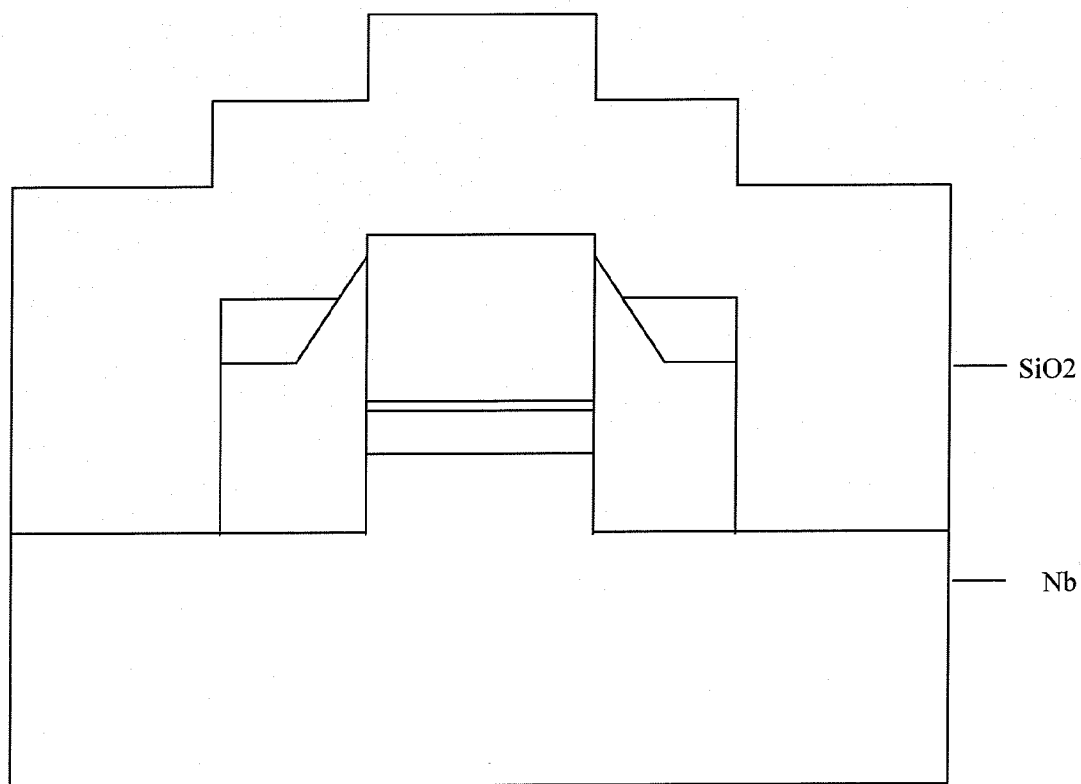
Figure 13

Figure 14

DOUBLE-MASKING TECHNIQUE FOR INCREASING FABRICATION YIELD IN SUPERCONDUCTING ELECTRONICS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation/Division of Ser. No. 11/616,382, filed Dec. 27, 2006, which is expressly incorporated herein by reference. This application is related to and claims priority to Provisional Application 60/826,262 filed Sep. 20, 2006 by inventor Sergey K. Tolpygo entitled A Double-Masking Technique for Increasing Fabrication Yield and Josephson Junction Quality in Superconducting Electronics, the contents of which are incorporated herein by reference in its entirety.

STATEMENT OF GOVERNMENT RIGHTS

[0002] This invention was developed in part under contract number N0014-03-C-0370 from the Office of Naval Research.

BACKGROUND OF THE INVENTION

[0003] 1. Field of the Invention
[0004] The invention is directed to fabrication of electronic devices and more particularly to the fabrication of superconducting electronic devices such as Josephson junctions.
[0005] 2. Description of the Prior Art
[0006] Superconducting integrated circuits (ICs) based on Josephson junctions offer the possibility of operation at clock frequencies of 100 GHz or above. In order to achieve this on an industrial scale, it is necessary to decrease junction size toward submicron dimensions, and increase junction density, so that chips with many thousands of Josephson junctions can be reliably manufactured. The key parameter is the critical current I_c of a junction, which must be defined to within about 1% of design specifications, without defects.
[0007] The most reliable junction fabrication technology is based on the superconductor niobium (Nb), and in particular on a trilayer structure based on an ultrathin insulating "tunnel barrier" layer of aluminum oxide (AlO_x), 1-2 nm thick, sandwiched between two layers of Nb. This provides a precise critical current density of the junction $J_c=I_c/A$, where A is the junction area. If the microlithography defines A accurately, without damaging the tunnel barrier layer, then I_c is also accurately defined. This becomes increasingly difficult as the dimensions of the junction decrease. Applications of standard microlithography techniques may produce junctions with edge damage that can reduce junction quality and yield.
[0008] Current Nb IC technology also incorporates multiple layers of superconducting Nb wiring to bias and connect the Josephson junctions. This requires high-quality insulating layers between Nb layers, which are typically provided by silicon dioxide (SiO_2). SiO_2 is of course a standard material in semiconductor technology, and standard procedures for fabricating high-quality films are available.
[0009] An established technique in the prior art to improve junction yield is the use of selective anodization (Meng 2003, Kerber 2006). Anodization is an electrolytic process of surface oxidation that passivates all exposed Nb and Al surfaces, preventing damage in subsequent lithographic steps. However, this has not completely eliminated defects and related

yield problems. It is essential to solve these problems to advance to the next stage of circuit integration.

PROBLEMS OF THE PRIOR ART

[0010] As indicated above, the techniques of the prior art have resulted in a number of problems. Specifically, the techniques of the prior art have resulted in low yield, that is, a large number of junctions fabricated on a silicon based wafer fail for a variety of reasons. This results in a substantial percentage of defective junctions on each wafer.
[0011] Sometimes part of a junction will simply peel off the wafer upon which it is fabricated, due in part to local stresses that result from the anodization procedure. Further, the prior art does not allow precise control of critical current densities of a junction. Yet another problem stems from the fact that the standard process includes a wet-etching step to remove the anodized AlOx layer, which also limits device yield.

BRIEF SUMMARY OF THE INVENTION

[0012] Maintaining ideal adhesion between layers is essential for microlithographic control, and is especially critical during the selective anodization step of junction definition. During this step, penetration of the anodization solution (the electrolyte) under the resist would cause major fabrication defects. Standard resists have been optimized for the semiconductor industry, where the most critical materials are Si and SiO_2, and adhesion of resists to these materials is outstanding. In contrast, no such optimization exists for Nb, the key material for superconducting circuits. In the present invention (see FIG. 2), a thin layer of SiO_2 is used as an adhesion layer in a double-layer mask for defining the area of Josephson junctions. The SiO_2 adheres well to Nb (since it has also been optimized for an insulation layer), and also adheres very well to the top resist layer. Furthermore, SiO_2 is inert with respect to both aqueous and organic solvents used in anodization processing and resist processing (for both positive and negative resists), but can also be removed where necessary by standard etching techniques.
[0013] The invention recognizes that failure of interlayer adhesion between photoresist and Nb is a major cause of defects in the fabrication technology of the prior art. By substantially improving such adhesion, the present invention offers the possibility of improved reliability and IC yield.
[0014] In the prior art, the very same photoresist mask had to survive two subsequent fabrication steps—etching and self-aligned junction anodization (passivation) without loss of adhesion. The new technique is more robust in this respect since the bottom layer of the double-layer would prevent defect formation during anodization even if the top (resist) layer fails. This technique has been incorporated into a complete IC process, and indeed has resulted in substantially improved IC yield, especially for the smallest junctions (below 1.5 microns size) where the problems had previously been the most severe.
[0015] The present invention does increase the number of steps in the full process, since the SiO2 layer in the mask must first be deposited, and subsequently etched away. (However, this etch-away step can be done simultaneously with the counter-electrode etching.) Nevertheless, this extra effort is easily worthwhile, since it enables the manufacturing (with reasonable yield) of higher-density superconducting ICs with greatly enhanced device speed and performance.

[0016] A second process improvement of the present invention replaces a wet-etch process for AlOx removal in the prior art with an optimized dry-etch (or argon ion mill) process, in order to enhance junction uniformity and yield for small junctions.

[0017] A detailed description of a preferred embodiment of the invention, including a step-by-step process with fabrication parameters, is shown below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] FIG. 1 shows a cross section of a wafer having Nb/Al/AlO$_x$/Nb layers as used in the fabrication of superconducting devices such as a Josephson junction.

[0019] FIG. 2 shows a modification of the prior art process whereby dielectric layer of SiO$_2$ is deposited to act as an adhesion layer between the Nb and the photoresist layer deposited during the next process step.

[0020] FIG. 3 shows application of a photoresist layer on top of the silicon dioxide layer in accordance with one aspect of the invention.

[0021] FIG. 4 shows the photoresist area that defines the junction area after exposure and development of the photoresist.

[0022] FIG. 5 shows the etching of the SiO$_2$ adhesion layer and Nb counter-electrode down to the AlO$_x$/Al barrier layer.

[0023] FIG. 6A shows the results of a selective anodization step whereby all the exposed Al and part of the underlying Nb are converted to insulating oxides.

[0024] FIG. 6B shows a magnified view of the region inside the small dashed box in FIG. 6A.

[0025] FIG. 7 shows the removal of the photoresist layer.

[0026] FIG. 8 shows the result of coating and patterning of another photoresist layer designed to produce a protective anodization ring around the junction area.

[0027] FIG. 9 shows the etching (by Ar ion milling or dry reactive ion etching) of the anodized oxide (both AlO$_x$ and NbO$_x$ layers) except in the anodization ring (under the photoresist mask)

[0028] FIG. 10 shows the removal of the photoresist defining the anodization ring.

[0029] FIG. 11 shows the deposition of an SiO$_2$ insulating layer, designed to isolate the junction from subsequent wiring layers.

[0030] FIG. 12 shows the coating and patterning of a third photoresist layer, designed to produce a contact via to the Nb junction from a Nb wiring layer.

[0031] FIG. 13 shows the selective etching of the SiO$_2$ Up to the Nb counter-electrode.

[0032] FIG. 14 shows the removal of the photoresist. Now the structure is ready for deposition of a Nb wiring layer

DETAILED DESCRIPTION OF THE INVENTION

[0033] A new fabrication method is proposed for increasing the yield and quality of superconducting junctions and more particularly Josephson junctions and Josephson-based digital and analog circuits in superconducting electronics. The method is based on using a double-layer mask for partial anodization of the junction side-walls and base-electrode around the junction. The top layer of this mask is a photoresist or electron-beam resist, and the bottom layer is a dielectric (e.g., SiO$_2$) that is insoluble in either aqueous or organic solvents. A more detailed description will now be given.

[0034] The existing fabrication scheme for making Nb-based Josephson tunnel junctions for superconducting electronics is comprised of the following fabrication steps:

[0035] 1. As shown in FIG. 1, a Nb/Al/AlO$_x$/Nb trilayer is deposited in-situ on a wafer that includes or will include several other patterned layers of metal and dielectric. A tunnel barrier is formed by in-situ thermal oxidation of the Al layer in oxygen or an oxygen/argon mixture at a defined pressure, to form a thin (.about.1-2 nm) layer of AlO$_x$. Both the oxidation time and the pressure determine the properties of the tunnel barrier such as the Josephson critical current density J$_c$. The bottom Nb layer is called the base electrode, and the top Nb layer is called the counter-electrode of the tunnel Josephson junctions.

[0036] 2. FIG. 2 shows a step that differs from prior art fabrication techniques and will be discussed in more detail hereinafter.

[0037] 3. The wafer is coated with either positive or negative resist (FIG. 3), and the resist etch mask is formed by optical or e-beam lithography (FIG. 4). The counter-electrode area is then defined by etching (FIG. 5), using e.g. plasma etching, reactive-ion etching, or high-density plasma etching. The AlO$_x$/Al layer acts as an etch stop. (Note—the prior art method does not include the thin SiO$_2$ layer shown in FIGS. 3, 4 and 5.)

[0038] 4. After etching and without removing the resist, the wafer is immersed in an anodization solution, and all the surfaces that are not protected by the resist mask formed in step 5 are anodized. That is, the same resist etch mask is also used as an anodization mask. Anodization creates a bilayer of anodized Al (AlO$_x$) and anodized Nb (NbO$_x$) on the surface of the base electrode (FIG. 6). A layer of anodized Nb is also formed on all sidewalls of the junction's counter-electrode. This anodization step is very important because it encapsulates the junction's tunnel barrier with an anodized NbO$_x$ layer, and this, protects it from reacting with water, oxygen, and other processing chemicals during all further wafer processing steps. This step also allows for opening a contact hole to the counter-electrode that is larger in size than the junction itself. The thickness of the anodized layer is controlled by the anodization voltage, usually in the range of 15-50 V. The initial anodization current density is in the range from 0.5-5 mA/cm^2.

[0039] 5. After anodization, the resist is stripped (FIG. 7), and the wafer proceeds to the next fabrication steps that are intended to pattern the base electrode of the junction by lithography and etching. This may also require removing the anodization layer in some parts of the circuit. It remains around the junction (the anodization ring of FIGS. 8-10).

[0040] 6.After base electrode patterning, the Josephson junction is completely formed. All other fabrication steps are necessary in order to interconnect junctions in the circuits (such as the SiO$_2$ insulating layer in FIGS. 11-14), and to create resistors for biasing and shunting the junctions. These steps may vary depending on the details the fabrication process.

[0041] One of the main sources of defects and loss of yield in this fabrication scheme is poor adhesion of the resist mask in step 3. Although this fact has not been recognized in the prior art. This may be due in part to the volume expansion of Nb and Al layers during anodization, which places signficant local stresses on the photoresist mask. As a result, some parts of the resist mask may peel off during anodization, or anodization solutions may leach under the resist mask. This is

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especially a problem with many negative resists such as UVN-30. Some photoresists may also be incompatible with (partially soluable in) the common anodization solutions. In these cases, some junctions may be degraded, or the counter-electrode of some junctions may be partially anodized, thus preventing a good (superconducting) electrical contact to be made to the junctions during the following fabrication steps.

[0042] One improvement of the invention is to use a double-layer anodization mask with the lower layer being an inorganic dielectric layer (such as SiO_2) that is insoluble in water, solvents, and components of the anodization solution, and the upper layer is the photoresist (or e-beam resist) layer. SiO_2 is especially suitable since it has already been optimized as an insulating layer in the prior-art Nb integrated circuit process, and is also fully compatible with standard Si-based resist processing. This double-layer mask is formed in the following simple way:

[0043] a. After the Josephson junction trilayer (Nb/Al/ AlO_x/Nb) is formed as in step 1 above, a pinhole-free layer of SiO_2 is deposited by any appropriate method (e.g., rf magnetron sputtering, or plasma-enhanced chemical vapor deposition—PECVD) on top of the trilayer (see FIG. 2). The layer thickness may be anywhere from 5 to 300 nm, and is not critical, as long as it is free from pinholes. Thicker layers require long etch times, making them impractical.

[0044] b. A resist mask is formed in the same way as in step 4 above.

[0045] c. Then etching is done, using reactive ion etching (RIE) or inductively coupled plasma (ICP) with fluorine-based chemistry (e.g., SF_6, NF_3, or CF_4+O_2) such that both the SiO_2 overlayer and the Nb counter-electrode are etched in the same process. This may be a one-step process when the same etch parameters are used for both layers, or a two-step process when different etch recipes are used for etching first the SiO_2 and then the Nb counter-electrode. After completing the etch down to the AlO_x/Al layer in the trilayer structure (FIG. 5), the top of the Josephson junction will have a double-layer structure (SiO_2+resist) that serves as the double-layer anodization mask.

[0046] d. Etching is immediately followed by the anodization step 3, without removing the resist mask (FIG. 6). Now there is a layer of SiO_2 under the resist mask for extra protection.

[0047] The advantages of the proposed method are as follows. The SiO_2 layer improves the adhesion of the resist, and does not allow the anodization solution to leach underneath. Since the adhesion of sputtered or PECVD-deposited SiO_2 to Nb has already been optimized, and is stronger than the adhesion of the resist to Nb, the double-layer also protects the junction counter-electrode from being anodized even in the unlikely event that a part of the resist mask pops off, or if the anodization solution does leach under the resist. In the rare case that the SiO_2 layer has a pinhole or other defect, the presence of the resist on top still provides protection during the anodization. The probability that both layers of the double-layer anodization mask fail in the same location is much smaller than the probability of a failure of a single-layer resist mask. As a result, a dramatic increase in the yield and junction quality is achieved.

[0048] Another improvement over the prior art is described in reference to FIGS. 8 and 9, in defining the anodization ring around the Josephson junction. In the prior art, the AlO_x layer was first removed by a wet etch process, followed by reactive ion etching (RIE) for removing the NbO_x layer. However, a wet etch process can cause problems, that should preferably be avoided in high-reliability VLSI processing, particularly if sub-micron resolution is required. In the process of the present invention, this wet etch step is discarded, and two new approaches have been successfully demonstrated. In approach A, ion-milling with a neutral beam of argon (Ar) atoms is used to remove both the AlO_x and the NbO_x layers. In approach B, plasma etching (RIE or ICP) is used in a two-step process. First, a chlorine-based plasma is used to remove AlO_x and then a fluorine-based plasma is used to remove the NbO_x. Either approach provides for increased yield and uniformity.

[0049] While various embodiments of the present invention have been illustrated herein in detail, it should be apparent that modifications and adaptations to those embodiments may occur to those skilled in the art without departing from the scope of the present invention as set forth in the following claims.

What is claimed is:

1. An integrated circuit having Josephson junctions, comprising:

(a) a Josephson junction trilayer formed into circuit elements on a substrate;

(b) at least one strongly adhering adhesion layer deposited on a Josephson junction trilayer; and

(c) a patterned resist formed on top of the at least one adhesion layer, which is formed by exposing the resist to radiation to define a latent pattern therein, and selectively removing a first portion of the resist in dependence on the defined latent pattern, wherein a second portion of the resist remains on the at least one adhesion layer having a strong adhesion thereto, a portion of the at least one adhesion layer being exposed by removal of the first portion of the resist and etching through the mask thereby formed, to selectively expose portions of the Josephson junction trilayer,

wherein the Josephson junction trilayer is selectively processed after forming the patterned resist thereon to form circuit elements therefrom.

2. The integrated circuit according to claim 1, wherein the circuit elements have minimum feature sizes less than 1.5 microns.

3. The integrated circuit according to claim 1, wherein circuit elements have submicron feature sizes.

4. The integrated circuit according to claim 1, wherein the at least one adhesion layer comprises SiO_2.

5. The integrated circuit according to claim 1, wherein the Josephson junction trilayer comprises a niobium-based superconductor.

6. The integrated circuit according to claim 1, wherein the resist comprises a photoresist.

7. The integrated circuit according to claim 1, wherein the resist comprises an electron beam exposed resist.

8. The integrated circuit according to claim 1, wherein the mask is etched by plasma etching.

9. The integrated circuit according to claim 1, wherein the mask is etched by reactive ion etching.

10. The integrated circuit according to claim 1, wherein the mask is etched by ion beam etching.

11. The integrated circuit according to claim 1, wherein the at least one adhesion layer is deposited substantially without formation of pin holes therethrough.

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12. The integrated circuit according to claim **1**, wherein the at least one adhesion layer is deposited by a sputtering process.

13. The integrated circuit according to claim **1**, wherein the Josephson junction circuit elements are formed by an anodization process.

14. The integrated circuit according to claim **1**, wherein the Josephson junction circuit elements are formed by a process substantially absent a wet etching step.

15. The integrated circuit according to claim **1**, wherein the Josephson junction circuit elements are formed by an anodization step adapted to convert at least a portion of the Josephson junction trilayer to an AlO_x layer over a NbO_x layer, and a portion of the converted Josephson junction trilayer is etched by ion-milling with a neutral beam of argon atoms to remove the AlO_x layer and the NbO_x layer.

16. The integrated circuit according to claim **1**, wherein the Josephson junction circuit elements are formed by an anodization step adapted to convert at least a portion of the Josephson junction trilayer to an AlO_x layer over a NbO_x layer, and a portion of the converted Josephson junction trilayer is etched by a chlorine-based plasma etching to remove the AlO_x layer, and a fluorine-based plasma is then used to remove the NbO_x layer.

17. The integrated circuit according to claim **1**, wherein the circuit elements comprise at least two separately operating Josephson junctions.

18. The integrated circuit according to claim **1**, further comprising an anodization ring formed from the Josephson junction trilayer around an active region of a circuit element.

19. A superconducting integrated circuit, comprising:

(a) a substrate;

(b) a plurality of circuit elements formed on the substrate from a Josephson junction trilayer;

(b) a patterned silicon dioxide layer formed on the Josephson junction trilayer, the patterned silicon dioxide layer being strongly adherent to a top layer of the Josephson junction trilayer; and

(c) a patterned resist formed on top of the adhesion layer, the patterned resist being strongly adherent to the adhesion layer;

wherein the patterned resist, patterned adhesion layer and plurality of circuit elements are formed by exposing an unpatterned resist to radiation to define a latent pattern therein, selectively removing a first portion of the resist in dependence on the defined latent pattern, wherein a second portion of the resist remains on the adhesion layer, a portion of the adhesion layer being exposed by removal of the first portion of the resist and etching through the mask thereby formed, to selectively expose portions of the Josephson junction trilayer, and selectively processing the exposed Josephson junction trilayer after forming the patterned resist thereon, to form the plurality of circuit elements.

20. The superconducting integrated circuit according to claim **19**, further comprising an anodization ring formed from the Josephson junction trilayer around an active region of a respective circuit element.

* * * * *