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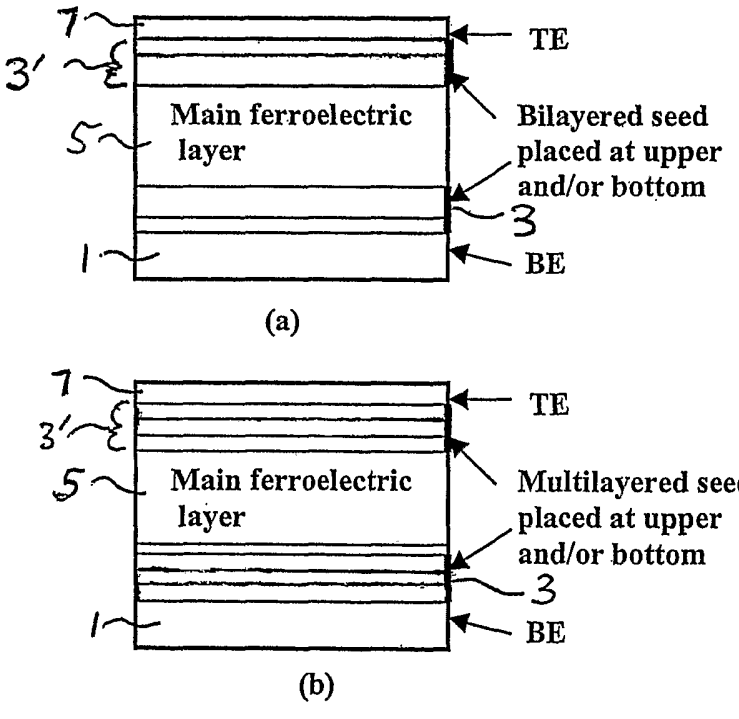
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[Continued on next page]

(54) Title: FERROELECTRIC CAPACITOR AND PROCESS FOR ITS MANUFACTURE



(57) Abstract: In a capacitor and a method for its manufacture, a first electrode layer and a second electrode layer are formed such that a ferroelectric layer is situated between the first and second electrode layer. A first bilayer or multi-layer seed structure is formed between the ferroelectric layer and either the first electrode layer or the second electrode layer.

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Ferroelectric Capacitor and Process for its Manufacture

TECHNICAL FIELD

The present invention relates to a method of manufacturing capacitors, especially for ferroelectric applications including non-volatile memories known as FeRAM and for high-k dynamic random access memory (DRAM). It also relates to capacitors producible by this method.

BACKGROUND OF THE INVENTION

Ferroelectic capacitors have the advantage that they are able to switch quickly and can be fabricated on a single VLSI chip.

FeRAM's are advantageous in that they have the endurance of DRAM, the fast read/write times of SRAM and the non-volatility of flash.

Conventionally, an FeRAM is manufactured by depositing a ferroelectric film, such as lead zirconate titanate (PZT), strontium bismuth tantalum oxide (SBT), bismuth lanthanum titanium oxide (BLT) on a first, planar, electrode film, and forming a second electrode film over the ferroelectric layer. The second electrode layer and the ferroelectric film are then etched using a reactive ion etch method, after which the first electrode film is etched using a similar method. The result is a number of stacks comprising a first and second electrode film sandwiching the ferroelectric film.

In such conventional manufacturing methods, ferroelectric films are deposited on the electrode by changing deposition parameters with the aim of matching morphologies as close by as possible or any rate, promoting computability of adjacent layers. However, ferroelectric capacitors made by this method still tend to have poor characteristics, necessitating optimization of the fabrication

method to minimise these problems. In order to improve ferroelectric properties, the introduction of a monolayered film prior to main ferroelectric film deposition has been reported in IFFF, 2002, Abstracts, 29B-FDI-5C, (2002), p. 49. It was shown that a $PbTiO_3$ seed layer can act as a good crystalline buffer for PZT.

However, because the seed layer's composition and ferroelectric properties are different from those of the main PZT layer, it is difficult to exclude formation of an interfacial layer which can cause undesirable properties due to parasitic ferroelectricity and capacitance at the interface. Actually, a $PbTiO_3$, seed layer can only form with tetragonal crystalline structure on the main PZT film. It can cause the enlargement of Vc (coercive voltage), and a large saturation voltage for ferroelectricity. In addition, further negative interface effects can be expected, since the fabrication method (Chemical Solution Deposition) for the $PbTiO_3$ seed-layer is different from that of main PZT layer formed by sputtering.

Figure 1 shows the hysteresis characteristics of a PZT capacitor fabricated by the conventional method. The capacitor structure is TEOS-substrate/Ti/Ir/IrO_2/Pt/PZT/SRO/Pt. In this case, no seed layer was employed prior to deposition of PZT layer. The poor ferroelectric properties are due to the poor crystallinity and poor composition of the PZT films which were grown on the Pt bottom electrode (BE). The PZT film shows a depletion of Pb near the interface between the PZT film and the BE-Pt, since the element Pb can easily diffuse into the Pt bottom electrode during crystallization annealing. This strongly affects the crystallinity of the PZT film and degrades the electrical properties of PZT capacitors.

SUMMARY OF THE INVENTION

In order to control the composition at the interface and to obtain good ferroelectric properties of capacitor, the present invention utilises a bilayered or a multi-layered seed structure. This solves the aforementioned problems which occurs at the electrode interface and provides a good crystalline template, optimization of the total composition of the ferroelectric capacitor layer, including interface composition, and results in good electrical properties of the resultant capacitor.

A first aspect of the present invention provides a capacitor comprising,

a first electrode layer;

a second electrode layer;

a ferroelectric layer situated between the first and second electrode layers; and

a first bilayer or multi-layer seed structure situated between the ferroelectric layer and either the first electrode layer or the second electrode layer.

A second aspect of the present invention provides a method of forming a capacitor, said method comprising the steps of:

forming a first electrode layer;

forming a second electrode layer;

forming a ferroelectric layer between the first and second electrode layers; and

forming a first bilayer or multi-layer seed structure between the ferroelectric layer and either the first or second electrode layer.

For the avoidance of doubt, reference herein to pluralities of seed layers in the seed layer structure includes both separate layers and a compositional graduation within a single layer.

DESCRIPTION OF THE FIGURES

The present invention will now be better explained by the following description of preferred embodiments and with reference to the accompanying drawings in which:

Figure 1 shows hysteresis curves of a PZT capacitor fabricated by the conventional method;

Figures 2A and 2B show a capacitor according to a first embodiment of the present invention and the bilayered seed structure thereof;

Figures 3A-3C show bilayered seed structures, respectively from PZT-, SBT- and BLT- capacitors;

Figures 3D shows a bilayered seed structure along with a bottom electrode using conductive perovskite oxide;

Figures 4A and 4B show alternative configurations for bilayered and multi-layered seed structures, respectively between the top electrode and/or the bottom electrode and the main ferroelectric layer; and

Figures 5A and 5B show curves illustrating electrical characteristics for a PZT capacitor according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Figure 2B shows an example of a bilayered seed structure used in a capacitor as shown in Fig. 2A, according to the present invention. In this capacitor, a bottom electrode (BE) layer 1 has formed thereon, a bilayer seed structure 3 on which is formed a ferroelectric layer 5. A final top electrode (TE) layer 7 is formed on the ferroelectric layer 5. The bilayer seed structure is composed of a first layer 9 which comprises at least one constituent element of the main ferroelectric film, and a second layer 11 which is identical with the main ferroelectric layer 5. Materials of the BE and TE layers can be metal films (Pt, Ir, Ru, Pd, Rh and etc.) or conductive oxide films ($SrRuO_3$, $SrVO_3$, LaSrCoOx, $LiNbO_3$, IrO_2, RuO_2 and etc.) deposited by using PVD (physical vapor deposition), CVD (chemical vapor deposition), CSD (chemical solution deposition), spin-on or other known techniques.

For PZT ($Pb_x(Zr_yTi_{1-y})O_3$) ferroelectric capacitors, the first layer 9 can be a Ti or Zr or Pb film with 0.1 – 10 nm thickness, and the second-layer can be a PZT layer itself with the thickness of 0.1 – 50 nm thickness, as shown in Fig. 3A. The composition can be controlled by the changing thickness of each first- and second-layer, which can control the interface composition of the resultant ferroelectric capacitors. The composition range of the bilayered seed layer can be in range of $Pb_x(Zr_yTi_{1-y})O_3$ ($0<y<1$, $0<x<1$). Compared with the known method using $PbTiO_3$ monolayer as seed, in the present invention, the bilayered seed structure can have a wide range of possible compositions, which makes it possible to change the ferroelectric domain from tetragonal to rhombohederal. When a different composition is required at the interface, the kind of first layer material can be changed to, for example, Zr or Pb. The change of material and thickness of each layer in bilayer can optimize the

interface status. For example, when the Ti-rich PZT interface layer is needed, the bilayer structure can be prepared by thick Ti and thin PZT with normal composition (wherein normal means the composition ration of Ti/Zr is approximately 60/40 to 70/30), which are crystallized. During crystallization annealing, mutual diffusion between the 1st and 2nd layers makes Ti-rich tetragonal PZT phases. Also, the composition of the interface layer can be controlled by changing the first layer's material, for example, by employing Pb or Zr instead of Ti. It is also possible to deposit a bilayered seed structure with composition which is graduated through the thickness of the layer, intentionally. This can sometimes avoid formation of trapping ions and/or electrons between the seed layer structure and main ferroelectric capacitor layer. After formation of the seed structure layers, a crystallization process can also be applied, for example, using an RTA (rapid thermal annealing) treatment, to create a crystalline structure from the amorphous phase. In the aforementioned known method, it is difficult to control the composition near the interface, since the seed layer structure has a composition which is fixed as that of $PbTiO_3$ film in which the seed layer can only form with the tetragonal structure of PZT main layer.

In Figures 3 and 4, like layers are denoted by the same reference numerals as used in Figures 2A and 2B,

As shown in Figure 3A, the bilayer structure can have a first (lower) layer 9 of Ti, Zr or Pb.

Referring to Figure 3B, for SBT ($SrBi_2Ta_2O_9$) ferroelectric capacitors, the first-layer 9 can be one of Bi, Sr or Ta film with 0.1 – 10 nm thickness, and

second-layer 11 can be a SBT layer itself with the thickness of 1 – 50 nm thickness. In the case of an SBT film, the diffusion of the Bi element is very severe during crystallization. For example, when Bi is chosen as the first-layer, Bi can act as a supplier of volatile Bi, and, in turn, can promote crystallization of the second-layer SBT film 11 during crystallization of this bilayered seed structure 3. The composition of Bi and the multi-layered seed structures can be controlled in the same way which is described for the bilayered seed for PZT capacitors. The composition range of the bilayered seed layer 3 can be one of in range of $Sr_aBi_bTa_cO_9$ ($0<a<1$, $0<b<1$, $0<c<1$).

For BLT ($(BiLa)_4Ti_3O_{12}$) ferroelectric capacitors (Fig. 3C), the first layer can be a Bi or La or Ti film with 0.1 – 10 nm thickness, and second layer can be an BLT layer with the thickness of 1 – 50 nm thickness. The composition range of the bilayered seed layer can be one of in range of $(Bi_zLa_{1-z})_4 Ti_wO_{12}$($0<z<1$, $0<w<1$).

Crystallinity of the bilayered seed structure can be improved by using crystalline conductive oxide with a perovskite structure (e.g., SrRuO3, LaNiO3, SrVO3, etc) as a first electrode 1, as shown in Fig. 3D. This is because perovskite-type conductive oxide can provide good nucleation sites for perovskite ferroelectric layers such as PZT, SBT and BLT.

It is important to note that there are no thickness limitations for first and second layers of seed structures and the above thickness values are given by example only.

When the composition needs to be controlled at the interface between the capacitor film and top electrode (TE), a bilayered seed structure 3' can be applied after formation of main ferroelectric film, as shown in Fig. 4A. By this procedure, the composition at the interface between ferroelectric film layer 5 and the TE layer 7 can be optimized with or without combination of applying a bilayered seed 3 at the interface between the BE layer 1 and the main ferroelectric film layer 5, which results in good electrical properties of the capacitor. Use of a bilayered seed structure (3 or 3') at the interface between the ferroelectric layer and the BE layer 1 or TE layer 7, controls the interface composition and gives a good crystalline template, giving improved electrical characteristics.

The composition can be further controlled by formation of multi-layered seed structure, which is composed of two or three layers which are stacked by, for example, Ti and Zr and Pb, on top of the PZT layer itself, as shown in Fig. 4B. Bilayered seed layers can be formed by using PVD (physical vapor deposition), CVD (chemical vapor deposition), CSD (chemical solution deposition), spin-on deposition or other known techniques.

Figure 5 shows the resulting electrical properties of a PZT capacitor with a bilayered seed structure of the present invention. The bilayered seed structure in this case is composed of a first layer of 2.5 nm-thick Ti film and a second layer of 7.5 nm-thickness PZT [$Pb(Zr_{40}Ti_{60})O_3$] film. After formation of the bilayered seed structure by sputtering, the bilayer was annealed at 650°C for 30 sec in O_2 ambient using RTA (rapid thermal process). Compared the conventional (without bilayered seed) method (cf. Fig. 1), the PZT capacitor shows hysteresis characteristics with good squareness (Fig. 5A). The capacitor structure was TEOS-substrate / Ti / Ir / Ir02 / Pt (10nm) / bilayered

seed / PZT / SRO (10nm) / Pt (50nm). The Vc of the capacitor is fairly low and saturation property is very good, which are parameters attributed to good PZT quality including good interface properties. Furthermore, this capacitor shows fatigue free characteristics, even after fatigue test of 10^{10} cycles (Fig. 5B).

CLAIMS

1. A capacitor comprising,

a first electrode layer;

a second electrode layer;

a ferroelectric layer situated between the first and second electrode layers; and

a first multi-layer seed structure situated between the ferroelectric layer and either the first electrode layer or the second electrode layer.

2. The capacitor of claim 1, wherein the seed structure is a multi-layer seed structure and comprises a first seed layer having substantially identical composition as, and in contact with, the ferroelectric layer and a second seed layer including one or more components of the ferroelectric layer and in contact with the adjacent electrode layer.

3. The capacitor of claim 2 wherein the first and second seed layers have a composition gradient between the ferroelectric layer and the adjacent electrode layer.

4. The capacitor of claim 1, wherein a second multi-layer seed structure is situated between the ferroelectric layer and other of the first electrode layer and second electrode layer.

5. The capacitor of claim 1, wherein the first electrode layer includes a crystalline conductive oxide for improving the crystallinity of the multi-layer seed structure.

6. The capacitor of claim 1, wherein the ferroelectric layer includes a material of the set consisting of: PZT, SBT and BLT.

7. The capacitor of claim 6, wherein the first multi-layer seed structure includes a material of the set consisting of: Ti, Zr, Pb, Bi, La, Ta, Sr.

8. A method of forming a capacitor, said method comprising the steps of:

forming a first electrode layer;

forming a second electrode layer;

forming a ferroelectric layer between the first and second electrode layers; and

forming a first multi-layer seed structure between the ferroelectric layer and either the first or second electrode layer;

9. The method of claim 8, wherein the seed structure is a bilayer seed structure and comprises a first seed layer having substantially identical composition as, and in contact with, the ferroelectric layer and a second seed layer consisting essentially of one or more components of the ferroelectric layer and in contact with the adjacent electrode layer

10. The method of claim 8, wherein the first electrode layer includes a crystalline conductive oxide for improving the crystallinity of the multi-layer seed structure.

11. The method of claim 8, wherein the ferroelectric layer includes a material of the set consisting of: PZT, SBT and BLT.

12. The method of claim 11, wherein the first multi-layer seed structure includes a material of the set consisting of: Ti, Zr, Pb, Bi, La, Ta, Sr.

13. The method of claim 8, wherein the first and second seed layers are formed with a composition gradient between the ferroelectric layer and the adjacent electrode layer.

14. The method of claim 8, wherein a second multi-layer seed structure is formed between the ferroelectric and the other of the first and second electrode layers.

15. A method of manufacturing a semiconductor device, said method comprising the steps of:

(a) forming on a substrate, a capacitor layer structure by:

forming a first electrode layer;

forming a second electrode layer;

forming a ferroelectric layer between the first and second electrode layers; and

forming a first multi-layer seed structure between the ferroelectric layer and either the first or second electrode layer; and

(b) patterning said capacitor layer structure to form individual capacitors, during or after formation of the layers which comprise the capacitor layer structure.

Prior Art

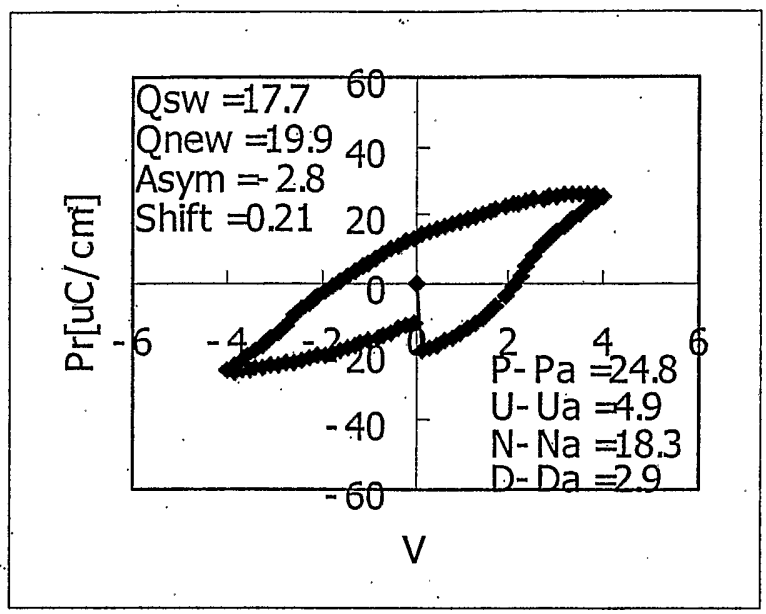


Fig. 1

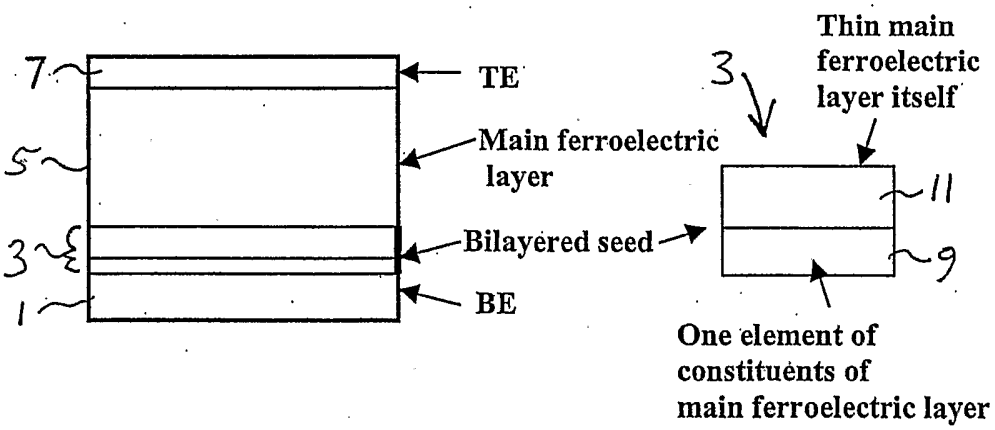


Fig. 2

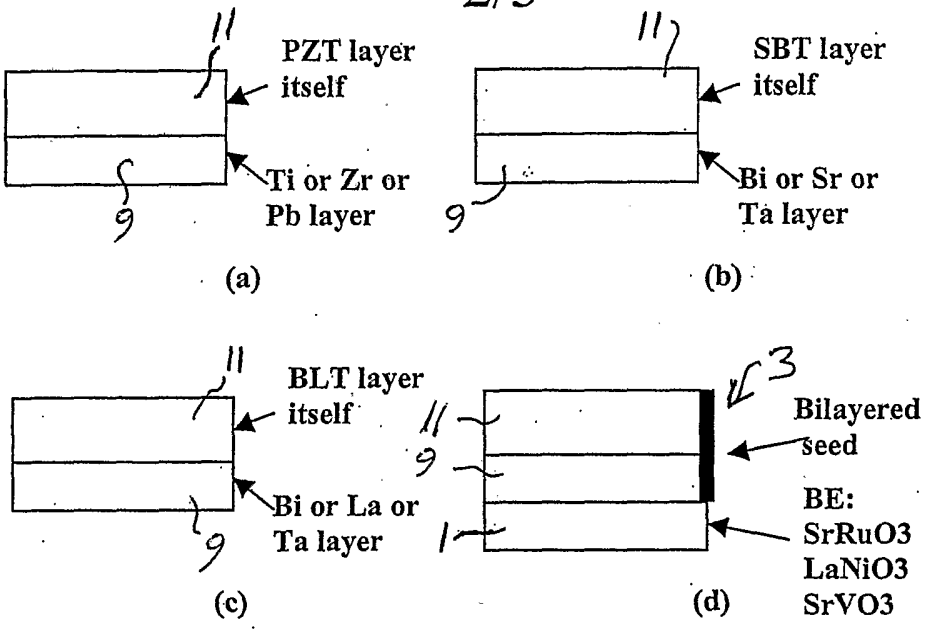

11
PZT layer itself
9
Ti or Zr or Pb layer
(a)
11
SBT layer itself
9
Bi or Sr or Ta layer
(b)
11
BLT layer itself
9
Bi or La or Ta layer
(c)
3
11
9
1
Bilayered seed
BE:
SrRuO3
LaNiO3
SrVO3
(d)

Fig. 3

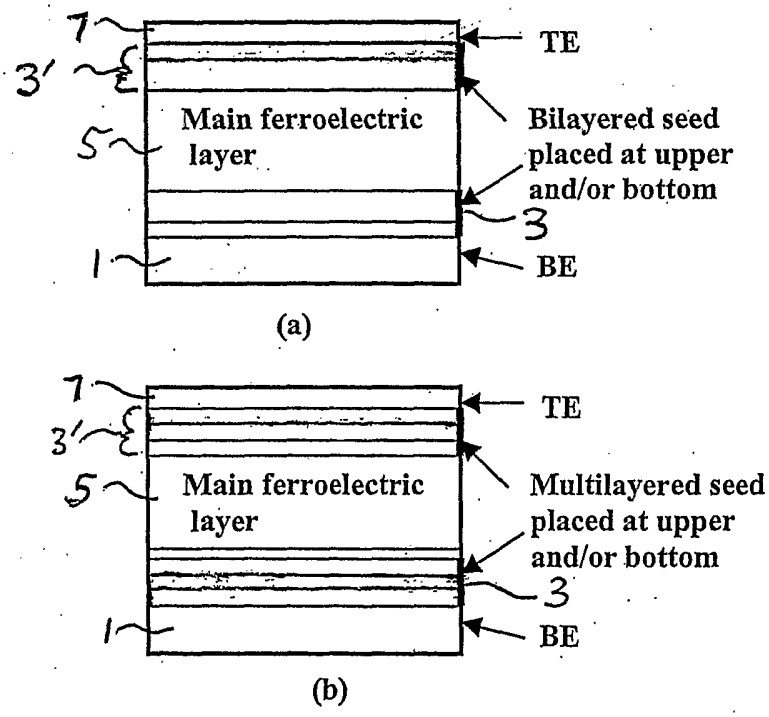
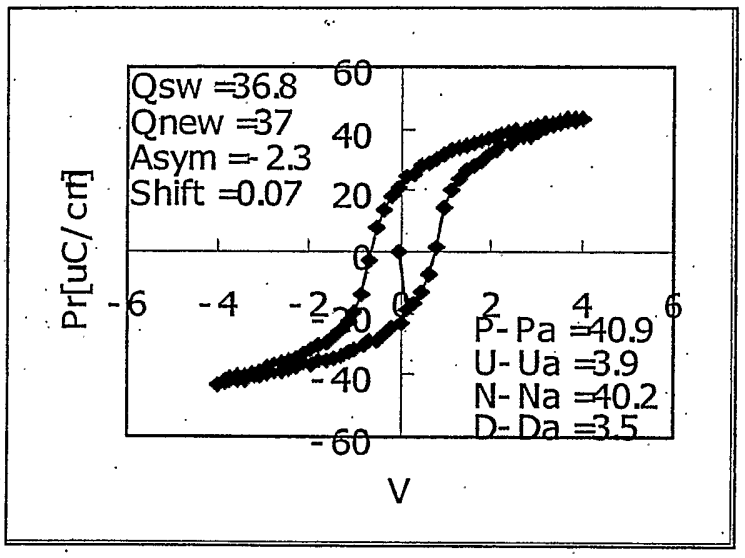
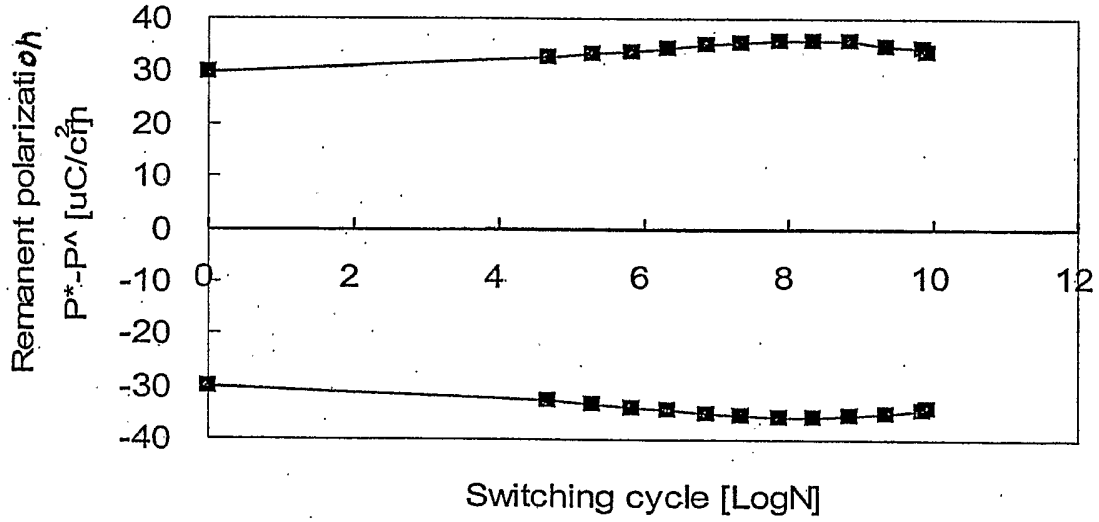

7
3'
5
1
TE
Main ferroelectric layer
Bilayered seed placed at upper and/or bottom
3
BE
(a)
7
3'
5
1
TE
Main ferroelectric layer
Multilayered seed placed at upper and/or bottom
3
BE
(b)

Fig. 4


Qsw =36.8
Qnew =37
Asym =-2.3
Shift =0.07
P-Pa =40.9
U-Ua =3.9
N-Na =40.2
D-Da =3.5
Pr[uC/cm]
V
60
40
20
0
-40
-60
-6
-4
-2
2
4
6

(a)


Remanent polarization
P*-P^ [uC/cm2]
Switching cycle [LogN]
40
30
20
10
0
-10
-20
-30
-40
0
2
4
6
8
10
12

(b)

Fig. 5

INTERNATIONAL SEARCH REPORT

tional Application No
PCT/SG 03/00277

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/02

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
29 April 2004	10/05/2004

Name and mailing address of the ISA	Authorized officer
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INTERNATIONAL SEARCH REPORT

International Application No
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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