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A RE-SEQUENCING UNIT

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(57) Claim

1. A resequencing unit for a node in a cell switching system, each cell being made up of a variable number of fixed length subcells, this node including a switching network transmitting cells with first variable delays, all subcells within the same cell undergoing a same first delay; this resequencing unit being fitted with some means used to store all cells which were transmitted via the switching network, and to transmit these cells over at least one output of the resequencing unit, upon expiry of various waiting times resulting in second delays such that, for each cell, the sum of the first delay and the second delay is equal to a preset value roughly identical for all cells, these means including:

- a buffer memory to store the subcells of each cell received by the resequencing unit;
- an address memory to store the address of the buffer memory containing the first subcell of each cell;

- means used to find the address of the address memory containing the first subcell of a cell, once the cell waiting time has expired and that an output designed to transmit this cell has become available;

wherein said means used to find the address of the buffer memory containing the first subcell of a cell include:

- a content addressable memory referred to as waiting-cell memory, to store a waiting-cell identifier, when a cell is stored in the buffer memory ; this identifier being stored at an address identical to that where the first subcell address is stored in the address memory; and this identifier consisting of: a time stamp identifying a time slot during which the cell waiting time expires, and of the identity of at least one output where the cell is to be transmitted.
- means of finding, within the waiting-cell memory, the identifier of each cell when its waiting time expires, and of supplying, for each identifier found, the address of the waiting-cell memory which contains this found identifier;
- content addressable queuing memories respectively associated with the node outputs, to store a sequence number for each cell intended for the output associated with the relevant memory;
- means of determining and writing a sequence number into a queuing memory, at the address supplied by the means used to find the identifier of each cell when its delay has expired;
- means of finding, in ascending order, each sequence number stored in the queuing memory of an output, when this output becomes available; and of restoring the address of this queuing memory containing the sequence number found; and

means of reading a first subcell address from the address memory at the address restored by the means used to find each sequence number.

output where the cell is to be transmitted.

- means of finding, within the waiting-cell memory, the identifier of each cell when its waiting time expires, and of supplying, for each identifier found, the address of the waiting-cell memory which contains this found identifier.
 - content addressable queuing memories respectively associated with the node outputs, to store a sequence number for each cell intended for the output associated with the relevant memory.
 - means of determining and writing a sequence number into a queuing memory, at the address supplied by the means used to find the identifier of each cell when its delay has expired.
 - means of finding, in ascending order, each sequence number stored in the queuing memory of an output, when this output becomes available; and of restoring the address of this queuing memory containing the sequence number found.
- means of reading a first subcell address from the address memory at the address restored by the means used to find each sequence number.

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ORIGINAL
COMPLETE SPECIFICATION
STANDARD PATENT

Invention Title:

"A RE-SEQUENCING UNIT"

The following statement is a full description of
this invention, including the best method of
performing it known to us:-

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This invention relates to a resequencing unit for a node in a cell switching system. It relates more precisely to switching systems handling variable length cells, whereby each cell may consist of a variable number of fixed length subcells.

Each time these cells transit via a switching system node, each of them is subjected to a delay which varies in accordance with the path followed within the switching network containing this node. The subcells within the same cell are linked in such a way that they follow the same path and are subjected to the same delay. Therefore, at the output of the switching network, the subcells within the same cell are still in their initial sequence, though the cells are not necessarily in their initial sequence due to the delay spread. A resequencing unit is used to reposition these cells in their initial sequence.

Australian patent No.632152 describes a resequencing process which consists of delaying each cell by a set delay such that the value of the total delay imposed by the switching network and the resequencing unit is roughly constant for all these cells, the value selected being generally greater than the maximum delay that may be generated by the switching network. If the total delay selected is lower than the maximum value of the delay that may be generated by the switching network, the probability of the initial sequence being disturbed is not nil, and depends on the value selected for the total delay. This known process includes two alternatives.

The first alternative consists of: associating each cell incoming in the switching network with a time stamp indicating at which time the cell entered the switching network; extracting the time stamp from each cell outgoing the switching network; storing each cell outgoing the network, until the time indicated by the stamp generator is equal to the time indicated by the cell time stamp, plus the selected total delay; and of enabling cell transmission via one output of the resequencing unit. Transmission effectively occurs as soon as the output the cell is intended for becomes available.

According to this alternative, the cell initial sequence is reconstituted without having to measure or estimate the delay of each cell transiting via the switching network. Nevertheless, the time supplied by the time stamp generator must be available in a device located at the network input to assign time stamps, and simultaneously, and it must be available in a resequencing unit located at the network

output, to enable the transmission of each cell at a suitable time.

According to another alternative of this known process, it consists of associating each cell outgoing the switching network with a stamp whose value is an estimate of the delay the cell undergoes during its transit via the network, and subjecting each cell to an additional delay having a duration equal to the difference between the preset value of the total delay and the estimated value of the delay during transit in the network, the latter value being read in the stamp associated with each cell. This alternative offers the advantage of not requiring a device associating time stamps with the cells incoming at the switching network inputs.

This patent also describes a resequencing device implementing the first alternative of the above mentioned process, for cells made up of a variable number of fixed length subcells. Each node output is fitted with one such device. This device includes:

- a time stamp generator, supplying a value incremented by one unit for each time slot corresponding to a subcell, with a cycle duration at least equal to the total preset delay to uniformly delay all cells.
- a buffer memory having an input coupled to an input of the resequencing unit, and an output coupled to an output of the resequencing unit; each memory location having a capacity equal to one subcell.
- a buffer memory management circuit, to supply the addresses of locations which are available within this buffer memory, and to store therein the subcells of each cell received by the resequencing unit.
- a read/write pointer associated with the buffer memory.
- an address memory whose locations correspond respectively to the various possible values of the time stamp; each address memory location storing a start of list pointer and an end of list pointer, which are respectively the addresses, in the buffer memory, of the first and the last subcell in a series containing all the cells having the same time stamp.
- a link memory, having the same set of addresses as the buffer memory, to store the links between the addresses of all the subcells having the same time stamp, and to store the links between the addresses of subcells belonging to cells which must be transmitted successively.

- a write pointer associated with this address memory to store in each location the first address and the last address of a list of location addresses of the buffer memory, containing all subcells of all the cells having the same time stamp.
- a read pointer associated with the address memory, operating cyclically, to successively read the contents of the locations of this address memory, in order to read the subcells in the buffer memory at addresses corresponding to time stamps increasing regularly.

Once the delay has expired for a series of cells having a given time stamp, i.e. when the time indicated by the stamp generator is equal to the sum of the given time stamp and of the total preset delay, the first and the last storage addresses for this series are read in the address memory location corresponding to this time stamp. The link memory then supplies the complete series of addresses, and hence it is possible to read from the buffer memory all subcells of all the cells having the relevant time stamp. These cells are read in an order defined by the links in the link memory, though this order is not important since all these cells have the same time stamp and are addressed to the same output. The link memory is also used to link up within the same queue the various series of subcells of cells having successive time stamps, thus ensuring their transmission in the correct sequence. This linkage is achieved by the link memory matching the end of the series of addresses of the subcells in a cell with the start of the series of addresses of the subcells in the cell to be transmitted next.

A first drawback of this device is that it does not allow for resequencing of cells incoming on the same input but intended for several outputs, especially when the same cell must be broadcast over several outputs. This impossibility is due to the operating principle of this known device, which requires to store, in the address memory, at each location, an address for the start of the series of addresses and an address for the end of the series of addresses of the subcells; and which requires to link via a link memory all the subcells which will have to be transmitted later on the same output. Therefore, the resequencing units associated with the various node outputs operate independently from one another.

A second drawback of this known device is that it does not allow for very long cells. Each address memory location corresponds to a time unit of the generator

supplying the time stamps. This time unit is equal to the duration of a subcell. The time stamp generator does not have an infinite capacity. Therefore, it periodically supplies identical stamp values. Each address memory location is read with a constant period, at the most equal to the period of the time stamp generator. At the time a location is read, the list must be fully compiled such that an end of list address can be validly read in the relevant location. Therefore, the time stamp generator period imposes a limitation to the number of subcells corresponding to this list, and finally, it limits the number of subcells that may be contained in each cell.

Furthermore, it is impossible to indefinitely increase the time stamp generator period since this requires an increase in the number of bits added to each cell in order to constitute a time stamp.

It is an object of the invention is to provide a resequencing unit making it possible to broadcast a cell from one input to several preset outputs of this resequencing unit. A second aim of the invention is to provide a resequencing unit which can be more easily adapted to accept cells made up of a large number of subcells.

According to the invention, there is provided a resequencing unit for a node in a cell switching system, each cell being made up of a variable number of fixed length subcells, this node including a switching network transmitting cells with some first and variable delays, all subcells within the same cell undergoing the same and first delay; this resequencing unit being fitted with some means used to store all cells which were transmitted via the switching network, and to transmit these cells over at least one output of the resequencing unit, upon expiry of various waiting times resulting in second delays such that, for each cell, the sum of the first delay and the second delay is equal to a preset value roughly identical for all cells, these means including:

- a buffer memory to store the subcells of each cell received by the resequencing unit.

- an address memory to store the address of the buffer memory containing the first subcell of each cell.

- means used to find the address of the address memory containing the first subcell of a cell, once the cell waiting time has expired and that an output designed

to transmit this cell has become available.

wherein, the means used to find the address of the buffer memory containing the first subcell of a cell include:

- a content addressable memory referred to as waiting cell memory, to store a waiting-cell identifier, when a cell is stored in the buffer memory; this identifier being stored at an address identical to that where the first subcell address *FSA* is stored in the address memory; and this identifier consisting of: a time stamp identifying a time slot during which the cell waiting time expires, and of the identity of at least one output where the cell is to be transmitted;

- means of finding, within the waiting cell memory, the identifier of each cell when its waiting time expires, and of supplying, for each identifier found, the address of the waiting-cell memory which contains this found identifier

- content addressable queuing memories respectively associated with the node outputs, to store a sequence number for each cell intended for the output associated with the relevant memory;

- means of determining and writing a sequence number into a queuing memory, at the address supplied by the means used to find the identifier of each cell when its delay has expired;

- means of finding, in ascending order, each sequence number stored in the queuing memory of an output, when this output becomes available; and of restoring the address of this queuing memory containing the sequence number found;

- means of reading a first subcell address from the address memory at the address restored by the means used to find each sequence number.

The unit thus characterised is compatible with broadcasting since it is associated with all the outputs of a node and since the waiting cell memory stores identifiers which can contain several destination output identities.

Furthermore, it is easier to implement for long cells since a waiting cell identifier can be stored in this memory without having to wait for all cell subcells to be effectively received by the node. Therefore, the first subcells of a cell can be transmitted over an output before the last subcells are received.

The invention will be better understood and other details will come to light after reading the following description and attached drawings in which:

- Figure 1 represents a block diagram of an example of implementation of the unit in accordance with the invention, connected to a switching network, to make up a node in a cell switching system.

- Figure 2 represents a more detailed diagram of this example of implementation.

Figure 1 represents the node of an asynchronous transfer telecommunications network, including a switching network *SW* and an example of implementation of the resequencing unit *RU* in accordance with the invention. This node includes *M* inputs *IN1* to *INM*, and *N* outputs *OU1* to *OUN*. This example of implementation of the resequencing unit *RU* includes:

M stamping circuits *IC1* to *ICM*, each having: an input respectively connected to a node input *IN1* to *INM*, an output respectively connected to one of the *N* inputs of switching network *SW*, and a common input.

- *M* input circuits *IL1* to *ILM*, each having: an input respectively connected to one of the *M* outputs of switching network *SW*, and an output connected to a time division multiplexing bus *TDM1*.

- A cell header processing circuit *HP* having a first input connected to bus *TDM1*.

- A control unit *CU* which will be described in detail later on, including a first input respectively connected to a first output of header processing circuit *HP*.

- A time stamp generator *TSG* having one output connected to the common input of stamper circuits *IC1* to *ICM*, this generator being made up of a clock and a counter (not shown) to supply a stamp value incremented by one unit for each time

slot corresponding to a subcell, from 0 to $TSTP_{max}$, modulo $TSTP_{max}$.

- A buffer memory BM associated with a buffer memory management unit $BMMU$, this set having: an input connected to a second output of head processing circuit HP , an output connected to a second input of circuit HP , and an input-output connected to a time division multiplex bus $TDM2$.

- A memory $FSAM$, referred to as address memory, having: a data input di connected to a third output of circuit HP , an address input ad connected to an output of unit CU , and an output do connected to a second input of unit CU .

- N output circuits $OL1$ to OLN each having: an input-output connected to bus $TDM2$, an output respectively connected to one of the node outputs $OU1$ to OUN , and an input-output connected to bus RQB , the latter being connected to an input-output of control unit CU .

- Inputs $IN1$ to INM receive fixed or variable length cells, each of these cells is made up of subcells having all the same number of bits and the same duration, this duration is called subcell period. The unit in accordance with the invention is particularly well suited to process variable length cells.

These cells are switched within switching network SW by routing all subcells within the same cell via the same path and maintaining cell continuity, i.e. without interlacing the subcells belonging to different cells. This makes it possible to assign a single time stamp to the set of subcells making up a cell. This time stamp indicates the time slot during which the first subcell of the relevant cell is received on one of the inputs $IN1$ to INM .

This stamp is used for resequencing the cells outgoing switching network SW : the first subcell is enabled to be output from the node when its waiting time has expired, i.e. during the time slot where generator TSG indicates a time equal to

the sum of the value of the time stamp assigned to the cell, and of a set value. But an additional condition exists in order to transmit the cell: the output designed to receive this cell must be available. Otherwise, the relevant cell must wait until this output becomes available.

5 Each subcell starts with two bits called subcell control field. In the first subcell of each cell, the value of these two bits may be 11 for instance. In all other subcells, except the last, the value of these two bits may be 00 for instance. In the last subcell, the value of these two bits may be 01 for instance. Furthermore, the first subcell contains a field called cell control header. This field contains the
10 identity of the output which is to transmit this cell, or the identity of several outputs if in a broadcasting situation. The other bits of the subcells transmit data.

The function of stampers *IC1 to ICM* is to insert, within the cell control field of each cell, a time stamp supplied by time generator *TSG* as soon as the first subcell of this cell is received by the node. This time stamp *TSTP* indicates the
15 time slot during which the cell waiting time will expire. It is set as a function of the contents of the *TSG* counter at cell arrival time, and as a function of the total preset delay each cell must undergo. In this preferred method of implementation, modulo *TSTPmax* of the counter is selected to be equal to this preset total delay, the value of time stamp *TSTP* is then numerically equal to the value supplied by
20 the counter, due to modulo *TSTPmax*.

When one of input circuits *IL1 to ILM* receives a cell, it requests from management unit *BMMU* the addresses available to respectively store the subcells of this cell in buffer memory *BM*. To optimise the use of buffer memory *BM*, the subcells within the same cells are not stored at consecutive addresses but at
25 random addresses. Management unit *BMMU* includes a read write control circuit

WRC, storing the addresses available in buffer memory *BM* as soon as they are released after cell transmission, it also includes a storage link memory *SLM* storing all the addresses of locations within buffer memory *BM* respectively storing all subcells within the same cell. Each buffer memory location has a capacity equal to one subcell.

Implementation of buffer memory *BM* and management unit *BMMU* is within the scope of the expert in the field since it is described in particular in European patent application EP 0 441 787 (HENRION 18). Preferably, buffer memory *BM* and link memory *SLM* have the same set of addresses to facilitate implementation.

The request issued by one of input circuits *IL 1* to *ILM* is transmitted via bus *TDM1*, then via header processing circuit *HP* to management unit *BMMU*. The latter allocates to the subcells of the relevant cell a series of locations available within buffer memory *BM*. A series of addresses indicating these available locations is supplied by circuit *WRC*. Links between addresses in this series are created by storing this series of addresses in link memory *SLM* at consecutive addresses. Management unit *BMMU* supplies header processing management circuit *HP* with a value *FSA* which is the first address in this series of addresses of locations within buffer memory *BM*. Address *FSA* is retransmitted on the third output of circuit *HP*. Address *FSA* is written at a location available in address memory *FSMA*, the location address is supplied by the output of unit *CU*.

Address *FSA* will later be used to find all subcells of this cell in buffer memory *BM*: Using address *FSA* it is possible to read, in link memory *SLM*, the address of the second subcell in buffer memory *BM*. Then, using the address of this second subcell, it is possible to read in link memory *SLM*, the address of the

third subcell in buffer memory *BM*. Therefore, from a single *FSA* address, it is possible to successively find the addresses of all subcells within the same cell.

These addresses are then used to read the subcells in buffer memory *BM*.

In the cell control field of the first subcell of each received cell, circuit *HP* extracts the field containing time stamp *TSTP* and a field containing the identity of the output, or outputs *OU1* to *OUN*, via which the cell must be transmitted. It supplies the first input of control unit *CU* with a cell queued identifier which is made up of this information.

In order to transmit a cell, control unit *CU* is set into operation by output circuits *OL1* to *OLN* when one of these output circuits becomes available, i.e. when it has finished transmitting a cell. It sends a message *IDL* to bus *RQB*, this message contains the identity of the output available and is addressed to control unit *CU*. Control unit *CU* then determines which cell will be transmitted on this output. Unit *CU* sends, to the requesting output circuit, the address *FSA'* of a location, in buffer memory *BM*, containing the first subcell of a cell. Then, the output circuit requests buffer memory *BM* and management unit *BMMU* to be provided with the complete series of subcells of this cell. It then transmits it on its output.

Figure 2 represents a block diagram of an example of implementation of control unit *CU*, which includes:

- A waiting-cell memory *VIM*, which is a content addressable memory and has the same set of addresses as memories *FSAM* and *BM*, and has a one bit output for each memory location, the number of locations being selected as a function of the number *N* of node outputs, and of the average waiting time of cells within buffer memory *BM*.

- An arbitration and coding circuit *AC* having several inputs respectively connected to the outputs of memory *VIM*.

- A multiplexer *DMX* having a data input, *N* outputs and a control input.

- A logic circuit *TC*, referred to as cell transfer control circuit.

5 - A multiplexer *MUX* having two data inputs, one output and one control input (not shown)

- A logic circuit *FMM* which manages the addresses of memories *VIM* and *FSAM*.

10 - *N* content addressable queuing memories *QC1 to QCN* having the same set of addresses as memory *VIM*, and each queuing memory having a one bit output for each memory location.

- *N* arbitration circuits *FFO1 to FFON* respectively associated with the *N* memories *QC to QCN* and each having several inputs respectively connected to the outputs of one of the memories *QC1 to QCN*.

15 - *N* logic circuits referred to as queuing circuits, *SNL1 to SNLN* respectively associated with the *N* memories *QC1 to QCN*.

The first input of control unit *CU*, which receives the waiting-cell identifier supplied by header processing circuit *HP*, is connected to a write data input *wd* of memory *VIM*. The second input of control unit *CU*, which receives address *FSA'* supplied by the data output of memory *FSAM*, is connected to bus *RQB* via an interface (not shown). Bus *RQB* is also connected via this interface to a first common input of queuing circuits *SNL1 to SNLN* to supply a signal *IDL* to one of these circuits when the corresponding output circuit *OL1 to OLN* is available to transmit a cell.

25 Waiting-cell Memory *VIM* also includes: an address input *ad* connected

to an output of management circuit *FMM*; and a comparison input *ci* connected to a first output of transfer control circuit *TC*. When a binary word is applied at the comparison input *ci*, memory *VIM* compares it with the binary words respectively contained within its memory locations. When comparisons generate a single positive result, memory *VIM* supplies a bit having a value of 1 to the output corresponding to this memory location. When comparisons generate several positive results, memory *VIM* supplies a bit having a value of 1 to each of the outputs corresponding to the memory locations where the result is positive.

The function of arbitration and coding circuit *AC* is to code each of the signals in the form of a binary word. Therefore, a first output of circuit *AC* supplies a binary word *NA* whose value is the address of the relevant memory location. The first output of arbitration and coding circuit *AC* is connected to the data input of demultiplexer *DMX* and to an input of management circuit *FMM*. Should the comparisons generate several positive results, circuit *AC* codes them successively, in the descending order of addresses for instance. Circuit *AC* has a second output which supplies, to an input of transfer control circuit *TC* and to a second input common to queuing circuits *SNL1* to *SNLN*, a logic signal *C* when there is at least one positive result, and which maintains it until circuit *AC* has supplied all addresses corresponding to these positive results. It is also fitted with a third output, connected to a third input common to all queuing circuits *SNL1* to *SNLN* to supply them with a logic signal *QR* made up of a pulse for each address supplied by circuit *AC*.

A second output of transfer control circuit *TC* is connected to the control input of demultiplexer *DMX* and to a fourth input common to all queuing circuits *SNL1* to *SNLN*.

Multiplexer MUX is fitted with a first input connected to a common output of arbitration circuits $FFO1$ to $FFON$; a second input connected to the output of address management circuit FMM ; an output making up the output of control unit CU , and connected to the read-write address input ad in memory $FSAM$; and a control input (not shown) which is connected to an output of a sequencer (not shown) which supplies control signals to all the components making up the control unit CU .

Demultiplexer DMX is fitted with N outputs respectively connected to the write address inputs wa of queuing memories $QC1$ to QCN . Each of queuing memories $QC1$ to QCN is fitted with: a comparison input ci , and a write data input wd , which are respectively connected to two outputs of queuing circuit $SNL1$ to $SNLN$, which correspond to the relevant memory.

Each queuing circuit $SNL1$ to $SNLN$ is fitted with:

- A last written sequence number counter $LWSN$.
- A last read sequence number counter $LRSN$,
- A logic circuit for sequence number management SNM .

Each counter $LWSN$ and $LRSN$ contains a control input and an output respectively connected to an output and an input of circuit SNM . Circuit SNM has four inputs which respectively constitute the first, second, third and fourth input of the queuing circuit; and has two outputs which respectively constitute the two queuing circuit outputs.

Let's successively consider the three main stages in cell processing performed by the resequencing unit: cell reception and cell queuing in the waiting-cell memory then cell finding, retrieval and transfer to the queuing memory, when the waiting time has expired, and finally cell transmission when the destination

output becomes available. First, let us assume that the unit only receives cells which are each intended for a single output represented by address OA .

When a cell is received by the resequencing unit, it is written to the buffer memory BM , and the buffer memory management unit $BMMU$ supplies to the data input di of memory $FSAM$, the address FSA of the buffer memory location containing the first subcell of this cell. Simultaneously, header processing circuit HP supplies a waiting cell identifier $TSTP\ OA$, to the write data input wd of memory VIM . This identifier contains: a field $TSTP$ which is a time stamp indicating the time slot during which the waiting time will expire; and a field OA indicating the cell destination output.

Memory address management circuit FMM , managing the addresses of memories VIM and $FSAM$, supplies an address available FA , at the write address input ad of memory VIM , and at the address input ad of memory $FSAM$, via multiplexer MUX. Therefore, identifier $TSTP-OA$ and first subcell address FSA are respectively written to memories VIM and $FSAM$ at the same address. A cell waiting time is equal to an integer multiple of the subcell period. At regular intervals, N -times smaller than the subcell period, the first output of transfer control circuit TC supplies a cell to-be-queued identifier $TSTP'-OA'$, which is made up of: $TSTP'$, the time stamp values of all cells whose waiting time expired during the current subcell period; and of OA' , the identity of a single output of the node.

Each cell to be queued identifier may identify several cells which are to be transmitted on the same output and whose waiting times expire during the same subcell period. Upon expiry of its waiting time a cell is authorised to be queued, in a symbolic form within the queuing memory corresponding to the destination output. Nevertheless, effective transmission of the cell is not yet

authorised.

Circuit TC includes a counter modulo $TSTP_{max}$ which is incremented at each subcell period and is initialised such that the value $TSTP'$ it supplies is equal to the value of the current time stamp minus a preset delay, equal for instance to the maximum duration for the transfer of a cell within the switched network SW . In a particularly simple example of implementation, the value of modulo $TSTP_{max}$ is chosen equal to the maximum duration for the transfer of a cell within the switched network SW , consequently, the value of $TSTP'$ is numerically equal to the value of the current time stamp $TSTP$, this permits to use the same counter for the current time stamp generator TSG and for the $TSTP'$ counter in the transfer control circuit TC .

Control circuit TC includes a second counter. For each subcell period, it supplies N values of OA' . Thus, circuit TC determines N cell to be queued identifiers $TSTP'-OA'$, made up of the same value $TSTP'$ and of N values of output address OA' which is for instance successively equal to 1, ..., N . The value of this output address is simultaneously supplied on the second output of circuit TC to be applied to the control input of demultiplexer DMX and to the fourth input common to all queuing circuits $SNL1$ to $SNLN$.

Each identifier $TSTP' OA'$ is applied to comparison input ci of memory VIM to find whether there are any waiting cell identifiers $TSTP-OA$ corresponding to this cell to be queued identifier. If the comparisons carried out by memory VIM , between identifier $TSTP'-OA'$ and identifiers $TSTP OA$ it contains, give positive results, there is a logic signal having a value of 1 on certain outputs of this memory. For instance, each of the outputs corresponding to addresses $AA1$, $AA2$, $AA3$ of this memory, supplies a signal indicating that the addresses contain

waiting cell identifiers $TSTP\ OA$ having the value of cell to be queued identifier $TSTP'-OA'$.

Arbitration and coding circuit AC receives these signals and first supplies a binary word NA having the value $AA1$, to the data input of demultiplexer DMX , and to the input of address management circuit FMM . It also supplies a logic signal C to transfer control circuit TC to indicate that at least one cell was found, and it supplies a logic signal QR to queuing circuits $SNL1$ to $SNLN$ asking them to queue up the cell which was found. Address OA' is simultaneously supplied to queuing circuits $SNL1$ to $SNLN$ in order to validate only the one corresponding to the destination output of the cell found. Furthermore, address OA' controls demultiplexer DMX such that the latter transmits address NA only to the queuing memory corresponding to the destination output of the cell found.

Then, circuit AC supplies an address NA having the value $AA2$ by maintaining signal C , and reiterating signal QR requesting a queue up. Finally, circuit AC supplies an address NA having the value $AA3$ by maintaining signal C , and reiterating signal QR to again request a queue up. Finally, circuit AC removes signal C to indicate to circuit TC that all cells found have been queued, and it is therefore possible to increment the value of output address OA' . All these queuing operations for the N values of output address OA' must be performed during a subcell period, such that the value of $TSTP'$ can be incremented in step with the incrementation of the values of the current time stamp $TSTP$.

Each time a cell has been queued, the location occupied by its identifier $TSTP-OA$ in memory VIM can be re used. This is why the address management circuit FMM of memories VIM and $FSAM$ each receives a value of address NA to store it as an available address.

When one of sequence number management circuits *SNM* receives logic signal *C*, being enabled by an output address *OA'* which is effectively its own, it increments by one unit, then reads, the contents of the last written sequence number counter *LWSN*. It then writes the contents value *SN*, at address *NA*, into queuing memory *QC1 to QCN* corresponding to output address *OA'*. Each pulse of signal *QR* controls the writing of a value *NA* to the same queuing memory.

In the example where *NA* successively takes the values *AA1*, *AA2*, *AA3*, sequence number *SN_i* is written at address *AA1* in the queuing memory corresponding to output address *OA'*. These operations are reiterated to process the next address: *AA2*. The same sequence number *SN_i* is written at address *AA2* in the same queuing memory. These operations are again reiterated to process the next address: *AA3*. Thus, sequence number *SN_i* is written at address *AA3* in the same queuing memory.

When there are no cells to be queued, circuit *AC* does not supply any signal *C* or *QR*. The value of the address *NA* supplied by circuit *AC* is nil, and does not mean anything. It is not taken into account, since there is no positive result signal *C*, and no queuing request signal *QR*.

We shall now consider the transmission of a cell when its destination output is available. The output circuit *OU1 to OUN* whose output is available sends a message to bus *RQB*. A signal *IDL* reaches the queuing circuit *SNL1 to SNLN* corresponding to the output available. Signal *IDL* controls the sequence number management circuit *SNM* to increment by one unit, then read, the contents of the last read sequence number counter *LRSN*. This content constitutes a sequence number *SN'* which will be searched in the queuing memory *QC1 to QCN* corresponding to the output available. Uniform incrementation of this sequence

number SN' ensures that the cells are retrieved in the sequence they were numbered at queuing up time, i.e. the sequence defined by the values of $TSTP'$, which is the chronological sequence in which the node receives the cells.

This number SN' is supplied at the comparison input ci of this queuing memory. This memory supplies a logic signal to one or several of its outputs, depending on whether there is one or several locations of this memory containing a sequence number identical to the number being searched: SN' . Arbitration circuit $FFO1$ to $FFON$ associated with the relevant memory, supplies a binary word whose value is successively equal to the rank of each of the outputs of this memory, which supply a signal. The values of these ranks represent the addresses NA' of the queuing memory locations containing the number being searched. These addresses NA' may for instance be successively restored in descending rank order.

When several cells have the same time stamp, they are queued with the same sequence number SN , since they can be transmitted in any given sequence without drawback. An advantage of the implementation method described above is that the capacity required for counters $LWSN$ and $LRSN$ is smaller than if a different sequence number were assigned to each cell queued in a given queuing memory.

For instance, if the sequence number being searched is SN_i , which is stored at three addresses $AA1$, $AA2$, $AA3$ in this memory, the arbitration circuit successively supplies the values $AA1$, $AA2$, $AA3$ of address NA' to the first input of multiplexer MUX . The latter sends these addresses to memory $FSAM$ to successively read three values of first subcell address FSA' . Each value of address FSA' is transmitted via bus RQB to the output circuit $OL1$ to OLN which sent the message containing signal IDL indicating that an output is available. The output

circuit retransmits these values of first cell address FSA' , via bus $TDM2$, to the buffer memory management unit $BMMU$ to read from this buffer memory BM all the subcells of the three cells corresponding to the three values of address FSA' . Then, these subcells are transmitted via bus $TDM2$ to this output circuit which

5 transmits them through its output.

The operation of this example of implementation can be slightly modified to allow for broadcasting of one cell to several outputs. The single output address OA is replaced with a binary word OM containing a number of bits equal to the number N of node outputs. Each cell destination output is indicated by the value 1 and each output not intended to receive a cell is indicated by the value 0, for

10 instance. Waiting cell memory VIM stores waiting cell identifiers $TSTP-OM$ instead of identifiers $TSTP-OA$.

Memory VIM has a comparison input ci , but it operates somewhat differently from the above-described memory VIM , since comparison involves field $TSTP'$ and the only bit in OM' which is not nil. The $N-1$ other bits in OM' and the corresponding $N-1$ other bits in the field OM of the stored identifiers $TSTP-OM$ are not to be compared. The bits of field OM in each $TSTP-OM$ word must be masked by the bits of field OM' in $TSTP'-OM'$ before comparing identifier $TSTP'-OM'$ with each waiting cell identifier $TSTP OM$ stored in memory VIM

Transfer control circuit TC is modified to supply cell to be queued identifiers $TSTP'-OM'$, where field $TSTP'$ is still the identity of a time slot during which a waiting time expires, but where OM' is an N bit word where only one bit has a value of 1. The rank of this bit designates a single output, for which circuit TC searches for cells to be queued.

25 Circuit TC includes a counter which successively supplies all values from

0 to $TSTP_{max}$, modulo $TSTP_{max}$, to make up field $TSTP'$; and a counter associated with a decoder which, for each value of $TSTP'$, successively supplies N values:

0000...0001

5

0000...0010

0000...0100

.....

1000...0000 to make up field OM' . The other components of the

resequencing unit are not modified.

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Let's consider an example where there are $N = 8$ outputs and where two cells have waiting times due to expire during the same subcell period, indicated by time stamp $TSTP_0$; and where the first cell is intended for the first and the fifth outputs, while the second cell is intended for the third and the fifth outputs. When the cell waiting times expire, transfer control circuit TC supplies a series of 8 cell to be queued identifiers $TSTP' OM'$ having the following values:

$TSTP_0$ - 0000...0001

$TSTP_0$ - 0000...0010

$TSTP_0$ - 0000...0100

.....

$TSTP_0$ - 1000...0000

In this example, circuit AC successively supplies:

1) A value $AD1$ of the address NA corresponding to the first cell together with positive result signal C and queuing request signal QR .

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2) A value nil of the address NA without signal C and without signal QR .

3) A value $AD2$ of the address NA corresponding to the second cell together

with signal C and signal QR

4) A value nil of the address NA without signal C and without signal QR .

5) A value $AD1$ of the address NA corresponding to the first cell together with a pulse of signal QR ; immediately followed by the value $AD2$ of the address NA

5 corresponding to the second cell, together with another pulse of signal QR ; and a common signal C .

6, 7, 8) Three successive values of the address NA , which are nil, without signal QR and without signal C .

10 In this example, only one sequence number is written to the queuing memory corresponding to the fifth output, to queue up two cells.

A location in memories VIM and FSA must not be re used while a cell has not been queued in the queuing memories of all destination outputs. All values of field OM' in identifier $TSTP'-OM'$ are scanned during a subcell period, consequently, any address NA supplied by circuit AC can be re-used by the address management circuit FMM as soon as the next period.

The unit in accordance with the invention is applicable for fixed length cells or for cells containing a variable number of fixed length subcells. To prevent any de-sequencing or loss of cell, the capacity of counters $LWSN$ and $LRSN$, supplying sequence numbers SN and SN' , must be greater than the maximum number of subcells a cell can contain, plus the number of subcell periods corresponding to the maximum transit time in the switching network SW .

To prevent any de sequencing, while tolerating the eventual loss of certain cells, it is possible not to abide by the above condition, in which case any overflow of counter $LWSN$ compared with counter $LWRN$ must be detected, to prevent new cells from been queued when a queuing memory is full, in order to keep the oldest

cells and tolerate the loss of the most recent ones, but always restores cells in the correct sequence.

A variation of the implementation consists of assigning a time stamp $TSTP$ to each cell outgoing the network SW , instead of assigning it at the network SW input. In this case, the time stamp generator TSG is different. It still includes a clock defining time slots of constant duration equal to a subcell period, and a counter modulo $TSTP_{max}$. But it also includes: a circuit to estimate the time taken by each cell to transit through the network SW ; a circuit to subtract this estimate from the contents of the counter; and a circuit to add to the result the duration of the total delay each cell must undergo. The result of this calculation constitutes the value of stamp $TSTP$ indicating the time slot during which the cell waiting time expires. It can be used exactly as the value of stamp $TSTP$ assigned at the network SW input, as described above. Implementation of these circuits is within the capabilities of the expert in the field.

Preferably, the time unit selected is equal to the subcell period since the duration of each cell is at least equal to one subcell period, though it is possible to use a smaller time unit.

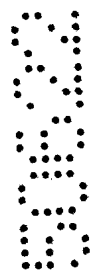
The claims defining the invention are as follows:

1. A resequencing unit for a node in a cell switching system, each cell being made up of a variable number of fixed length subcells, this node including a switching network transmitting cells with first variable delays, all subcells within the same cell undergoing a same first delay; this resequencing unit being fitted with some means used to store all cells which were transmitted via the switching network, and to transmit these cells over at least one output of the resequencing unit, upon expiry of various waiting times resulting in second delays such that, for each cell, the sum of the first delay and the second delay is equal to a preset value roughly identical for all cells, these means including:

- a buffer memory to store the subcells of each cell received by the resequencing unit;
- an address memory to store the address of the buffer memory containing the first subcell of each cell;
- means used to find the address of the address memory containing the first subcell of a cell, once the cell waiting time has expired and that an output designed to transmit this cell has become available;

wherein said means used to find the address of the buffer memory containing the first subcell of a cell include:

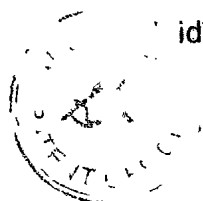
- a content addressable memory referred to as waiting-cell memory, to store a waiting-cell identifier, when a cell is stored in the buffer memory ; this identifier being stored at an address identical to that where the first subcell address is stored in the address memory; and this identifier consisting of: a time stamp identifying a time slot during which the cell waiting time expires, and of the



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identity of at least one output where the cell is to be transmitted.

- means of finding, within the waiting-cell memory, the identifier of each cell when its waiting time expires, and of supplying, for each identifier found, the address of the waiting-cell memory which contains this found identifier;

5 - content addressable queuing memories respectively associated with the node outputs, to store a sequence number for each cell intended for the output associated with the relevant memory;

- means of determining and writing a sequence number into a queuing memory, at the address supplied by the means used to find the identifier of each

10 cell when its delay has expired;

- means of finding, in ascending order, each sequence number stored in the queuing memory of an output, when this output becomes available; and of restoring the address of this queuing memory containing the sequence number found; *and*

15 means of reading a first subcell address from the address memory at the address restored by the means used to find each sequence number.

2. A unit as claimed in claim 1, wherein said means of finding, within the waiting-cell memory, the identifier of each cell when its waiting time expires, and of supplying, for each identifier found, the address of the waiting-cell memory which contains this found identifier, include:

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- means used to supply, to a comparison input of waiting cell memory, for each time slot corresponding to a waiting time expiring, a series of cell to-be-transmitted identifiers, each comprising of the identity of the current time slot, and the identity of a single node output; this series being made up of the identities of

all node outputs;

- means coupled to outputs of waiting cell memory to successively supply each address of the waiting cell memory, containing the identifier found.

3. A unit as claimed in claim 1, wherein said means of determining and writing

5 to a queuing memory a sequence number, include for each node output, a counter supplying a sequence number which is incremented by one unit when at least one waiting cell identifier is found in the waiting cell memory for a given time slot and a given output.

4. A unit as claimed in claim 1, said means of finding, in an ascending order,

10 each stored sequence number, include for each node output, a counter supplying a sequence number to be found which is incremented by one unit when this output becomes available, this sequence number to be found being applied to the comparison input of the queuing memory associated with this output.

15 5. A re-sequencing unit substantially as herein described will reference to Figures 1 - 2 of the accompanying drawings.

DATED THIS *TWENTY-FOURTH* DAY OF *APRIL 1996*

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ABSTRACT

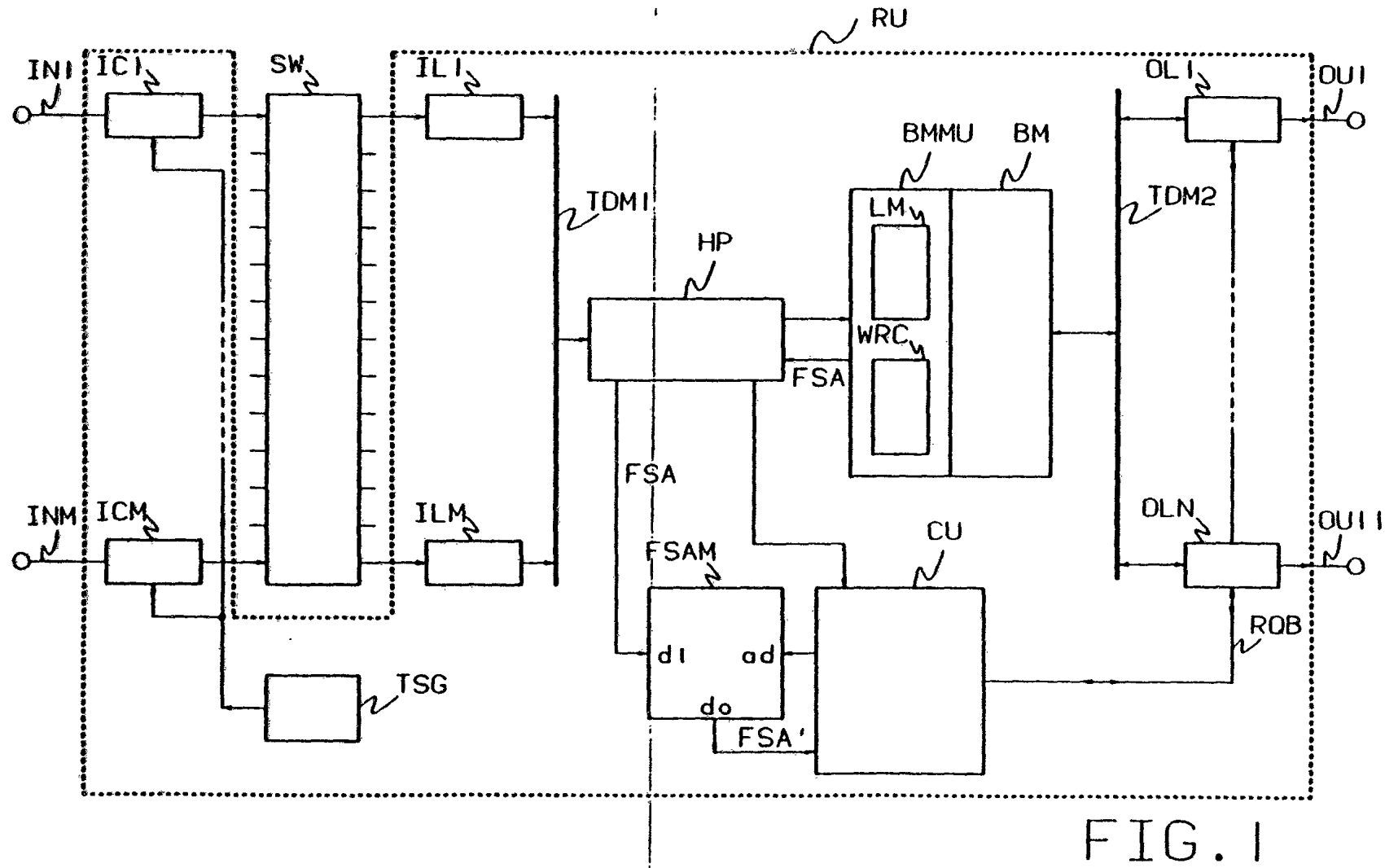
A resequencing unit for a node in a cell switching system, including a time stamp generator (TSG), to assign a time stamp to each cell, a buffer memory (BM), an address memory (FSAM) to store the address of the first subcell of each cell, a link memory (LM), and

A circuit (CU) to find the address of the buffer memory containing the first subcell of a cell. This circuit includes in particular: a content addressable memory, to store a waiting cell identifier, each identifier being made up of the identity of a time slot during which the cell waiting time will expire, and the identity of at least one output where the cell is to be transmitted; and a queuing memory for each output, where is written a sequence number each time a waiting time expires for at least one cell intended to be transmitted to this output; each queuing memory is a content addressable memory, and the sequence numbers are searched according to an ascending order, when this output is available.

Applicable to asynchronous transfer mode telecommunication networks.

FIGURE TO BE PUBLISHED: Figure 1.

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