

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
29 December 2004 (29.12.2004)

PCT

(10) International Publication Number
WO 2004/113935 A2

(51) International Patent Classification⁷: **G01R 1/04**

(21) International Application Number:
PCT/US2004/019760

(22) International Filing Date: 21 June 2004 (21.06.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/480,419 20 June 2003 (20.06.2003) US

(71) Applicant (for all designated States except US): **THE TRUSTEES OF DARTMOUTH COLLEGE** [US/US];
11 Rope Ferry Road, Hanover, NH 03755 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **SULLIVAN, Charles, Roger** [US/US]; 13 Gilson Road, West Lebanon, NH 03784 (US). **PRABHAKARAN, Satish** [IN/US]; 13 A Seminary Hill, West Lebanon, NH 03755 (US).

(74) Agent: **KNOPS, Peter, C.**; Lathrop & Gage LC, Suite 2400, 2345 Grand Boulevard, Kansas City, MO 64108 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— without international search report and to be republished upon receipt of that report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: LOW IMPEDANCE TEST FIXTURE FOR IMPEDANCE MEASUREMENTS

(57) Abstract: A test fixture couples with a test instrument to measure impedance of a device. An upper layer of the test fixture has (a) a first and a second solder pad for electrical connection to the device, (b) a first, second, third and fourth tri-solder pad for electrical connection to four SMA connectors of the type that match the test instrument, (c) a first copper track for connecting the first solder pad to a middle solder pad of the first tri-solder pad, (d) a second copper track for connecting the first solder pad to a middle solder pad of the second tri-solder pad, (e) a third copper track for connecting the second solder pad to a middle solder pad of the third tri-solder pad, and (f) a fourth copper track for connecting the second solder pad to a middle solder pad of the fourth tri-solder pad. Each tri-solder pad has a pair of ground solder pads. A lower layer of the test fixture has copper tracks connected to ground and to each pair of ground solder pads. A polyimide substrate of the test fixture has substantially uniform thickness separating the upper layer from the bottom layer.



WO 2004/113935 A2

LOW IMPEDANCE TEST FIXTURE FOR IMPEDANCE MEASUREMENTS

RELATED APPLICATIONS

This application claims priority to U.S. Application No. 60/480,419, entitled
5 Low Impedance Test Fixture for Impedance Measurements and incorporated herein
by reference.

BACKGROUND

For electrical and electronic component testing, a test fixture is a convenient
and reliable way of connecting a "device under test" ("DUT") to test equipment. The
10 test fixture is designed to remove measurement current from the sensing circuit,
thereby eliminating spurious voltages from the sensing circuit. Typically, a four-
terminal-pair ("4TP") test fixture is used to measure impedance of electronic
components. The 4TP test fixture attempts to measure the voltage across the device
under test and the current flowing there through. One pair of terminals measures
15 current and a second pair measures voltage.

The impedance of the DUT is calculated from the relationship $Z=V/I$, where
Z is the impedance of the DUT, V is the voltage measured across the DUT, and I is
the current flowing through the DUT. The measurement current is normally
sinusoidal, and includes both magnitude and phase components for current and
20 voltage. From these measurements, both the resistive and reactive components of the
DUT are determined. For example, the impedance of an inductor consists of both its
inductance and a resistive components.

The test fixture typically incorporates stray impedance. In cases where the
stray impedance is significantly less than the impedance of the DUT, it is often
25 ignored. The stray impedance can be reduced by a calibration procedure, which
involves temporarily replacing the DUT with a short, and then 'zeroing' test
equipment (often achieved by an auto balance configuration).

A wide range of commercially available test fixtures are used throughout
industry; they are often designed for ease of use, and accept a wide range of
30 DUTs.

Recent improvements in test equipment performance allow low impedances

to be measured more accurately. However, the stray impedance of most test fixtures significantly limits the accuracy of these measurements. The way in which the DUT is mounted contributes significantly to the stray impedance. Most commercially available 4TP test fixtures have stray impedance levels that prevent accurate
5 measurement of low impedances, even after calibration.

SUMMARY

A test fixture couples with a test instrument to measure impedance of a device. An upper layer of the test fixture has (a) a first and a second solder pad for electrical connection to the device, (b) a first, second, third and fourth tri-solder pad
10 for electrical connection to four SMA connectors of the type that match the test instrument, (c) a first copper track for connecting the first solder pad to a middle solder pad of the first tri-solder pad, (d) a second copper track for connecting the first solder pad to a middle solder pad of the second tri-solder pad, (e) a third copper track
15 for connecting the second solder pad to a middle solder pad of the third tri-solder pad, and (f) a fourth copper track for connecting the second solder pad to a middle solder pad of the fourth tri-solder pad. Each tri-solder pad has a pair of ground solder pads. A lower layer of the test fixture has copper tracks connected to ground and to each pair of ground solder pads. A polyimide substrate of the test fixture has uniform thickness separating the upper layer from the bottom layer.

20 In one embodiment, a process measures impedance of a device with test equipment and a low impedance test fixture. A short is soldered to solder pads of the test fixture and the test equipment is calibrated to the test fixture. The device is soldered to the solder pads in place of the short. The test equipment is operated to measure the impedance of the device.

25 In one embodiment, a test fixture couples with a test instrument to measure impedance of a device. An upper layer has (a) a first and a second solder pad for electrical connection to the device, (b) a plurality of multi-solder pads for electrical connection to a like plurality of connectors of the type that match the test instrument, (c) a plurality of copper tracks for connecting the first solder pad to select solder pads
30 of first set of the multi-solder pads, and (c) a plurality of copper tracks for connecting the second solder pad to select solder pads of a second set of the multi-solder pads. A lower layer has copper tracks connected to ground and to at least one ground solder

pad of each of the multi-solder pads. A polyimide substrate of uniform thickness separates the upper layer from the bottom layer.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a block diagram illustrating an embodiment of one low impedance test fixture for impedance measurement.

FIG. 2 shows a top view, including an upper layer embodiment of the test fixture of FIG. 1.

FIG. 3 shows a top view, including a lower layer embodiment of the test fixture of FIG. 1.

FIG. 4 is a flowchart illustrating a process embodiment for measuring impedance with a low impedance test fixture.

DETAILED DESCRIPTION OF THE FIGURES

FIG. 1 is a block diagram illustrating one low impedance test fixture 10 for impedance measurement. In FIG. 1, test fixture 10 is illustratively shown measuring the impedance of a device under test ("DUT") 12, and is connected to a test instrument 16 by connections 18, 20, 22 and 24. In one embodiment, test fixture 10 is designed to measure the impedance of power devices (e.g., DUT 12) using a four-terminal-pair ("4TP") auto balance bridge system (described below). Such power devices are typically utilized in high-performance, high-current power supplies where measurement of low impedances is critical. To measure low impedances, particularly at frequencies extending into the MHz range, test fixture 10 operates with low stray impedance, since stray impedance introduces errors into measurements. Test fixture 10 has less than about 100pH stray inductance and is therefore suitable for such measurements.

Test instrument 16 is for example an impedance analyzer that uses the 4TP auto balance bridge system (e.g., analyzer 4294A made by Agilent).

In one embodiment, test fixture 10 includes a two-layer printed circuit board construction based on a substrate of 75 μ m polyimide (shown as surface 34 in FIG. 2), with copper tracking. In FIG. 2, layer A represents an upper layer of test fixture 10. Layer A shows two solder pads, 30 and 32, that connect to DUT 12 (e.g., DUT 12 is soldered to pads 30 and 32 to make the measurement). Layer A also contains solder

pads 44, 46, 48, 50, 52, 54, 56, 58, 60, 62, 64 and 66 that allow surface mount assembly ("SMA") type connectors to be attached to test fixture 10. SMA type connectors provide for connectivity between test fixture 10 and test instrument 16, for example. Three solder pads connect to each SMA connector. Solder pads 44, 46 and 48 connect to a first SMA connector; solder pads 50, 52 and 54 connect to a second SMA connector; solder pads 56, 58 and 60 connect to a third SMA connector; and solder pads 62, 64 and 66 connect to a fourth SMA connector. Layer A also contains tracks 36, 38, 40 and 42 that respectively connect DUT 12 to solder pads 46, 52, 58 and 64.

FIG. 3 is a schematic diagram illustrating a layer B representing a lower layer of test fixture 10, viewed from above. Layer B shows solder pads 44 through 66 of FIG. 2 (in dotted outline) for purposes of illustration, though some or all pads 44 through 66 may alternatively be included on lower layer B of test fixture 10 as a matter of design choice. Layer B also includes a ground track 68 that connects to solder pads 44, 48, 50, 54, 56, 60, 62 and 66 of layer A (and/or optionally of layer B).

With reference to FIG. 2 and FIG. 3, it can be seen that ground track 68 is a closely-spaced ground/return path that induces low stray inductance and duplicates boundary conditions and field configuration in a typical high-performance application. By using wide copper traces on the thin polyimide substrate, stray inductance is reduced, for example, to 62pH. While the resistance of solder pads 30 and 32 may in some cases be significant, results are more repeatable than those obtained using test fixtures with dry contacts. Further, solder pads 30 and 32 realistically model the way in which a component is used.

Solder pads 32 and 32 are large rectangular areas on layer A with equal areas in ground track 68 of layer B. On layer B, ground track 68 follows the same path as tracks 36, 38, 40 and 42 of layer A, thereby forming 50 Ohm transmission lines used by test instrument 16, FIG. 1.

Solder pads 30 and 32 may be designed such that measurements are repeatable with DUT 12 soldered in different positions. Solder pads 30 and 32 may thus be constructed to minimize effects of different soldering positions, particularly when replacing a short, soldered to solder pads 30 and 32 for calibration of test fixture 10, with DUT 12, which would induce errors.

Test fixture 10 may reduce the effect of stray capacitance due to the shielding effect of the close-spaced ground track 68. The combination of low stray inductance and low stray capacitance means that the frequency range of test fixture 10 is 0 – 40GHz without the resonant frequency of test fixture 10 having measurement effect. Further, the low stray impedance of test fixture 10 may allow test fixture 10 to measure low impedance devices more accurately than prior art test fixtures. The design of test fixture 10 may reduce construction costs compared to other commercially available test fixtures.

FIG. 4 shows a process 100 for measuring impedance of a device with test equipment and a low impedance test fixture. In step 102, a short is soldered to solder pads of the test fixture and the test equipment is calibrated to the test fixture. In step 104, the device is soldered to the solder pads in place of the short. In step 106, the test equipment is operated to measure the impedance of the device.

Changes may be made in the above methods and systems without departing from the scope hereof. It should thus be noted that the matter contained in the above description or shown in the accompanying drawings should be interpreted as illustrative and not in a limiting sense. The following claims are intended to cover all generic and specific features described herein, as well as all statements of the scope of the present method and system, which, as a matter of language, might be said to fall there between.

CLAIMS

What is claimed is:

1. A test fixture for coupling with a test instrument to measure impedance of a device, comprising:
 - 5 an upper layer having (a) a first and a second solder pad for electrical connection to the device, (b) a first, second, third and fourth tri-solder pad for electrical connection to four SMA connectors of the type that match the test instrument, (c) a first copper track for connecting the first solder pad to a middle solder pad of the first tri-solder pad, (d) a second copper track for connecting the first solder pad to a middle solder pad of the second tri-solder pad, (e) a third copper track for connecting the second solder pad to a middle solder pad of the third tri-solder pad, and (f) a fourth copper track for connecting the second solder pad to a middle solder pad of the fourth tri-solder pad, each tri-solder pad having a pair of ground solder pads;
 - 10 a lower layer having copper tracks connected to ground and to each pair of ground solder pads; and
 - 15 a polyimide substrate of uniform thickness separating the upper layer from the bottom layer.
2. A method for measuring impedance of a device using a test fixture connected to a test instrument, wherein the test fixture has low stray impedance and solder pads for connection to the device, comprising:
 - 20 soldering a short to the solder pads and calibrating the test equipment to the test fixture;
 - soldering the device to the solder pads in place of the short; and
 - operating the test equipment to measure the impedance of the device.
- 25 3. A test fixture for coupling with a test instrument to measure impedance of a device, comprising:
 - an upper layer having (a) a first and a second solder pad for electrical connection to the device, (b) a plurality of multi-solder pads for electrical connection to a like plurality of connectors of the type that match the test instrument, (c) a plurality of
 - 30 copper tracks for connecting the first solder pad to select solder pads of first set of the

- multi-solder pads, and (c) a plurality of copper tracks for connecting the second solder pad to select solder pads of a second set of the multi-solder pads,
- a lower layer having copper tracks connected to ground and to at least one ground solder pad of each of the multi-solder pads; and
- 5 a polyimide substrate of uniform thickness separating the upper layer from the bottom layer.

FIG 1

1/3

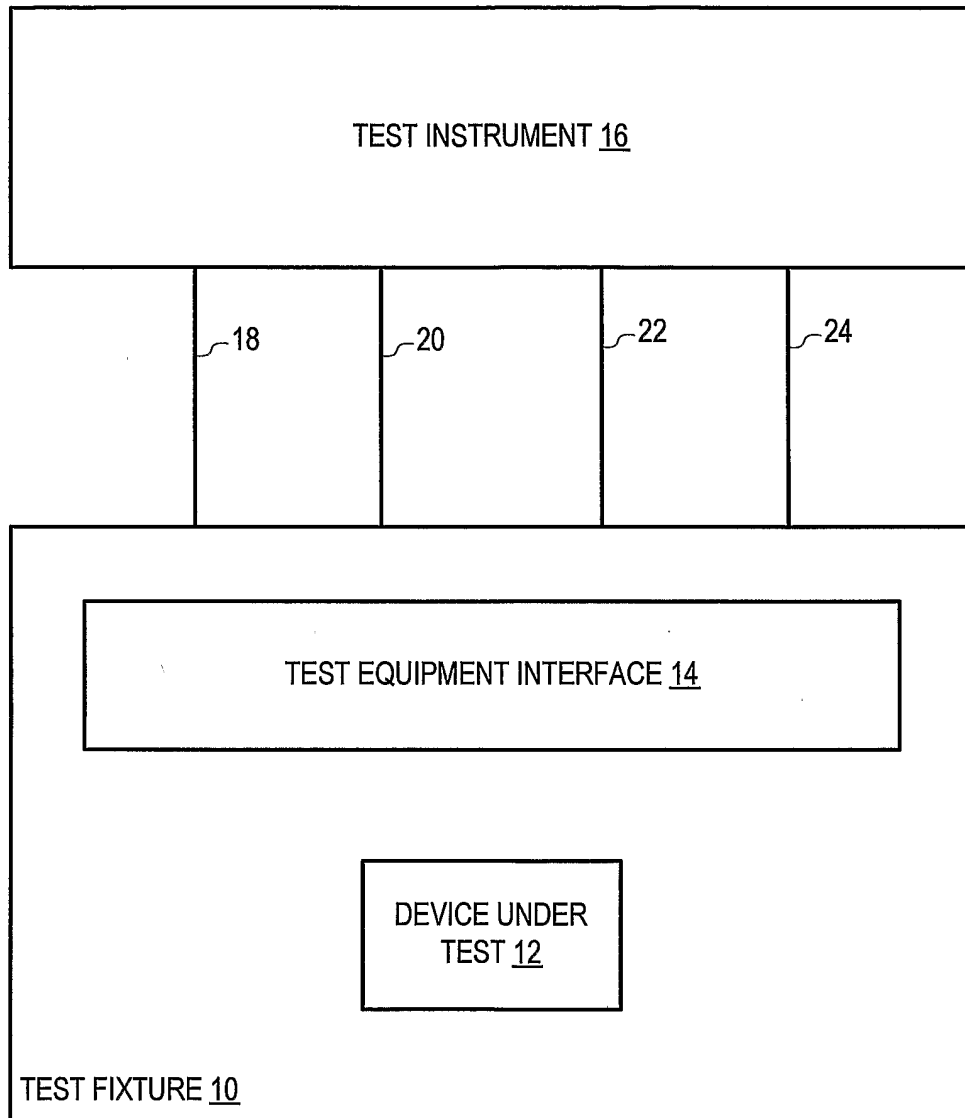


FIG 2

2/3

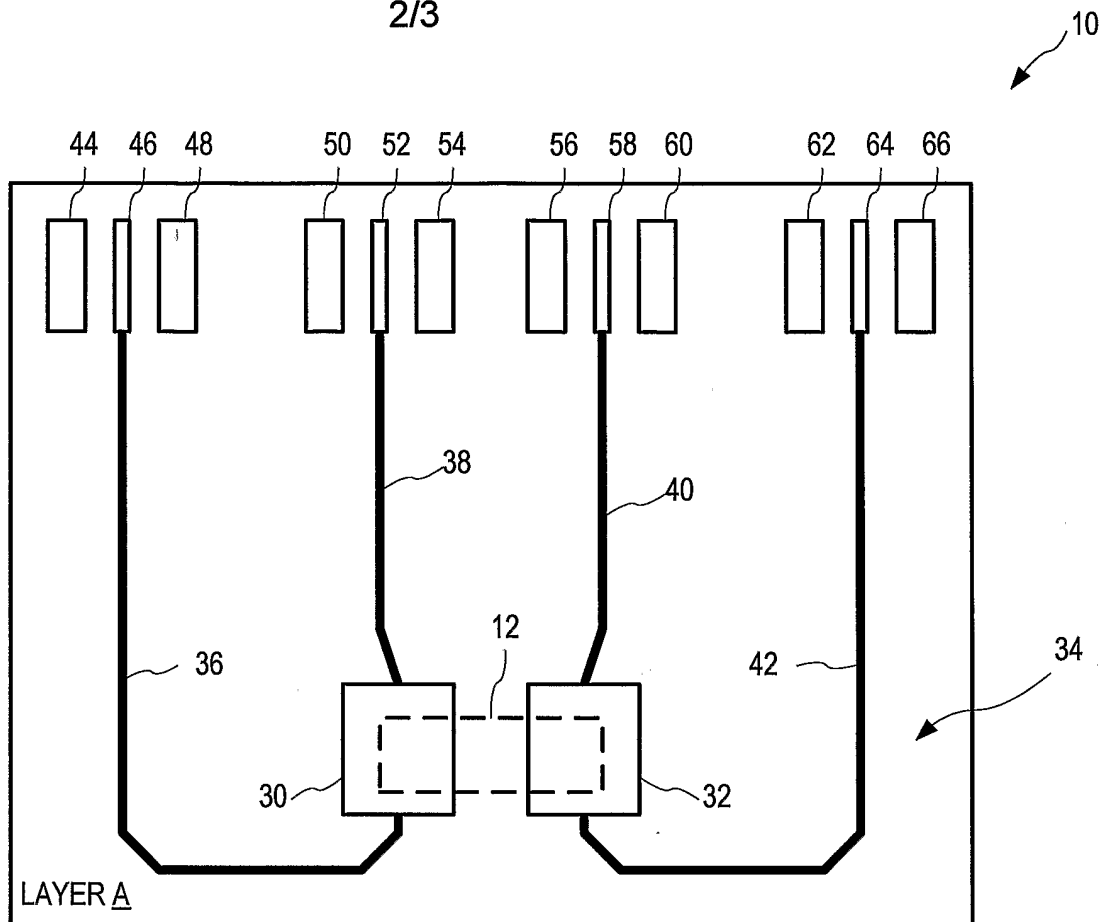
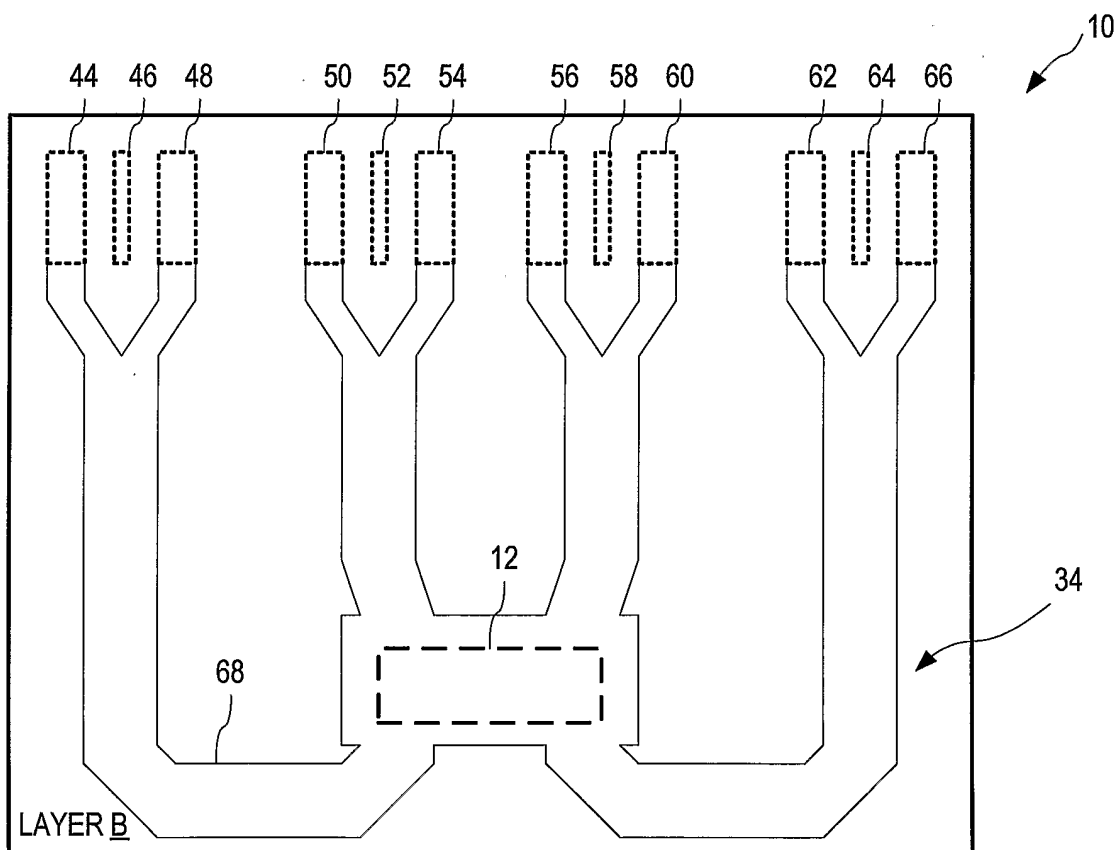


FIG 3



3/3

FIG 4

