



(51) International Patent Classification:
G11C 21/02 (2006.01)

(21) International Application Number:
PCT/US2015/014324

(22) International Filing Date:
3 February 2015 (03.02.2015)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
61/935,310 3 February 2014 (03.02.2014) US

(71) Applicant: CORNELL UNIVERSITY [US/US]; 395
Pine Tree Road, Suite 310, Ithaca, NY 14850 (US).

(72) Inventors: LAL, Amit; 610 The Parkway, Ithaca, NY
14850 (US). KUO, Justin, C.; 220 Triphammer Road,
Apt. 11, Ithaca, NY 14850 (US).

(74) Agent: AI, Bing; Perkins Coie LLP, P.O. Box 1247,
Seattle, WA 98111-1247 (US).

(81) Designated States (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,
BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,

DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR,
KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG,
MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM,
PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,
SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ,
TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU,
TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,
DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,
LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,
SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, KM, ML, MR, NE, SN, TD, TG).

Published:

- with international search report (Art. 21(3))
- before the expiration of the time limit for amending the
claims and to be republished in the event of receipt of
amendments (Rule 48.2(h))

(88) Date of publication of the international search report:
30 December 2015

(54) Title: PIEZOELECTRIC AND LOGIC INTEGRATED DELAY LINE MEMORY

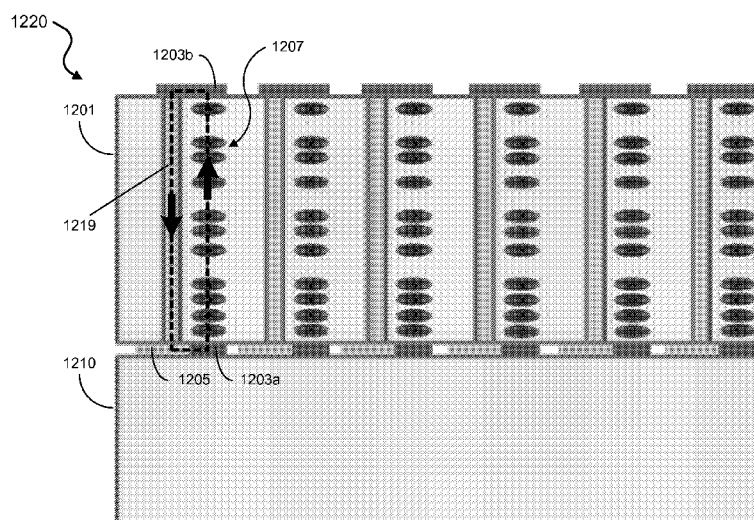


FIG. 12B

(57) Abstract: Delay line memory device, systems and methods are disclosed. In one aspect, a delay line memory device includes a substrate; an electronic unit disposed on the substrate and operable to receive, amplify, and/or synchronize data signals into a bit stream to be transmitted as acoustic pulses carrying data stored in the delay line memory device; a first and a second piezoelectric transducer disposed on the substrate and in communication with the electronic unit, in which the first piezoelectric transducer is operable to transmit the data signals to the acoustic pulses that carry the data through the bulk of the substrate, and the second piezoelectric transducer is operable to transduce the received acoustic pulses to intermediate electrical signals containing the data, which are transferred to the electronic unit via an electrical interconnect to cause refresh of the data in the delay line memory device.



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/014324**A. CLASSIFICATION OF SUBJECT MATTER****G11C 21/02(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11C 21/02; H03H 9/26; G11C 27/00; H01L 21/77; H03H 9/30; H01L 27/00; G11C 11/30

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: delay, line, memory, substrate, electronic, unit, receive, amplify, synchronize, data, signal, transmit, acoustic, pulse, piezoelectric, transducer, communication

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2014-014968 A1 (CORNELL UNIVERSITY) 23 January 2014 See paragraphs [0006], [0049]-[0050], [0052]-[0054], [0058], [0061], [0064], [0101], [0107], [0114]; and figures 1A-1D, 11A-11C, 11E-11F.	1-14, 35-48
A		15-34
Y	US 03668662 A1 (ROBERT L. ZIMMERMAN et al.) 06 June 1972 See column 2, lines 43-52; column 4, lines 37-43, 58-64; and figure 1.	1-14, 35-48
A	US 03940720 A (JOHN B. HARRINGTON) 24 February 1976 See column 2, lines 40-64; and figure 1.	1-48
A	US 03845420 A (MELVIN G. HOLLAND et al.) 29 October 1974 See column 2, lines 28-63; and figure 1.	1-48
A	US 03886529 A (ALAIN BERT et al.) 27 May 1975 See column 1, lines 5-57; and figure 1.	1-48



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

11 November 2015 (11.11.2015)

Date of mailing of the international search report

11 November 2015 (11.11.2015)

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon Metropolitan City, 35208,
Republic of Korea

Facsimile No. +82-42-472-7140

Authorized officer

BYUN, Sung Cheal

Telephone No. +82-42-481-8262



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/014324

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2014-014968 A1	23/01/2014	None	
US 03668662 A1	06/06/1972	None	
US 03940720 A	24/02/1976	None	
US 03845420 A	29/10/1974	JP 50-002841 A JP 55-135524 U JP 57-040577 Y	13/01/1975 26/09/1980 06/09/1982
US 03886529 A	27/05/1975	None	