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(56) Documents Cited
GB 2285202 A **GB 2271256 A** **GB 2255882 A**
EP 0255065 A2 **EP 0179465 A2** **DE 004400819 A1**

(58) Field of Search
UK CL (Edition N) **H4P PEM PEP**
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Online: WPI

(54) Error rate calculation using viterbi decoding/correction

(57) A bit error rate (BER) for a received signal is calculated by error correcting in a unit 10 the received signal to provide a corrected output signal (14). This is re-encoded in unit (24) to produce an encoded signal (26) indicative of an error-free signal ideally received by unit 10. Then, comparison of the received signal (12) with the encoded signal allows determination of a number of bit errors in the received signal. FIG. 2 (not shown) contemplates a comparison between logical binary values otherwise providing a soft data input to a Viterbi decoder (10). This can be used for GSM cellular communications.

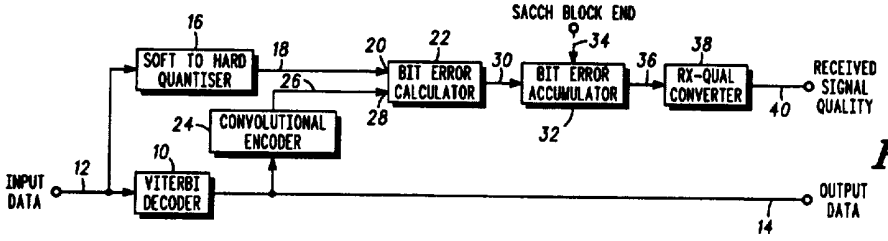

FIG.1

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

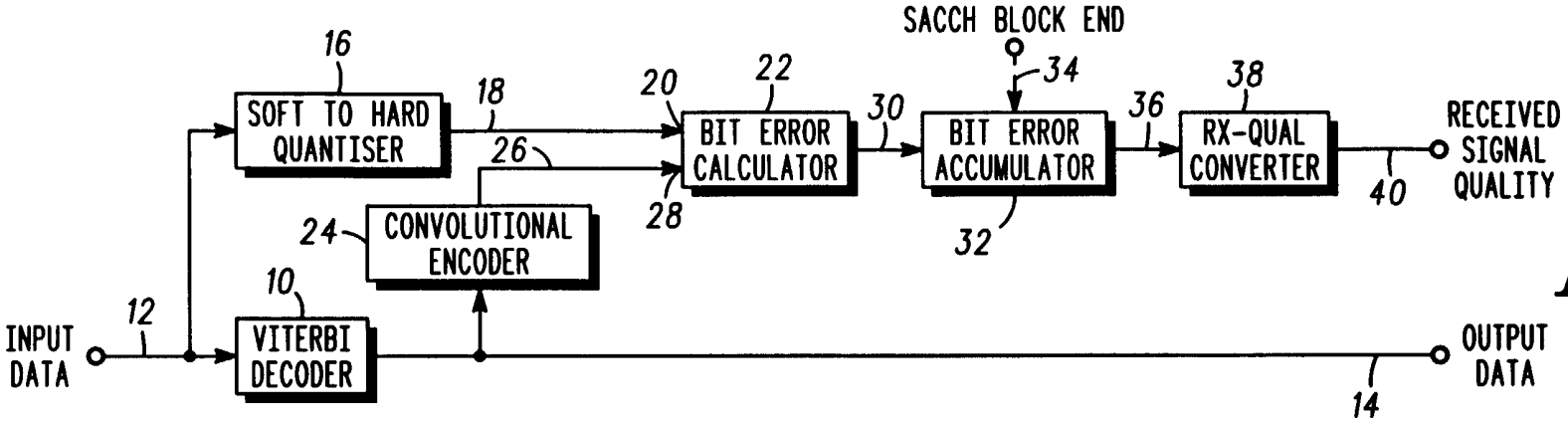


FIG. 1

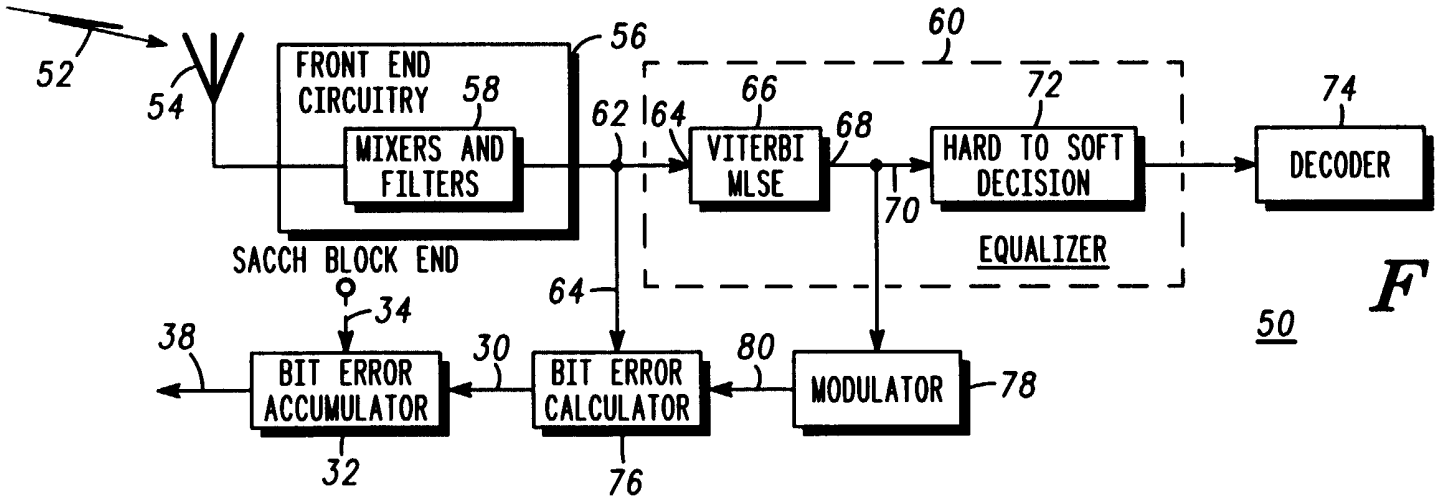
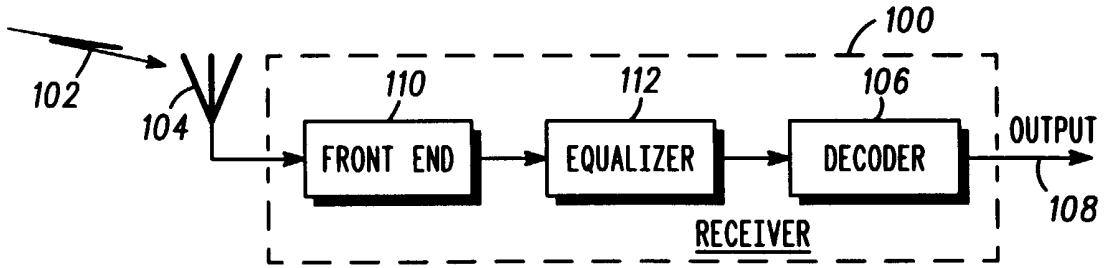


FIG. 2

FIG. 3



METHOD OF BIT ERROR RATE CALCULATION AND APPARATUS THEREFOR

Field of the Invention

This invention relates, in general, to a method of calculating a Bit Error Rate (BER) and is particularly, but not exclusively, applicable to calculating a BER using a Viterbi co-processor in a communication device, such as a radio transceiver.

Summary of the Prior Art

Modern communication systems, such as the pan-European Groupe Speciale Mobile (GSM) cellular communication system, specify the requirement for received signal quality measurements for use in radio frequency (RF) power control and handover processes.

More particularly, and by way of example, received signal quality is assessed in the GSM cellular communication system using bit error rate (BER) calculations on a midamble sequence transmitted in every burst. This BER calculation typically takes one of two forms.

First, since the midamble is known to a receiver, each received bit of information in the midamble sequence can be compared directly against its corresponding, known value to identify any discrepancy. However, since the midamble is only a relatively small portion of the total transmitted burst, there is no averaging of the number of errors over time, and the calculation of the BER for the midamble is somewhat irrelevant with respect to the errors contained in the data and/or speech blocks of the transmitted burst (which blocks account for a relatively large portion of the total transmitted burst and which are located on either side of the midamble).

Second, since the midamble sequence is a pseudo-random noise sequence, a BER calculation may be based on an auto-correlation technique. More particularly, auto-correlation of the pseudo-random noise sequence provides a sharply defined delta-function having a high correlation peak.

Therefore, by comparing a maximum theoretical peak for an ideal channel to a peak for an actual channel (provided by the received midamble sequence), a BER can be interpolated for the actual channel.

As such, a need exists for an improved, more reliable method of assessing BER.

Summary of the Invention

According to the present invention there is provided a method of calculating a bit error rate (BER) for a received signal, comprising the steps of: error correcting, in a correction element, the received signal to provide a corrected output signal; re-encoding the corrected output signal to produce an encoded signal indicative of an error-free signal ideally received by the correction element; and comparing of the received signal with the encoded signal to determine a number of bit errors in the received signal.

In a second aspect of the present invention there is provided apparatus for determining a bit error rate of a received signal, comprising: means for error correcting the received signal to provide a corrected output signal; means for re-encoding the corrected output signal to produce an encoded signal indicative of an error-free signal ideally received by the correction element; and means for comparing of the received signal with the encoded signal to determine a number of bit errors in the received signal.

Exemplary embodiments of the present invention will now be described with reference to the accompanying drawings.

Brief Description of the Drawings

FIG. 1 is a block diagram of a channel decoder arranged to assess bit error rate according to a preferred embodiment of the present invention.

FIG. 2 is a block diagram of a channel equalizer arranged to assess bit error rate according to an alternate embodiment of the present invention.

FIG. 3 shows a receiver which may utilise the bit error rate methodology and structure illustrated in FIGs. 1 and 2.

Detailed Description of a Preferred Embodiment

Referring to FIG. 1, there is shown a block diagram of a channel decoder (of a radio receiver) arranged to assess bit error rates according to a preferred embodiment of the present invention.

As will be appreciated, the channel decoder comprises a Viterbi decoder 10 that receives encoded input data 12 from a preceding stage (e.g. an equalizer) of the radio receiver. The Viterbi decoder 10 processes (decodes) the encoded input data 12 to produce hard-decision output data 14. More particularly, the input data 12 consists of soft-decision symbols from the channel equalization process, with the soft-decision symbols representing the likelihood of a received bit being a logical "0" or a logical "1".

The encoded input data is also coupled to a soft-to-hard quantizer 16, which translates soft-decision integer values to hard-decision logical binary values 18. These logical binary values provide a first input 20 to a bit error calculator 22. The output data 14 generated by Viterbi decoder 10 is tapped and fed into a convolutional coder 24, which re-encodes the output data to generate "ideal" simulated input data 26. The ideal simulated input data 26 is provided to a second input of bit error calculator 22. As such, the number of bits corrected by the Viterbi decoder 10 can be determined.

The bit error calculator 22 acts as a comparison unit and compares logical binary values 18 with corresponding information bits of the ideal simulated input data 26, and generates a bit error signal 30 in response to each logical discrepancy therebetween. Expressed in an alternative way, the bit error detector 22 compares a translated input sequence with a convolutionally-encoded copy of the output signal 14, and provides an indication of any difference (which, of course, represents a bit error in the translated input sequence).

The bit error signal 30 is coupled to a bit error accumulator 32 which provides a summation (count) of the number of bit error signals generated

over a specified period of time. In this respect, the bit error accumulator 32 is (in a preferred embodiment) responsive to a slow associated control channel signal (SACCH) 34, such that an average BER is provided over a reporting period of one SACCH block, for example. However, in the case when the present invention is applied to a traffic channel (used to communicate user-data rather than control information) of a multiplexed communication system, the bit error accumulator 32 must also maintain a separate total of the discontinuous slot transmissions (DTx) in order to present an accurate representation of BER for a particular channel resource (i.e. time-slot) over a predetermined period of time.

An output 36 from the bit error accumulator 32 is coupled to a received quality (Rx-Qual) converter 38 which transforms a bit error count, periodically provided by the bit error accumulator 32, to a bit error rate, and then provides a received signal quality value 40 for use by the radio receiver (or a transceiver, where applicable).

By assuming that the output data 14 provided by the Viterbi decoder 10 is error-free, re-encoding of this error-free output signal necessarily provides an apparent replica of the encoded signal originally transmitted to the radio receiver. Therefore, any discrepancies between respective bits of the re-encoded convolutional code and a hard-decision binary equivalent of the input data processed by the Viterbi decoder 10 can be used to determine a real-time BER.

As an alternative to performing the BER assessment in the channel decoder, a second embodiment of the present invention contemplates the adaptation and use of channel equalization circuitry for the same effect, as shown in FIG. 2. Specifically, a receiver (generally denoted 50) is responsive to signals 52 containing encoded information that has been transmitted from a transmitter (not shown). The signals 52, which are subject to general channel distortion and particularly inter-symbol interference (ISI), are received by an antenna 54 and then communicated through front-end circuitry 56 (containing mixers and filters 58, for example) to a channel equalizer 60. At node 62 (located between the equalizer 60 and an output of the front-end circuitry 58), signals 64 originally received by the receiver 50 will typically contain distorted

symbols, and will still be in a Gaussian Minimum Shift-Keyed (GMSK) format (or the like). Therefore, in accordance with known techniques, the channel equalizer 60 is arranged to eliminate ISI in signals 64 by passing the signals 64 through a Viterbi Maximum Likelihood Sequence Estimator (MLSE) 66. An output 68 from Viterbi MLSE 66 provides "distortionless" (error-free) symbols 70 to a hard-to-soft decision converter block 72, which eventually communicates "soft" symbols to a decoder 74.

In accordance with the second embodiment of the present invention, node 62 provides a first input to a bit error calculator 76, and the distortionless symbols 70 are re-modulated (re-encoded) in modulator 78 such that an "ideal" waveform 80 is provided at an output of the modulator 78. The ideal waveform 80 is coupled to bit error detector 76 as a second input. More specifically, in the case where the signal 64 is in a GMSK format, the distortionless symbols 70 are re-modulated with a GMSK baseband waveform, thereby producing an ideal waveform 80 that aspires to represent an original signal transmitted to the receiver 50. Hence, the number of bits corrected by the Viterbi MLSE 66 can be determined.

Again, bit error calculator 76 acts as a comparison unit and compares signal 64 with corresponding information bits of the ideal waveform 80, and generates a bit error signal 30 in response to a logical discrepancy therebetween. In a similar manner to that previously described for the first embodiment, the bit error signal 30 is coupled to a bit error accumulator 32 which provides a summation (count) of the number of bit error signals generated over a specified period of time. Again, the bit error accumulator 32 is (in a preferred embodiment) responsive to a slow associated control channel signal (SACCH) 34, such that an average BER is provided over a reporting period of one SACCH block, for example. Although not shown (and for the sake of brevity), an output 36 from the bit error accumulator 32 is coupled to a received quality (Rx-Qual) converter 38 in the way previously described. Furthermore, the considerations regarding traffic channels equally apply to this embodiment.

FIG. 3 illustrates a receiver 100 (possibly implemented within a transceiver) which may utilise the bit error rate methodology and

structure of the preferred embodiments of the present invention. The receiver 100 is responsive to radio frequency signals 102 containing convolutionally-encoded information that has been transmitted from a transmitter (not shown). The radio frequency signals 102 are received by an antenna 104 of the receiver 100. The convolutionally-encoded information is eventually decoded by a decoding unit 106 of the receiver 100 to provide an output 108, with the convolutionally-encoded information previously having passed through front-end circuitry 110 (containing filters and mixers, amongst other things) and equalizer circuitry 112.

As will be appreciated, the present invention may be employed in any radio receiver, such as a mobile cellular telephone or a base station.

As such, the general principle underlying the present invention is that by assuming that an output signal is error-free and represents an information signal that was originally encoded at a transmitter, this output signal can be re-encoded to simulate an "ideal" (error-free) input signal for a preceding (error correcting operational) stage, which simulated ideal signal can be compared against the actual input signal (applied to the preceding stage) to produce a real-time assessment of BER. Generally, the key to the BER calculation of the present invention is the determination of the number of bit errors corrected in the Viterbi decoder or the Viterbi MLSE compared against an "error-free" signal produced by the re-encoding/re-modulation of the actual output signal.

In summary, the present invention provides an improved method for calculating bit error rates, which method has greater accuracy as a direct consequence of the ability to provide BER information over an entire transmitted burst. Moreover, the present invention provides a measurement of signal quality (Rx-Qual in GSM terms) without the need for a distinct BER calculation on a specific portion of a frame.

It will, of course, be understood that the above description has been given by way of example only, and that modifications in detail may be made within the scope of the invention. For example, the channel decoder and the channel equaliser may be used independently of each other, or in a complementary arrangement.

Claims

1. A method of calculating a bit error rate (BER) for a received signal, comprising the steps of:

error correcting, in a correction element, the received signal to provide a corrected output signal;

re-encoding the corrected output signal to produce an encoded signal indicative of an error-free signal ideally received by the correction element; and

comparing of the received signal with the encoded signal to determine a number of bit errors in the received signal.

2. Apparatus for determining a bit error rate of a received signal, comprising:

means for error correcting the received signal to provide a corrected output signal;

means for re-encoding the corrected output signal to produce an encoded signal indicative of an error-free signal ideally received by the correction element; and

means for comparing of the received signal with the encoded signal to determine a number of bit errors in the received signal.

3. Apparatus according to claim 2, wherein the means for re-encoding is a convolutional coder and the means for error correcting is a Viterbi decoder.

4. Apparatus according to claim 2, wherein the means for re-encoding is a modulator and the means for error correcting is a Viterbi Maximum Likelihood Sequence Estimator (MLSE).

5. Apparatus according to claim 2 or 3, further comprising a soft-to-hard quantizer for quantizing the received signal to produce logical binary values, the soft-to-hard quantizer coupling the received signal to the means for comparing.

6. Apparatus according to claim 2, 3 or 4, wherein the means for comparing further comprises:

a bit error calculator for comparing respective bits of the received signal and the encoded signal and for generating an error signal in response to a difference therebetween; and

a bit error accumulator, responsive to error signals generated by the bit error calculator, for counting a number of error signals provided thereto.

7. Apparatus according to claim 6, further comprising timing means, coupled to the bit error accumulator, for providing a timing signal thereto, the timing signal arranged to time a predetermined period in which the number of error signals provided to the bit error accumulator is assessed.

8. Apparatus according to claim 7, wherein the timing signal is provided periodically.

9. A radio communication device comprising the apparatus of any one of claims 2 to 8.

10. A method of calculating a bit error rate (BER) for a received signal substantially as hereinbefore described with reference to FIGs. 1 and 2 of the accompanying drawings.

11. Apparatus for determining a bit error rate of a received signal substantially as hereinbefore described with reference to FIGs. 1 and 2 of the accompanying drawings.

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Patents Act 1977
Examiner's report to the Comptroller under Section 17
(The Search report)

Application number
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Relevant Technical Fields

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(ii) Int Cl (Ed.6) H04L 1/00, H03M 13/00

Search Examiner
MR B J SPEAR

Date of completion of Search
10 NOVEMBER 1995

Databases (see below)
(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii) ONLINE: WPI

Documents considered relevant following a search in respect of Claims :-
1-11

Categories of documents

X: Document indicating lack of novelty or of inventive step.

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A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
Y	GB 2285202 A	(MOTOROLA) Figures 3 and 6 and, eg, page 10 line 32 to page 11 line 26	1-3, 9
Y	GB 2271256 A	(MOTOROLA) Figure 5 and, eg, page 17 line 1 to page 18 line 13	1-3, 9
Y	GB 2255882 A	(MOTOROLA) Figure 3 and, eg, page 11 line 29 to page 13 line 23	1-3, 9
X, Y	EP 0255065 A2	(NEC CORP) Figures 5 and 7 and, eg, page 4 lines 29 to 40	1-3, 6-9
A	EP 0179465 A2	(NEC) Figure 1	
X, Y	DE 4400819 A1	(NEC) whole document, especially Figure 3. This document has several equivalents including US 5455536	1-3, 6-9

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents).