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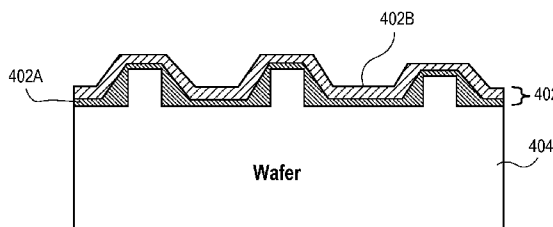
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(54) **Title:** WATER SOLUBLE FILM AND UV-CURABLE FILM HYBRID MASK FOR WAFER DICING USING LASER SCRIBING AND PLASMA ETCH

**FIG. 4B**

(57) **Abstract:** Methods of using a hybrid mask composed of a water soluble film layer and a UV-curable film layer for wafer dicing using laser scribing and plasma etch described. In an example, a method of dicing a semiconductor wafer having a plurality of integrated circuits includes forming a hybrid mask above the semiconductor wafer, the hybrid mask composed of a water-soluble layer formed on the integrated circuits and a UV-curable layer formed on the water-soluble layer. The hybrid mask is patterned with a laser scribing process to provide a patterned hybrid mask with gaps to expose regions of the semiconductor wafer between the integrated circuits. The semiconductor wafer is etched through the gaps in the patterned hybrid mask to singulate the integrated circuits.

WATER SOLUBLE FILM AND UV-CURABLE FILM HYBRID MASK FOR WAFER DICING USING LASER SCRIBING AND PLASMA ETCH

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 61/764,156, filed on February 13, 2013, the entire contents of which are hereby incorporated by reference herein.

BACKGROUND

1) FIELD

[0002] Embodiments of the present invention pertain to the field of semiconductor processing and, in particular, to methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon.

2) DESCRIPTION OF RELATED ART

[0003] In semiconductor wafer processing, integrated circuits are formed on a wafer (also referred to as a substrate) composed of silicon or other semiconductor material. In general, layers of various materials which are either semiconducting, conducting or insulating are utilized to form the integrated circuits. These materials are doped, deposited and etched using various well-known processes to form integrated circuits. Each wafer is processed to form a large number of individual regions containing integrated circuits known as dice.

[0004] Following the integrated circuit formation process, the wafer is "diced" to separate the individual die from one another for packaging or for use in an unpackaged form within larger circuits. The two main techniques that are used for wafer dicing are scribing and sawing. With scribing, a diamond tipped scribe is moved across the wafer surface along pre-formed scribe lines. These scribe lines extend along the spaces between the dice. These spaces are commonly referred to as "streets." The diamond scribe forms shallow scratches in the wafer surface along the streets. Upon the application of pressure, such as with a roller, the wafer separates along the scribe lines. The breaks in the wafer follow the crystal lattice structure of the wafer substrate. Scribing can be used for wafers that are about 10 mils (thousandths of an inch) or less in thickness. For thicker wafers, sawing is presently the preferred method for dicing.

[0005] With sawing, a diamond tipped saw rotating at high revolutions per minute contacts the wafer surface and saws the wafer along the streets. The wafer is mounted on a supporting member such as an adhesive film stretched across a film frame and the saw is repeatedly applied to both the vertical and horizontal streets. One problem with either scribing or sawing is that chips and gouges can form along the severed edges of the dice. In addition, cracks can form and propagate from the edges of the dice into the substrate and render the integrated circuit inoperative. Chipping and cracking are particularly a problem with scribing because only one side of a square or rectangular die can be scribed in the $\langle 110 \rangle$ direction of the crystalline structure. Consequently, cleaving of the other side of the die results in a jagged separation line. Because of chipping and cracking, additional spacing is required between the dice on the wafer to prevent damage to the integrated circuits, e.g., the chips and cracks are maintained at a distance from the actual integrated circuits. As a result of the spacing requirements, not as many dice can be formed on a standard sized wafer and wafer real estate that could otherwise be used for circuitry is wasted. The use of a saw exacerbates the waste of real estate on a semiconductor wafer. The blade of the saw is approximate 15 microns thick. As such, to insure that cracking and other damage surrounding the cut made by the saw does not harm the integrated circuits, three to five hundred microns often must separate the circuitry of each of the dice. Furthermore, after cutting, each die requires substantial cleaning to remove particles and other contaminants that result from the sawing process.

[0006] Plasma dicing has also been used, but may have limitations as well. For example, one limitation hampering implementation of plasma dicing may be cost. A standard lithography operation for patterning resist may render implementation cost prohibitive. Another limitation possibly hampering implementation of plasma dicing is that plasma processing of commonly encountered metals (e.g., copper) in dicing along streets can create production issues or throughput limits.

SUMMARY

[0007] Embodiments of the present invention include methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon.

[0008] In an embodiment, a method of dicing a semiconductor wafer having a plurality of integrated circuits includes forming a hybrid mask above the semiconductor wafer, the hybrid mask composed of a water-soluble layer formed on the integrated circuits and a UV-curable layer formed on the water-soluble layer. The hybrid mask is patterned with a laser scribing

process to provide a patterned hybrid mask with gaps to expose regions of the semiconductor wafer between the integrated circuits. The semiconductor wafer is etched through the gaps in the patterned hybrid mask to singulate the integrated circuits.

[0009] In another embodiment, a method of dicing a semiconductor wafer having a plurality of integrated circuits involves providing a semiconductor wafer having a hybrid mask disposed thereon, the hybrid mask including a water-soluble layer disposed on the integrated circuits and a UV-curable layer disposed on the water-soluble layer. The method also involves patterning the hybrid mask with a laser scribing process to provide a patterned hybrid mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits. The method also involves etching the semiconductor wafer through the gaps in the patterned hybrid mask to singulate the integrated circuits.

[0010] In another embodiment, a method of dicing a semiconductor wafer having a plurality of integrated circuits involves providing a semiconductor wafer having a patterned hybrid mask disposed thereon, the patterned hybrid mask including a water-soluble layer disposed on the integrated circuits and a UV-curable layer disposed on the water-soluble layer. The patterned hybrid mask has gaps exposing regions of the semiconductor wafer between the integrated circuits. The method also involves etching the semiconductor wafer through the gaps in the patterned hybrid mask to singulate the integrated circuits.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] Figure 1 illustrates a top plan of a semiconductor wafer to be diced, in accordance with an embodiment of the present invention.

[0012] Figure 2 illustrates a top plan of a semiconductor wafer to be diced that has a dicing mask formed thereon, in accordance with an embodiment of the present invention.

[0013] Figure 3 is a Flowchart representing operations in a method of dicing a semiconductor wafer including a plurality of integrated circuits, in accordance with an embodiment of the present invention.

[0014] Figures 4A-4E illustrate cross-sectional views of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, in accordance with an embodiment of the present invention.

[0015] Figure 5 illustrates the effects of using a laser pulse in the femtosecond range versus longer pulse times, in accordance with an embodiment of the present invention.

[0016] Figure 6 illustrates a cross-sectional view of a stack of materials that may be used in a street region of a semiconductor wafer or substrate, in accordance with an embodiment of

the present invention.

[0017] Figure 7 includes a plot of absorption coefficient as a function of photon energy for crystalline silicon (c-Si), copper (Cu), crystalline silicon dioxide (c-SiO₂), and amorphous silicon dioxide (a-SiO₂), in accordance with an embodiment of the present invention.

[0018] Figure 8 is an equation showing the relationship of laser intensity for a given laser as a function of laser pulse energy, laser pulse width, and laser beam radius.

[0019] Figures 9A-9D illustrate cross-sectional views of various operations in a method of dicing a semiconductor wafer, in accordance with an embodiment of the present invention.

[0020] Figure 10 illustrates compaction on a semiconductor wafer achieved by using narrower streets versus conventional dicing which may be limited to a minimum width, in accordance with an embodiment of the present invention.

[0021] Figure 11 illustrates freeform integrated circuit arrangement allowing denser packing and, hence, more die per wafer versus grid alignment approaches, in accordance with an embodiment of the present invention.

[0022] Figure 12 illustrates a block diagram of a tool layout for laser and plasma dicing of wafers or substrates, in accordance with an embodiment of the present invention.

[0023] Figure 13 illustrates a block diagram of an exemplary computer system, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[0024] Methods of dicing semiconductor wafers, each wafer having a plurality of integrated circuits thereon, are described. In the following description, numerous specific details are set forth, such as femtosecond-based laser scribing and plasma etching conditions and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known aspects, such as integrated circuit fabrication, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

[0025] A hybrid wafer or substrate dicing process involving an initial laser scribe and subsequent plasma etch may be implemented for die singulation. The laser scribe process may be used to cleanly remove a mask layer, organic and inorganic dielectric layers, and device layers. The laser etch process may then be terminated upon exposure of, or partial etch

of, the wafer or substrate. The plasma etch portion of the dicing process may then be employed to etch through the bulk of the wafer or substrate, such as through bulk single crystalline silicon, to yield die or chip singulation or dicing.

[0026] One or more embodiments described herein are targeted to methods of using a hybrid mask composed of a water soluble film layer and an ultra-violet (UV)-curable film layer for wafer dicing processes using laser scribing and plasma etching. To provide context, in the phase of integrated circuit (IC) chip singulation, the IC chips bear a polymer film layer (e.g., a polyimide layer) on the top surface for the purposes of stress relieving and masking around bump pads. For the proposed laser scribing + plasma etch dicing processes, a mask layer needs to be added on top of the wafer subjected to singulation. The mask layer is typically removed following singulation, and preferably without damaging or contaminating the pre-existing polymer layer and bump pads on the IC chips.

[0027] Advantages of using a hybrid mask such as described and illustrated in the embodiments below can include achieving a good balance between mask functionality and process simplicity. For example, a water soluble film can provide access to readily available aqueous removal techniques, such as an aqueous cleans operation, for post etch mask removal operations. However, common low-cost water soluble materials may be highly transparent to photons in the wavelength regime from 250nm to 1600nm for most industrial solid state lasers. For example, polyvinyl alcohol (PVA) is highly transparent even in the 350nm to 800nm range. Accordingly, in an embodiment, use of a combination of a very thin water soluble film and a second UV curable film layer provides access to improved laser ablation process quality, while rendering a more facile post-etch mask removal process. Another advantage can involve widening the options of applicable laser sources. For example, the water soluble film/UV curable film hybrid mask configuration can enable the use of common solid state nanosecond and picosecond UV lasers, as UV curable polymers couple well with UV laser irradiation. This may reduce actual laser processing cost or cost of ownership.

[0028] More generally, conventional wafer dicing approaches include diamond saw cutting based on a purely mechanical separation, initial laser scribing and subsequent diamond saw dicing, or nanosecond or picosecond laser dicing. For thin wafer or substrate singulation, such as 50 microns thick bulk silicon singulation, the conventional approaches have yielded only poor process quality. Some of the challenges that may be faced when singulating die from thin wafers or substrates may include microcrack formation or delamination between different layers, chipping of inorganic dielectric layers, retention of strict kerf width control, or precise ablation depth control. Embodiments of the present invention include a hybrid laser

scribing and plasma etching die singulation approach that may be useful for overcoming one or more of the above challenges.

[0029] In accordance with an embodiment of the present invention, a combination of laser scribing (e.g., femtosecond-based) and plasma etching is used to dice a semiconductor wafer into individualized or singulated integrated circuits. In one embodiment, femtosecond-based laser scribing is used as an essentially, if not totally, non-thermal process. For example, the femtosecond-based laser scribing may be localized with no or negligible heat damage zone. In an embodiment, approaches herein are used to singulated integrated circuits having ultra-low k films. With convention dicing, saws may need to be slowed down to accommodate such low k films. Furthermore, semiconductor wafers are now often thinned prior to dicing. As such, in an embodiment, a combination of mask patterning and partial wafer scribing with a femtosecond-based laser, followed by a plasma etch process, is now practical. In one embodiment, direct writing with laser can eliminate need for a lithography patterning operation of a photo-resist layer and can be implemented with very little cost. In one embodiment, through-via type silicon etching is used to complete the dicing process in a plasma etching environment.

[0030] Thus, in an aspect of the present invention, a combination of femtosecond-based laser scribing and plasma etching may be used to dice a semiconductor wafer into singulated integrated circuits. Figure 1 illustrates a top plan of a semiconductor wafer to be diced, in accordance with an embodiment of the present invention. Figure 2 illustrates a top plan of a semiconductor wafer to be diced that has a dicing mask formed thereon, in accordance with an embodiment of the present invention.

[0031] Referring to Figure 1, a semiconductor wafer 100 has a plurality of regions 102 that include integrated circuits. The regions 102 are separated by vertical streets 104 and horizontal streets 106. The streets 104 and 106 are areas of semiconductor wafer that do not contain integrated circuits and are designed as locations along which the wafer will be diced. Some embodiments of the present invention involve the use of a combination femtosecond-based laser scribe and plasma etch technique to cut trenches through the semiconductor wafer along the streets such that the dice are separated into individual chips or die. Since both a laser scribe and a plasma etch process are crystal structure orientation independent, the crystal structure of the semiconductor wafer to be diced may be immaterial to achieving a vertical trench through the wafer.

[0032] Referring to Figure 2, the semiconductor wafer 100 has a mask 200 deposited upon the semiconductor wafer 100. In one embodiment, the mask is a hybrid mask composed

of a water soluble film layer and a UV-curable film layer. The mask 200 and a portion of the semiconductor wafer 100 are patterned with a laser scribing process to define the locations (e.g., gaps 202 and 204) along the streets 104 and 106 where the semiconductor wafer 100 will be diced. The integrated circuit regions of the semiconductor wafer 100 are covered and protected by the mask 200. The regions 206 of the mask 200 are positioned such that during a subsequent etching process, the integrated circuits are not degraded by the etch process. Horizontal gaps 204 and vertical gaps 202 are formed between the regions 206 to define the areas that will be etched during the etching process to finally dice the semiconductor wafer 100.

[0033] Figure 3 is a Flowchart 300 representing operations in a method of dicing a semiconductor wafer including a plurality of integrated circuits, in accordance with an embodiment of the present invention. Figures 4A-4E illustrate cross-sectional views of a semiconductor wafer including a plurality of integrated circuits during performing of a method of dicing the semiconductor wafer, corresponding to operations of Flowchart 300, in accordance with an embodiment of the present invention.

[0034] Referring to portion 302 of Flowchart 300, and corresponding Figures 4A and 4B, a hybrid mask 402 is formed above a semiconductor wafer or substrate 404. The hybrid mask 402 includes a water-soluble layer 402A covering and protecting integrated circuits including metallic bumps or pillars 499 formed on the surface of semiconductor wafer 404, as depicted in Figure 4A. The hybrid mask 402 also includes a UV-curable layer 402B disposed on the water-soluble layer 402A, as depicted in Figure 4B.

[0035] In an embodiment, referring to operation 352 of portion 302 of Flowchart 300, and corresponding Figure 4A, the hybrid mask 402 is formed by first forming the water-soluble layer 402A. The water-soluble layer 402A may be formed by a coating process such as a spin-on coating process. Referring to operation 354, a baking operation may be performed following deposition of the water-soluble layer 402A, e.g., to remove any solvents used to spin-on the layer. Referring now to operation 356 of portion 302 of Flowchart 300, and corresponding Figure 4B, formation of the hybrid mask 402 next includes forming the UV-curable layer 402B. The UV-curable layer 402B may be formed by a coating process such as a spin-on coating process. Referring to operation 358, a baking operation may be performed following deposition of the UV-curable layer 402B, e.g., to remove any solvents used to spin-on the layer.

[0036] Overall, in an embodiment, hybrid mask 402 is most effective if having at least one, if not all of the following characteristics: (1) enables up to approximately 500 micron

etch depth, (2) applicable to thin wafer (e.g., film + frame) applications, (3) applicable to pre-thinned wafers, (4) allows for clean ablation with a laser scribing process, (5) applicable atop polyimide (PI) or molding compound, (6) removable without oxidizing bumps on the integrated circuits of the wafer, or (7) removable without changing properties of under-layer films and materials. In one embodiment, hybrid mask 402 is formed by applying two different films to form the mask layer. The first layer is a thin water soluble solid film (e.g., having a thickness less than approximately 6 microns) directly coated atop the wafer front surface. The water soluble film is then baked. Then, a second layer is applied atop the first layer of water soluble film, and the second layer is then baked. The second layer is composed of material such as a UV-curable polymer. The second layer (also referred to herein as the UV-curable film) can be a single layer or have two sub-layers involving a thin UV adhesive layer (e.g., to be in direct contact with the water soluble film) and a common non-UV curable polyimide. In a specific embodiment, the thickness of the first water soluble layer is minimized to an extent that the as-deposited layer builds up only approximately 1.5 microns of thick mask atop the bumps on a wafer. The thickness of the second UV curable layer, as is typically used in UV curable wafer dicing tape, is sufficient to protect the dies on a wafer from being damaged during a subsequent etch process.

[0037] In an embodiment, the water-soluble layer of hybrid mask 402 is readily dissolvable in an aqueous media. For example, in one embodiment, the water-soluble layer is composed of a material that is soluble in one or more of an alkaline solution, an acidic solution, or in deionized water.

[0038] In an embodiment, the water-soluble layer maintains its water solubility upon a heating process, such as heating approximately in the range of 50 – 160 degrees Celsius. For example, in one embodiment, the water-soluble layer is soluble in aqueous solutions following exposure to chamber conditions used in a laser and plasma etch singulation process. In one embodiment, the water-soluble die layer is composed of a material such as, but not limited to, polyvinyl alcohol, polyacrylic acid, dextran, polymethacrylic acid, polyethylene imine, or polyethylene oxide. In a specific embodiment, the water-soluble layer has an etch rate in an aqueous solution approximately in the range of 1 – 15 microns per minute and, more particularly, approximately 1.3 microns per minute. In another specific embodiment, the water-soluble layer is formed by a spin-on technique.

[0039] In an embodiment, the UV-curable layer is a layer or stack of layers having a susceptibility to UV light that reduces an adhesiveness of the UV-curable layer by at least approximately 80%. In one such embodiment, the UV layer is composed of polyvinyl

chloride or an acrylic-based material. In an embodiment, the UV-curable later is composed of a material or stack of materials with an adhesive property that weakens upon exposure to UV light. In an embodiment, the UV-curable adhesive film is sensitive to approximately 365nm UV light. In one such embodiment, this sensitivity enables use of LED light to perform a cure.

[0040] Thus, in an embodiment, a method of forming a hybrid mask on bumps/metal pillars and saw street/wafer field is provided. In one or more embodiment, such a mask layer enables up to 500 micron etch depth, is applicable to thin wafer (film+frame) scenarios, is applicable to pre-thin scenarios, provides for subsequent clean ablation with a laser, is applicable atop polyimide (PI) or molding compounds, is removable without oxidizing bumps/pillars, is removable without changing properties of under-layers, and/or has uniform thickness on the bump/metal pillar top and saw street.

[0041] Referring to Figures 4C-4E, the laser scribing and etching portion of the dicing process is illustrated. For the sake of convenience, mask 402 and wafer 404 are depicted once again, but without the illustration of bumps and pillars. Instead, in Figure 4C, intervening streets 407 formed between each of the integrated circuits 406 are emphasized. However, it is to be understood that the bumps/pillars 499 and hybrid mask 402 are still contemplated in the following description.

[0042] In an embodiment, semiconductor wafer or substrate 404 is composed of a material suitable to withstand a fabrication process and upon which semiconductor processing layers may suitably be disposed. For example, in one embodiment, semiconductor wafer or substrate 404 is composed of a group IV-based material such as, but not limited to, crystalline silicon, germanium or silicon/germanium. In a specific embodiment, providing semiconductor wafer 404 includes providing a monocrystalline silicon substrate. In a particular embodiment, the monocrystalline silicon substrate is doped with impurity atoms. In another embodiment, semiconductor wafer or substrate 404 is composed of a III-V material such as, e.g., a III-V material substrate used in the fabrication of light emitting diodes (LEDs).

[0043] In an embodiment, semiconductor wafer or substrate 404 has disposed thereon or therein, as a portion of the integrated circuits 406, an array of semiconductor devices. Examples of such semiconductor devices include, but are not limited to, memory devices or complimentary metal-oxide-semiconductor (CMOS) transistors fabricated in a silicon substrate and encased in a dielectric layer. A plurality of metal interconnects may be formed above the devices or transistors, and in surrounding dielectric layers, and may be used to electrically couple the devices or transistors to form the integrated circuits 406. Materials

making up the streets 407 may be similar to or the same as those materials used to form the integrated circuits 406. For example, streets 407 may be composed of layers of dielectric materials, semiconductor materials, and metallization. In one embodiment, one or more of the streets 407 includes test devices similar to the actual devices of the integrated circuits 406.

[0044] Referring to portion 304 of Flowchart 300, and corresponding Figure 4D, the hybrid mask 402 is patterned with a laser scribing process to provide a patterned hybrid mask 408 with gaps 410, exposing regions of the semiconductor wafer or substrate 404 between the integrated circuits 406. As such, the laser scribing process is used to remove the material of the streets 407 originally formed between the integrated circuits 406. In accordance with an embodiment of the present invention, patterning the mask 402 with the femtosecond-based laser scribing process includes forming trenches 412 partially into the regions of the semiconductor wafer 404 between the integrated circuits 406, as depicted in Figure 4D.

[0045] In an embodiment, patterning the mask 406 with the laser scribing process includes using a laser having a pulse width in the femtosecond range. Specifically, a laser with a wavelength in the visible spectrum plus the ultra-violet (UV) and infra-red (IR) ranges (totaling a broadband optical spectrum) may be used to provide a femtosecond-based laser, i.e., a laser with a pulse width on the order of the femtosecond (10^{-15} seconds). In one embodiment, ablation is not, or is essentially not, wavelength dependent and is thus suitable for complex films such as films of the mask 402, the streets 407 and, possibly, a portion of the semiconductor wafer or substrate 404.

[0046] Figure 5 illustrates the effects of using a laser pulse in the femtosecond range versus longer frequencies, in accordance with an embodiment of the present invention. Referring to Figure 5, by using a laser with a pulse width in the femtosecond range heat damage issues are mitigated or eliminated (e.g., minimal to no damage 502C with femtosecond processing of a via 500C) versus longer pulse widths (e.g., damage 502B with picosecond processing of a via 500B and significant damage 502A with nanosecond processing of a via 500A). The elimination or mitigation of damage during formation of via 500C may be due to a lack of low energy recoupling (as is seen for picosecond-based laser ablation) or thermal equilibrium (as is seen for nanosecond-based laser ablation), as depicted in Figure 5.

[0047] Laser parameters selection, such as pulse width, may be critical to developing a successful laser scribing and dicing process that minimizes chipping, microcracks and delamination in order to achieve clean laser scribe cuts. The cleaner the laser scribe cut, the smoother an etch process that may be performed for ultimate die singulation. In

semiconductor device wafers, many functional layers of different material types (e.g., conductors, insulators, semiconductors) and thicknesses are typically disposed thereon. Such materials may include, but are not limited to, organic materials such as polymers, metals, or inorganic dielectrics such as silicon dioxide and silicon nitride.

[0048] A street between individual integrated circuits disposed on a wafer or substrate may include the similar or same layers as the integrated circuits themselves. For example, Figure 6 illustrates a cross-sectional view of a stack of materials that may be used in a street region of a semiconductor wafer or substrate, in accordance with an embodiment of the present invention.

[0049] Referring to Figure 6, a street region 600 includes the top portion 602 of a silicon substrate, a first silicon dioxide layer 604, a first etch stop layer 606, a first low K dielectric layer 608 (e.g., having a dielectric constant of less than the dielectric constant of 4.0 for silicon dioxide), a second etch stop layer 610, a second low K dielectric layer 612, a third etch stop layer 614, an undoped silica glass (USG) layer 616, a second silicon dioxide layer 618, and a hybrid mask 620 composed of a water soluble film layer and a UV-curable film layer, with relative thicknesses depicted. Copper metallization 622 is disposed between the first and third etch stop layers 606 and 614 and through the second etch stop layer 610. In a specific embodiment, the first, second and third etch stop layers 606, 610 and 614 are composed of silicon nitride, while low K dielectric layers 608 and 612 are composed of a carbon-doped silicon oxide material.

[0050] Under conventional laser irradiation (such as nanosecond-based or picosecond-based laser irradiation), the materials of street 600 behave quite differently in terms of optical absorption and ablation mechanisms. For example, dielectrics layers such as silicon dioxide, is essentially transparent to all commercially available laser wavelengths under normal conditions. By contrast, metals, organics (e.g., low K materials) and silicon can couple photons very easily, particularly in response to nanosecond-based or picosecond-based laser irradiation. For example, Figure 7 includes a plot 700 of absorption coefficient as a function of photon energy for crystalline silicon (c-Si, 702), copper (Cu, 704), crystalline silicon dioxide (c-SiO₂, 706), and amorphous silicon dioxide (a-SiO₂, 708), in accordance with an embodiment of the present invention. Figure 8 is an equation 800 showing the relationship of laser intensity for a given laser as a function of laser pulse energy, laser pulse width, and laser beam radius.

[0051] Using equation 800 and the plot 700 of absorption coefficients, in an embodiment, parameters for a femtosecond laser-based process may be selected to have an essentially

common ablation effect on the inorganic and organic dielectrics, metals, and semiconductors even though the general energy absorption characteristics of such materials may differ widely under certain conditions. For example, the absorptivity of silicon dioxide is non-linear and may be brought more in-line with that of organic dielectrics, semiconductors and metals under the appropriate laser ablation parameters. In one such embodiment, a high intensity and short pulse width femtosecond-based laser process is used to ablate a stack of layers including a silicon dioxide layer and one or more of an organic dielectric, a semiconductor, or a metal. In a specific embodiment, pulses of approximately less than or equal to 400 femtoseconds are used in a femtosecond-based laser irradiation process to remove a hybrid mask composed of a water soluble film layer and a UV-curable film layer, a street, and a portion of a silicon substrate.

[0052] By contrast, if non-optimal laser parameters are selected, in a stacked structure that involves two or more of an inorganic dielectric, an organic dielectric, a semiconductor, or a metal, a laser ablation process may cause delamination issues. For example, a laser penetrate through high bandgap energy dielectrics (such as silicon dioxide with an approximately of 9eV bandgap) without measurable absorption. However, the laser energy may be absorbed in an underlying metal or silicon layer, causing significant vaporization of the metal or silicon layers. The vaporization may generate high pressures to lift-off the overlying silicon dioxide dielectric layer and potentially causing severe interlayer delamination and microcracking. In an embodiment, while picoseconds-based laser irradiation processes lead to microcracking and delaminating in complex stacks, femtosecond-based laser irradiation processes have been demonstrated to not lead to microcracking or delamination of the same material stacks.

[0053] In order to be able to directly ablate dielectric layers, ionization of the dielectric materials may need to occur such that they behave similar to a conductive material by strongly absorbing photons. The absorption may block a majority of the laser energy from penetrating through to underlying silicon or metal layers before ultimate ablation of the dielectric layer. In an embodiment, ionization of inorganic dielectrics is feasible when the laser intensity is sufficiently high to initiate photon-ionization and impact ionization in the inorganic dielectric materials.

[0054] In accordance with an embodiment of the present invention, suitable femtosecond-based laser processes are characterized by a high peak intensity (irradiance) that usually leads to nonlinear interactions in various materials. In one such embodiment, the femtosecond laser sources have a pulse width approximately in the range of 10 femtoseconds to 500

femtoseconds, although preferably in the range of 100 femtoseconds to 400 femtoseconds. In one embodiment, the femtosecond laser sources have a wavelength approximately in the range of 1570 nanometers to 200 nanometers, although preferably in the range of 540 nanometers to 250 nanometers. In one embodiment, the laser and corresponding optical system provide a focal spot at the work surface approximately in the range of 3 microns to 15 microns, though preferably approximately in the range of 5 microns to 10 microns.

[0055] The spacial beam profile at the work surface may be a single mode (Gaussian) or have a shaped top-hat profile. In an embodiment, the laser source has a pulse repetition rate approximately in the range of 200 kHz to 10 MHz, although preferably approximately in the range of 500kHz to 5MHz. In an embodiment, the laser source delivers pulse energy at the work surface approximately in the range of 0.5 uJ to 100 uJ, although preferably approximately in the range of 1uJ to 5uJ. In an embodiment, the laser scribing process runs along a work piece surface at a speed approximately in the range of 500mm/sec to 5m/sec, although preferably approximately in the range of 600mm/sec to 2m/sec.

[0056] The scribing process may be run in single pass only, or in multiple passes, but, in an embodiment, preferably 1-2 passes. In one embodiment, the scribing depth in the work piece is approximately in the range of 5 microns to 50 microns deep, preferably approximately in the range of 10 microns to 20 microns deep. The laser may be applied either in a train of single pulses at a given pulse repetition rate or a train of pulse bursts. In an embodiment, the kerf width of the laser beam generated is approximately in the range of 2 microns to 15 microns, although in silicon wafer scribing/dicing preferably approximately in the range of 6 microns to 10 microns, measured at the device/silicon interface.

[0057] Laser parameters may be selected with benefits and advantages such as providing sufficiently high laser intensity to achieve ionization of inorganic dielectrics (e.g., silicon dioxide) and to minimize delamination and chipping caused by underlayer damage prior to direct ablation of inorganic dielectrics. Also, parameters may be selected to provide meaningful process throughput for industrial applications with precisely controlled ablation width (e.g., kerf width) and depth. As described above, a femtosecond-based laser is far more suitable to providing such advantages, as compared with picosecond-based and nanosecond-based laser ablation processes. However, even in the spectrum of femtosecond-based laser ablation, certain wavelengths may provide better performance than others. For example, in one embodiment, a femtosecond-based laser process having a wavelength closer to or in the UV range provides a cleaner ablation process than a femtosecond-based laser process having a wavelength closer to or in the IR range. In a specific such embodiment, a femtosecond-based

laser process suitable for semiconductor wafer or substrate scribing is based on a laser having a wavelength of approximately less than or equal to 540 nanometers. In a particular such embodiment, pulses of approximately less than or equal to 400 femtoseconds of the laser having the wavelength of approximately less than or equal to 540 nanometers are used. However, in an alternative embodiment, dual laser wavelengths (e.g., a combination of an IR laser and a UV laser) are used.

[0058] Referring to portion 306 of Flowchart 300, and corresponding Figure 4E, the semiconductor wafer 404 is etched through the gaps 410 in the patterned mask 408 to singulate the integrated circuits 406. In accordance with an embodiment of the present invention, etching the semiconductor wafer 404 includes etching the trenches 412 formed with the femtosecond-based laser scribing process to ultimately etch entirely through semiconductor wafer 404, as depicted in Figure 4E. In one embodiment, the etching is performed by using a first etching operation 360 to provide a bulk etch, and then performing a second etching operation 362 to smooth exposed surfaces of the diced wafer or substrate, as depicted in Flowchart 300.

[0059] In an embodiment, etching the semiconductor wafer 404 includes using a plasma etching process. In one embodiment, a through-silicon via type etch process is used. For example, in a specific embodiment, the etch rate of the material of semiconductor wafer 404 is greater than 25 microns per minute. An ultra-high-density plasma source may be used for the plasma etching portion of the die singulation process. An example of a process chamber suitable to perform such a plasma etch process is the Applied Centura® Silvia™ Etch system available from Applied Materials of Sunnyvale, CA, USA. The Applied Centura® Silvia™ Etch system combines the capacitive and inductive RF coupling, which gives much more independent control of the ion density and ion energy than was possible with the capacitive coupling only, even with the improvements provided by magnetic enhancement. This combination enables effective decoupling of the ion density from ion energy, so as to achieve relatively high density plasmas without the high, potentially damaging, DC bias levels, even at very low pressures. This results in an exceptionally wide process window. However, any plasma etch chamber capable of etching silicon may be used. In an exemplary embodiment, a deep silicon etch is used to etch a single crystalline silicon substrate or wafer 404 at an etch rate greater than approximately 40% of conventional silicon etch rates while maintaining essentially precise profile control and virtually scallop-free sidewalls. In a specific embodiment, a through-silicon via type etch process is used. The etch process is based on a plasma generated from a reactive gas, which generally a fluorine-based gas such as SF₆, C₄F₈,

CHF₃, XeF₂, or any other reactant gas capable of etching silicon at a relatively fast etch rate. In an embodiment, the patterned hybrid mask composed of a water soluble film layer and a UV-curable film layer 408 is removed after the singulation process, as depicted in Figure 4E.

[0060] In an embodiment, following the laser and etch processes, such as those processes described above, the dies are singulated. Next, the wafer first goes through UV curing treatment (e.g., operation 364 of Flowchart 300) to reduce the adhesion of the second layer (UV-curable layer) to the water soluble film layer of the hybrid mask. Then, the now cured UV-curable layer can be peeled, and the remaining portions of the hybrid mask (e.g., essentially the water-soluble portion) is removed using water or another aqueous medium as described above. Alternatively, both layers may be removed directly upon aqueous treatment, following UV exposure. It is to be understood that other orderings of operations can be contemplated within the spirit and scope of embodiments of the present invention.

[0061] Accordingly, referring again to Flowchart 300 and Figures 4A-4E, wafer dicing may be preformed by initial laser ablation through a mask layer, through wafer streets (including metallization), and partially into a silicon substrate. The laser pulse width may be selected in the femtosecond range. Die singulation may then be completed by subsequent through-silicon deep plasma etching. A specific example of a materials stack for dicing is described below in association with Figures 9A-9D, in accordance with an embodiment of the present invention.

[0062] Referring to Figure 9A, a materials stack for hybrid laser ablation and plasma etch dicing includes a hybrid mask 902 composed of a water soluble film layer and a UV-curable film layer, a device layer 904, and a substrate 906. The mask layer, device layer, and substrate are disposed above a die attach film 908 which is affixed to a backing tape 910. In an embodiment, the hybrid mask 902 is a mask such as described above in association with mask 402. The device layer 904 includes an inorganic dielectric layer (such as silicon dioxide) disposed above one or more metal layers (such as copper layers) and one or more low K dielectric layers (such as carbon-doped oxide layers). The device layer 904 also includes streets arranged between integrated circuits, the streets including the same or similar layers to the integrated circuits. The substrate 906 is a bulk single-crystalline silicon substrate.

[0063] In an embodiment, the bulk single-crystalline silicon substrate 906 is thinned from the backside prior to being affixed to the die attach film 908. The thinning may be performed by a backside grind process. In one embodiment, the bulk single-crystalline silicon substrate 906 is thinned to a thickness approximately in the range of 50 – 100 microns. It is important to note that, in an embodiment, the thinning is performed prior to a laser ablation and plasma

etch dicing process. In an embodiment, the spin-on mask layer 902 is an approximately 20-150 micron thick layer and the device layer 904 has a thickness approximately in the range of 2 – 3 microns. In an embodiment, the die attach film 908 (or any suitable substitute capable of bonding a thinned or thin wafer or substrate to the backing tape 910) has a thickness of approximately 20 microns.

[0064] Referring to Figure 9B, the hybrid mask 902, the device layer 904 and a portion of the substrate 906 are patterned with a femtosecond-based laser scribing process 912 to form trenches 914 in the substrate 906. Referring to Figure 9C, a through-silicon deep plasma etch process 916 is used to extend the trench 914 down to the die attach film 908, exposing the top portion of the die attach film 908 and singulating the silicon substrate 906. The device layer 904 is protected by the spin-on mask layer 902 during the through-silicon deep plasma etch process 916.

[0065] Referring to Figure 9D, the singulation process may further include patterning the die attach film 908, exposing the top portion of the backing tape 910 and singulating the die attach film 908. In an embodiment, the die attach film is singulated by a laser process or by an etch process. Further embodiments may include subsequently removing the singulated portions of substrate 906 (e.g., as individual integrated circuits) from the backing tape 910. In one embodiment, the singulated die attach film 908 is retained on the back sides of the singulated portions of substrate 906. Other embodiments may include removing the hybrid mask 902 from the device layer 904. In an alternative embodiment, in the case that substrate 906 is thinner than approximately 50 microns, the laser ablation process 912 is used to completely singulate substrate 906 without the use of an additional plasma process.

[0066] Subsequent to singulating the die attach film 908, in an embodiment, the hybrid mask 902 is removed from the device layer 904. In an embodiment, the singulated integrated circuits are removed from the backing tape 910 for packaging. In one such embodiment, the patterned die attach film 908 is retained on the backside of each integrated circuit and included in the final packaging. However, in another embodiment, the patterned die attach film 908 is removed during or subsequent to the singulation process.

[0067] Referring again to Figures 4A-4E, the plurality of integrated circuits 406 may be separated by streets 407 having a width of approximately 10 microns or smaller. The use of a femtosecond-based laser scribing approach, at least in part due to the tight profile control of the laser, may enable such compaction in a layout of integrated circuits. For example, Figure 10 illustrates compaction on a semiconductor wafer or substrate achieved by using narrower streets versus conventional dicing which may be limited to a minimum width, in accordance

with an embodiment of the present invention.

[0068] Referring to Figure 10, compaction on a semiconductor wafer is achieved by using narrower streets (e.g., widths of approximately 10 microns or smaller in layout 1002) versus conventional dicing which may be limited to a minimum width (e.g., widths of approximately 70 microns or larger in layout 1000). It is to be understood, however, that it may not always be desirable to reduce the street width to less than 10 microns even if otherwise enabled by a femtosecond-based laser scribing process. For example, some applications may require a street width of at least 40 microns in order to fabricate dummy or test devices in the streets separating the integrated circuits.

[0069] Referring again to Figures 4A-4E, the plurality of integrated circuits 406 may be arranged on semiconductor wafer or substrate 404 in a non-restricted layout. For example, Figure 11 illustrates freeform integrated circuit arrangement allowing denser packing. The denser packing may provide for more die per wafer versus grid alignment approaches, in accordance with an embodiment of the present invention. Referring to Figure 11, a freeform layout (e.g., a non-restricted layout on semiconductor wafer or substrate 1102) allows denser packing and hence more die per wafer versus grid alignment approaches (e.g., a restricted layout on semiconductor wafer or substrate 1100). In an embodiment, the speed of the laser ablation and plasma etch singulation process is independent of die size, layout or the number of streets.

[0070] A single process tool may be configured to perform many or all of the operations in a hybrid laser ablation and plasma etch singulation process. For example, Figure 12 illustrates a block diagram of a tool layout for laser and plasma dicing of wafers or substrates, in accordance with an embodiment of the present invention.

[0071] Referring to Figure 12, a process tool 1200 includes a factory interface 1202 (FI) having a plurality of load locks 1204 coupled therewith. A cluster tool 1206 is coupled with the factory interface 1202. The cluster tool 1206 includes one or more plasma etch chambers, such as plasma etch chamber 1208. A laser scribe apparatus 1210 is also coupled to the factory interface 1202. The overall footprint of the process tool 1200 may be, in one embodiment, approximately 3500 millimeters (3.5 meters) by approximately 3800 millimeters (3.8 meters), as depicted in Figure 12.

[0072] In an embodiment, the laser scribe apparatus 1210 houses a femtosecond-based laser. The femtosecond-based laser is suitable for performing a laser ablation portion of a hybrid laser and etch singulation process, such as the laser ablation processes described above. In one embodiment, a moveable stage is also included in laser scribe apparatus 1200,

the moveable stage configured for moving a wafer or substrate (or a carrier thereof) relative to the femtosecond-based laser. In a specific embodiment, the femtosecond-based laser is also moveable. The overall footprint of the laser scribe apparatus 1210 may be, in one embodiment, approximately 2240 millimeters by approximately 1270 millimeters, as depicted in Figure 12.

[0073] In an embodiment, the one or more plasma etch chambers 1208 is configured for etching a wafer or substrate through the gaps in a patterned mask to singulate a plurality of integrated circuits. In one such embodiment, the one or more plasma etch chambers 1208 is configured to perform a deep silicon etch process. In a specific embodiment, the one or more plasma etch chambers 1208 is an Applied Centura® Silvia™ Etch system, available from Applied Materials of Sunnyvale, CA, USA. The etch chamber may be specifically designed for a deep silicon etch used to create singulate integrated circuits housed on or in single crystalline silicon substrates or wafers. In an embodiment, a high-density plasma source is included in the plasma etch chamber 1208 to facilitate high silicon etch rates. In an embodiment, more than one etch chamber is included in the cluster tool 1206 portion of process tool 1200 to enable high manufacturing throughput of the singulation or dicing process.

[0074] The factory interface 1202 may be a suitable atmospheric port to interface between an outside manufacturing facility with laser scribe apparatus 1210 and cluster tool 1206. The factory interface 1202 may include robots with arms or blades for transferring wafers (or carriers thereof) from storage units (such as front opening unified pods) into either cluster tool 1206 or laser scribe apparatus 1210, or both.

[0075] Cluster tool 1206 may include other chambers suitable for performing functions in a method of singulation. For example, in one embodiment, in place of an additional etch chamber, a deposition chamber 1212 is included. The deposition chamber 1212 may be configured for mask deposition on or above a device layer of a wafer or substrate prior to laser scribing of the wafer or substrate, e.g., by a spin-on process. In one such embodiment, the deposition chamber 1212 is suitable for depositing a water-soluble layer followed by deposition of a UV-curable layer, to provide a hybrid mask. In another embodiment, in place of an additional etch chamber, a wet/dry station 1214 is included. The wet/dry station may be suitable for cleaning residues and fragments, or for removing a mask having a water-soluble portion, subsequent to a laser scribe and plasma etch singulation process of a substrate or wafer. In an embodiment, an ultra-violet (UV) irradiation station (shown for convenience as 1214), e.g., including a UV light source, is included for weakening a UV-curable layer of a

hybrid mask. In one such embodiment, the UV irradiation station is configured to reduce an adhesiveness of the UV-curable layer by at least approximately 90%. In an embodiment, a metrology station is also included as a component of process tool 1200.

[0076] Embodiments of the present invention may be provided as a computer program product, or software, that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer system (or other electronic devices) to perform a process according to embodiments of the present invention. In one embodiment, the computer system is coupled with process tool 1200 described in association with Figure 12. A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable (e.g., computer-readable) medium includes a machine (e.g., a computer) readable storage medium (e.g., read only memory (“ROM”), random access memory (“RAM”), magnetic disk storage media, optical storage media, flash memory devices, etc.), a machine (e.g., computer) readable transmission medium (electrical, optical, acoustical or other form of propagated signals (e.g., infrared signals, digital signals, etc.)), etc.

[0077] Figure 13 illustrates a diagrammatic representation of a machine in the exemplary form of a computer system 1300 within which a set of instructions, for causing the machine to perform any one or more of the methodologies described herein, may be executed. In alternative embodiments, the machine may be connected (e.g., networked) to other machines in a Local Area Network (LAN), an intranet, an extranet, or the Internet. The machine may operate in the capacity of a server or a client machine in a client-server network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The machine may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular telephone, a web appliance, a server, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while only a single machine is illustrated, the term “machine” shall also be taken to include any collection of machines (e.g., computers) that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies described herein.

[0078] The exemplary computer system 1300 includes a processor 1302, a main memory 1304 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory 1306 (e.g., flash memory, static random access memory (SRAM), etc.), and a secondary memory 1318 (e.g., a data storage device), which communicate with each other via

a bus 1330.

[0079] Processor 1302 represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor 1302 may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 1302 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like. Processor 1302 is configured to execute the processing logic 1326 for performing the operations described herein.

[0080] The computer system 1300 may further include a network interface device 1308. The computer system 1300 also may include a video display unit 1310 (e.g., a liquid crystal display (LCD), a light emitting diode display (LED), or a cathode ray tube (CRT)), an alphanumeric input device 1312 (e.g., a keyboard), a cursor control device 1314 (e.g., a mouse), and a signal generation device 1316 (e.g., a speaker).

[0081] The secondary memory 1318 may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) 1331 on which is stored one or more sets of instructions (e.g., software 1322) embodying any one or more of the methodologies or functions described herein. The software 1322 may also reside, completely or at least partially, within the main memory 1304 and/or within the processor 1302 during execution thereof by the computer system 1300, the main memory 1304 and the processor 1302 also constituting machine-readable storage media. The software 1322 may further be transmitted or received over a network 1320 via the network interface device 1308.

[0082] While the machine-accessible storage medium 1331 is shown in an exemplary embodiment to be a single medium, the term “machine-readable storage medium” should be taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term “machine-readable storage medium” shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present invention. The term “machine-readable storage medium” shall accordingly be taken to include, but not be limited to, solid-state memories, and optical and magnetic media.

[0083] In accordance with an embodiment of the present invention, a machine-accessible

storage medium has instructions stored thereon which cause a data processing system to perform a method of dicing a semiconductor wafer having a plurality of integrated circuits. The method includes forming a hybrid mask above the semiconductor wafer, the hybrid mask composed of a water-soluble layer disposed on the integrated circuits, and a UV-curable layer disposed on the water-soluble layer. The hybrid mask is patterned with a laser scribing process to provide a patterned hybrid mask with gaps to expose regions of the semiconductor wafer between the integrated circuits. The semiconductor wafer is etched through the gaps in the patterned hybrid mask to singulate the integrated circuits.

[0084] Thus, methods of using a hybrid mask composed of a water soluble film layer and a UV-curable film layer for wafer dicing using laser scribing and plasma etch have been disclosed.

CLAIMS

What is claimed is:

1. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:
 - forming a hybrid mask above the semiconductor wafer, the hybrid mask comprising a water-soluble layer formed on the integrated circuits and a UV-curable layer formed on the water-soluble layer;
 - patterning the hybrid mask with a laser scribing process to provide a patterned hybrid mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits; and
 - etching the semiconductor wafer through the gaps in the patterned hybrid mask to singulate the integrated circuits.
2. The method of claim 1, further comprising:
 - subsequent to etching the semiconductor wafer, removing the patterned hybrid mask.
3. The method of claim 2, wherein the removing comprises exposing the patterned hybrid mask to UV light and, subsequently, exposing the patterned hybrid mask to an aqueous solution.
4. The method of claim 1, wherein the water-soluble layer comprises a material selected from the group consisting of polyvinyl alcohol, polyacrylic acid, dextran, polymethacrylic acid, polyethylene imine, and polyethylene oxide.
5. The method of claim 1, wherein the UV-curable layer comprises a material selected from the group consisting of polyvinyl chloride and an acrylic-based material.
6. The method of claim 1, wherein patterning the hybrid mask with the laser scribing process comprises using a femtosecond-based laser.
7. The method of claim 1, wherein patterning the mask with the laser scribing process comprises forming trenches in the regions of the semiconductor wafer between the integrated circuits, and wherein plasma etching the semiconductor wafer comprises extending the

trenches to form corresponding trench extensions.

8. The method of claim 7, wherein each of the trenches has a width, and wherein each of the corresponding trench extensions has the width.

9. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:

providing a semiconductor wafer having a hybrid mask disposed thereon, the hybrid mask comprising a water-soluble layer disposed on the integrated circuits and a UV-curable layer disposed on the water-soluble layer;

patterning the hybrid mask with a laser scribing process to provide a patterned hybrid mask with gaps, exposing regions of the semiconductor wafer between the integrated circuits; and

etching the semiconductor wafer through the gaps in the patterned hybrid mask to singulate the integrated circuits.

10. The method of claim 9, further comprising:

subsequent to etching the semiconductor wafer, removing the patterned hybrid mask.

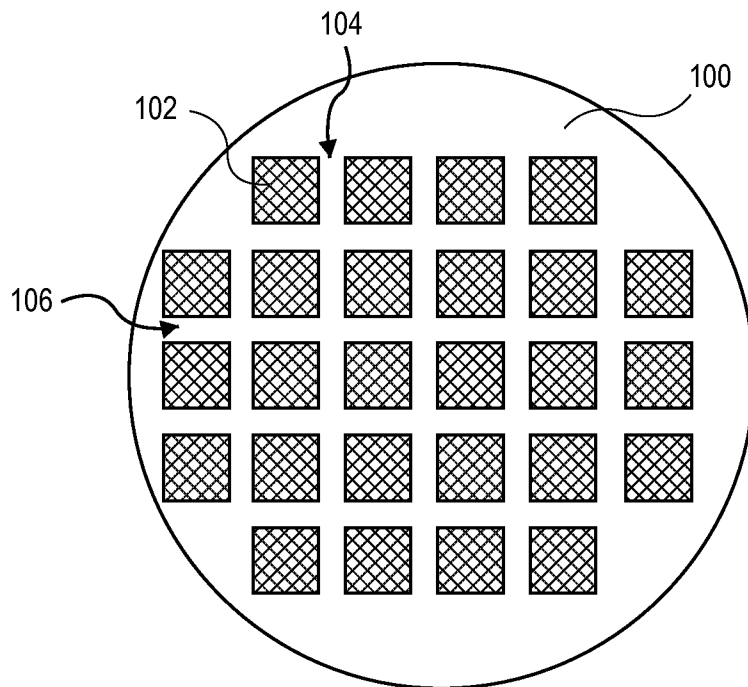
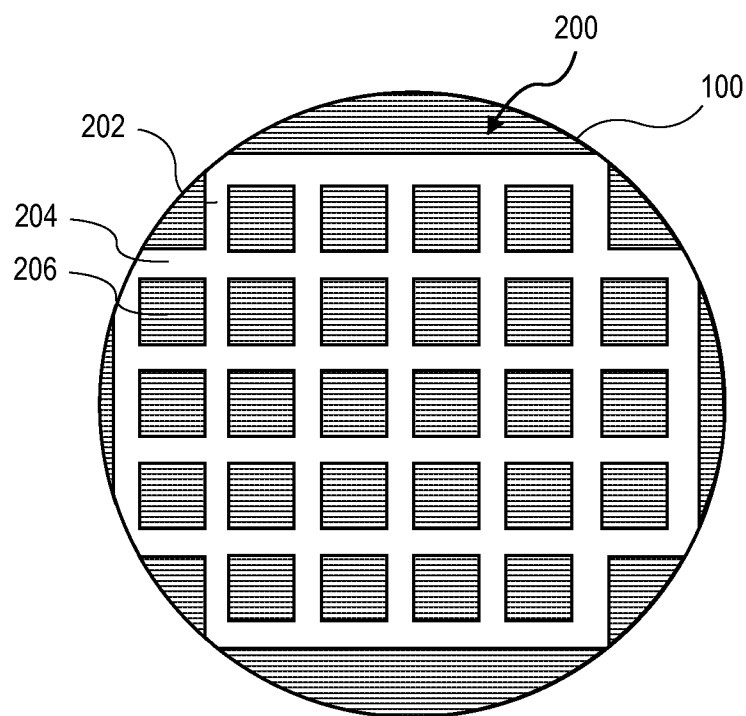
11. The method of claim 10, wherein the removing comprises exposing the patterned hybrid mask to UV light and, subsequently, exposing the patterned hybrid mask to an aqueous solution.

12. The method of claim 9, wherein the water-soluble layer comprises a material selected from the group consisting of polyvinyl alcohol, polyacrylic acid, dextran, polymethacrylic acid, polyethylene imine, and polyethylene oxide.

13. The method of claim 9, wherein the UV-curable layer comprises a material selected from the group consisting of polyvinyl chloride and an acrylic-based material.

14. The method of claim 9, wherein patterning the hybrid mask with the laser scribing process comprises using a femtosecond-based laser.

15. The method of claim 9, wherein patterning the mask with the laser scribing process comprises forming trenches in the regions of the semiconductor wafer between the integrated circuits, wherein plasma etching the semiconductor wafer comprises extending the trenches to form corresponding trench extensions, wherein each of the trenches has a width, and wherein each of the corresponding trench extensions has the width.

**FIG. 1****FIG. 2**

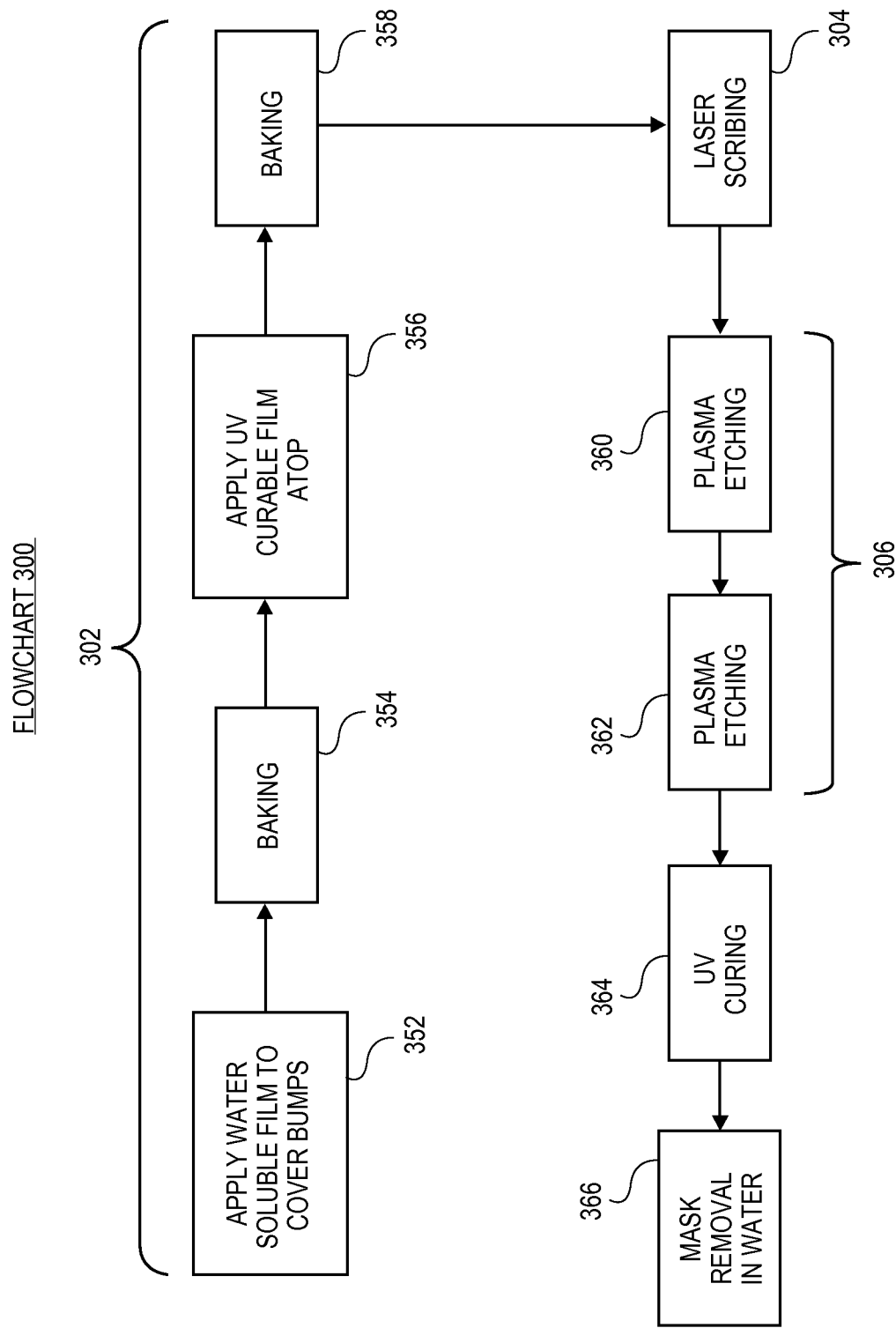
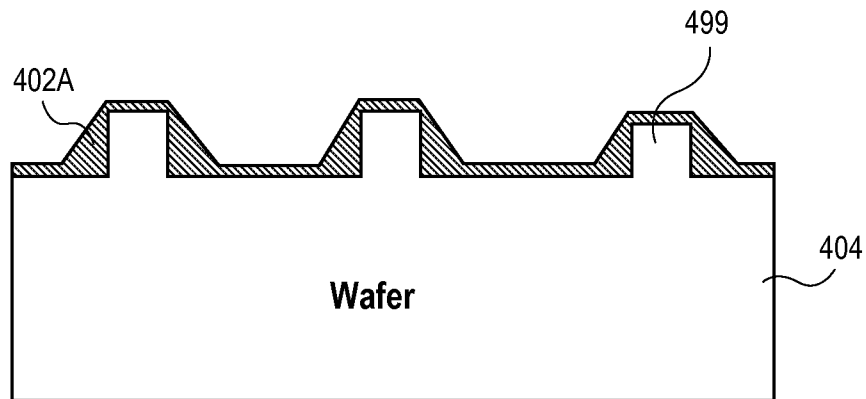
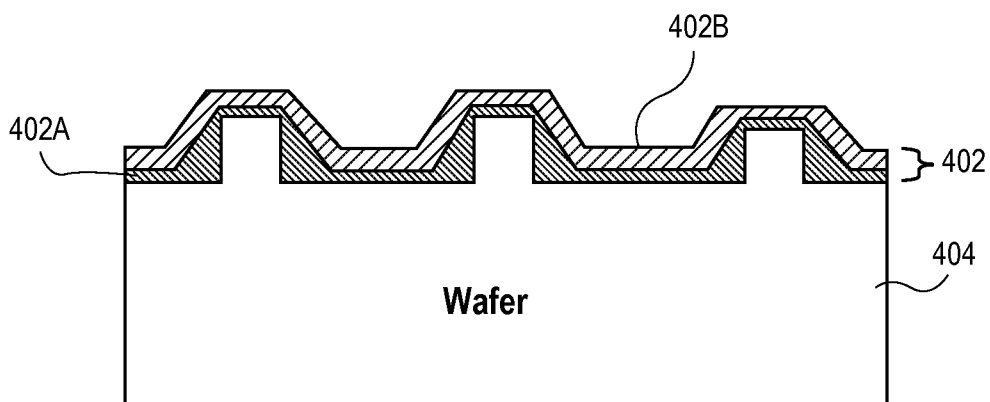


FIG. 3

**FIG. 4A****FIG. 4B**

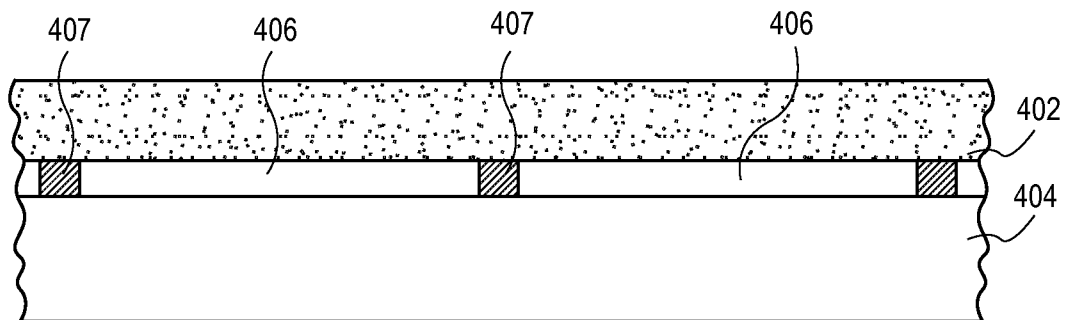


FIG. 4C

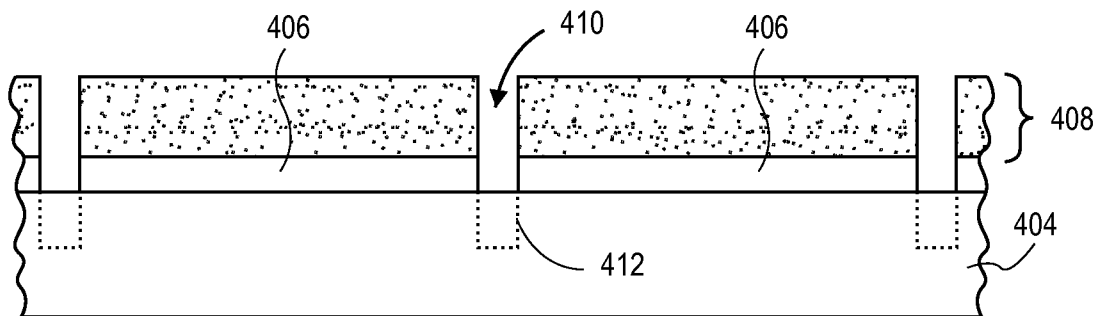


FIG. 4D

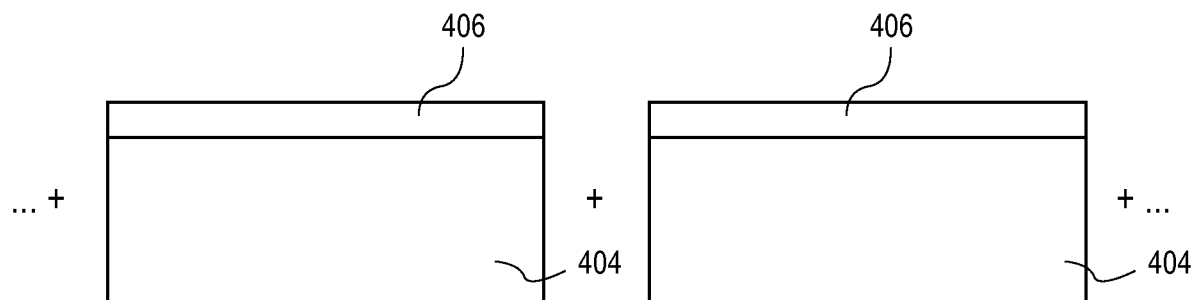


FIG. 4E

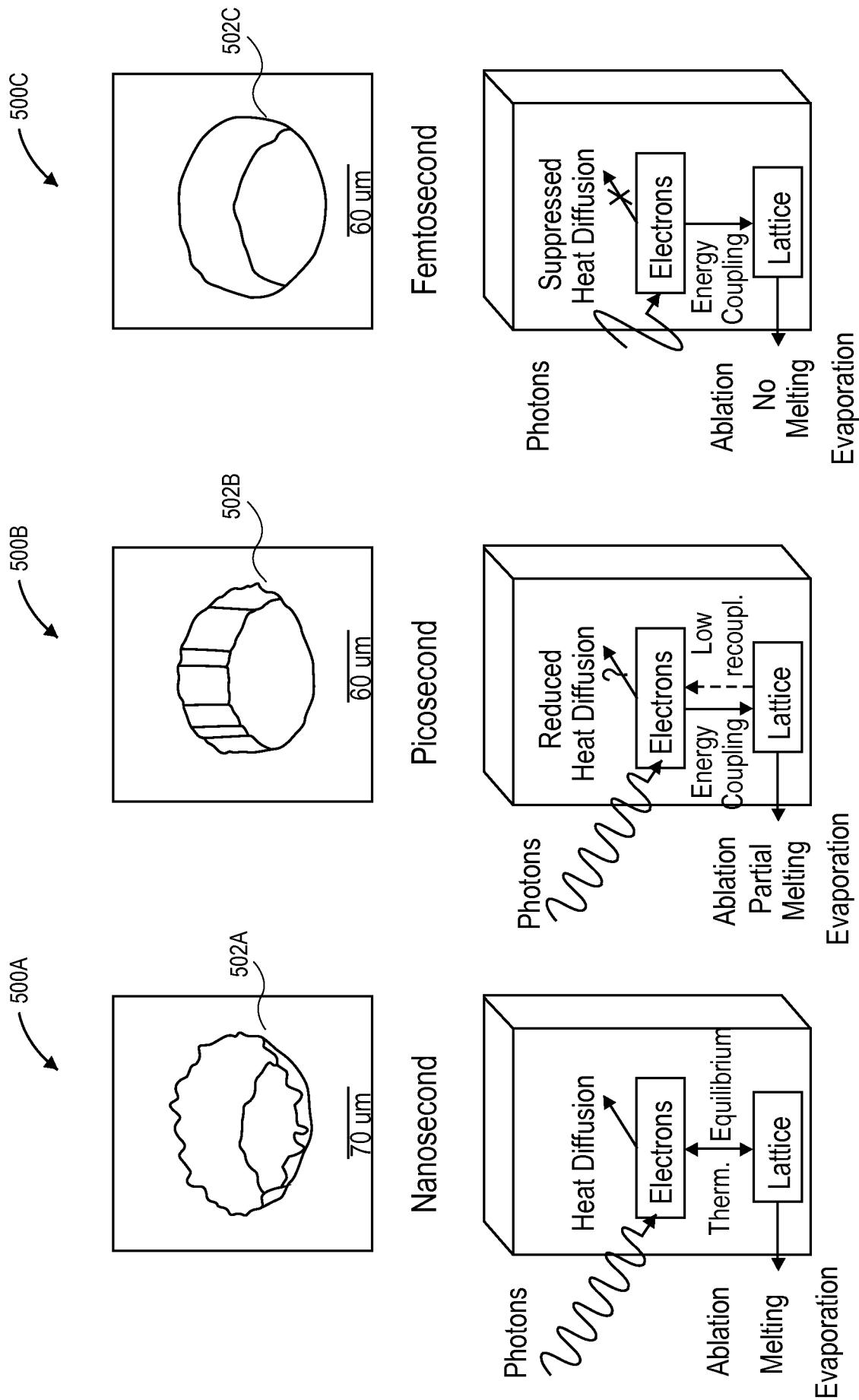


FIG. 5

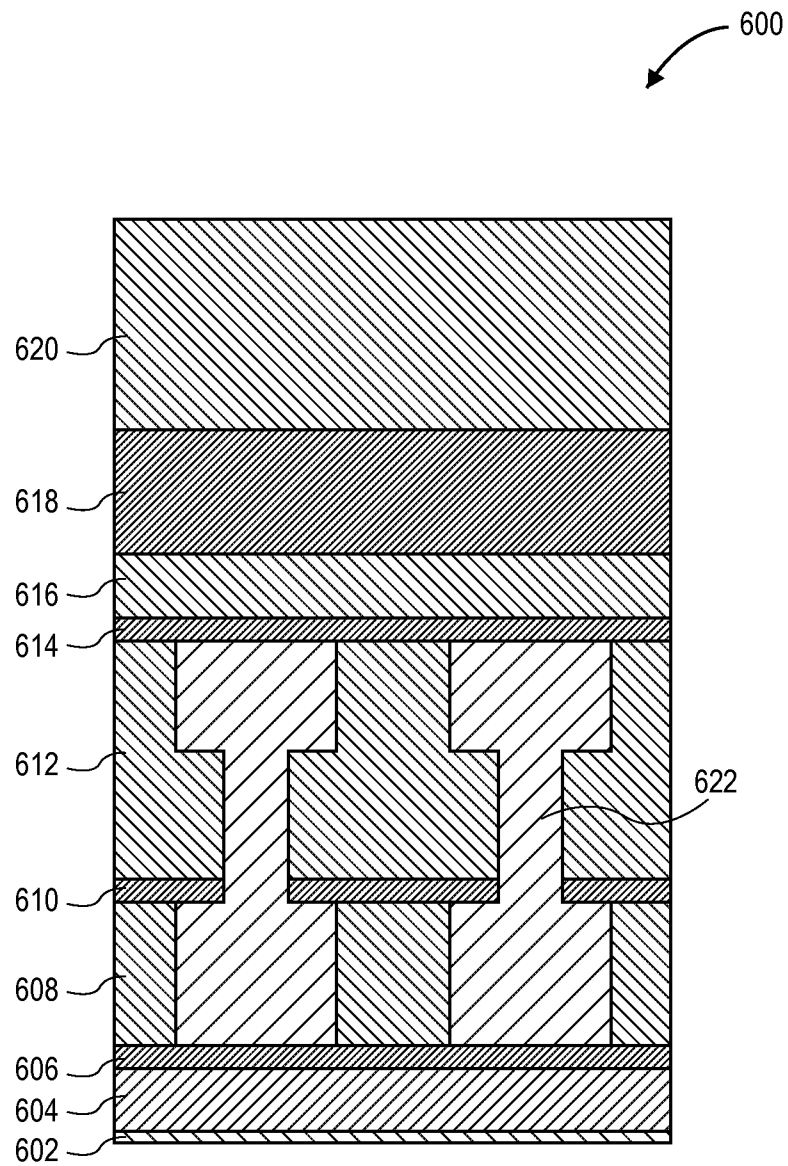
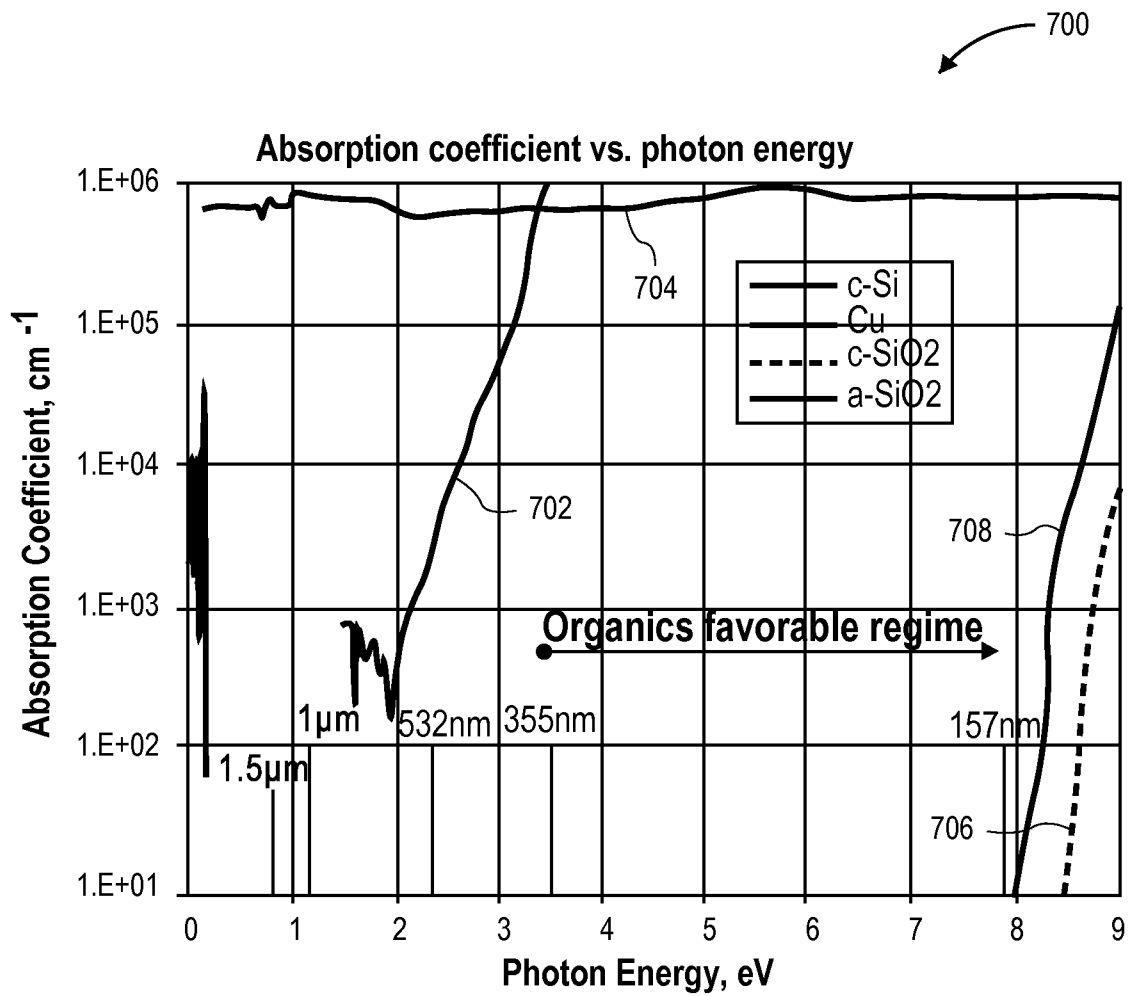


FIG. 6



$$I = \frac{\text{Pulse Energy } E_p}{\pi \cdot w_0^2 \cdot \tau}$$

Intensity

Beam Radius

Pulse Width

FIG. 8

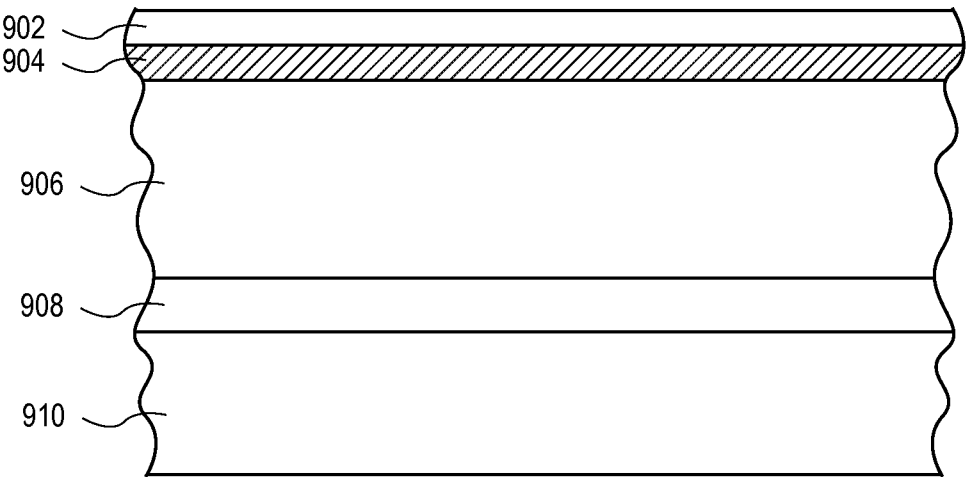


FIG. 9A

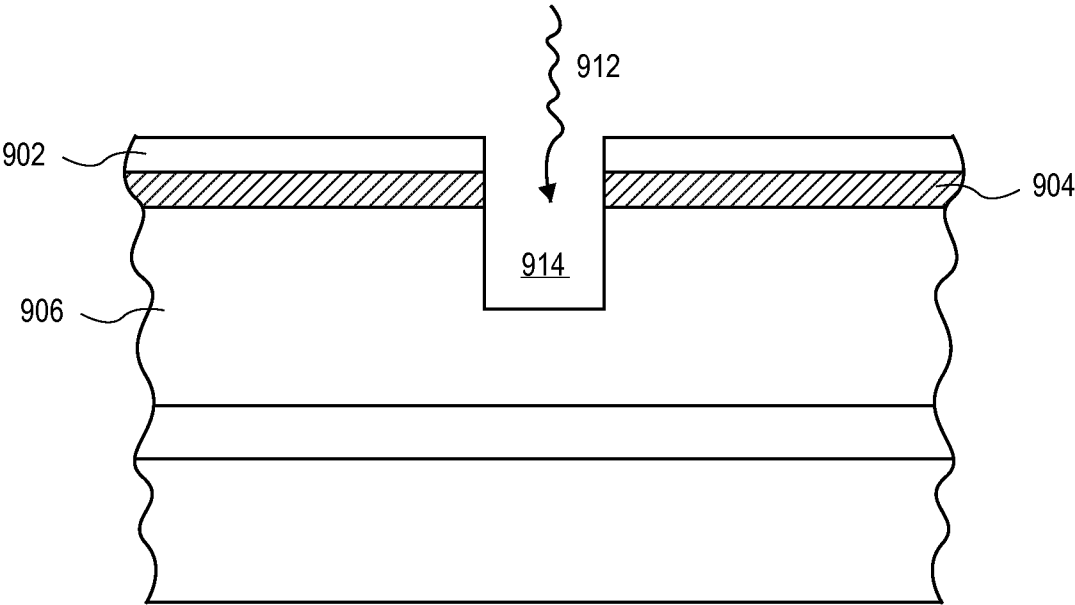


FIG. 9B

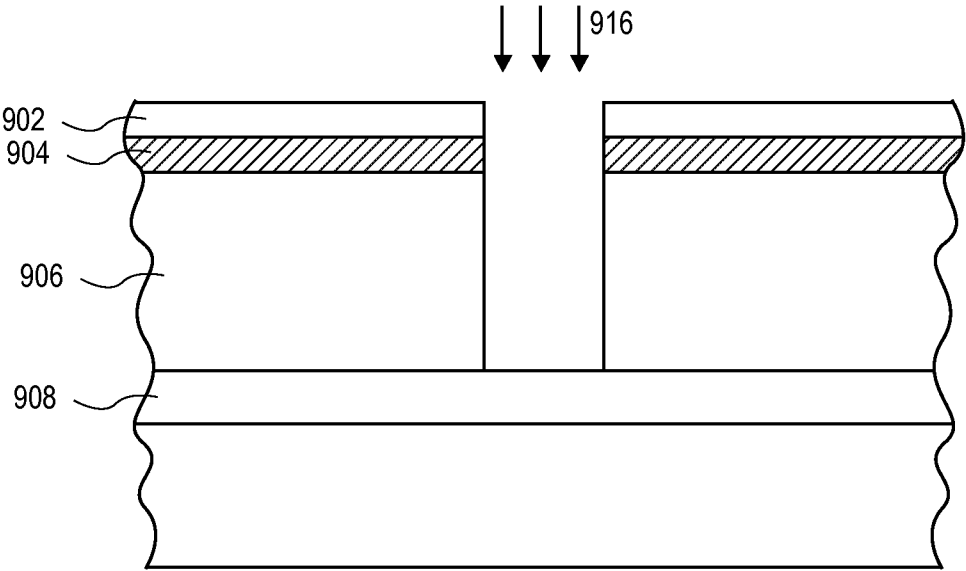


FIG. 9C

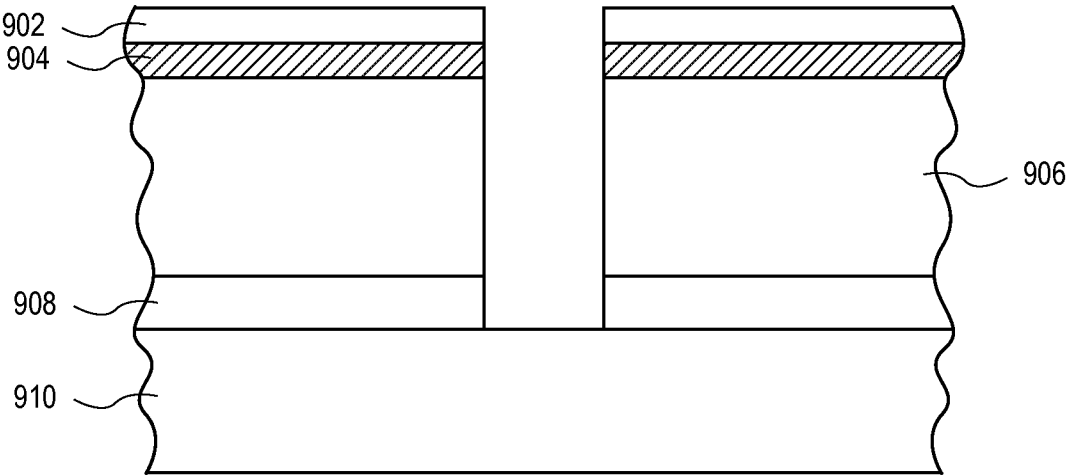


FIG. 9D

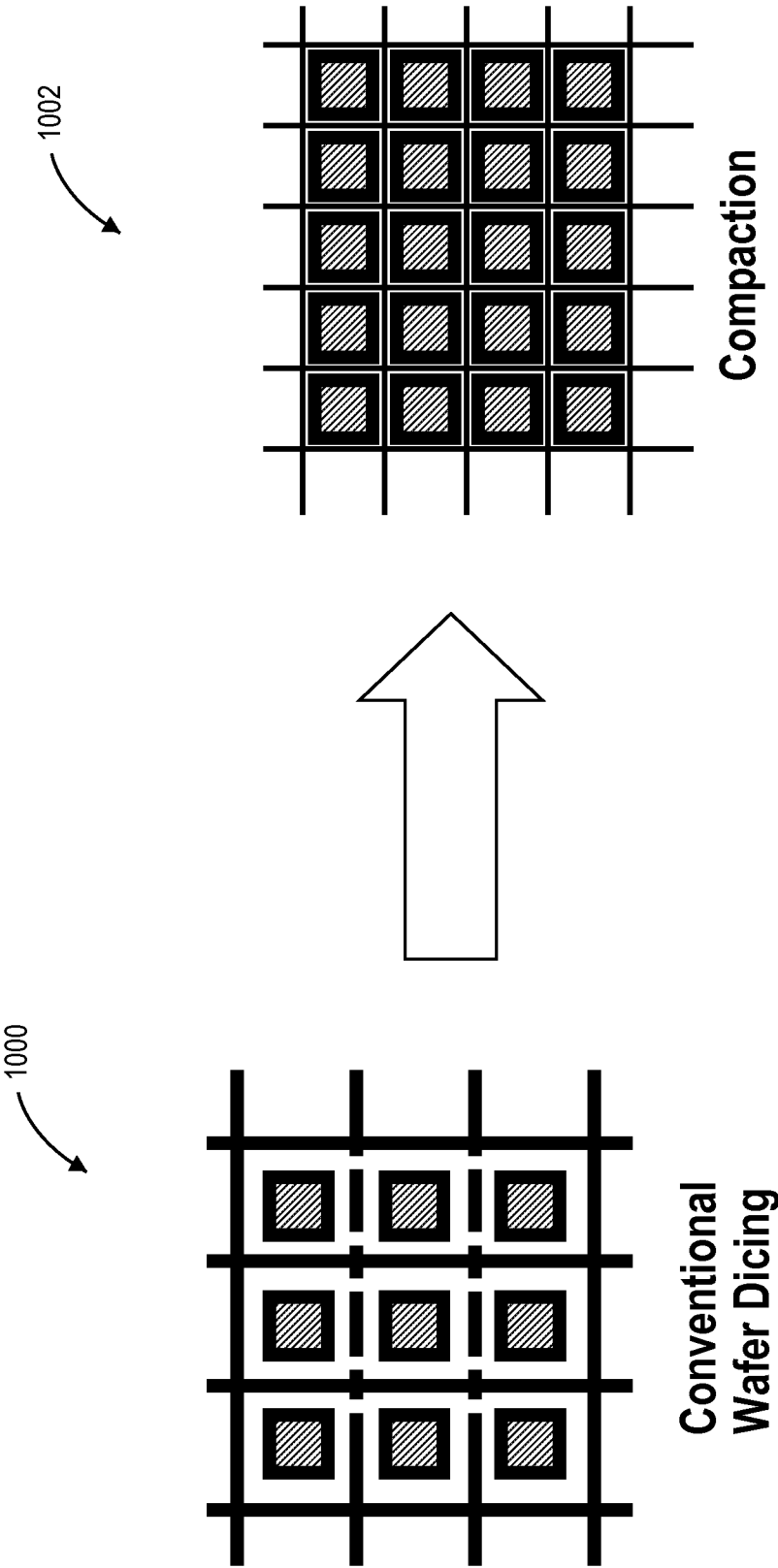


FIG. 10

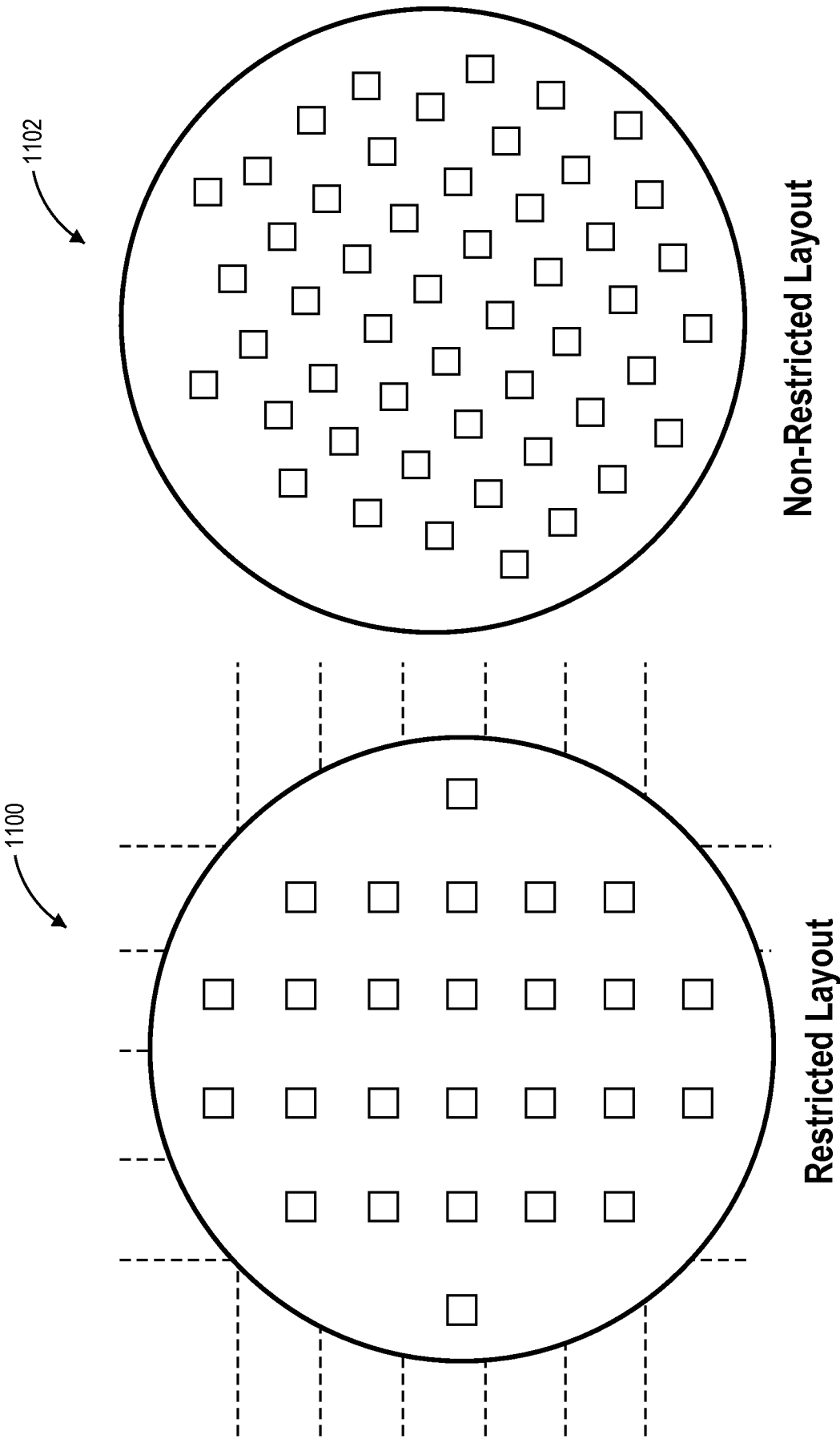


FIG. 11

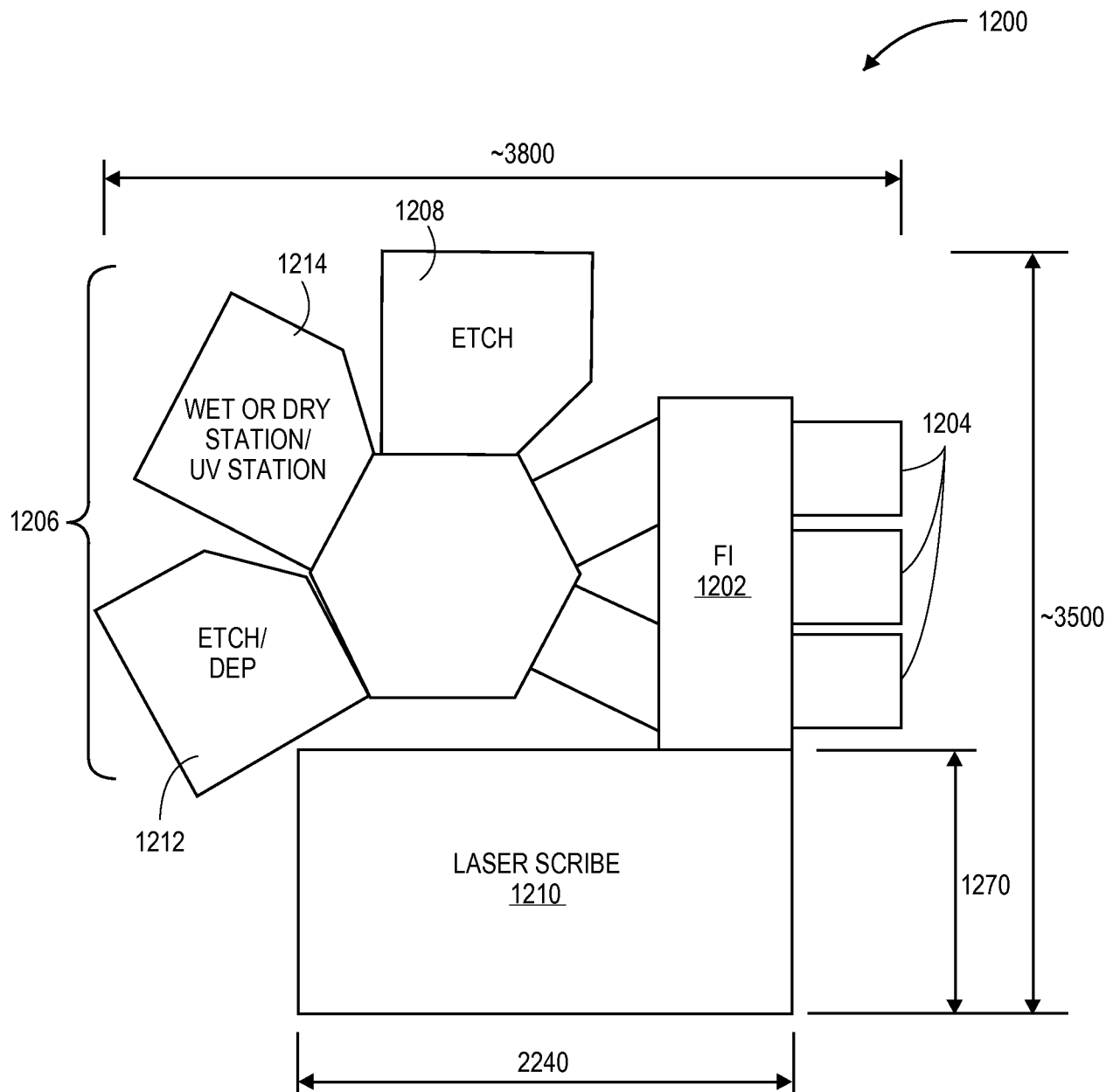
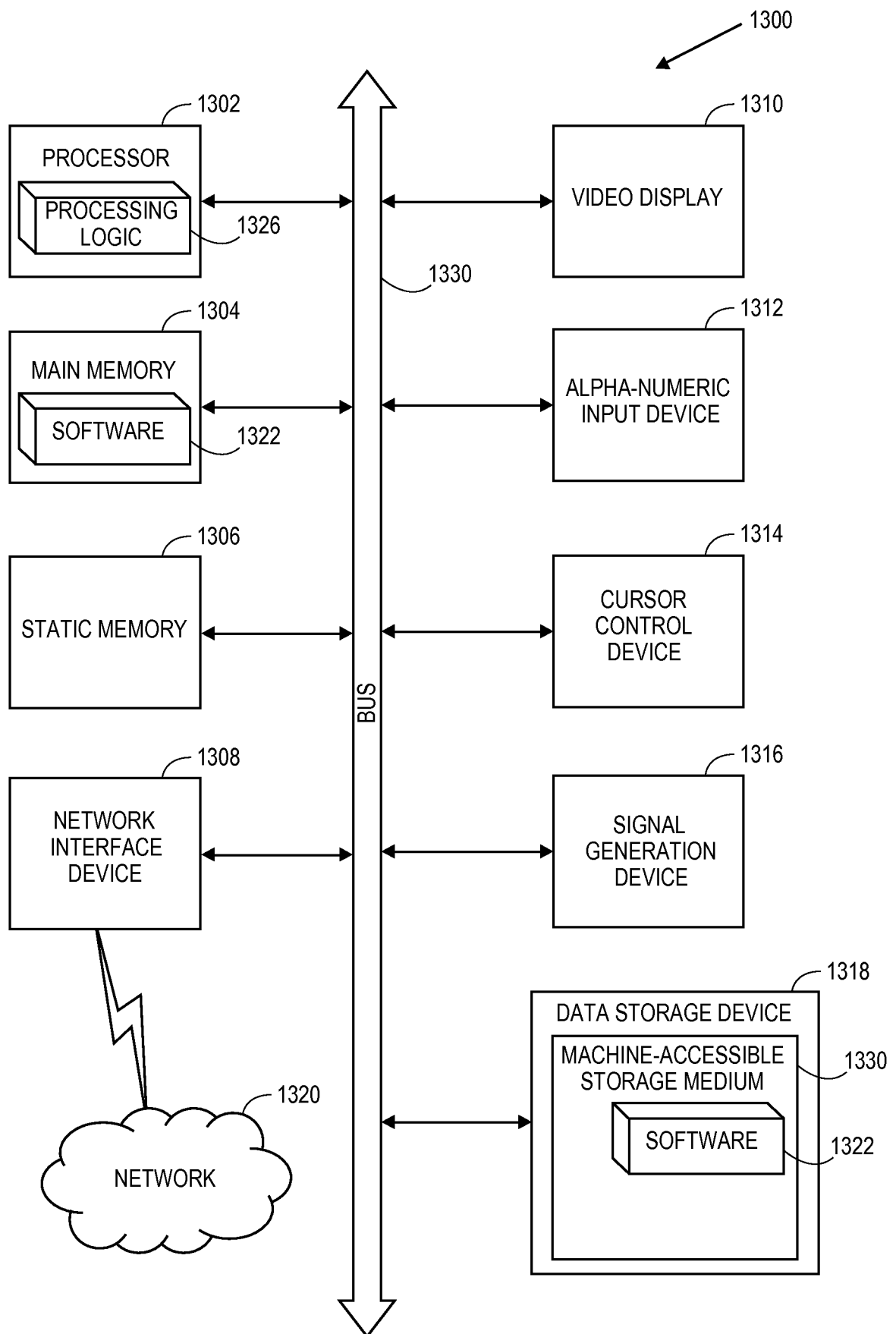


FIG. 12

**FIG. 13**