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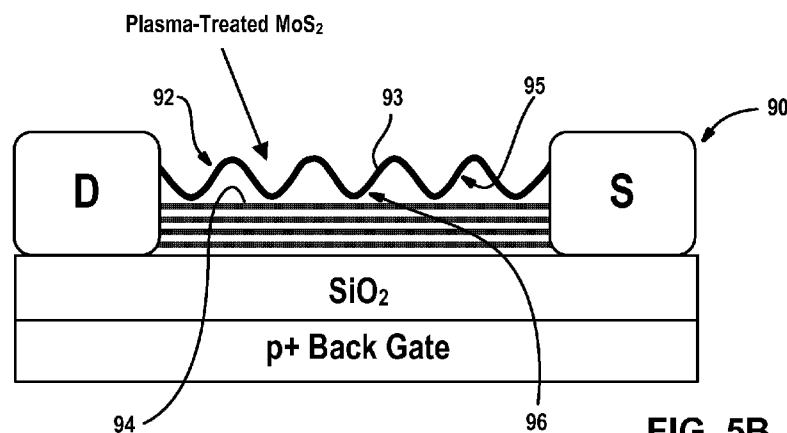
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(54) Title: FIELD EFFECT TRANSISTOR MEMORY DEVICE

**FIG. 5B**

(57) Abstract: A method for generating a non-volatile memory device may comprise: applying plasma for a preset time period to an exposed surface of a channel of a field effect transistor such that a plurality of charge-trapping sites are formed at the channel. The channel is comprised of a multi-layer structure of atomically thin two-dimensional sheets.

## FIELD EFFECT TRANSISTOR MEMORY DEVICE

## GOVERNMENT INTEREST

**[0001]** This invention was made with government support under  
5 CMMI1232883 awarded by the National Science Foundation. The Government  
has certain rights in the invention.

## CROSS-REFERENCE TO RELATED APPLICATIONS

**[0002]** This application claims the benefit of U.S. Provisional Application  
10 No. 61/948,633 filed on March 6, 2014. The entire disclosure of the above  
application is incorporated herein by reference.

## FIELD

**[0003]** The present disclosure relates to solid state drives based memory,  
15 and more particularly to memory devices formed by field effect transistors.

## BACKGROUND

**[0004]** Solid state drives (SSDs) based on flash memory technology can  
be more expensive than hard disk drives (HDDs) in terms of cost per unit bit  
20 storage. To reduce the cost of SSDs, it is desirable to develop low-cost memory  
fabrication processes as well as new memory architectures for improving the  
storage density.

**[0005]** One such effort is to create multi-bit data storage memory devices  
to achieve a higher storage density. The fabrication of multi-bit (or multi-level cell  
25 (MLC)) flash memories can require precise deposition of multiple semiconductor  
layers and multiple overlay lithography processes to create complicated memory  
transistors consisting of multiple floating gates and blocking and tunneling layers.  
This significantly increases the complexity of the memory cells. While MLC flash  
memories are developed to enable low-cost manufacturing of such complicated  
30 cells, the future scale-down of MLC circuits may require new MLC with simpler  
architectures as well as updated manufacturing systems with lower processing  
cost and higher throughput.

**[0006]** Recent efforts have demonstrated other multi-bit memories based on different materials and device structures, including memories based on organic semiconductors with ambipolar transport properties, memory transistors based on nanostructured materials, flash memory-like transistors with capacitively coupled nanoparticle(NP)-based floating gates, and multi-level resistive memories based on phase-change materials. However, relatively complicated and expensive processes are still required to make these devices.

**[0007]** This section provides background information related to the present disclosure which is not necessarily prior art.

## SUMMARY

**[0008]** This section provides a general summary of the disclosure, and is not a comprehensive disclosure of its full scope or all of its features.

**[0009]** In one aspect of the disclosure, a method for generating a non-volatile memory device is provided. The method includes: applying a plasma for a preset time period to an exposed surface of a channel of a field effect transistor such that a plurality of charge-trapping sites are formed at the channel. The channel may be comprised of a multi-layer structure of atomically thin two-dimensional sheets.

**[0010]** The preset time period for applying the plasma may be set between 5-20 seconds. Alternatively, the preset time period may be equal to or greater than one minute.

**[0011]** In another aspect of the disclosure, the channel may be made of a transition metal.

**[0012]** In yet another aspect of the disclosure, the plasma may be made of oxygen.

**[0013]** In another aspect of the disclosure, the method may further include: applying a polymer layer to a first area of the channel prior to applying the plasma, where the channel has the first area and a second area not having the polymer layer, and the first area is smaller than the second area; and removing the polymer layer from the first area after applying the plasma to the channel.

**[0014]** In yet another aspect of the disclosure, the charge-trapping sites may be formed between a first layer and a second layer of the channel, where the first layer is treated with the plasma and is above the second layer of the channel, which is not treated by the plasma. The first layer may include one or more sheets and the second layer may include one or more sheets different from the first layer.

**[0015]** In another aspect of the disclosure, the plasma may have at least one of a radio frequency power of approximately 200 W, a pressure of approximately 10 mTorr, and a precursor gas flow rate of approximately 10 sccm.

**[0016]** In an aspect of the disclosure, a memory device is provided. The memory device includes a field effect transistor that includes a source, a drain, a gate, and a channel portion located between the source and the drain. The channel portion may be comprised of a multi-layer structure of atomically thin two-dimensional sheets. The channel portion may include a first layer and a second layer and define multiple charge gaps between the first layer and the second layer. The first layer may include multiple ripples, and the multiple charge gaps may be defined by the multiple ripples and the second layer.

**[0017]** In an aspect of the disclosure, the first layer of the channel may be a plasma-doped layer and the second layer of the channel may be an un-doped layer.

**[0018]** In yet another aspect of the disclosure, the second layer of the channel may be substantially flat and under the first layer of the channel.

**[0019]** In an aspect of the disclosure, the field effect transistor may be made of molybdenum disulfide.

**[0020]** In yet another aspect of the disclosure, the field effect transistor may be a back gated transistor.

**[0021]** In an aspect of the disclosure a memory setting speed of the field effect transistor may be proportional to an area of the channel that includes the charge gaps.

**[0022]** In yet another aspect of the disclosure, the field effect transistor may store n-bits and includes  $2^n$  distinguishable data levels, where n is an integer.

[0023] In an aspect of the disclosure, the first layer may include one or more sheets and the second layer may include one or more sheets different from the first layer. The one or more sheets of the first layer may be doped with plasma, and the one or more sheets of the second layer may be un-doped.

5 [0024] Further areas of applicability will become apparent from the description provided herein. The description and specific examples in this summary are intended for purposes of illustration only and are not intended to limit the scope of the present disclosure.

## 10 DRAWINGS

[0025] The drawings described herein are for illustrative purposes only of selected embodiments and not all possible implementations, and are not intended to limit the scope of the present disclosure.

15 [0026] Figure 1A illustrates a back-gated MoS<sub>2</sub> field effect transistor (FET) receiving plasma treatment;

[0027] Figure 1B is an optical micrograph image of a memory FET;

[0028] Figure 1C is a graph of transfer curves of the memory FET of Figure 1B;

20 [0029] Figure 1D is a graph of retention characteristics of the memory FET of Figure 1B;

[0030] Figures 2A-1, 2A-2, 2A-3, and 2A-4 illustrate V<sub>G</sub> signals used for programming the memory FET into four data states;

[0031] Figure 2B is a graph of retention characteristics of the four data states recorded for 3 days;

25 [0032] Figure 2C illustrates the V<sub>G</sub> signals for programming the memory FET into ten data states;

[0033] Figure 2D is a graph of retention characteristics of the ten data states for 2000s.

30 [0034] Figure 3A is a graph of transfer curves corresponding to eight data states measured for 10 sequential cycles;

[0035] Figure 3B is a graph of data levels recorded for 100 sequential cycles;

[0036] Figure 4A is a graph of retention characteristics of binary data states in a microscale size memory FET;

[0037] Figure 4B illustrates a memory FET fabricated by using selected-area plasma treatment;

5 [0038] Figure 4C is a scanning electron microscope (SEM) image of a memory FET having an nanoscale plasma treated area;

[0039] Figure 4D is a graph of retention characteristics of the binary data states of the memory FET of Figure 4C;

10 [0040] Figure 5A is an SEM image of an O<sub>2</sub> plasma-treated MoS<sub>2</sub> surface that features nanoscale roughness features;

[0041] Figure 5B is a cross-sectional illustration of a memory FET treated with plasma;

[0042] Figures 5C-1, 5C-2, 5C-3, 5C-4, and 5C-5 illustrate a write and an erase scheme for memory FET;

15 [0043] Figure 6A is an optical image of a plasma-treated MoS<sub>2</sub> memory FET used for Kelvin probe force microscope (KFM) imaging;

[0044] Figure 6B are KFM images of the MoS<sub>2</sub> channel of Figure 6A after the FET was programmed by V<sub>G</sub> pulses;

20 [0045] Figure 6C is a graph of KFM scanlines showing the V<sub>CPD</sub> values of the MoS<sub>2</sub> channel after the FET was programmed;

[0046] Figure 7 illustrates 2-bit data levels (i.e., "00", "01", "10", "11" states) of five O<sub>2</sub> plasma-treated memory FET that were fabricated in the same batch; and

[0047] Figure 8 is an example method for generating memory FET.

25 [0048] Corresponding reference numerals indicate corresponding parts throughout the several views of the drawings.

#### DETAILED DESCRIPTION

30 [0049] The present disclosure will now be described more fully with reference to the accompanying drawings. Field-effect transistors (FET) made of multi-layer structure of atomically thin two-dimensional (2D) sheets present excellent electronic and mechanical properties, low manufacturing cost, and

potential large-area integration capability. The FET may be made of semiconducting layered transition metal dichalcogenides (LTMDs), such as MoS<sub>2</sub>, WSe<sub>2</sub>, and WS<sub>2</sub>. The stacking of MoS<sub>2</sub> layers and/or other 2D layers is used for making high-performance non-volatile memory transistors. In particular, the present disclosure describes the fabrication and characterization of a non-volatile memory device formed from a FET made of the multi-layer structure of atomically thin 2D sheets.

**[0050]** The memory device may be a MoS<sub>2</sub>-based floating-gate-free, non-volatile, multi-bit memory FET. The multi-bit memory FET is formed by treating the channel of the MoS<sub>2</sub> FET with highly energetic plasmas. The plasma-treated MoS<sub>2</sub> FET, provide reliable binary and 2-bit (i.e., 4-level) data states with potential for year-scale data retention, as well as 3-bit (i.e., 8-level) data states suitable for at least day-scale storage. The non-volatile memory device of the present disclosure may also be referred to as a memory FET.

**[0051]** The initial MoS<sub>2</sub> FET are fabricated by using a printing-based approach, which is described in *MoS<sub>2</sub> Transistors Fabricated via Plasma-Assisted Nanoprinting of Few-Layer-MoS<sub>2</sub> Flakes into Large-Area Arrays*. Nam, H.; Wi, S.; Rokni, H.; Chen, M.; Priessnitz, G.; Lu, W.; Liang, X. *ACS Nano* 2013, 7, 5870-5881, the entire disclosure of which is incorporated herein by reference. Generally, to fabricate back-gated MoS<sub>2</sub> FET, the metallic drain/source contacts (5 nm Ti/55 nm Au) are fabricated by photolithography or electron-beam lithography followed by metal deposition and lift-off. In particular, photolithography is used for fabricating FET based on the inner flakes of MoS<sub>2</sub> pixels. Electron beam lithography (EBL) may be used for fabricating FET based on the outer edge ribbons of MoS<sub>2</sub> pixels. Subsequently, another metallic contact is made onto the p<sup>+</sup>-Si substrate, which serves as a back gate contact.

**[0052]** Large-area arrays of pre-patterned multilayer MoS<sub>2</sub> features are created using bulk MoS<sub>2</sub> films that are pre-structured with relief patterns by lithographic techniques and subsequently serve as stamps for print out MoS<sub>2</sub> flakes on pristine and plasma charged SiO<sub>2</sub> substrates. While SiO<sub>2</sub> is chosen as the substrate material because SiOx-based substrates are widely used for electronic applications, the substrate may be made of other suitable material. The

few-layer MoS<sub>2</sub> flake pixels printed on such SiO<sub>x</sub> substrates can be used to create the MoS<sub>2</sub> FET.

[0053] In the example embodiment, the channel thickness ( $t_{\text{MoS}_2}$ ) of the MoS<sub>2</sub> is controlled to be approximately 15-30 nm in order to achieve relatively high field-effect mobility values (e.g.,  $\mu = 20$  to  $30 \text{ cm}^2/\text{Vs}$ ). The channel length (L) is approximately 2 to 10  $\mu\text{m}$ , and the average channel width (W) is approximately 5 to 15  $\mu\text{m}$ . Ti (5 nm)/Au (50 nm) electrode pairs serve as drain (D) and source (S) contacts, which are fabricated by using photolithography followed with metal deposition and lift-off in a solvent. The p<sup>+</sup>-Si substrates are used as back gates (G). Thermally grown SiO<sub>2</sub> layers (300 nm thick) are used as the gate dielectrics.

[0054] A relatively thick SiO<sub>2</sub> layers are used as gate dielectrics so that a simple color coding method for quickly locating MoS<sub>2</sub> flakes with suitable thicknesses (e.g., flakes thickness between 15-30 nm) may be employed. In this method, MoS<sub>2</sub> flakes are usually deposited on Si substrates coated with 300 nm thick SiO<sub>2</sub> layers, which results in an optimal color contrast of few-layer MoS<sub>2</sub> device features against the substrate background under the illumination of a regular photo-aligner, and may therefore make it convenient to perform overlay alignment. However, by using other advanced tools for imaging MoS<sub>2</sub> features (e.g., a Micro-Raman tool), a 300 nm thick gate dielectrics is not required and the FET may be made on thinner gate dielectrics to scale down the required programming voltages.

[0055] As described further below, the top surface layers of a MoS<sub>2</sub> FET channel is treated (or doped) with plasma in an inductively coupled plasma-based reactive ion etching (RIE) tool. As an example, for a given plasma recipe, the RF power is fixed to approximately 200 W; the pressure is approximately 10 mTorr; the precursor gas flow rate is approximately 10 sccm; and the treatment time for each FET is fixed to a preset time period (e.g., 5 seconds, 20 seconds, 1 minute, 2 minutes). The surface morphology of plasma-treated MoS<sub>2</sub> FET may be characterized by using a scanning electron microscope (SEM).

[0056] The electronic characterization of the memory FET may be performed by using a HP4145 semiconductor parameter analyzer that generates gate voltage ( $V_G$ ) pulses with duration widths ranging from 10 ms to 1 s. To

characterize the hysteretic behaviors of the transfer curves of the memory FET, a graph of the drain-source current ( $I_{DS}$ ) versus the gate voltage ( $V_G$ ) is acquired along two different  $V_G$  sweep directions with a constant sweep rate of 10 V/s. To configure a memory FET into binary data states, a +100V  $V_G$  pulse (duration  $\Delta t$ : 10 ms -1 s) is applied to induce a low conductance erase (ER) state and a -100V  $V_G$  pulse (duration  $\Delta t$ : 10 ms -1 s) is applied to induce a high-conductance write (WR) state in the FET. To evaluate the retention properties of data states, time-dependent  $I_{DS}$  values (i.e.,  $I_{DS}$ -t curves) are measured under fixed  $V_{DS}$  and  $V_G$  (typically  $V_G = 0$  and  $V_{DS} = 0.01$  to  $0.1$  V) after the initial settings of the memory FET with specific  $V_G$  pulses. A Kelvin force microscope (KFM) may be employed to probe the polarity and amount of the trapped charge in plasma-treated MoS<sub>2</sub> layers, which are modulated by the  $V_G$  pulse amplitude.

**[0057]** The memory capability of the memory FET is hypothesized to be caused by the spontaneous separation of plasma-doped MoS<sub>2</sub> layers from undoped layers, which forms an ambipolar charge-trapping layer interfacing the FET channel through a tunneling barrier. This structure enables the non-volatile retention of charged carriers as well as the reversible modulation of polarity and amount of the trapped charge, therefore resulting in multi-level data states in FET.

**[0058]** Figure 1A illustrates a MoS<sub>2</sub> FET 10 that includes a drain (D) 12, a source (S) 14, and a channel 16 disposed between the drain 12 and the source 14. The MoS<sub>2</sub> FET 10 is a MoS<sub>2</sub>-based back-gated FET having a gate 18 on an opposite side of the drain 12 and source 14. The MoS<sub>2</sub> FET 10 is formed into a memory FET by treating a top surface 20 (i.e., an exposed surface) of the MoS<sub>2</sub> channel 16 with energetic plasmas (e.g., CHF<sub>3</sub>, CF<sub>4</sub>, and O<sub>2</sub>-based plasmas) that may be generated in the RIE. An example pulse train 22 illustrates an erase pulse 22A for setting the memory FET into the "Erase" state (or "0" state) and a write pulse 22B for setting the memory FET into the "Write" state (or "1" state). Pulses 22A and 22B can realize the binary data storage in the memory FET. Figure 1B is an optical micrograph (OM) image 24 of a MoS<sub>2</sub> memory FET treated with O<sub>2</sub> plasma. In the example of Figure 1B, the MoS<sub>2</sub> memory FET has

the following parameters: channel length:  $L \approx 2 \mu\text{m}$ ; channel width:  $W \approx 5 \mu\text{m}$ ;  $\text{MoS}_2$  thickness:  $t_{\text{MoS}_2} \approx 20 \text{ nm}$ .

**[0059]** Plasma-treated FET exhibit well-differentiated binary data states with excellent retention properties. For example, Figures 1C and 1D display transfer and retention characteristics of an  $\text{O}_2$  plasma-treated FET of Figure 1B. That is, Figure 1C illustrates transfer curves ( $I_{\text{DS}}-V_{\text{G}}$  curves) that are acquired along two different  $V_{\text{G}}$  sweep directions with a sweep rate of 10 V/s and Figure 1D illustrates retention characteristics ( $I_{\text{DS}}-t$  curves) under  $V_{\text{DS}} = 0.01 \text{ V}$  and  $V_{\text{G}} = 0 \text{ V}$  recorded for 3 days. The memory FET exhibits a high write/erase (WR/ER) ratio (i.e.,  $I_{\text{DS(WR)}}/I_{\text{DS(ER)}}$ ) that is approximately 103 after a 1-hour retention test and approximately 400 after a 3-day retention test. Based on the 3-day retention test data plotted in Figure 1D, the WR/ER ratio after 10 years is estimated to be approximately 64, which may still enable an unambiguous reading of distinguishable  $I_{\text{DS}}$  values for “write” and “erase” states.

**[0060]** Plasma-induced charge-trapping levels in  $\text{MoS}_2$ , in comparison with, for example, un-doped  $\text{MoS}_2/\text{SiO}_2$  interfaces, retain trapped charges for a longer period of time and are potentially suitable for long-term data storage applications. In addition, the areal density of such plasma-induced charge-trapping states may be estimated by using  $\sigma_{\text{N}} = C_{\text{ox}}\Delta V_{\text{G}}/2e$ , where  $\Delta V_{\text{G}}$  is the hysteresis window;  $C_{\text{ox}}$  is the gate dielectric capacitance; and  $e$  is the elementary charge. With  $\Delta V_{\text{G}}$  being about 50 V,  $\sigma_{\text{N}}$  is estimated to be  $10^{12} \text{ cm}^{-2}$ .

**[0061]** While the memory FET of Figure 1B receives an  $\text{O}_2$ -based plasma, other plasmas may be used to treat the channel of the  $\text{MoS}_2$  FET. As an example,  $\text{CF}_4$  and  $\text{CHF}_3$  based plasmas may also be used to treat the  $\text{MoS}_2$  FET.  $\text{CF}_4$  and  $\text{CHF}_3$  plasma-treated FET typically exhibit relatively lower WR/ER ratios (e.g., 10 to 100 after 2000s retention tests) in comparison with those of  $\text{O}_2$  plasma-treated ones (e.g., 100 to 1,500 after 2000s retention tests).

**[0062]**  $\text{O}_2$  plasma-treated FET were further used for demonstrating multi-bit storage capability of the memory FET. To obtain an  $n$ -bit/FET storage capability, a memory FET needs to have at least  $2^n$  distinguishable data levels. As an example, the memory FET shown in Figure 1B is used for realizing 2-bit storage that needs 4 data levels. Figures 2A-1 to 2A-4 illustrate four  $V_{\text{G}}$  signals

used for configuring the memory FET into 4 data states ("00", "01", "10", "11"). The signals labeled with "00" and "11", as shown in Figures 2A-1 and 2A-4, are the same  $\pm 100$  V, one second  $V_G$  pulse signals used for setting the memory FET into binary "erase" (now as "00") and "write" (now as "11") states, respectively.

5       **[0063]** In Figure 2A-2, the  $V_G$  signal for setting the "01" state is a dual-pulse signal that consists of one -100V, one second pulse (i.e.,  $V_{G1}$ ) immediately followed with another +75V, one second pulse (i.e.,  $V_{G2}$ ). In Figure 2A-3, the  $V_G$  signal for setting the "10" state is a dual-pulse signal that consists of one +100V, one second pulse ( $V_{G1}$ ) immediately followed with another -75V, one second pulse (i.e.,  $V_{G2}$ ). Here, the first pulse ( $V_{G1}$ ) is used to release any previously trapped charge that has the same polarity as that of the to-be-refreshed charge or reset the FET back to the initial neutral state. The second pulse ( $V_{G2}$ ) sets the FET with a new charging state.

10       **[0064]** Figure 2B illustrates a 3-day retention test data of the 4 data levels of Figures 2A-1 to 2A-4. For these retention measurements,  $V_{DS} = 0.01$  V and  $V_G = 0$  V. Based on the extrapolated  $I_{DS}$ -t curves (solid lines in log scales) shown in Figure 2B, these 4 data states are anticipated to be distinguishable after 10 years. Therefore,  $O_2$  plasma-treated  $MoS_2$  FET (i.e., memory FET) may serve as a 2-bit memory with a year-scale data storage capability.

20       **[0065]** In another example, a  $O_2$  plasma-treated FET was set into ten distinguishable data states (i.e., "0" to "9") by using the dual-pulse  $V_G$  signals illustrated in Figure 2C. The second pulses ( $V_{G2}$ ) of these signals have different polarities and amplitudes, which may result in different amounts and polarities of the trapped charge in the FET and therefore generate multiple data levels. Figure 2D illustrates the retention behaviors of the ten data levels set by the signals of Figures 2C. Based on the retention test data, it is estimated that these ten data levels are distinguishable within day-scale time durations after the initial setting. Therefore, the memory FET may enable a 3-bit (at least 8 data levels) storage capability and may be used for electronic applications requiring hour- or day-scale data storage functionalities, such as central processing unit (CPU) cache memories, disposable electronic tags, and buffer memories for displays.

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**[0066]** To evaluate the endurance property of multi-bit memory states, an  $O_2$  plasma-treated FET, such as the one illustrated in Figure 1B, was periodically programmed into eight data states (i.e., “0” to “1” to “2” ... to “7” then repeat) by repeatedly applying eight dual-pulse  $V_G$  signals. Figure 3A illustrates the transfer curves corresponding to eight data states measured for ten sequential cycles. In Figure 3A, lines 30 represents  $V_G$  signal for zero data state (“0” or “000”), lines 32 represents  $V_G$  signal for first data state (“1” or “001”), lines 34 represents  $V_G$  signal for second data state (“2” or “010”), lines 36 represents  $V_G$  signal for third data state (“3” or “011”), lines 38 represents  $V_G$  signal for fourth data state (“4” or “100”), lines 40 represents  $V_G$  signal for fifth data state (“5” or “101”), lines 42 represents  $V_G$  signal for sixth data state (“6” or “110”), and lines 44 represents  $V_G$  signal for seventh data state (“7” or “111”). When the memory FET was switched into a data state, its current transfer characteristic curve (i.e.,  $I_{DS}$ - $V_G$  curve for  $V_G = -10$  to  $10$  V;  $V_{DS} = 50$  mV) was recorded. Figure 3B plots  $I_{DS}$  values (measured under  $V_G = 0$  V,  $V_{DS} = 50$  mV) of 8 data states recorded for 100 cycles. The results shown in Figure 3B indicate that plasma-induced multi-bit memory states exhibit a good endurance property.

**[0067]** To evaluate the effect of the  $V_G$  pulse duration ( $\Delta t$ ) on the resulted data levels, the retention curves of the binary data levels of the memory FET was measured after applying  $\pm 100$  V  $V_G$  pulses with different time durations ranging from 10 ms to 1 s. For the test, an  $O_2$  plasma-treated FET was used, where the FET had a channel length of approximately 2  $\mu m$  and width of approximately 5  $\mu m$ . Figure 4A illustrates that the  $I_{DS}$  value of the write state exhibits a weak dependence on  $\Delta t$ , whereas the  $I_{DS}$  value of the erase state highly depends on  $\Delta t$ , therefore resulting in a strong dependence of the WR/ER ratio on  $\Delta t$ . When  $\Delta t$  is reduced from 1 s to 10 ms, the WR/ER ratio drops from approximately 100 to 15. This suggests that a long pulse duration ( $\Delta t > 1$  s) may be needed to fully charge (or discharge) all plasma-induced charge-trapping states in a microscale size FET.

**[0068]** Assuming that the capacitance associated with plasma-induced charge-trapping states is proportional to the total  $MoS_2$  surface area treated with plasma, the required memory setting time may be reduced by reducing the total

plasma-treated area. Figure 4B illustrates a MoS<sub>2</sub> memory FET 50 having a drain 52, a source 54, and a channel 56 disposed between the drain 52 and the source 54. The channel 56 includes a selected area 58 and an unselected area 60. The selected area 58 is treated with plasma, whereas the unselected area 60 is not treated with plasma. Here, the selected area 58 is a line with a nanoscale width across the whole FET channel 56. To create the selected area 58, a polymer layer may be disposed onto the area of the channel that is not to receive the plasma (e.g., area 60). Plasma is then applied to the channel such that the area without the polymer layer is treated or doped with the plasma (e.g., area 58). The polymer layer is then removed from the channel of the MoS<sub>2</sub> FET leaving a pristine untreated area and a treated (doped) area of the channel.

**[0069]** As an example, Figure 4C is a scanning electron microscope (SEM) image 64 of a MoS<sub>2</sub> FET surface with a 46 nm wide plasma-treated line region 66 across the whole FET channel and untreated pristine region 68. The region 66 is formed by using O<sub>2</sub> plasma treatment through a PMMA resist layer patterned by electron-beam lithography (EBL). That is, prior to applying the plasma to the channel, the region 66 is isolated from the region 68, so that only the region 66 receives the plasma.

**[0070]** Figure 4D displays the retention curves of binary data levels of the memory FET illustrated in Figure 4C after it was set by applying  $\pm 100\text{V}$   $V_G$  pulses with different time durations ranging from 10 ms to 1 s. Although the memory FET has the same total channel area (i.e.,  $L \sim 2\text{ }\mu\text{m}$ ,  $W \sim 5\text{ }\mu\text{m}$ ) as that of the blank-treated FET shown in Figure 1B, both its “write” and “erase”  $I_{DS}$  values as well as WR/ER ratio exhibit a quite weak dependence on  $\Delta t$  values. This indicates that the selected-area plasma treatment, as compared to the blank treatment, may result in a much smaller capacitance of plasma-induced charge-trapping states and therefore a faster memory setting speed, but can still generate reasonably good WR/ER ratios (40 to 100) suitable for practical memory-related applications. The result of Figure 4D also indicates that the MoS<sub>2</sub> memory FET may be scaled down to the smaller devices with sub-50 nm scale channel lengths. Such sub-50 nm size memory FET are also anticipated to have the faster writing/erasing speeds as compared to the current microscale ones.

**[0071]** To explore the physical mechanism responsible for the memory capability of the memory FET of the present disclosure, Figure 5A illustrates a SEM image 80 of the MoS<sub>2</sub> FET surface treated with O<sub>2</sub> plasma, where a scale bar 82 is approximately 100nm. The SEM image 80 shows that the O<sub>2</sub> plasma-treated MoS<sub>2</sub> surface exhibits a nanoscale roughness with average period of approximately 10 nm. Such a roughness, in contrast with the flat surface of a pristine MoS<sub>2</sub> sample, is attributed to the plasma-induced doping of external atoms, which may induce an expansion of the MoS<sub>2</sub> layers and let these layers ripple up and down. This ripple effect could partially exfoliate the plasma-doped top layers from the un-doped pristine MoS<sub>2</sub> layers, where the un-doped pristine MoS<sub>2</sub> layers are under the dope layers and untreated by the plasma. The ripples of the plasma doped top layers and the un-doped pristine MoS<sub>2</sub> layers form charge-trapping sites slightly isolated from the FET channel.

**[0072]** By way of explanation, Figure 5B illustrates a cross-sectional illustration of a MoS<sub>2</sub> memory FET 90 that is treated with plasma. A top few MoS<sub>2</sub> layers (i.e., treated layers 92) become rough (ripples 93) because of the doping of plasma. The treated layers 92 may include one or more layers (e.g., 1-3). A part of the treated layers 92 may be mechanically separated and electrically insulated from intact underlying layers 94. The treated layers 92 serves as a non-volatile charge-trapping layer that defines charge trapping sites 95. Plasma-induced gaps 96 defined between the charge-trapping layer (i.e., treated layer 92) and the intact MoS<sub>2</sub> channel (i.e., intact layer 94) may serve as a tunneling barrier layer for retaining trapped charges and switching the memory states. The size of the gap 96, which is defined between the charge-trapping sites and the un-doped MoS<sub>2</sub> channel is estimated to be in the same order of the magnitude as the average period of the ripple features in the top layers (i.e., 5-10 nm).

**[0073]** Figures 5C-1 to 5C-5 illustrate a band structure (i.e., the density of states (DOS) function) of a plasma-treated MoS<sub>2</sub> FET. The untreated (or pristine) MoS<sub>2</sub> layers of the FET channel region are expected to have a typical band structure of lightly doped semiconductors with a relatively low density of impurity states in the bandgap, whereas the plasma-treated top layers are expected to exhibit a rich of plasma-induced localized trapping states in the bandgap. The

trapping states may be distributed over a broad energy range in the bandgap and they are likely to be a mixture of donor-type, acceptor-type, and isoelectronic deep-level traps. Such a large variety and broad energy distribution of plasma-induced traps are hypothesized based on the fact that energetic plasma species, similar to electron irradiation, may generate a broad variety of defect configurations in MoS<sub>2</sub> layers, including sulfur vacancies, substitutional donor/acceptor defects, adatoms with charge, and isoelectronic impurities. Therefore, the plasma-treated MoS<sub>2</sub> top layers may serve as an ambipolar charge-trapping layer.

**[0074]** Figure 5C-1 illustrates the initial neutral state, in which the net charge in the plasma-treated layers is assumed to be close to zero (i.e., all donor-type traps are occupied with electrons, and all acceptor-type traps are vacant). To obtain an “erase” state, a positive  $V_G$  pulse is applied (Figure 5C-2). In this case, the Fermi level is elevated and the conduction (C) band of untreated layers (i.e., the FET channel) is populated with electrons. These electrons have a high probability to tunnel through the barrier and are injected into the conduction band of the plasma-treated top layers. The injected electrons may quickly relax to the localized trapping states with the lower energies. When the  $V_G$  is set back to zero (Figure 5C-3), the trapped electrons may be retained in the top layers for a long storage time, because of the existence of a barrier layer between plasma-treated and untreated layers as well as the lack of target states in the bandgap of untreated layers that may effectively prevent electrons to tunnel back from the trapping states to the FET channel.

**[0075]** To obtain a “write” state, a negative  $V_G$  pulse is applied (Figure 5C-4). In this case, the Fermi level is lowered and the valence (V) band of untreated layers (i.e., the FET channel) is populated with holes. These holes have a high probability to tunnel through the barrier and are injected into the valence band of the plasma-treated top layers. The injected holes may quickly relax to the localized trapping states with the lower energies. When the  $V_G$  is set back to zero (Figure 5C-5), the trapped holes may be retained in the top layers for a long storage time, because of the existence of a barrier layer between plasma-treated and untreated layers as well as the lack of target states in the bandgap of

untreated layers that may effectively prevent holes to tunnel back from the trapping states to the FET channel.

**[0076]** The model of Figures 5C-1 to 5C-5 also implies that the  $V_G$  pulse amplitude may modulate the total amount of charged carriers injected into the charge-trapping states in plasma-treated  $\text{MoS}_2$  layers. Such trapping states, which are different from the discrete trap levels in conventional memory FET with floating gates, may be distributed over a broad energy range and may accommodate different amounts of injected carriers with different polarities, therefore resulting in multiple data levels (i.e., multiple  $I_{DS}$  values). Such a hypothesized model could preliminarily explain the observed multi-bit data storage capability.

**[0077]** In addition, as implied by this model, the electrons of erase state (or the holes for write) that are trapped at relatively high-energy states and are close to the conduction (or valence for write) band could easily tunnel back to the FET channel and result in a slow relaxation of  $I_{DS}$  values with time. During the initial memory setting, the higher  $V_G$  pulse could induce the trapping of more charged carriers in such high-energy states and therefore result in a more prominent relaxation of  $I_{DS}$  values with time. This implication from the model is consistent with the observation in the retention tests illustrated in Figures 2C and 2D that the data states with the highest or the lowest  $I_{DS}$  values, typically configured by  $\pm 100\text{V}$   $V_G$  pulses, exhibit more prominent relaxation behaviors than other intermediate data states between them.

**[0078]** To further support and verify that plasma-treated  $\text{MoS}_2$  layers indeed serve as charge-trapping layers, a Kelvin force microscope (KFM) is utilized to image and measure the contact potential (or work function) difference ( $V_{CPD}$ ) between  $V_G$ -modulated  $\text{MoS}_2$  FET surfaces and the KFM tip. Figure 6A illustrates an optical image (OM) 100 of an  $\text{O}_2$  plasma-treated  $\text{MoS}_2$  FET (i.e., memory FET) having plasma treated channel 102. In OM 100 a dashed box 104 denotes a KFM-imaged area.

**[0079]** Figure 6B shows a KFM image 110 that was captured after the FET was configured by applying a  $-100\text{V}$ ,  $1\text{s}$   $V_G$  pulse 112 and a KFM image 114 that was captured after the FET was configured by applying a  $+100\text{V}$ ,  $1\text{s}$   $V_G$  pulse

116. Scanlines denoted by the solid lines 118 and 120 are accordingly plotted in Figure 6C. Figures 6B and 6C show that the polarity switching of the applied  $V_G$  pulse may accordingly switch the  $V_{CPD}$  polarity on the  $MoS_2$  surface but does not noticeably change the  $V_{CPD}$  value on the  $SiO_2$  surface. Here, the  $V_{CPD}$  value on the  $MoS_2$  surface is directly associated with the electrostatic interaction between the trapped charge in the top  $MoS_2$  layers and the KFM tip. It should be noted that the charge trapped at other interfaces (e.g.,  $MoS_2/SiO_2$  and  $Si/SiO_2$  interfaces) may hardly affect the  $V_{CPD}$  value on the  $MoS_2$  surface because of the screening effect of multilayer  $MoS_2$  channels (the electric-field screening length in  $MoS_2$  is 3-5 nm; the thickness of our FET channels is 20-30 nm). Therefore, the  $V_G$ -modulated memory states observed in the  $MoS_2$  FET are attributed to the charge-trapping states in plasma-treated top  $MoS_2$  layers, which may enable the ambipolar charge retention and modulation.

**[0080]** Although the electric field generated by the back gate is expected not to directly affect the charge-trapping states in the plasma-treated top layers, this gating field may directly modulate the carrier (electron or hole) concentrations in the untreated layers, and these densely populated carriers could diffuse to the interface between untreated and treated layers and subsequently transport through the tunneling barrier formed at this interface, as illustrated in Figures 5C-1 to 5C-5). In this way, the back gate voltage could indirectly modulate the charge trapping and switching in the top  $MoS_2$  layers.

**[0081]** By unifying processing conditions and device geometries, it is possible to make large arrays of plasma-treated  $MoS_2$  memory FET with high uniformity in all registered data levels. As an example, five memory FET that were fabricated in the same batch and were expected to have very similar doping profiles in their  $MoS_2$  channels. All five devices have very close  $MoS_2$  channel thicknesses (20 to 25 nm) and lengths ( $\sim 5 \mu m$ ), but very different channel widths (2-10  $\mu m$ ). To eliminate the effect of lateral pattern shapes on the memory data levels, average conductivity ( $\sigma$ ) values, instead of  $I_{DS}$  values, of  $MoS_2$  channels were used to denote the memory states. Figure 7 plots the 2-bit data levels of the five memory FET (i.e., 1-5 along x-axis), which were measured after the FET were set by the  $V_G$  signals listed in Figure 2A. In Figure 7, data state "00" is

represented by bars 150, data state "01" is represented by bars 152, data state "10" is represented by bars 154, data state "11" is represented by bars 156. As shown, the FET exhibit a reasonably good uniformity and consistency in all plasma-induced data levels.

5       **[0082]**     The method for forming the memory FET of the present disclosure can be generalized with reference to Figure 8. Figure 8 is a flowchart of an example method 200 for making a memory FET of the present disclosure. At 202, a FET having multi-layer structure of atomically thin 2D sheets is acquired. The FET may be made of transition metals, such as MoS<sub>2</sub>, WSe<sub>2</sub>, and WS<sub>2</sub>.

10       **[0083]**     At 204 the FET is arranged such that a surface (i.e., top surface) of the channel receives plasma. At 206, plasma (e.g., CHF<sub>3</sub>, CF<sub>4</sub>, and O<sub>2</sub>-based plasmas) is applied to the channel of the FET for a preset time period, such as 5 seconds, 15 seconds, one minute, or other suitable time period for forming the charge trapping sites. The plasma causes one or more of the layers of the  
15     channel region to wrinkle or form ripples. That is, the plasma induces an expansion of the MoS<sub>2</sub> layers causing the one or more layers to ripple up and down to form a plasma-doped layer that slightly separates from an un-doped pristine MoS<sub>2</sub> layers. The un-doped pristine MoS<sub>2</sub> layers are under the doped layers and are untreated by the plasma. The ripples of the plasma doped layers  
20     and the un-doped pristine MoS<sub>2</sub> layers form charge-trapping sites.

**[0084]**     At 208, the method determines if the preset time period has elapsed. If the preset time period has not elapsed, plasma is still applied to the channel at 206. If the preset time period has elapsed, the plasma is turned off at 210, and at 212 the FET is inspected to determine if the FET operates as a  
25     memory. That is, the inspection may analyze the channel to determine if the channel includes un-doped plasma layers and plasma treated layers having ripples that form the charge-trapping sites. The inspection can be a series of test that analyzes the structure and/or performance of the FET. At 214, the method determines if the FET is operable as a memory based on the inspection at 212. If  
30     the FET is not operable as a memory, the FET is declared as abnormal at 216. If the FET is operable as a memory, the FET is declared as a memory device at 218.

**[0085]** If the memory FET is configured to have a nanoscale plasma treated area, as shown in Figures 4B and 4C, than a selected region of the channel that is to receive the plasma may be isolated from the other region of the channel that is not to receive the plasma. For example, at 202, a polymer layer  
5 may be disposed at the region of the channel that does not receive the plasma. After the plasma is applied at 210 the polymer layer is removed from the region. Thus, a selected region of the channel is doped with the plasma and the region that included the polymer layer is not doped.

**[0086]** Once formed, the memory FET may be used as a multi-bit memory  
10 device. For instance, a first pulse is applied for setting the memory FET into an erase state or "0" state and a second pulse is applied for setting the memory FET into the write state or "1" state). The first pulse and the second pulse may be of opposite polarity (e.g., erase +100V and write -100V) and are used to store binary data in the memory FET.

**[0087]** The memory devices of the present disclosure are plasma-treated  
15 MoS<sub>2</sub> FET and serve as multi-bit memory devices with a year-scale 2-bit/transistor (or day-scale 3-bit/transistor) storage capability. The data storage capability is attributed to the plasma-induced ripple and partial separation of the top MoS<sub>2</sub> layers from the underlying pristine layers, which form a memory FET  
20 structure bearing an ambipolar charge-trapping layer coupled with the FET channel through a tunneling barrier. Such multi-bit memories exhibit a unique combination of excellent retention and endurance characteristics, extremely simple structures, and low fabrication costs. The programming speed of such memories may be increased by using nanoscale-area plasma treatment  
25 processes.

**[0088]** The foregoing description of the embodiments has been provided  
for purposes of illustration and description. It is not intended to be exhaustive or to limit the disclosure. Individual elements or features of a particular embodiment are generally not limited to that particular embodiment, but, where applicable, are  
30 interchangeable and can be used in a selected embodiment, even if not specifically shown or described. The same may also be varied in many ways.

Such variations are not to be regarded as a departure from the disclosure, and all such modifications are intended to be included within the scope of the disclosure.

**[0089]** Example embodiments are provided so that this disclosure will be thorough, and will fully convey the scope to those who are skilled in the art.

5 Numerous specific details are set forth such as examples of specific components, devices, and methods, to provide a thorough understanding of embodiments of the present disclosure. It will be apparent to those skilled in the art that specific details need not be employed, that example embodiments may be embodied in many different forms and that neither should be construed to limit the scope of  
10 the disclosure. In some example embodiments, well-known processes, well-known device structures, and well-known technologies are not described in detail.

**[0090]** The terminology used herein is for the purpose of describing particular example embodiments only and is not intended to be limiting. As used herein, the singular forms "a," "an," and "the" may be intended to include the  
15 plural forms as well, unless the context clearly indicates otherwise. The terms "comprises," "comprising," "including," and "having," are inclusive and therefore specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups  
20 thereof. The method steps, processes, and operations described herein are not to be construed as necessarily requiring their performance in the particular order discussed or illustrated, unless specifically identified as an order of performance. It is also to be understood that additional or alternative steps may be employed.

**[0091]** When an element or layer is referred to as being "on," "engaged to,"  
25 "connected to," or "coupled to" another element or layer, it may be directly on, engaged, connected or coupled to the other element or layer, or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on," "directly engaged to," "directly connected to," or "directly coupled to" another element or layer, there may be no intervening elements or  
30 layers present. Other words used to describe the relationship between elements should be interpreted in a like fashion (e.g., "between" versus "directly between,"

"adjacent" versus "directly adjacent," etc.). As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

**[0092]** Although the terms first, second, third, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these  
5 elements, components, regions, layers and/or sections should not be limited by these terms. These terms may be only used to distinguish one element, component, region, layer or section from another region, layer or section. Terms such as "first," "second," and other numerical terms when used herein do not imply a sequence or order unless clearly indicated by the context. Thus, a first  
10 element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the example embodiments.

**[0093]** Spatially relative terms, such as "inner," "outer," "beneath," "below," "lower," "above," "upper," and the like, may be used herein for ease of description  
15 to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. Spatially relative terms may be intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below" or "beneath" other elements or  
20 features would then be oriented "above" the other elements or features. Thus, the example term "below" can encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

25

## CLAIMS

What is claimed is:

1. A method for generating a non-volatile memory device, the method comprising:
  - 5 applying a plasma for a preset time period to an exposed surface of a channel of a field effect transistor such that a plurality of charge-trapping sites are formed at the channel, wherein the channel is comprised of a multi-layer structure of atomically thin two-dimensional sheets.
- 10 2. The method of claim 1 wherein the preset time period is set between 5-20 seconds.
3. The method of claim 1 wherein the preset time period is equal to or greater than one minute.
- 15 4. The method of claim 1 wherein the channel is made of a transition metal.
5. The method of claim 1 wherein the plasma is made of oxygen.
- 20 6. The method of claim 1 further comprising:
  - applying a polymer layer to a first area of the channel prior to applying the plasma, wherein the channel has the first area and a second area not having the polymer layer, and the first area is smaller than the second area; and
  - 25 removing the polymer layer from the first area after applying the plasma to the channel.
7. The method of claim 1 wherein the charge-trapping sites are formed between a first layer and a second layer of the channel, the first layer is treated with the plasma and is above the second layer of the channel, the second layer of the channel is not treated by the plasma, the first layer includes one or more
- 30

sheets and the second layer includes one or more sheets different from the first layer.

8. The method of claim 1 wherein the plasma has at least one of a radio frequency power of approximately 200 W, a pressure of approximately 10  
5 mTorr, and a precursor gas flow rate of approximately 10 sccm.

9. A memory device comprising:

a field effect transistor including a source, a drain, a gate, and a channel portion located between the source and the drain, wherein:

10 the channel portion is comprised of a multi-layer structure of atomically thin two-dimensional sheets,

the channel portion includes a first layer and a second layer and defines multiple charge gaps between the first layer and the second layer,

the first layer includes multiple ripples, and the multiple charge gaps are  
15 defined by the multiple ripples and the second layer.

10. The memory device of claim 9 wherein the first layer is a plasma-doped layer and the second layer is an un-doped layer.

20 11. The memory device of claim 9 wherein the channel is made of a transition metal.

12. The memory device of claim 9 wherein the second layer is substantially flat and under the first layer.

25

13. The memory device of claim 9 wherein the field effect transistor is made of molybdenum disulfide.

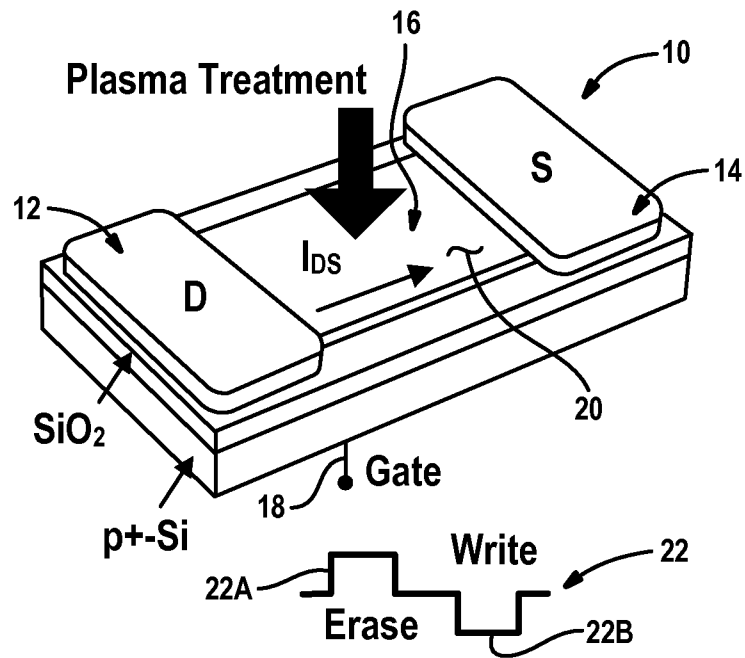
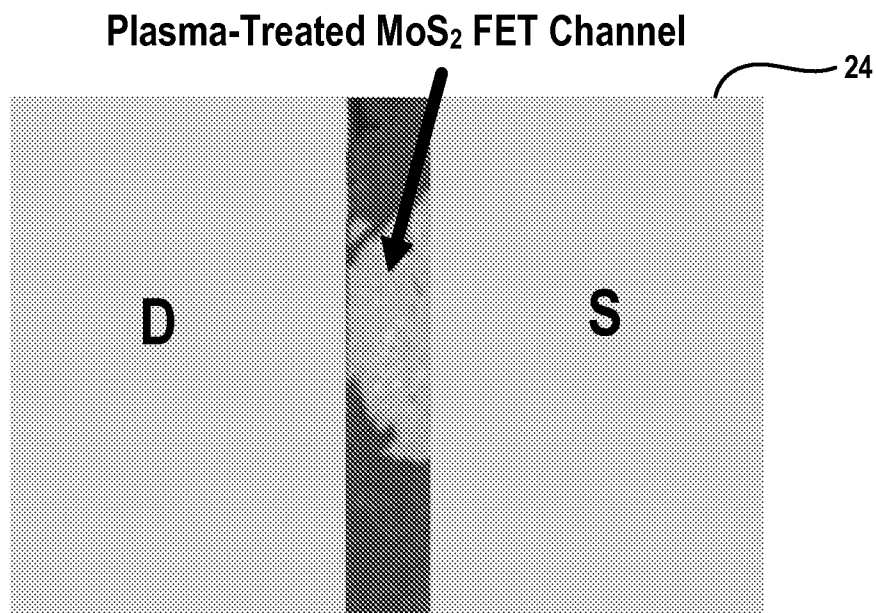
14. The memory device of claim 9 wherein a memory setting speed is  
30 proportional to an area of the channel that includes the charge gaps.

15. The memory device of claim 9 wherein the field effect transistor is a back gated transistor.

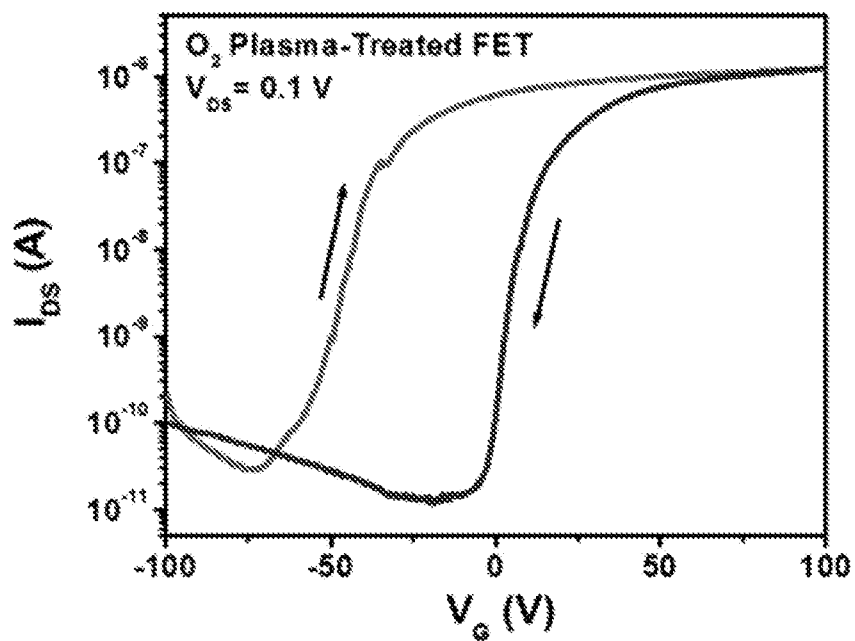
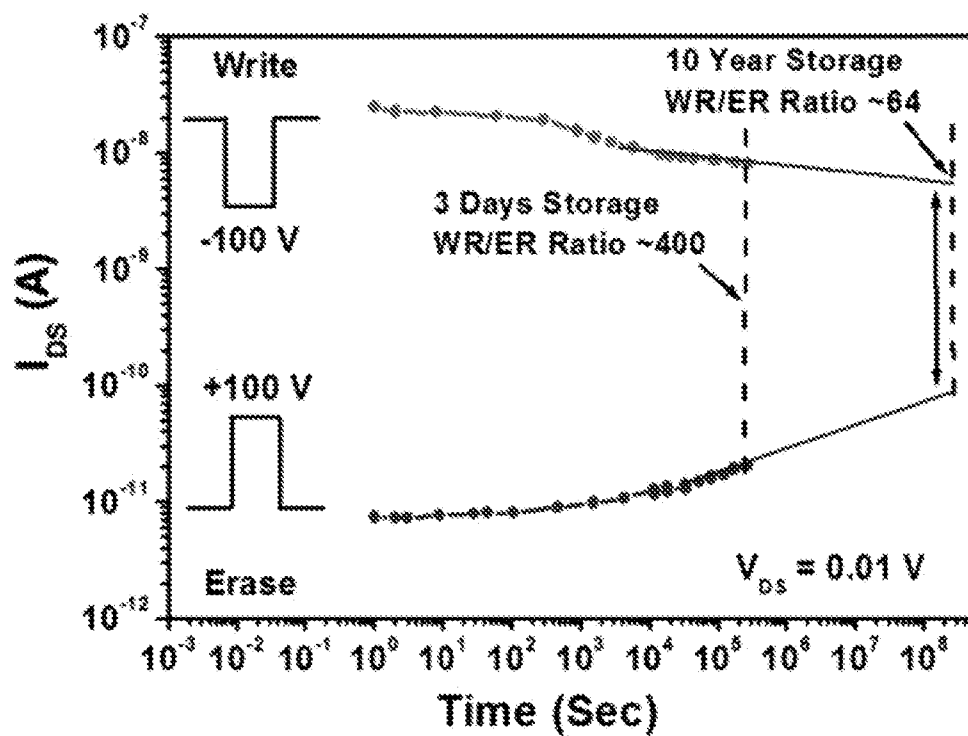
16. The memory device of claim 9 wherein the field effect transistor  
5 stores n-bits and includes  $2^n$  distinguishable data levels, and n is an integer.

17. The memory device of claim 9 wherein the first layer includes one  
or more sheets and the second layer includes one or more sheets different from  
the first layer, the one or more sheets of the first layer are doped with plasma,  
10 and the one or more sheets of the second layer are un-doped.

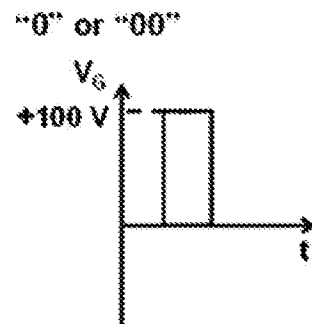
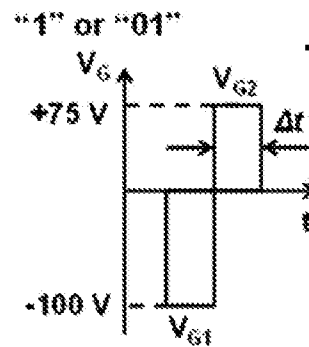
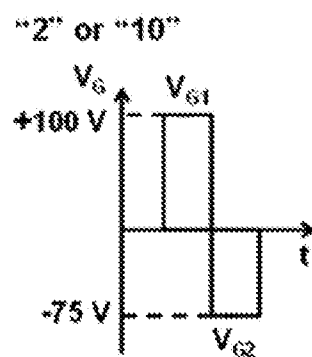
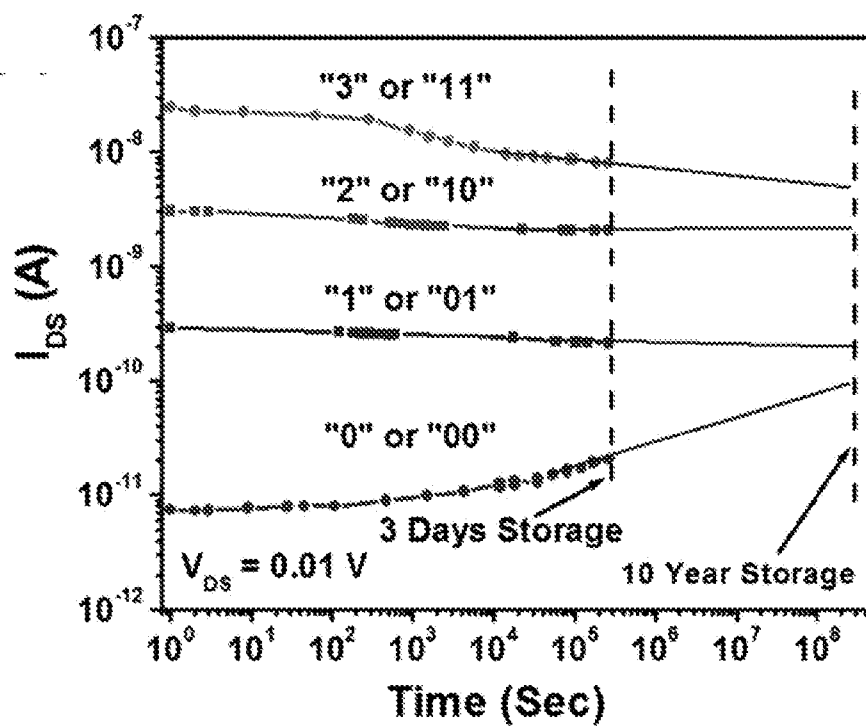
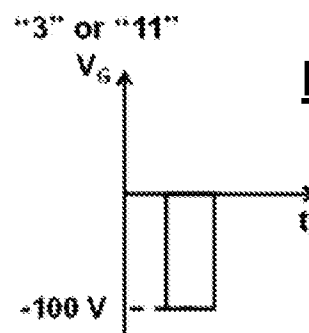
1/12

**FIG. 1A****FIG. 1B**

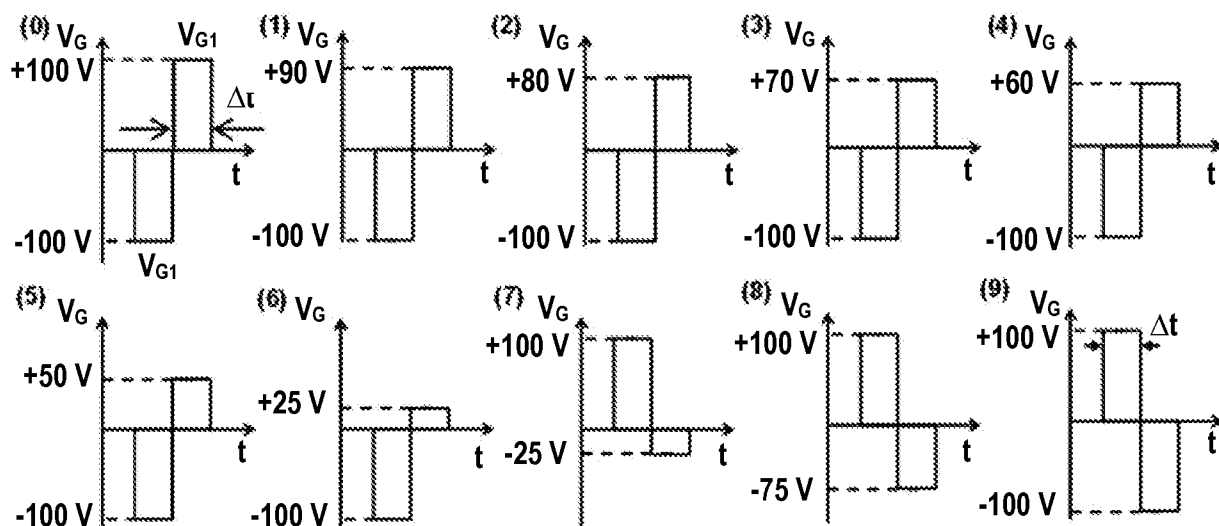
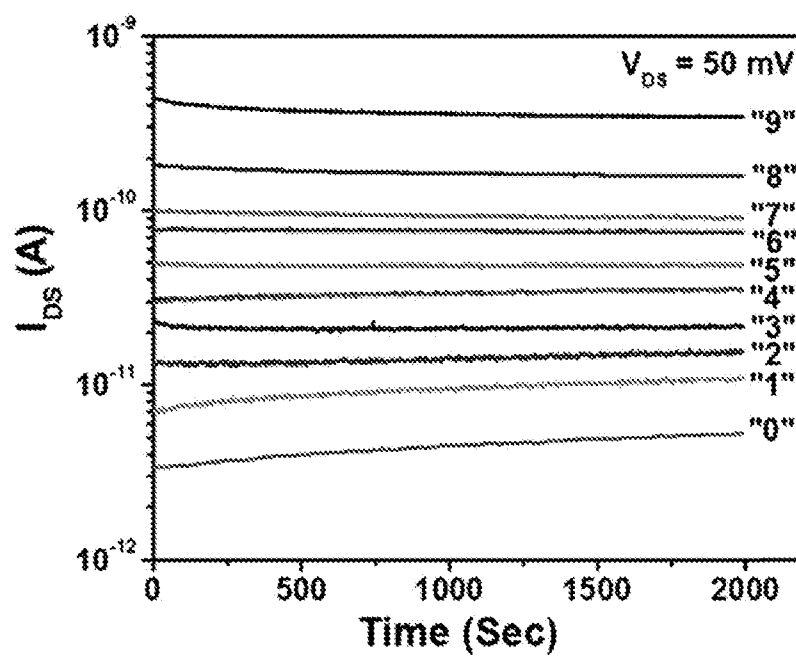
2/12

**FIG. 1C****FIG. 1D**

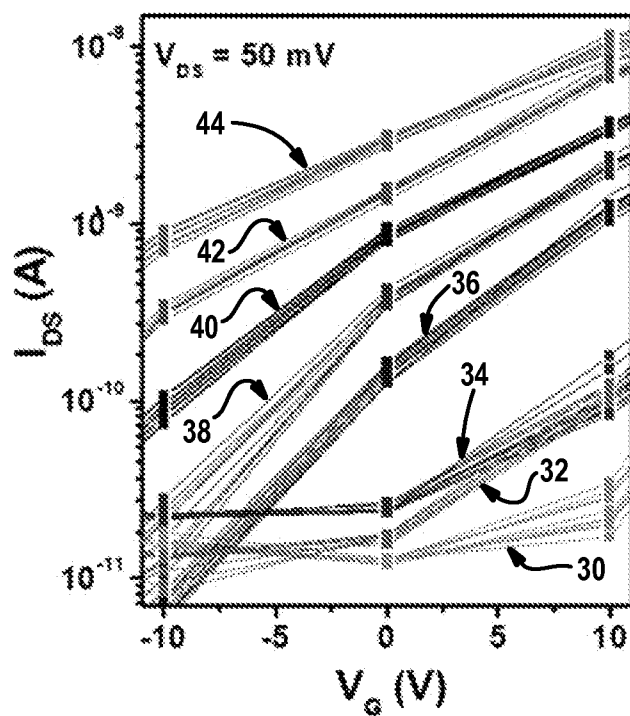
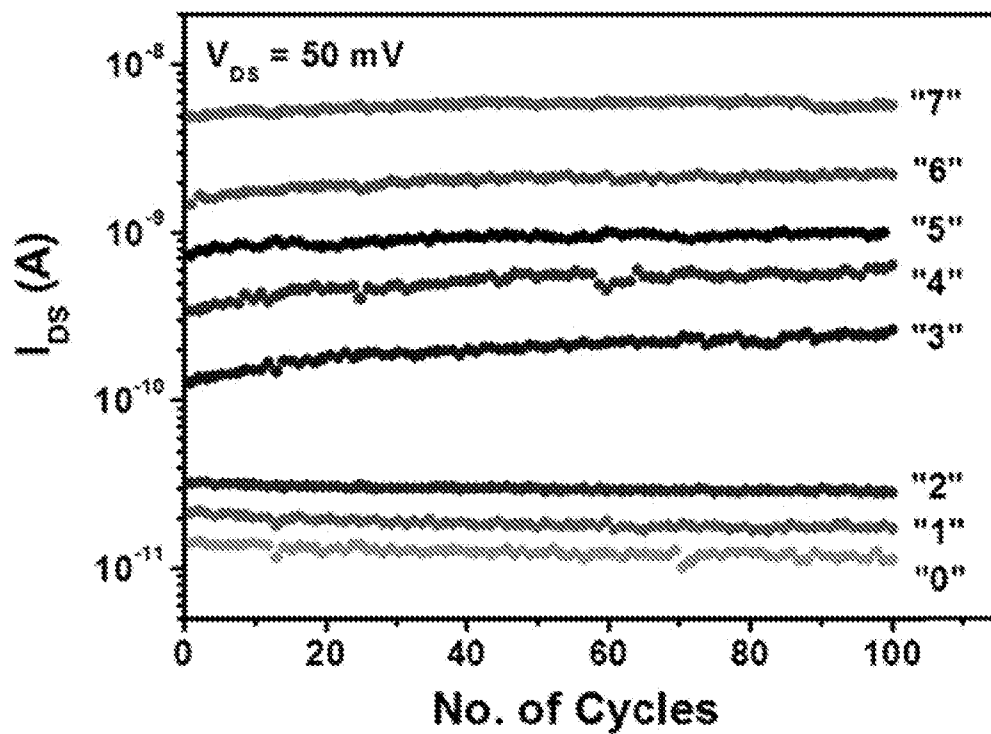
3/12

**FIG. 2A-1****FIG. 2A-2****FIG. 2A-3****FIG. 2A-4****FIG. 2B**

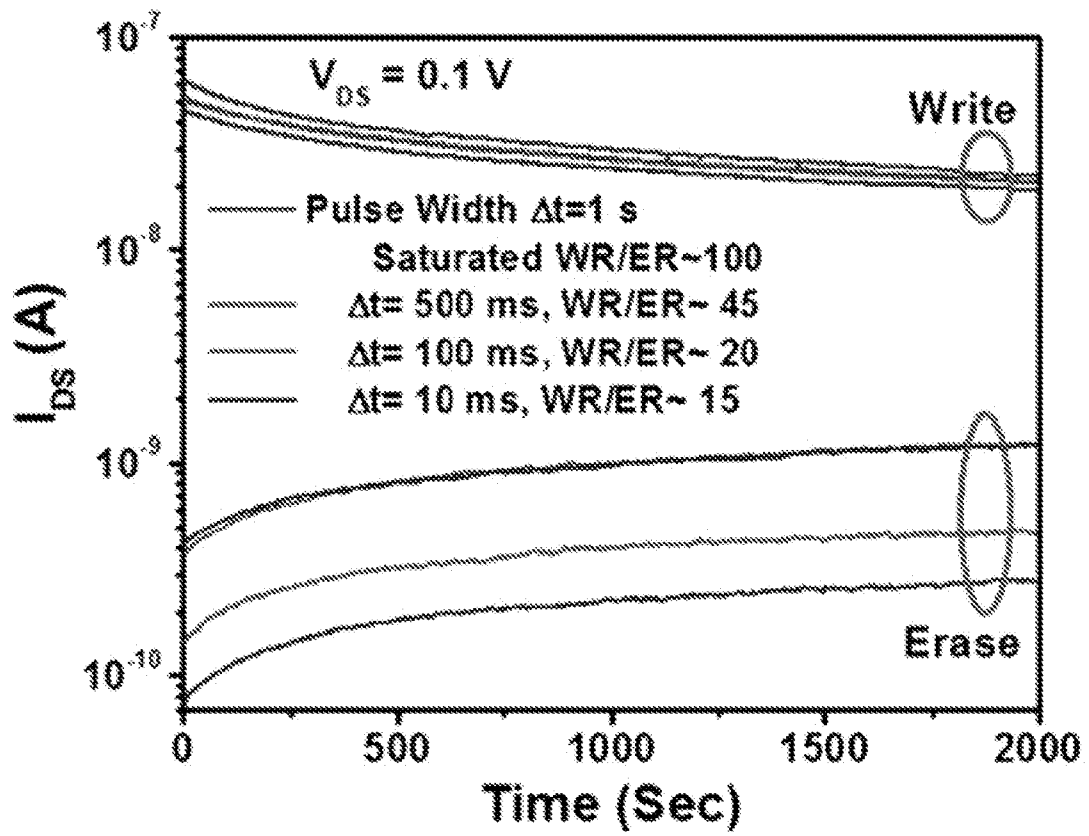
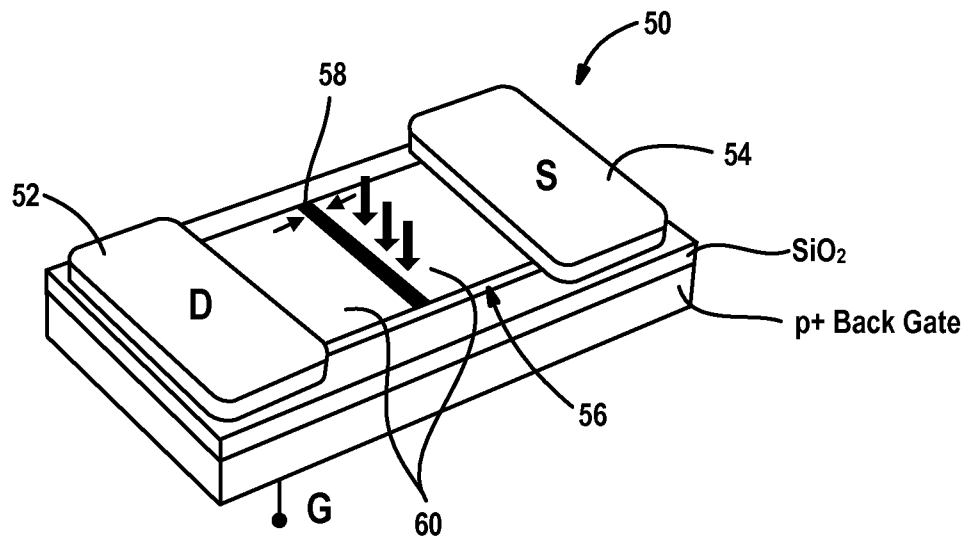
4/12

**FIG. 2C****FIG. 2D**

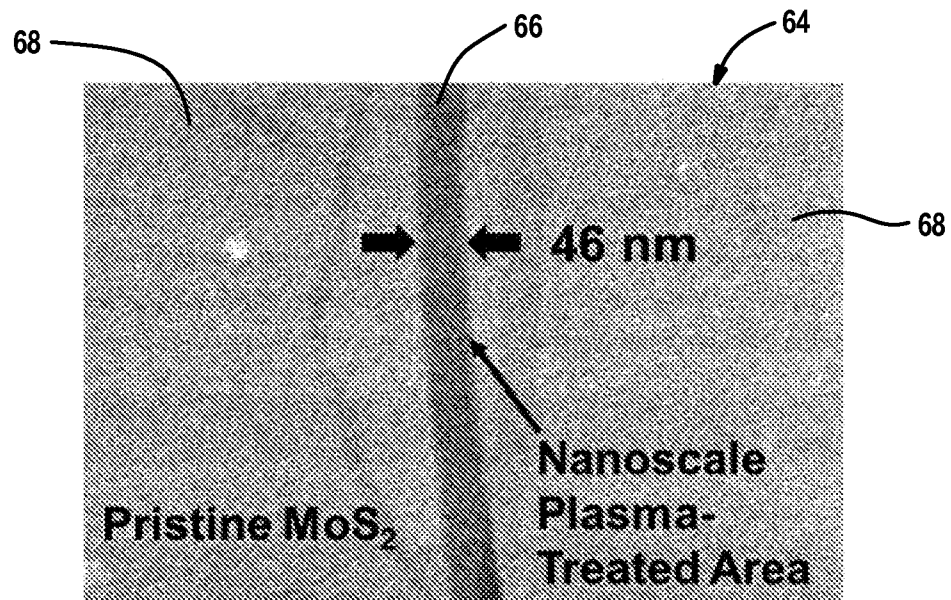
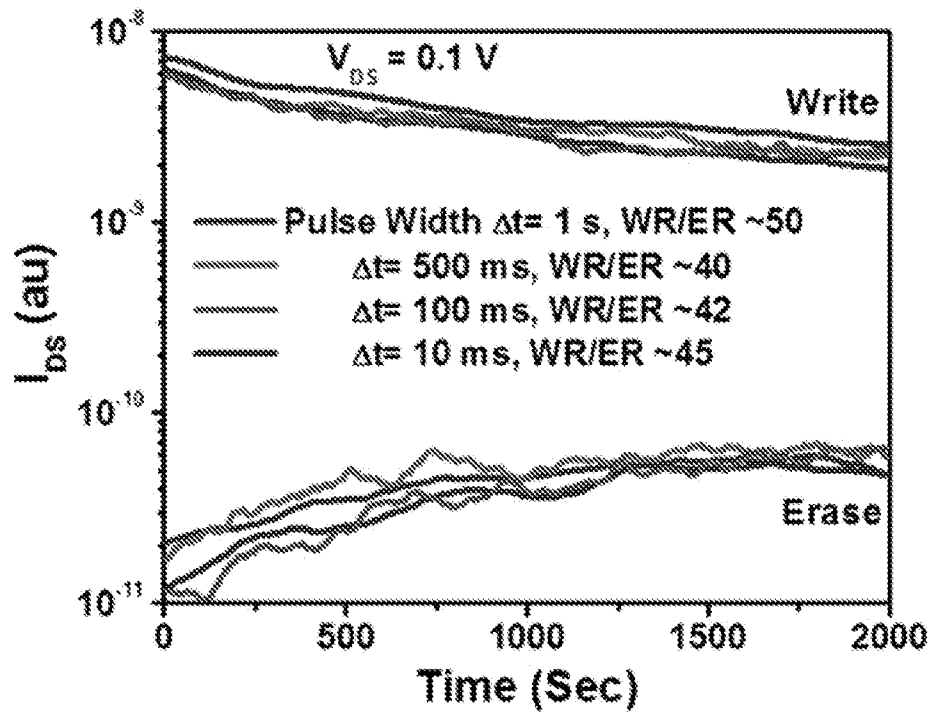
5/12

**FIG. 3A****FIG. 3B**

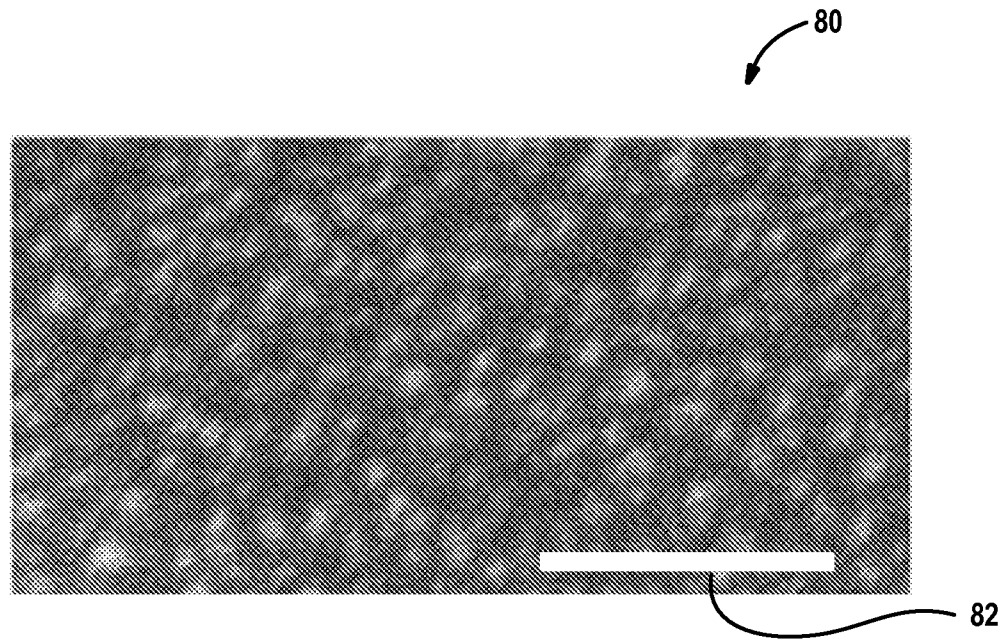
6/12

**FIG. 4A****FIG. 4B**

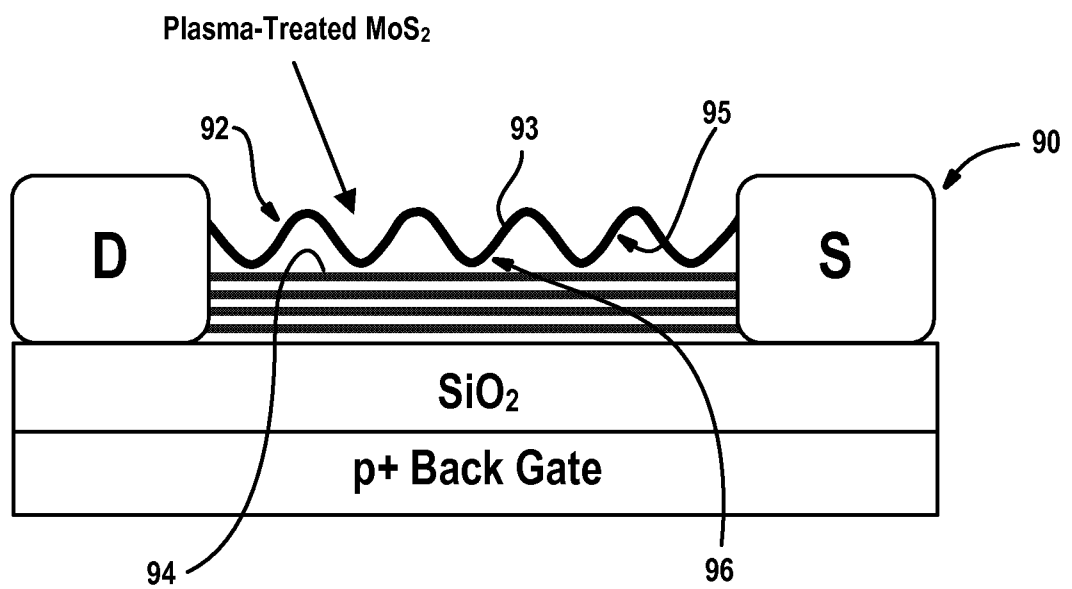
7/12

**FIG. 4C****FIG. 4D**

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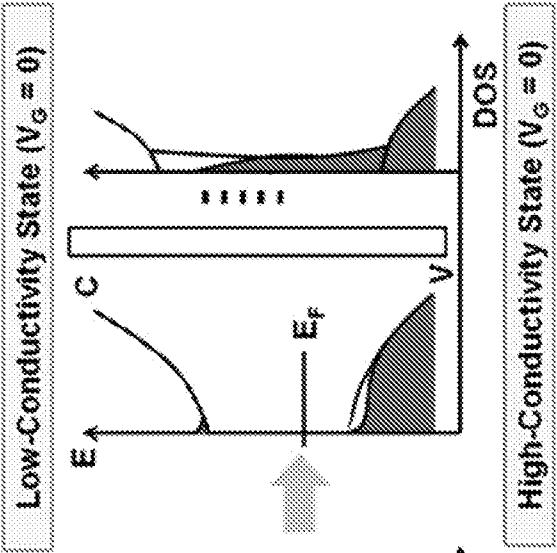


**FIG. 5A**

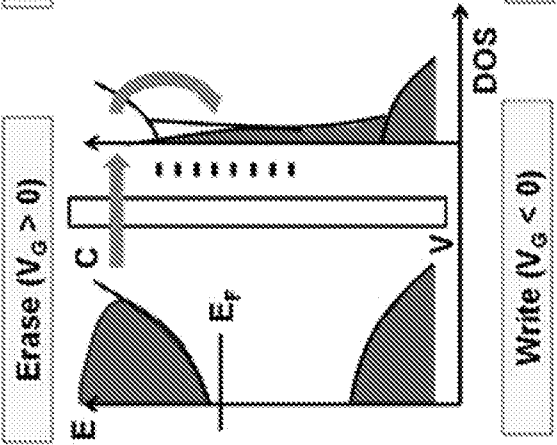


**FIG. 5B**

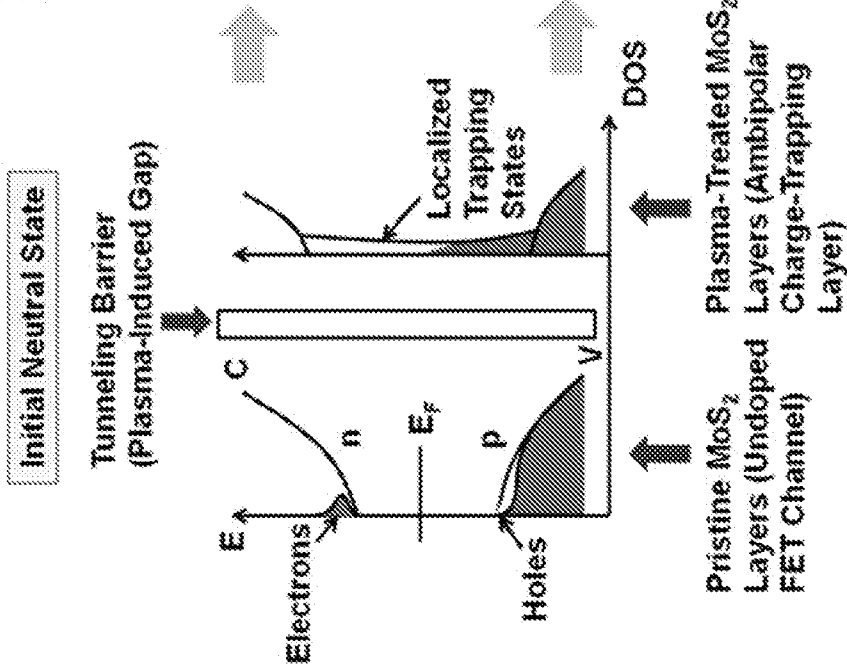
**FIG. 5C-3**



**FIG. 5C-2**



**FIG. 5C-1**



**FIG. 5C-5**

**FIG. 5C-4**

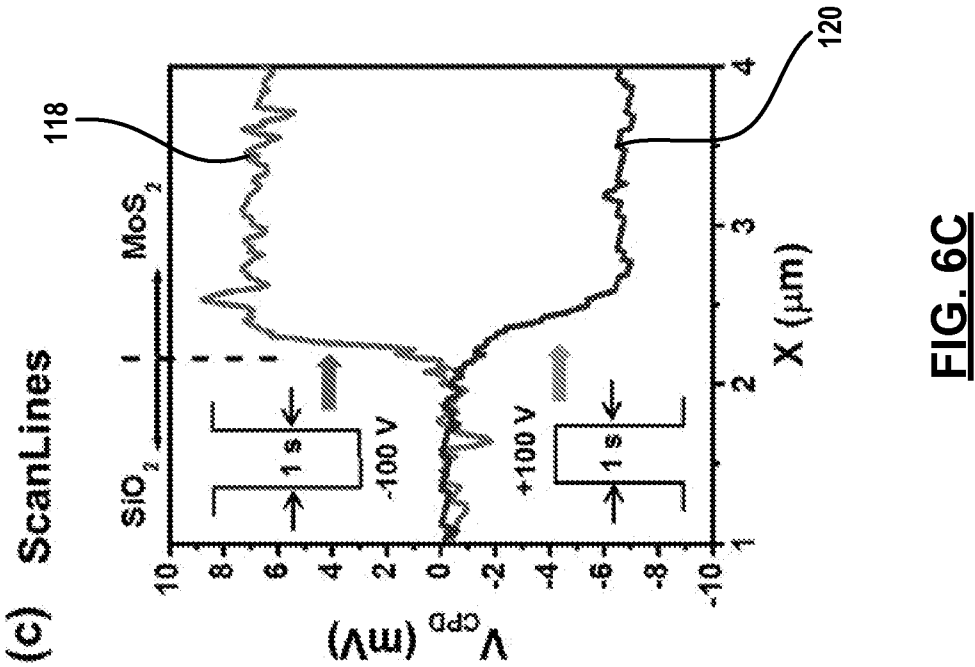


FIG. 6C

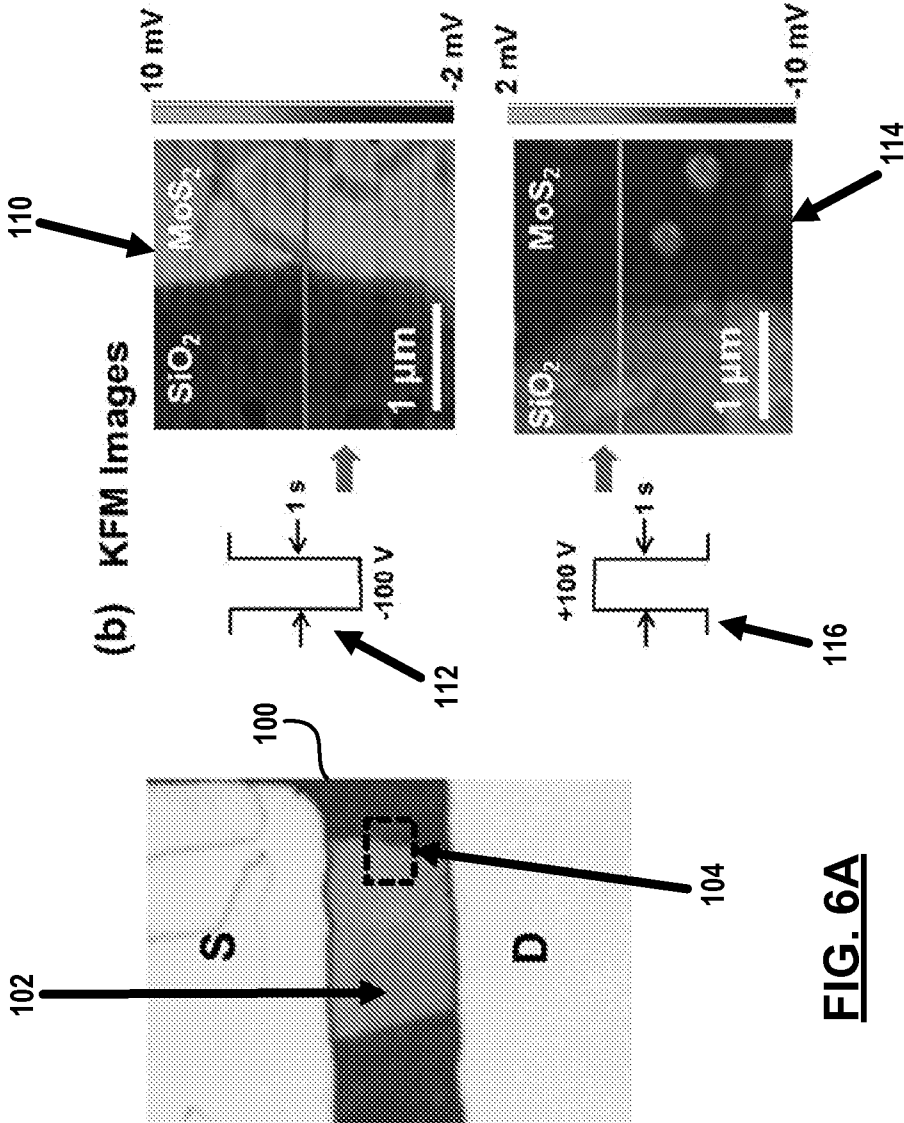


FIG. 6B

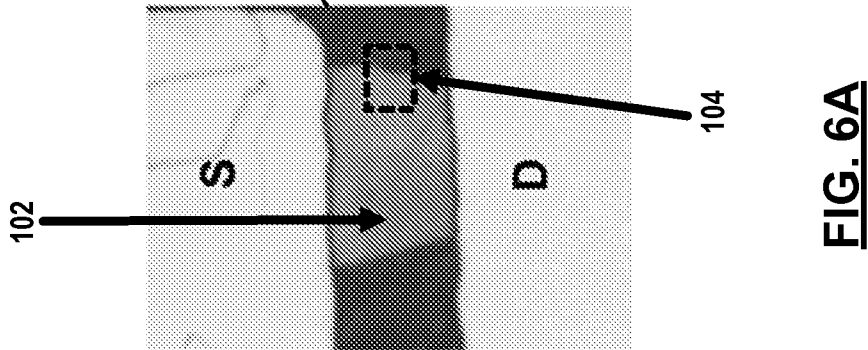
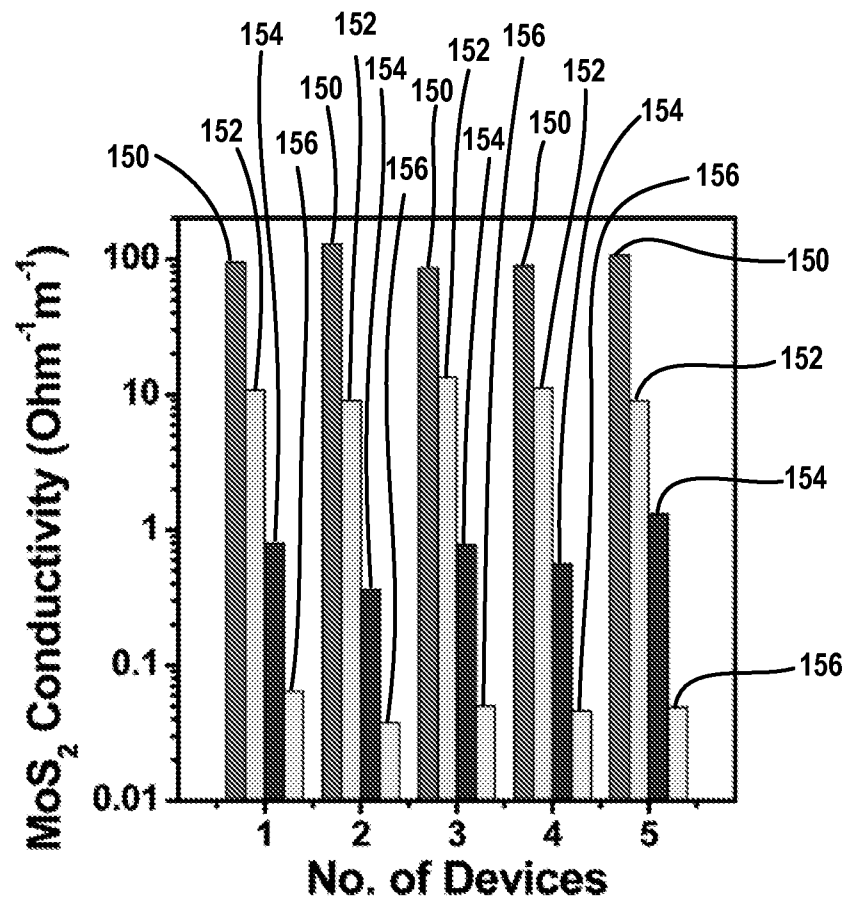
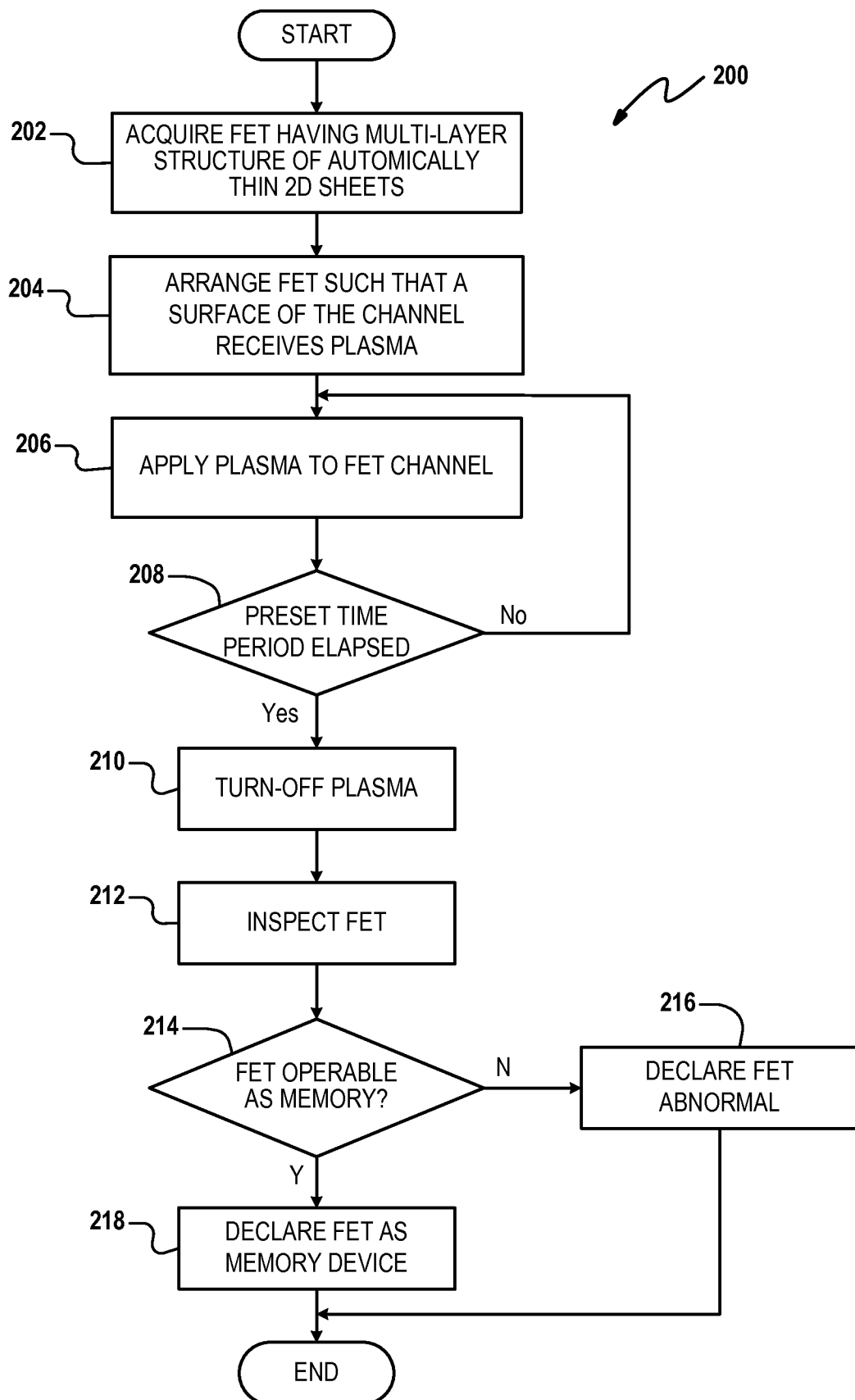


FIG. 6A

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**FIG. 7**

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**FIG. 8**

## INTERNATIONAL SEARCH REPORT

International application No.  
**PCT/US2015/019247****A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/8247(2006.01)i, H01L 27/115(2006.01)i, H01L 29/78(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/8247; H01L 27/115; G11C 11/22; H01L 29/786; H01L 29/78; H01L 29/792; H01L 33/00; H01L 29/66; H01L 33/40

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) &amp; Keywords: memory, two-dimensional sheet, plasma, ripple

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category* | Citation of document, with indication, where appropriate, of the relevant passages                                               | Relevant to claim No. |
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| A         | US 2011-0170330 A1 (BARBAROS OEZYILMAZ et al.) 14 July 2011<br>See abstract, paragraphs [0044]-[0054] and figures 1A-4C.         | 1-17                  |
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| A         | WO 2012-093360 A1 (ECOLE POLYTECHNIQUE FEDERALE DE LAUSANNE (EPFL))<br>12 July 2012<br>See abstract, pages 8-10 and figures 3-4. | 1-17                  |
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Further documents are listed in the continuation of Box C.



See patent family annex.

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"&amp;" document member of the same patent family

Date of the actual completion of the international search

24 June 2015 (24.06.2015)

Date of mailing of the international search report

**24 June 2015 (24.06.2015)**

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**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/US2015/019247**

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