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(54) **MEMORY DEVICE AND METHOD FOR MANUFACTURING THE SAME**

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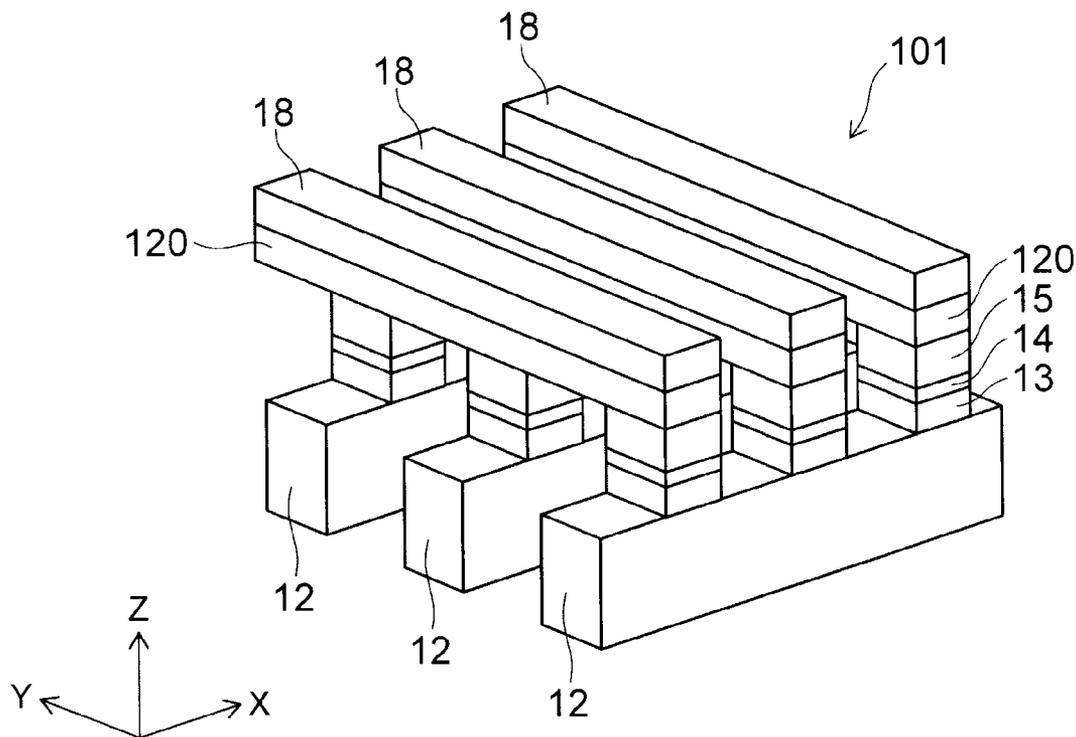
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- (60) Provisional application No. 62/035,137, filed on Aug. 8, 2014.

(57) **ABSTRACT**
A memory device according to one embodiment includes a resistance change film, an insulating film provided on the resistance change film, a first wiring provided on the insulating film and being not in contact with the resistance change film, and a high resistance film having a higher resistivity than the first wiring. The high resistance film is provided on a side surface of a stacked body including the insulating film and the first wiring, and the high resistance film is electrically connected between the first wiring and the resistance change film.



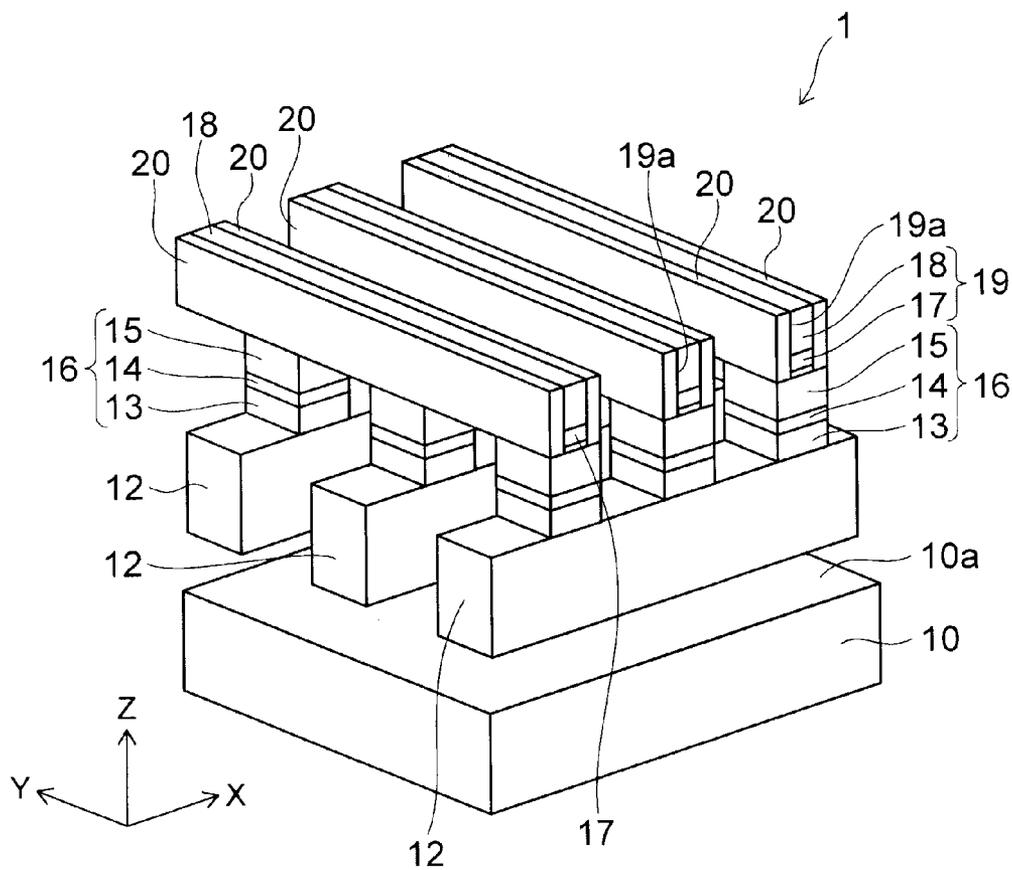


FIG. 1

FIG. 2A

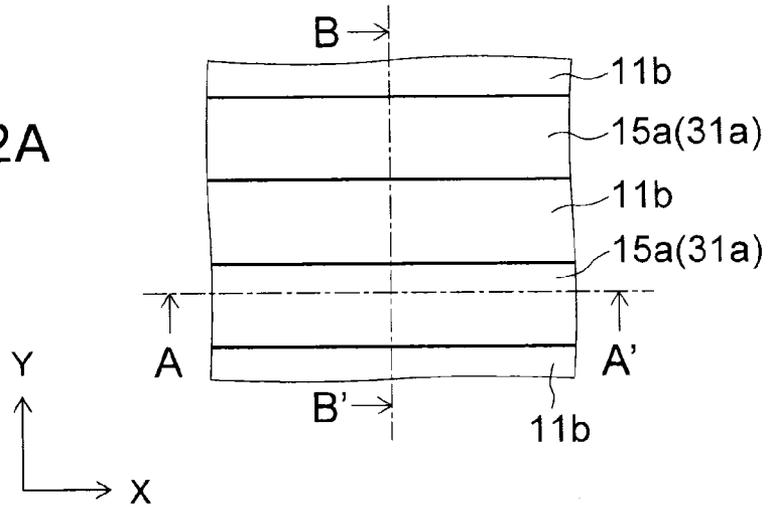


FIG. 2B

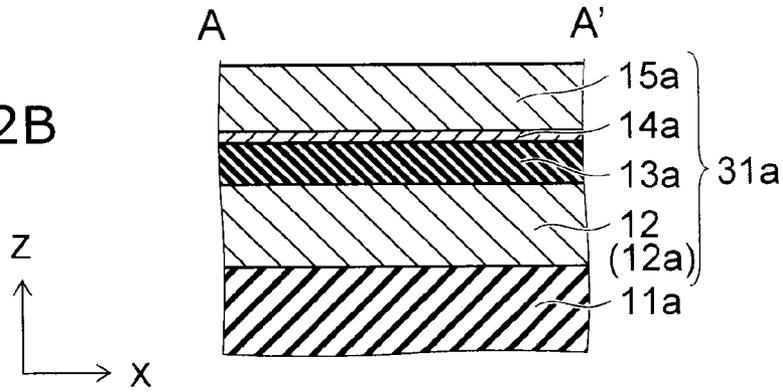


FIG. 2C

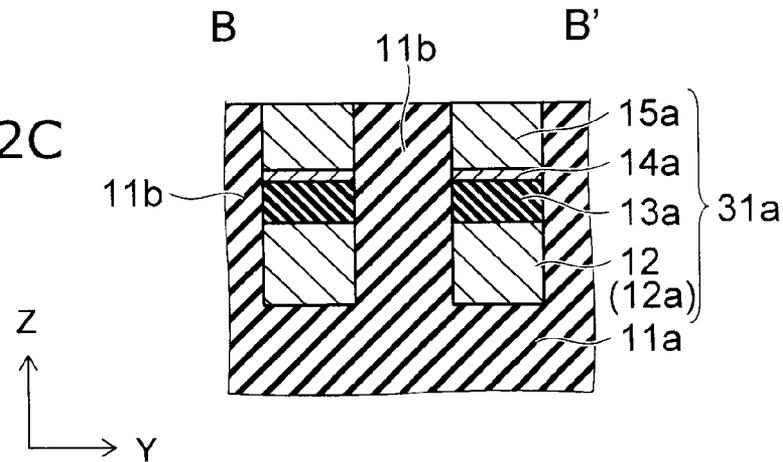


FIG. 3A

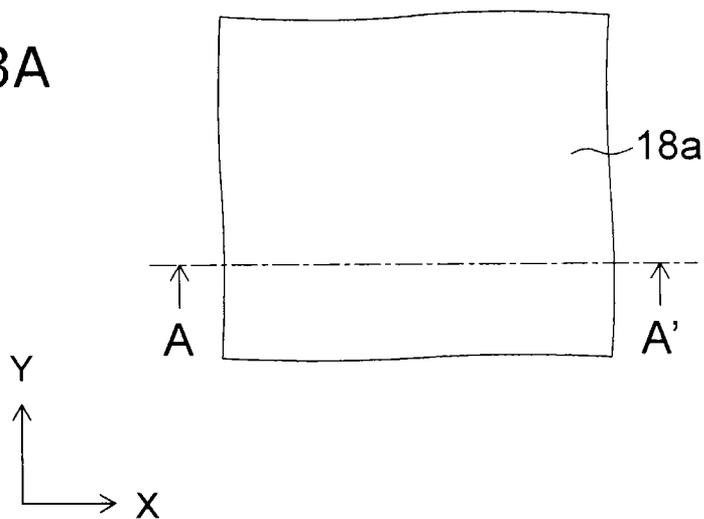


FIG. 3B

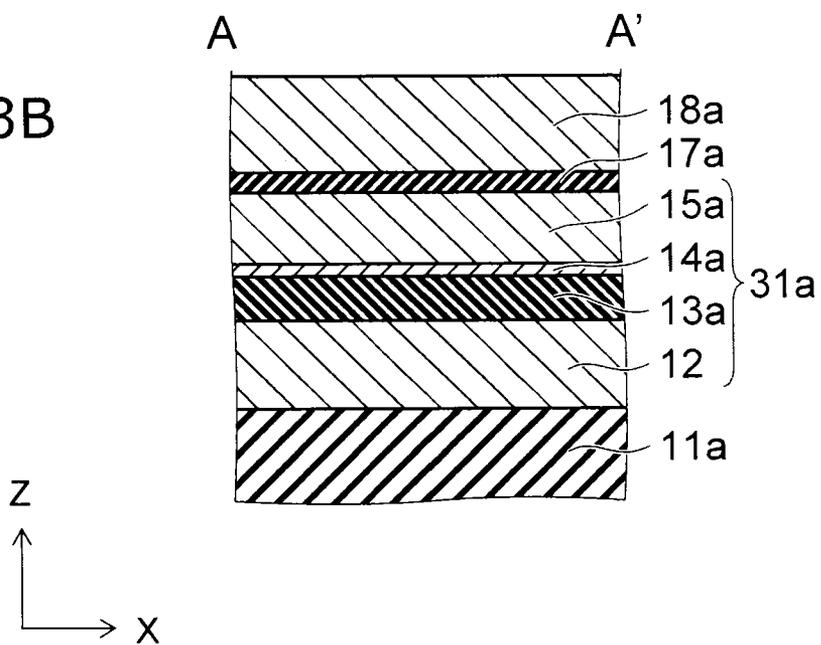
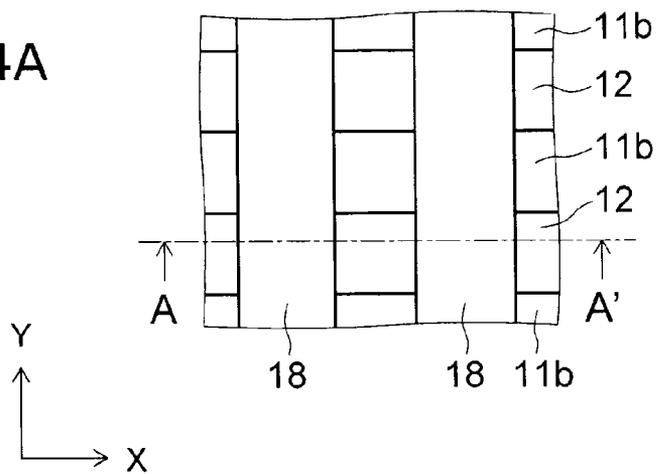


FIG. 4A



A

A'

FIG. 4B

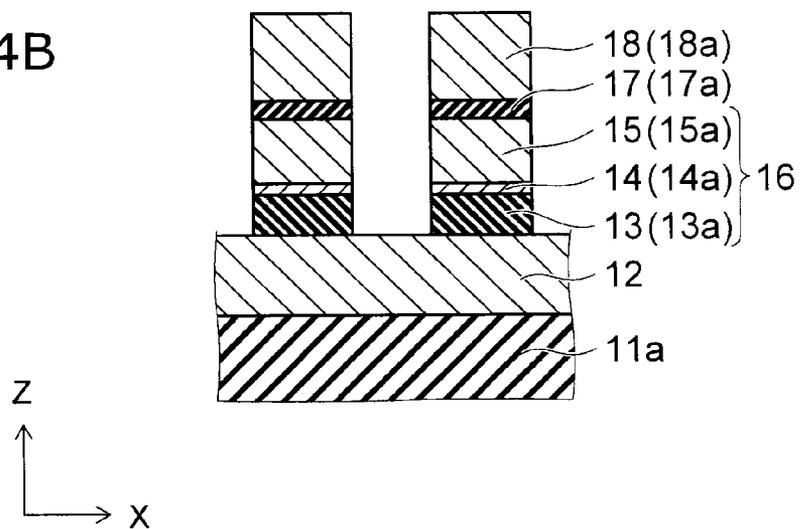


FIG. 5A

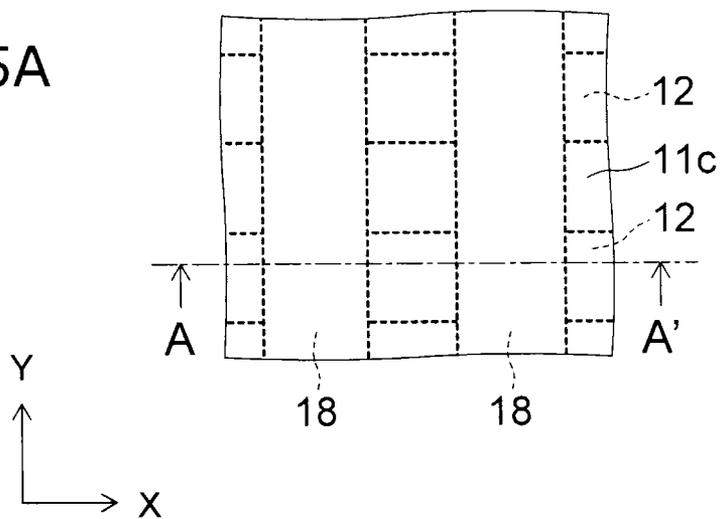


FIG. 5B

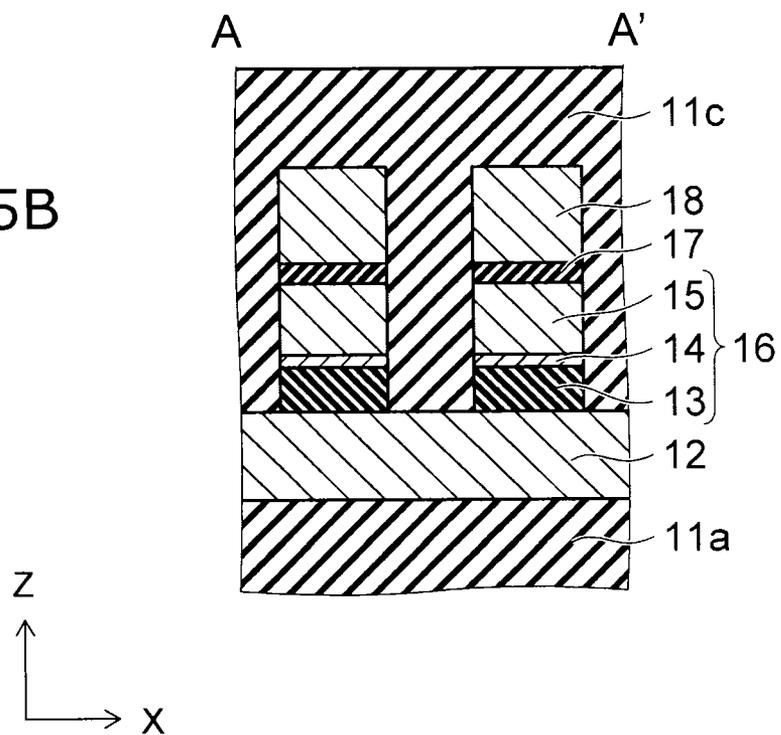


FIG. 6A

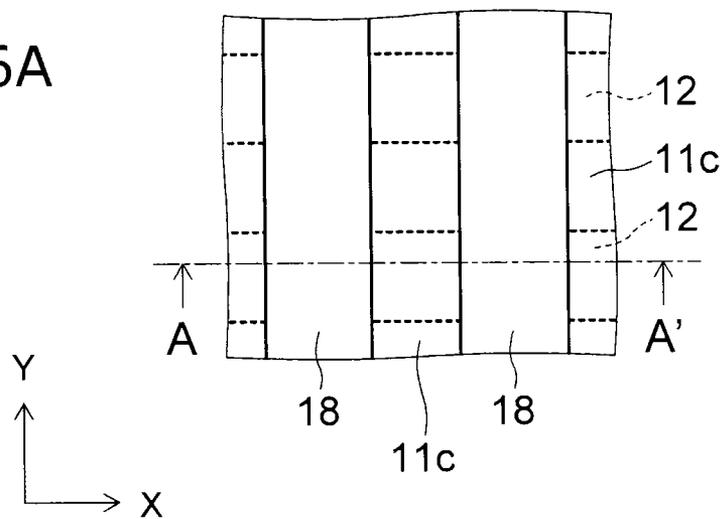


FIG. 6B

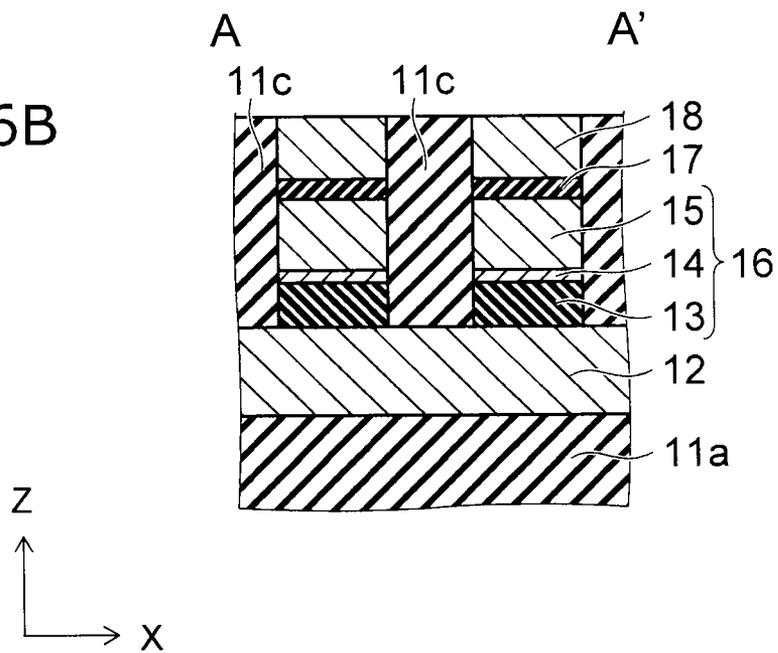


FIG. 7A

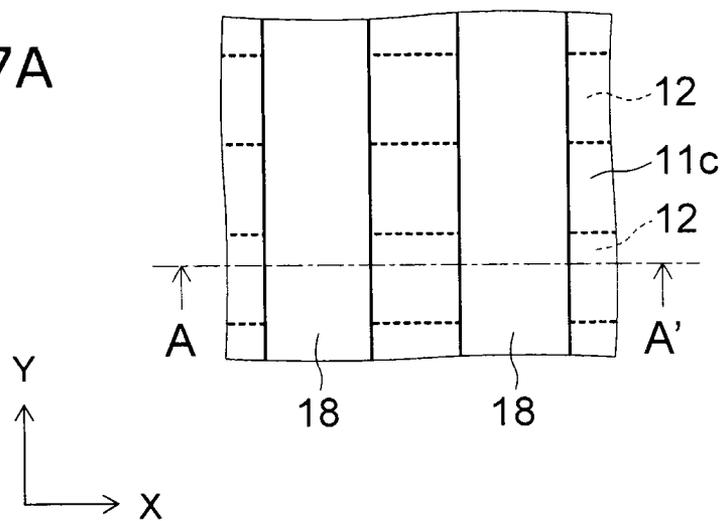


FIG. 7B

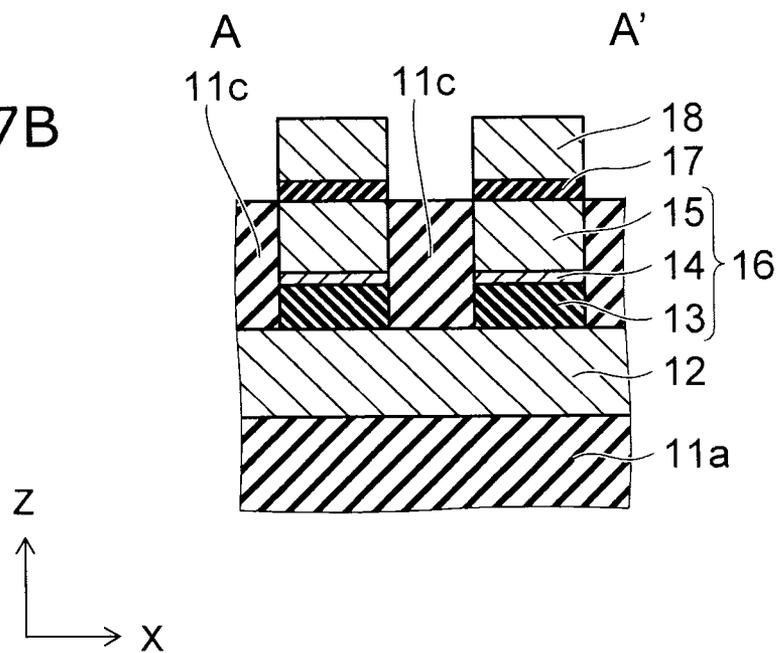


FIG. 8A

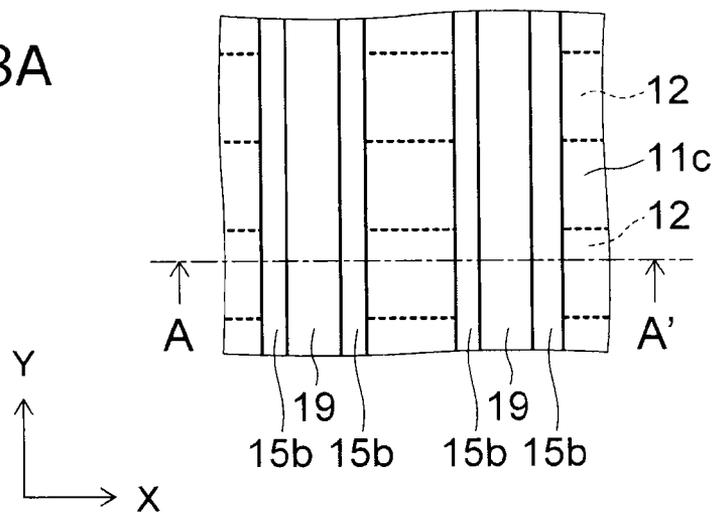


FIG. 8B

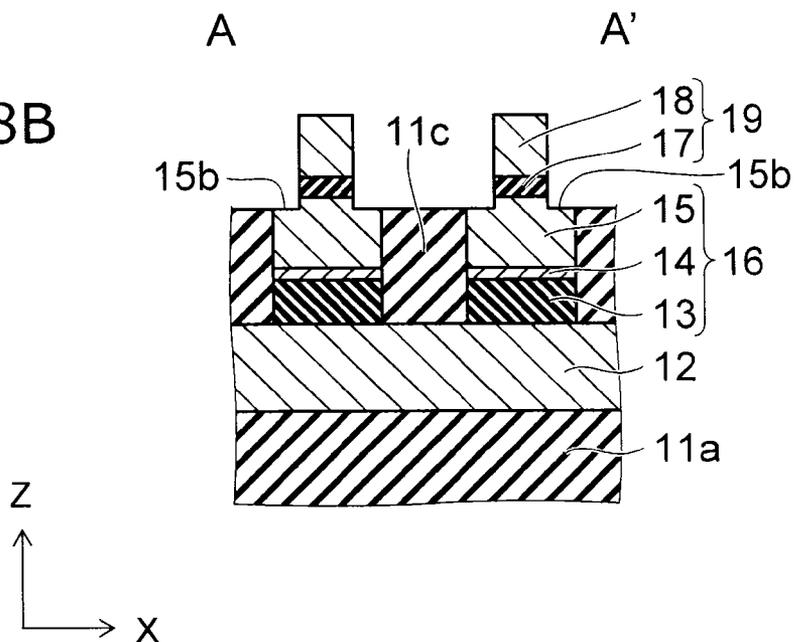


FIG. 9A

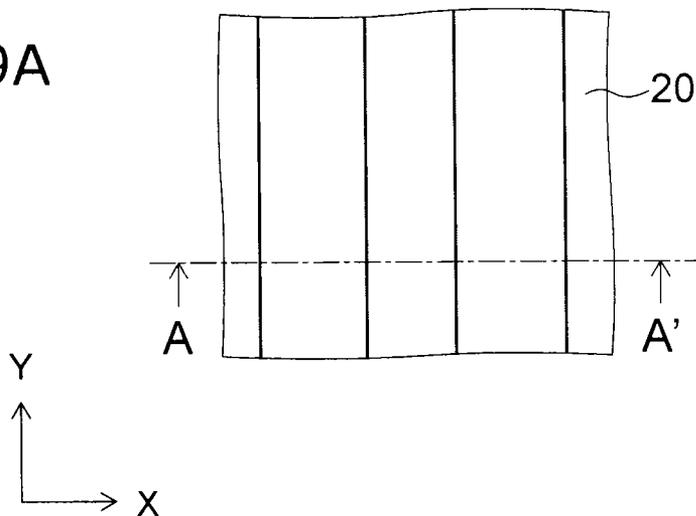


FIG. 9B

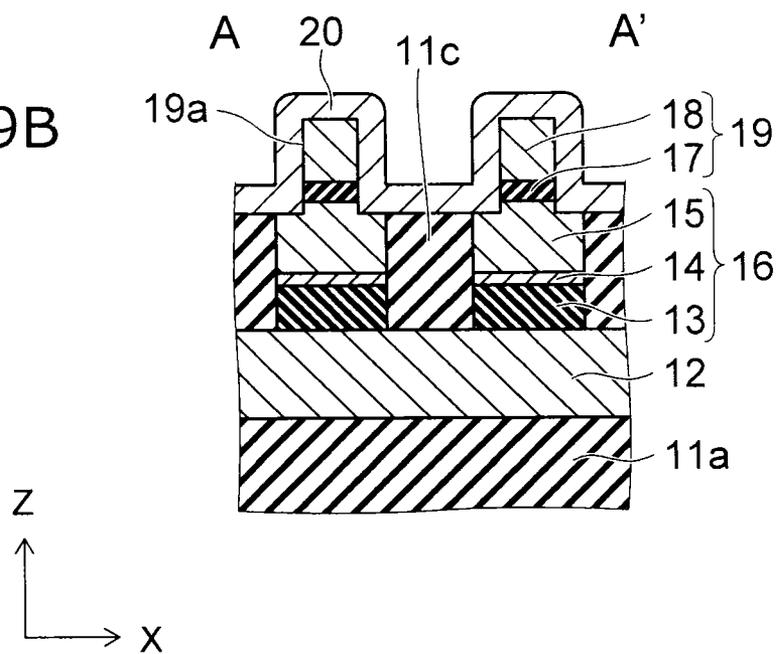


FIG. 10A

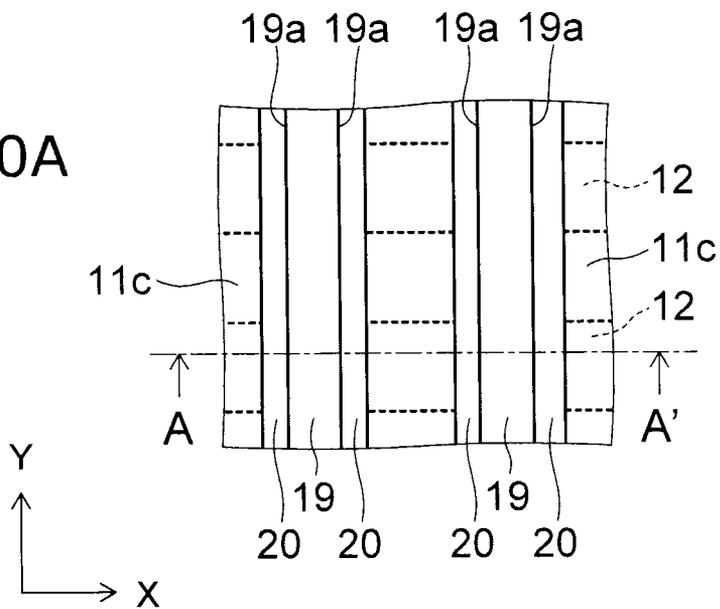


FIG. 10B

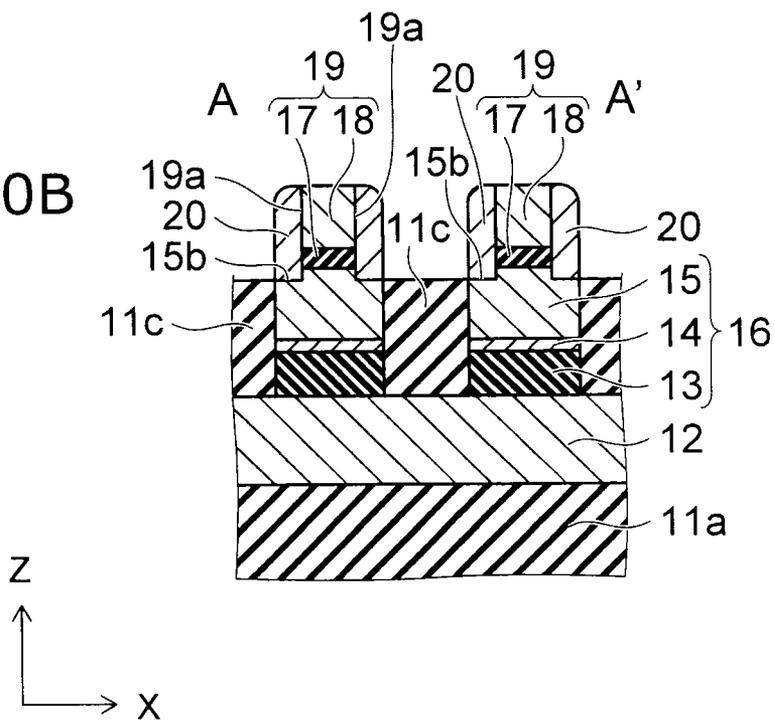


FIG. 11A

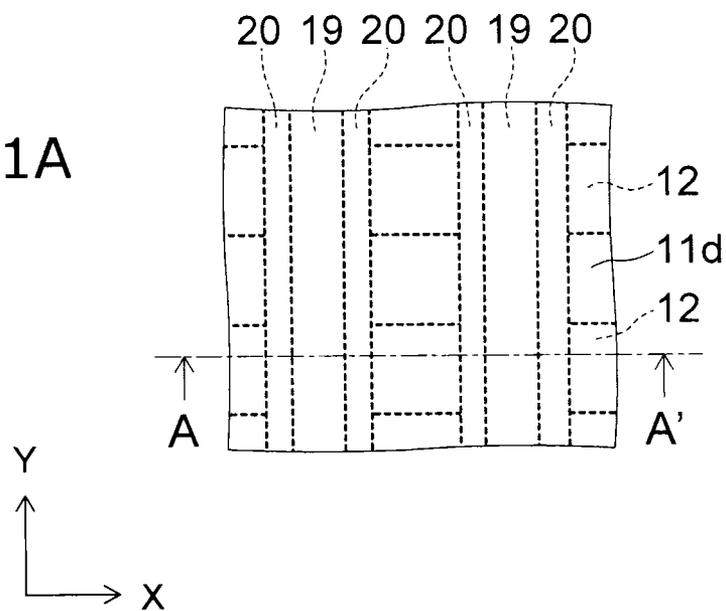


FIG. 11B

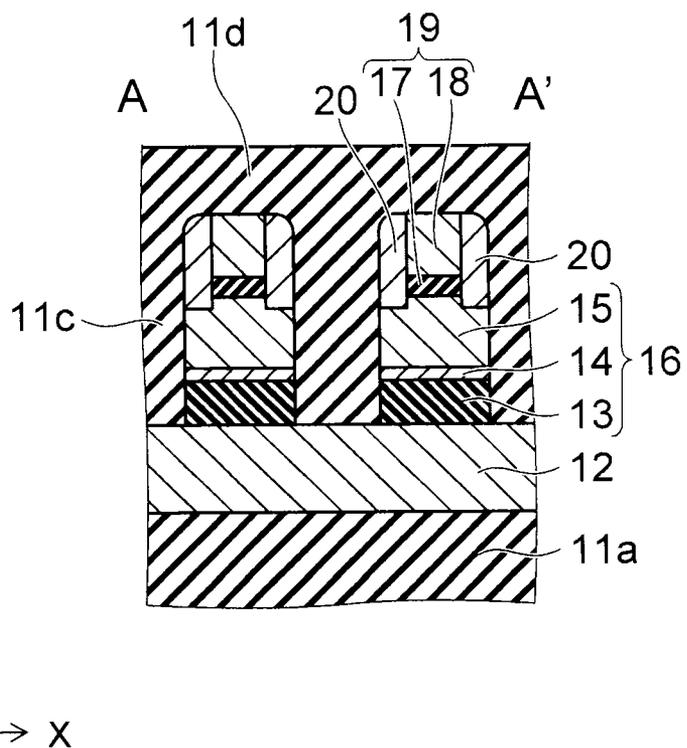


FIG. 12A

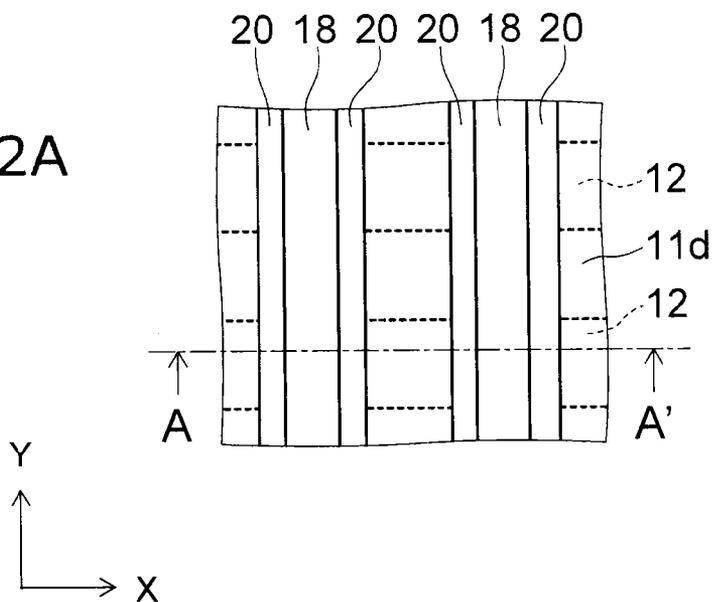
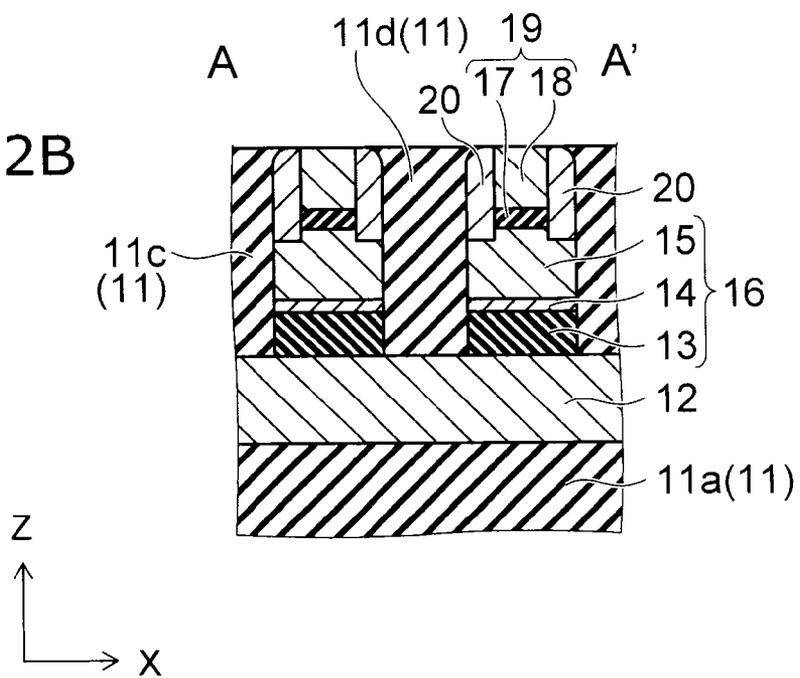


FIG. 12B



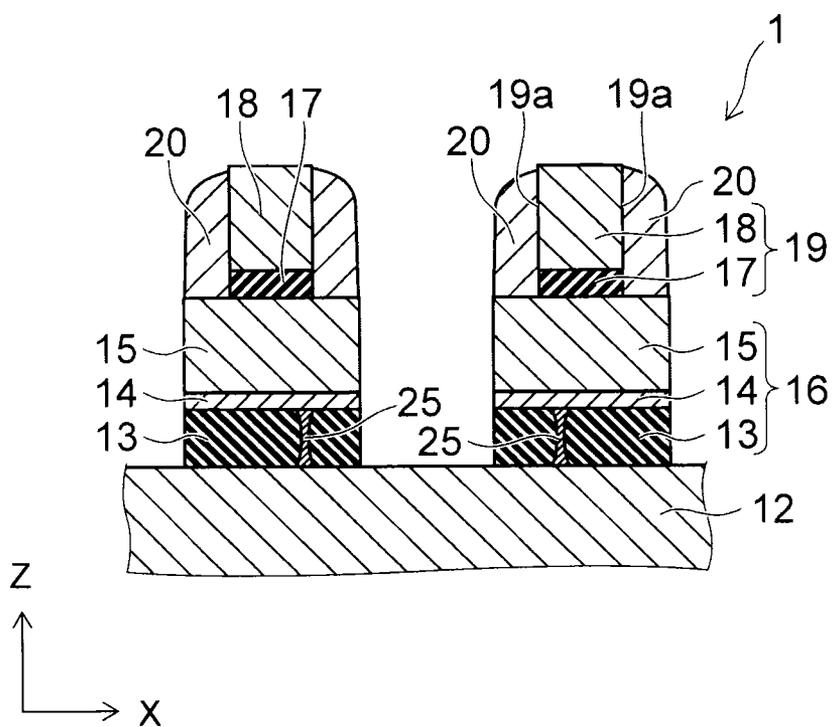


FIG. 13

FIG. 14A

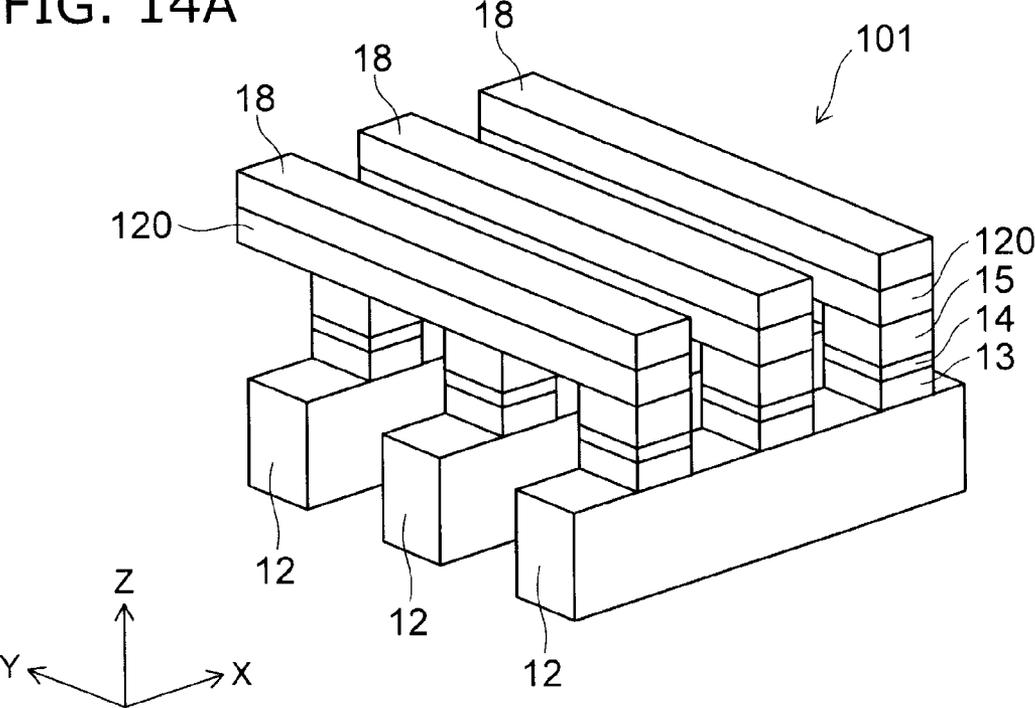
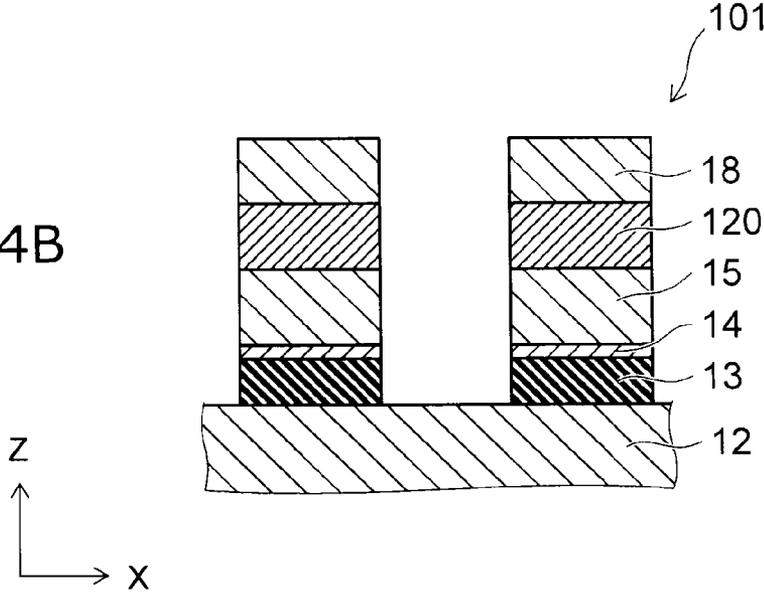


FIG. 14B



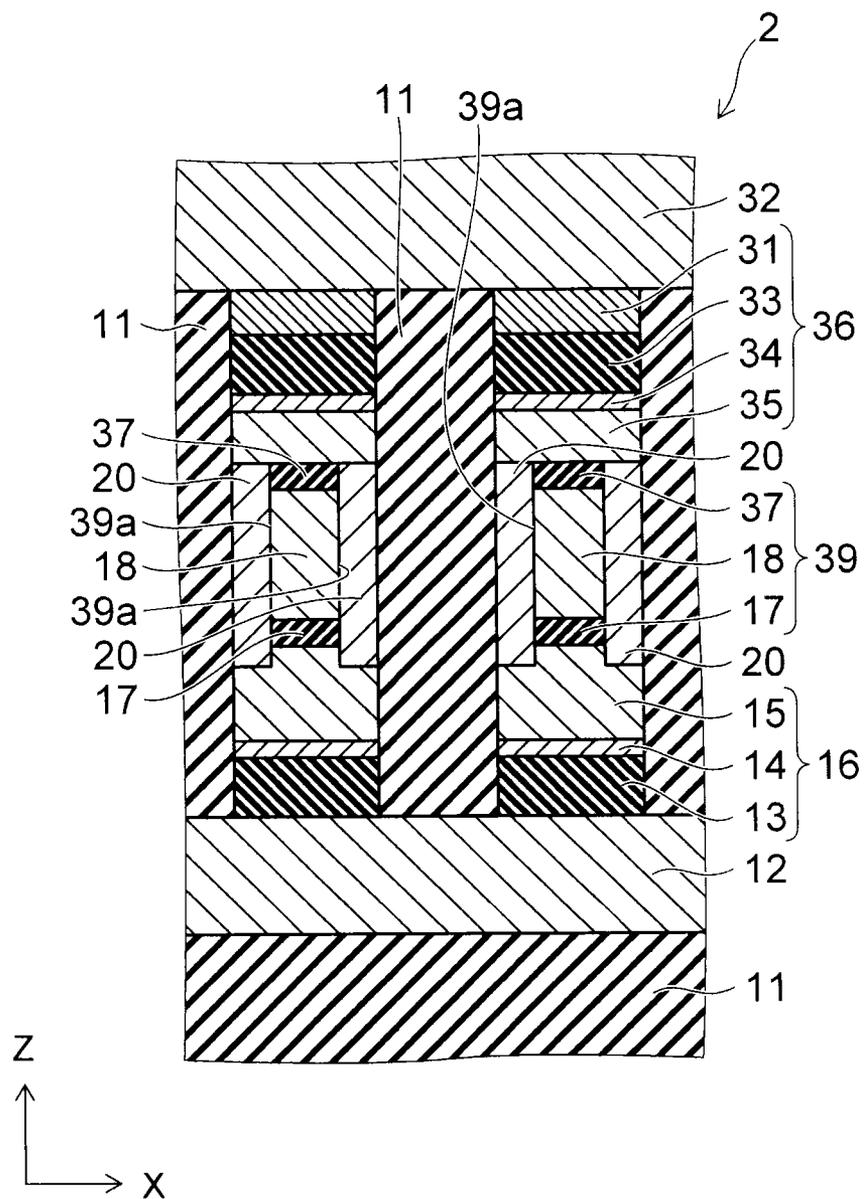


FIG. 15

MEMORY DEVICE AND METHOD FOR MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from U.S. Provisional Patent Application 62/035,137, filed on Aug. 8, 2014; the entire contents of which are incorporated herein by reference.

FIELD

[0002] Embodiments described herein relate generally to a memory device and a method for manufacturing the same.

BACKGROUND

[0003] Recently, there has been proposed a memory device for storing data by changing the electrical resistance of memory cells. In improving the memory density of such a memory device, it is advantageous to integrate a large number of memory cells in a cross-point structure. On the other hand, each memory cell is preferably provided with a current limiting layer for preventing excessive flow of current.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. 1 is a perspective view showing a memory device according to a first embodiment;

[0005] FIGS. 2A to 12B show a method for manufacturing a memory device according to the first embodiment;

[0006] FIG. 13 is a sectional view showing an operation of the memory device according to the first embodiment;

[0007] FIG. 14A is a perspective view showing a memory device according to a comparative example, FIG. 14B is a sectional view thereof; and

[0008] FIG. 15 is a sectional view showing a memory device according to a second embodiment.

DETAILED DESCRIPTION

[0009] In general, a memory device according to one embodiment includes a resistance change film, an insulating film provided on the resistance change film, a first wiring provided on the insulating film and being not in contact with the resistance change film, and a high resistance film having a higher resistivity than the first wiring. The high resistance film is provided on a side surface of a stacked body including the insulating film and the first wiring, and the high resistance film is electrically connected between the first wiring and the resistance change film.

[0010] Embodiments of the invention will now be described with reference to the drawings.

First Embodiment

[0011] First, a first embodiment is described.

[0012] FIG. 1 is a perspective view showing a memory device according to the embodiment.

[0013] For convenience of illustration, the interlayer insulating film is not shown in FIG. 1.

[0014] As shown in FIG. 1, the memory device 1 according to the embodiment includes a silicon substrate 10.

[0015] In the following, for convenience of description, an XYZ orthogonal coordinate system is adopted in this specification. Two directions parallel to the upper surface 10a of the silicon substrate 10 and orthogonal to each other are

referred to as “X-direction” and “Y-direction”. The direction perpendicular to the upper surface 10a is referred to as “Z-direction”.

[0016] An interlayer insulating film 11 (see FIG. 12B) is provided on the silicon substrate 10. The interlayer insulating film 11 is formed from an insulating material such as silicon oxide (SiO₂). A plurality of word lines 12 extending in the X-direction are provided in the interlayer insulating film 11. The word lines 12 are arranged periodically in the Y-direction. The word line 12 is formed from a conductive material such as tungsten (W). The plurality of word lines 12 placed on the same XY-plane constitute a word line wiring layer.

[0017] A resistance change layer 13 is provided intermittently along the X-direction directly above each word line 12. In the memory device 1 as a whole, a plurality of resistance change layers 13 are arranged in a matrix along the X-direction and the Y-direction. The resistance change layer 13 is formed from e.g. amorphous silicon (a-Si) or silicon oxide (SiO₂).

[0018] A metal layer 14 is provided directly above each resistance change layer 13. The metal layer 14 is in contact with the resistance change layer 13. The metal layer 14 contains a metal element, e.g. silver (Ag), cobalt (Co), nickel (Ni), or copper (Cu), the ion of which can migrate in the resistance change layer 13. For instance, the metal layer 14 is formed from silver. The resistance change layer 13 and the metal layer 14 constitute a resistance change film. The resistance change film is a film with variable resistance.

[0019] An electrode 15 is provided directly above each metal layer 14. The electrode 15 is formed from a conductive material such as tungsten. The resistance change layer 13, the metal layer 14, and the electrode 15 form a pillar 16 extending in the Z-direction. The pillar 16 is shaped like e.g. a quadrangular column.

[0020] A plurality of insulating films 17 extending in the Y-direction are provided on the electrode 15. The insulating film 17 is formed from an insulating material, e.g., silicon oxide or silicon nitride (Si₃N₄). Each insulating film 17 is shaped like a strip. Each insulating film 17 passes through the region directly above a plurality of pillars 16 arranged in a line along the Y-direction. The width or X-direction length of the insulating film 17 is narrower than the width or X-direction length of the electrode 15. Thus, each insulating film 17 is placed in a central region in the region directly above the corresponding electrode 15 except both X-direction end parts, and in a region between the central regions of the electrodes 15 adjacent in the Y-direction.

[0021] A bit line 18 extending in the Y-direction is provided directly above the insulating film 17. The bit line 18 is formed from a conductive material such as tungsten. The plurality of bit lines 18 placed on the same XY-plane constitute a bit line wiring layer. The insulating film 17 and the bit line 18 constitute a stacked body 19. The width or X-direction length of the stacked body 19 is narrower than the width or X-direction length of the pillar 16.

[0022] A high resistance film 20 is provided on both side surfaces 19a directed in the X-direction of the stacked body 19. The resistivity of the high resistance film 20 is higher than the resistivity of the word line 12, the resistivity of the electrode 15, and the resistivity of the bit line 18, but lower than the resistivity of the insulating film 17. The high resistance film 20 is formed from e.g. tantalum silicon nitride (TaSiN).

[0023] The side surface of the high resistance film 20 is in contact with the side surface of the bit line 18. Thus, the high

resistance film 20 is connected to the bit line 18. The lower end of the high resistance film 20 is in contact with the upper surface of the electrode 15. Thus, the high resistance film 20 is connected to the electrode 15. On the other hand, the bit line 18 is not in contact with the electrode 15. The insulating film 17 is interposed between the bit line 18 and the electrode 15. Thus, the bit line 18 is connected to the electrode 15 through the high resistance film 20. Furthermore, the electrode 15 is connected to the word line 12 through the metal layer 14 and the resistance change layer 13. Furthermore, in the case where the filament 25 described later is not formed in the resistance change layer 13, the resistivity of the resistance change layer 13 is higher than the resistivity of the word line 12, the resistivity of the electrode 15, and the resistivity of the bit line 18.

[0024] Next, a method for manufacturing a memory device according to the embodiment is described.

[0025] FIGS. 2A to 12B show a method for manufacturing a memory device according to the embodiment.

[0026] FIG. 2A is a plan view. FIG. 2B is a sectional view taken along line A-A' shown in FIG. 2A. FIG. 2C is a sectional view taken along line B-B' shown in FIG. 2A. Furthermore, FIG. 3A is a plan view. FIG. 3B is a sectional view taken along line A-A' shown in FIG. 3A. This also similarly applies to FIGS. 4A to 12B.

[0027] First, as shown in FIGS. 2A to 2C, an interlayer insulating film 11a is formed on a silicon substrate 10 (see FIG. 1). Next, a word line film 12a, a resistance change layer 13a, a metal layer 14a, and an electrode film 15a are formed in this order. Next, the stacked film composed of the word line film 12a, the resistance change layer 13a, the metal layer 14a, and the electrode film 15a is selectively removed and processed into a line-and-space pattern extending in the X-direction. Thus, a plurality of stacked bodies 31a extending in the X-direction are formed. At this time, the word line film 12a is divided into a plurality of word lines 12 extending in the X-direction.

[0028] Next, an interlayer insulating film 11b is embedded between the stacked bodies 31a. In FIG. 2C, the interlayer insulating films 11a and 11b are shown integrally. Next, the upper surface of the interlayer insulating film 11b is subjected to CMP (chemical mechanical polishing) using the electrode film 15a as a stopper. Thus, the upper surface of the interlayer insulating film 11b is set to the same position in the Z-direction as the upper surface of the stacked body 31a.

[0029] Next, as shown in FIGS. 3A and 3B, an insulating film 17a is formed by depositing an insulating material such as silicon oxide on the stacked body 31a and the interlayer insulating film 11b. Next, a bit line film 18a is formed by depositing a conductive material such as tungsten.

[0030] Next, as shown in FIGS. 4A and 4B, the stacked body composed of the bit line film 18a, the insulating film 17a, the electrode film 15a, the metal layer 14a, and the resistance change layer 13a is selectively removed by anisotropic etching such as RIE (reactive ion etching). Thus, the stacked body is processed into a line-and-space pattern extending in the Y-direction. However, the word line 12 and the interlayer insulating films 11b and 11a are not processed. Thus, the bit line film 18a and the insulating film 17a are processed into strips extending in the Y-direction and constitute a plurality of bit lines 18 and insulating films 17, respectively. The electrode film 15a, the metal layer 14a, and the resistance change layer 13a are divided in a matrix along both the X-direction and the Y-direction and constitute an elec-

trode 15, a metal layer 14, and a resistance change layer 13, respectively. As a result, a pillar 16 is formed.

[0031] Next, as shown in FIGS. 5A and 5B, an insulating material is deposited on the entire surface to form an interlayer insulating film 11c. The interlayer insulating film 11c covers the pillar 16, the insulating film 17, and the bit line 18.

[0032] Next, as shown in FIGS. 6A and 6B, the upper surface of the interlayer insulating film 11c is subjected to CMP using the bit line 18 as a stopper. Thus, the upper surface of the interlayer insulating film 11c is set to the same position in the Z-direction as the upper surface of the bit line 18.

[0033] Next, as shown in FIGS. 7A and 7B, the interlayer insulating film 11c is etched back. Thus, the upper surface of the interlayer insulating film 11c is set back close to the interface between the electrode 15 and the insulating film 17.

[0034] Next, as shown in FIGS. 8A and 8B, the bit line 18 and the insulating film 17 are subjected to isotropic etching. Thus, the width or X-direction length of the stacked body 19 including the bit line 18 and the insulating film 17 is reduced. As a result, the regions 15b on both X-direction end parts of the upper surface of the electrode 15 are exposed. In this isotropic etching, the upper part of the electrode 15 and the upper part of the interlayer insulating film 11c are also etched to some extent.

[0035] Next, as shown in FIGS. 9A and 9B, a high resistance material such as tantalum silicon nitride (TaSiN) is deposited on the entire surface by e.g. sputtering technique to form a high resistance film 20. The high resistance film 20 covers the upper surface and the side surface of the stacked body 19.

[0036] Next, as shown in FIGS. 10A and 10B, the high resistance film 20 is subjected to anisotropic etching such as RIE. Thus, the high resistance film 20 is removed from above the upper surface of the interlayer insulating film 11c and from above the upper surface of the stacked body 19. However, the high resistance film 20 is left on the side surface 19a of the stacked body 19 and on the region 15b of the electrode 15.

[0037] Next, as shown in FIGS. 11A and 11B, an insulating material is deposited on the entire surface. Thus, an interlayer insulating film 11d is formed on the interlayer insulating film 11c so as to cover the stacked body 19 and the high resistance film 20.

[0038] Next, as shown in FIGS. 12A and 12B, the upper surface of the interlayer insulating film 11d is subjected to CMP using the bit line 18 as a stopper. Thus, the upper surface of the interlayer insulating film 11d is set to the same position in the Z-direction as the upper surface of the bit line 18.

[0039] Thus, the memory device 1 shown in FIG. 1 is manufactured. Here, the interlayer insulating films 11a-11d constitute part of the interlayer insulating film 11.

[0040] Next, the operation of the memory device according to the embodiment is described.

[0041] FIG. 13 is a sectional view showing the operation of the memory device according to the embodiment.

[0042] The resistivity of the resistance change layer 13 is higher than the resistivity of the word line 12 and the bit line 18. Thus, when the filament 25 described later is not formed, the resistance change layer 13 is in a high resistance state. Here, as shown in FIG. 13, a positive voltage with the bit line 18 serving as a positive electrode and the word line 12 serving as a negative electrode is applied between the bit line 18 and the word line 12. Then, the metal such as silver contained in the metal layer 14 is ionized into a cation (Ag^+) and migrates

toward the word line 12 serving as a negative electrode. Furthermore, in the resistance change layer 13, the cation is combined with an electron supplied from the word line 12 and precipitated as a silver atom. Thus, a filament 25 is formed in the resistance change layer 13 and constitutes a current path. As a result, the resistance of the resistance change layer 13 is decreased. Thus, the resistance change layer 13 turns to a low resistance state.

[0043] Here, the bit line 18 and the electrode 15 are separated from each other by the insulating film 17 and not in direct contact with each other. Thus, the bit line 18 is connected to the electrode 15 through the high resistance film 20. As a result, a current path from the bit line 18 through the high resistance film 20, the electrode 15, the metal layer 14, and the resistance change layer 13 (filament 25) to the word line 12 is formed between the bit line 18 and the word line 12. Furthermore, the high resistance film 20 functions as a current limiting layer and suppresses the amount of current. Thus, no excessive current flows in the aforementioned current path. Accordingly, the pillar 16 is not destroyed by overcurrent.

[0044] On the other hand, a negative voltage with the bit line 18 serving as a negative electrode and the word line 12 serving as a positive electrode may be applied between the bit line 18 and the word line 12. Then, the silver atom forming the filament 25 turns to a cation and migrates toward the bit line 18 serving as a negative electrode. This eliminates part of the filament 25 and breaks the current path. As a result, the resistance of the resistance change layer 13 is increased. Thus, the resistance change layer 13 returns to the high resistance state.

[0045] Thus, one bit of data can be stored by realizing two levels of resistance states in the resistance change layer 13. That is, a memory cell can be formed for each pillar 16.

[0046] Next, the effect of the embodiment is described.

[0047] In the memory device 1 according to the embodiment, the high resistance film 20 is connected between the bit line 18 and the electrode 15. Thus, the high resistance film 20 functions as a current limiting layer. Accordingly, no excessive current flows in each pillar 16.

[0048] In the embodiment, in the steps shown in FIGS. 9A and 9B and FIGS. 10A and 10B, the high resistance film 20 is formed on the side surface 19a of the stacked body 19. Thus, in the step shown in FIGS. 4A and 4B, when the bit line film 18a, the insulating film 17a, the electrode film 15a, the metal layer 14a, and the resistance change layer 13a are processed, the high resistance film 20 has not been formed yet. Accordingly, there is no need to process the high resistance film 20. Thus, in the step shown in FIGS. 4A and 4B, the aspect ratio of processing is lower. Accordingly, trouble due to processing failure is less likely to occur. As a result, the yield of the memory device 1 is increased.

[0049] Furthermore, in the embodiment, the high resistance film 20 is formed as a sidewall of the stacked body 19. Thus, the width of the high resistance film 20 can be controlled by the amount of deposition of the high resistance material. This facilitates forming a thin high resistance film 20. As a result, the current path formed in the high resistance film 20 can be provided with high resistance even if the current path is not lengthened by excessively thickening the insulating film 17. This can also reduce the aspect ratio of processing shown in FIGS. 4A and 4B.

COMPARITIVE EXAMPLE

[0050] Next, a comparative example is described.

[0051] FIG. 14A is a perspective view showing a memory device according to this comparative example. FIG. 14B is a sectional view thereof.

[0052] As shown in FIGS. 14A and 14B, in the memory device 101 according to the comparative example, the high resistance film 120 is shaped not like a sidewall, but like a strip extending in the Y-direction. The high resistance film 120 is placed between the bit line 18 and the electrode 15. Furthermore, the memory device 101 does not include the insulating film 17 (see FIG. 1).

[0053] In this comparative example, when the bit line 18, the electrode 15, the metal layer 14, and the resistance change layer 13 are processed by anisotropic etching, the high resistance film 120 also needs to be processed. Thus, the aspect ratio of processing is higher. As a result, processing is made difficult. This decreases the yield of the memory device 101. Here, it is also considered that the high resistance film 120 may be thinned in order to reduce the aspect ratio of processing. However, in this case, it is difficult to provide a desired resistance to the high resistance film 120.

Second Embodiment

[0054] Next, a second embodiment is described.

[0055] FIG. 15 is a sectional view showing a memory device according to the embodiment.

[0056] As shown in FIG. 15, in the memory device 2 according to the embodiment, an insulating film 37 shaped like a strip extending in the Y-direction is provided directly above the bit line 18. The high resistance film 20 is provided on a side surface 39a directed in the X-direction of the stacked body 39 composed of the insulating film 17, the bit line 18, and the insulating film 37.

[0057] Furthermore, an electrode 35 is provided on the insulating film 37 and the high resistance film 20. The electrode 35 is provided directly above the electrode 15. The electrode 35 is divided along both the X-direction and the Y-direction. A metal layer 34, a resistance change layer 33, and an electrode 31 are stacked in this order directly above the electrode 35. The metal layer 34 and the resistance change layer 33 constitute a resistance change film. The electrode 35, the metal layer 34, the resistance change layer 33, and the electrode 31 constitute a pillar 36 extending in the Z-direction. The pillar 36 is placed directly above the pillar 16.

[0058] The electrode 35 and the electrode 31 are formed from the same material as the electrode 15, such as tungsten. The metal layer 34 is formed from the same material as the metal layer 14. The metal layer 34 contains e.g. silver, cobalt, nickel, or copper. The metal layer 34 is formed from e.g. silver. The resistance change layer 33 is formed from the same material as the resistance change layer 13. The resistance change layer 33 is formed from e.g. amorphous silicon or silicon oxide.

[0059] A word line 32 extending in the X-direction is provided on the electrode 31. The word lines 32 are provided in a plurality and arranged periodically along the Y-direction. Each word line 32 is placed directly above the word line 12. The word line 32 is formed from the same material as the word line 12, such as tungsten.

[0060] Thus, in the memory device 2, the word line 32 is provided on the bit line 18. The pillar 36 is connected between

the bit line **18** and the word line **32**. Like the pillar **16**, the pillar **36** can also constitute a memory cell.

[0061] According to the embodiment, the memory cells can be integrated in three dimensions. This can further increase the memory density per unit area. The configuration, manufacturing method, operation, and effect of the embodiment other than the foregoing are similar to those of the above first embodiment.

[0062] In the embodiment, another pillar including a resistance change film may be provided on the word line **32**, and a bit line extending in the Y-direction may be provided on the pillar. Thus, word line wiring layers each including a plurality of word lines extending in the X-direction and bit line wiring layers each including a plurality of bit lines extending in the Y-direction may be alternately stacked on the silicon substrate **10**. A pillar including a resistance change film may be connected between each word line and each bit line. This can realize a memory device including a plurality of word line wiring layers and bit line wiring layers in which memory cells are stacked in three or more stages.

[0063] Also in this case, an insulating film is provided on the upper surface and the lower surface of each bit line. A high resistance film is provided on the side surface of the stacked body composed of each bit line and two insulating films provided on the upper and lower surfaces of the bit line. The high resistance film is connected to the electrode by bringing the end surface of the high resistance film into contact with the electrode. Thus, the bit line is connected to the electrode through the high resistance film without bringing the bit line into contact with the electrode. On the other hand, the resistance change film is connected between the word line and the high resistance film.

[0064] The above embodiments have been described with reference to an example in which the resistance change film is a stacked film including a resistance change layer and a metal layer. However, the resistance change film is not limited thereto. For instance, the resistance change film may be a monolayer film made of metal oxide.

[0065] The embodiments described above can realize a memory device being easy to manufacture, and a method for manufacturing the same.

[0066] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the invention.

What is claimed is:

1. A memory device comprising:

- a resistance change film;
- an insulating film provided on the resistance change film;
- a first wiring provided on the insulating film and being not in contact with the resistance change film; and
- a high resistance film having a higher resistivity than the first wiring, provided on a side surface of a stacked body including the insulating film and the first wiring, and electrically connected between the first wiring and the resistance change film.

2. The device according to claim 1, wherein width of the stacked body is narrower than width of the resistance change film.

3. The device according to claim 2, further comprising: an electrode having a lower resistivity than the high resistance film and placed between the resistance change film and the high resistance film.

4. The device according to claim 3, wherein the width of the stacked body is narrower than width of the electrode, and a lower end of the high resistance film is in contact with the electrode.

5. The device according to claim 1, further comprising: a second wiring extending in a direction crossing a direction in that the first wiring extends, provided below the resistance change film, and connected to the resistance change film.

6. The device according to claim 1, wherein the high resistance film contains tantalum, silicon, and nitrogen.

7. The device according to claim 1, wherein the resistance change film includes:

- a resistance change layer having a higher resistivity than the first wiring; and
- a metal layer in contact with the resistance change layer.

8. The device according to claim 7, wherein the resistance change layer contains silicon, and the metal layer contains one or more metals selected from the group consisting of silver, cobalt, nickel, and copper.

9. A memory device comprising: a plurality of first wiring layers each including a plurality of first wirings extending in a first direction;

a plurality of second wiring layers each including a plurality of second wirings extending in a second direction crossing the first direction;

a first insulating film provided on an upper surface of each of the second wirings;

a second insulating film provided on a lower surface of each of the second wirings;

a high resistance film having a higher resistivity than the first wiring and the second wiring, provided on a side surface of a stacked body including the second insulating film, the second wiring, and the first insulating film, and connected to the second wiring; and

a resistance change film electrically connected between each of the first wirings and the high resistance film and being not in contact with the second wirings, the first wiring layers and the second wiring layers being stacked alternately.

10. The device according to claim 9, wherein length in the first direction of the stacked body is shorter than length in the first direction of the resistance change film.

11. The device according to claim 10, further comprising: an electrode having a lower resistivity than the high resistance film and placed between the resistance change film and the high resistance film.

12. The device according to claim 11, wherein width of the stacked body is narrower than width of the electrode, and an end surface of the high resistance film is in contact with the electrode.

13. The device according to claim 9, wherein the high resistance film contains tantalum, silicon, and nitrogen.

14. The device according to claim 9, wherein the resistance change film includes:

a resistance change layer having a higher resistivity than the first wiring; and

a metal layer in contact with the resistance change layer.

15. The device according to claim **14**, wherein the resistance change layer contains silicon, and the metal layer contains one or more metals selected from the group consisting of silver, cobalt, nickel, and copper.

16. A method for manufacturing a memory device, comprising:

forming a resistance change film on a first wiring film; processing the resistance change film into a strip extending in a first direction and processing the first wiring film into a plurality of first wirings extending in the first direction by selectively removing the resistance change film and the first wiring film;

forming an insulating film and a second wiring film in this order;

processing the second wiring film into a plurality of second wirings extending in a second direction crossing the first direction, processing the insulating film into a strip extending in the second direction, and dividing the resistance change film along the first direction by selectively removing the second wiring film, the insulating film, and the resistance change film;

reducing width of a stacked body including the insulating film and the second wiring; and

forming a high resistance film on a side surface of the stacked body, the high resistance film having a higher

resistivity than the first wiring film and the second wiring film and being electrically connected to the resistance change film.

17. The method according to claim **16**, wherein the forming the high resistance film includes:

depositing the high resistance film so as to cover the stacked body; and

removing a portion of the high resistance film located on an upper surface of the stacked body and leaving a portion of the high resistance film located on a side surface of the stacked body by etching the high resistance film.

18. The method according to claim **16**, wherein the reducing the width of the stacked body includes performing isotropic etching on the insulating film and the second wiring.

19. The method according to claim **16**, wherein the dividing includes performing anisotropic etching on the second wiring film, the insulating film, and the resistance change film.

20. The method according to claim **16**, further comprising: forming an electrode film on the resistance change film, wherein in the processing into the plurality of first wirings, the electrode film is also processed into a strip extending in the first direction,

in the dividing, the electrode film is processed into a plurality of electrodes arranged along both the first direction and the second direction, and

in the forming the high resistance film, the high resistance film is brought into contact with the electrode.

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