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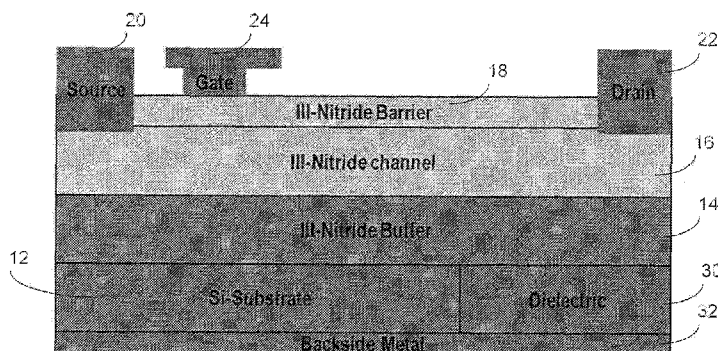


FIG. 1

(57) Abstract: A transistor includes a plurality of epi layers, a drain electrode electrically connected to a channel layer in the epi layers, a source electrode electrically connected to the channel layer, a backside metal layer, a substrate between a first portion of the epi layers and the backside metal layer, and a dielectric between a second portion of the epi layers and the backside metal layer.

III-NITRIDE TRANSISTOR WITH ENGINEERED SUBSTRATE

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to and claims priority to U.S. Application Serial No. 13/838,546 filed March 15, 2013, which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[0002] This disclosure relates to III-nitride transistors and GaN-on-Si transistors, and in particular to breakdown voltages in III-nitride transistors.

BACKGROUND

[0003] GaN-on-Si transistors are suitable for making high-efficiency and low-cost power switching module; however, the voltage breakdown performance of GaN-on-Si transistors is limited by the thickness of the III-nitride epilayer stack. It is challenging to grow III-nitride epilayer stack thicker than 5 micrometers, due to the large thermal mismatch between the III-nitride material and the Si substrate.

[0004] It is well known that the Si substrate can limit the breakdown voltage of GaN-on-Si transistors. Bin Lu and Tomas Palacios, "High Breakdown (>1500V) AlGaIn/GaN HEMTs by Substrate-Transfer," IEEE Electron Device Letters, vol. 31, no. 9, pp. 951-953, Sep 2010 describe the removal of the Si substrate, and the subsequent transfer of the device to a glass substrate. Devices showed higher breakdown voltage

after the substrate transfer; however, a disadvantage of this approach is that it is difficult to handle large-size wafers with their substrates completely removed, resulting in low yield and high cost.

[0005] P. Srivastava, J. Das, D. Visalli, M. V. Hove, P. E. Malinowski, D. Marcon, S. Lenci, K. Geens, K. Cheng, M. Leys, S. Decoutere, R. Mertens, and G. Borghs, "Record Breakdown Voltage (2200V) of GaN DHFETs on Si with 2- μ m Buffer Thickness by Local Substrate Removal," IEEE Electron Device Letters, vol. 32, no. 1, pp. 30-32, Jan. 2011 describe an improvement in breakdown voltage after local removal of the Si substrate between the source and the drain. A disadvantage of this approach to improving breakdown voltage is that an unfilled trench in the Si substrate may cause electron trapping problems, which affect the dynamic characteristics of the GaN FETs. In particular the devices with an etched substrate may have poor dynamic on-resistance due to trapping at the substrate/air interface.

[0006] What is needed are III-nitride transistors and a method to fabricate III-nitride transistors with improved breakdown voltage that have good performance characteristics and are cost effective to fabricate. The embodiments of the present disclosure answer these and other needs.

SUMMARY

[0007] In a first embodiment disclosed herein, a transistor comprises a plurality of epi layers, a drain electrode electrically connected to a channel layer in the epi layers, a source electrode electrically connected to the channel layer, a backside metal layer, a substrate between a

first portion of the epi layers and the backside metal layer; and a dielectric between a second portion of the epi layers and the backside metal layer.

[0008] In another embodiment disclosed herein, a method of fabricating a transistor comprises forming a plurality of epi layers on a substrate, forming a drain electrode electrically connected to a channel layer in the epi layers, forming a source electrode electrically connected to the channel layer in the epi layers, coating the drain electrode, the source electrode and a top layer of the epi layers with a removable material, bonding a carrier wafer to the removable material, etching away a portion of the substrate under the drain, depositing dielectric in the etched away portion of the substrate, depositing backside metal on the substrate and the dielectric, and removing the carrier wafer and the removable material

[0009] These and other features and advantages will become further apparent from the detailed description and accompanying figures that follow. In the figures and description, numerals indicate the various features, like numerals referring to like features throughout both the drawings and the description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 shows an elevation sectional view of a III-nitride transistor in accordance with the present disclosure; and

[0011] FIGS. 2A to 2D show a method to fabricate a III-nitride transistor in accordance with the present disclosure.

DETAILED DESCRIPTION

[0012] In the following description, numerous specific details are set forth to clearly describe various specific embodiments disclosed herein. One skilled in the art, however, will understand that the presently claimed invention may be practiced without all of the specific details discussed below. In other instances, well known features have not been described so as not to obscure the invention.

[0013] FIG. 1 shows an elevation sectional view of a III-nitride transistor in accordance with the present disclosure. The substrate 12, which may be silicon (Si), is partially removed in an area underneath the drain 22 and filled with a dielectric 30, which may be benzo-cyclo-butene (BCB). Backside metal 32 is deposited on the backside of substrate 12 as well as the dielectric 30.

[0014] For the transistor in FIG. 1 the drain 22 may be at a high voltage and the backside metal 32 may be a ground. Because a silicon substrate 12 is conductive all of the voltage between the drain 22 and the backside metal 32 must be dropped across the III-nitride layers. By removing at least some or all of the substrate 12 underneath the drain 22, and filling it in with a dielectric 30, some of the voltage drop can be across the dielectric 30, which reduces the amount of voltage drop that would otherwise be across the III-nitride layers, thus improving the breakdown voltage of the device. Note that other substrates may also be conductive such as a type of silicon carbide (SiC) substrate.

[0015] A buffer layer 14 is over the substrate 12 and the dielectric 30. The buffer layer 14 may be a III-nitride material. A channel layer 16 is over the buffer layer 14, and may be a III-nitride material. Typically the channel layer is un-intentionally doped GaN layer with the thickness ranging from 5 nanometers (nm) to about 2 micrometers.

[0016] A barrier layer 18 is over the channel layer 16, and may be a stack of III-nitride materials. The barrier layer 18 has a greater energy bandgap than the channel layer 16. Typically the barrier layer 18 may be an AlGa_N alloy with the Al content of 10~30% and the thickness of 5-30 nanometers (nm).

[0017] A source electrode 20 and a drain electrode 22 are on opposite ends of the barrier layer 18 and the channel layer 16, and are typically formed by alloying a stack of Ti/Al/Ni/Au. The source electrode 20 and the drain electrode 22 are in electrical contact with the channel layer 16. A gate electrode 24 is on top of the barrier layer 18, and between the source 20 and drain 22 electrodes.

[0018] Transistors with III-nitride on Si, such as GaN-on-Si transistors employing the structure of FIG. 1 have increased breakdown voltage ratings without the necessity of increasing the thickness of the III-nitride epilayers for the buffer layer 14, channel layer 16, and barrier layer 18.

[0019] FIGs. 2A to 2D show a method to fabricate a III-nitride transistor in accordance with the present disclosure.

[0020] First, as shown in FIG. 2A, a III-nitride transistor is formed by growing a buffer layer 14 on a substrate 12, which may be silicon (Si). The buffer layer 14 may be a stack of III-nitride materials grown on the

substrate 12 by chemical vapor deposition or molecular beam epitaxy.

[0021] Then a channel layer 16 is grown on the buffer layer 14. The channel layer 16 may be a III-nitride material grown on the buffer layer 14 by chemical vapor deposition or molecular beam epitaxy. Typically the channel layer is unintentionally doped III-nitride layer, such as GaN, with the thickness ranging from 5 nanometers to a few micrometers.

[0022] Next a barrier layer 18 is grown on the channel layer 16. The barrier layer 18 may be a stack of III-nitride materials grown on the channel layer 16 by chemical vapor deposition or molecular beam epitaxy. The barrier layer 18 is formed to have a greater energy bandgap than the channel layer 16. Typically the barrier layer 18 may be an III-nitride, such as an AlGaN alloy with the Al content of 10~30% and the thickness of 5-30nm.

[0023] Then a source electrode 20 and a drain electrode 22 are formed on opposite ends of the barrier layer 18 and the channel layer 16, and are typically formed by alloying a stack of Ti/Al/Ni/Au. The source electrode 20 and the drain electrode 22 are formed in electrical contact with the channel layer 16. Finally, a gate electrode 24 is formed on top of the barrier layer 18, and between the source 20 and drain 22 electrodes.

[0024] Next, as shown in FIG. 2B, the structure is mounted onto a carrier wafer 42 after the epi layer and other front side processes, such as forming the electrodes, are complete. The source 20, drain 22, gate 24 electrodes and the barrier layer 18 are coated with a removable material 40 such as wax. Then a carrier wafer 42 is bonded to the removable material 40.

[0025] Once the carrier wafer 42 is attached, the entire structure can be turned over and a portion 44 of the substrate 12 under the drain may be etched away by using plasma etching.

[0026] Then, as shown in FIG. 2C, dielectric 30 is coated on the backside of the structure in the area 44 of the etched away substrate, and then polished. Next backside metal 32, such as AuGe, is deposited onto the substrate 12 and the filled dielectric 30.

[0027] Then, as shown in FIG. 2D, the carrier wafer 42 and the wax 40 are removed. The result is the structure shown also in FIG. 1.

[0028] As described, foregoing method of selective removal of the substrate and deposition of a dielectric in place of the substrate enhances the breakdown voltage rating of III-nitride devices, such as GaN on Si high electron mobility transistors (HEMTs).

[0029] All elements, parts and steps described herein are preferably included. It is to be understood that any of these elements, parts and steps may be replaced by other elements, parts and steps or deleted altogether as will be obvious to those skilled in the art.

[0030] CONCEPTS

At least the following concepts are included in the present disclosure.

Concept 1. A transistor comprising:

- a plurality of epi layers;
- a drain electrode electrically connected to a channel layer in the epi layers;
- a source electrode electrically connected to the channel layer;
- a backside metal layer;
- a substrate between a first portion of the epi layers and the backside metal layer; and
- a dielectric between a second portion of the epi layers and the backside metal layer.

Concept 2. The transistor of concept 1:

- wherein the plurality of epi layers comprise:
 - a buffer layer;
 - the channel layer over the buffer layer; and
 - a barrier layer over the channel layer; and
- wherein the transistor further comprises:
 - a gate electrode on the barrier layer between the source electrode and the drain electrode; and
- wherein:
 - the substrate is between a first portion of the buffer layer and the backside metal layer; and
 - the dielectric is between a second portion of the buffer layer and the backside metal layer.

Concept 3. The transistor of concept 1 wherein the substrate comprises silicon.

Concept 4. The transistor of concept 1 wherein the dielectric comprises benzo-cyclo-butene (BCB).

Concept 5. The transistor of concept 2 wherein:
the buffer layer comprises a III-nitride material;
the channel layer comprises a III-nitride material;
the barrier layer comprises a III-nitride materials and has a greater energy bandgap than the channel layer.

Concept 6. The transistor of concept 1 wherein the backside metal layer is in electrical contact with the substrate and the dielectric.

Concept 7. The transistor of concept 1 wherein the backside metal layer is at a ground voltage.

Concept 8. The transistor of concept 2 wherein:
the channel layer comprises GaN; and
the barrier layer comprises AlGaN.

Concept 9. The transistor of concept 1 wherein:
the backside metal comprises AuGe.

Concept 10. The transistor of concept 2 wherein:
the channel layer has a thickness ranging from 5 nanometers to a two micrometers; and
the barrier layer has a thickness ranging from 5-30 nanometers.

Concept 11. The transistor of concept 1 wherein:
the plurality of epi layers comprise III-nitride layers.

Concept 12. The transistor of concept 1 wherein:
the dielectric is on a side of the transistor under the drain electrode.

Concept 13. A method of fabricating a transistor comprising:
forming a plurality of epi layers on a substrate;
forming a drain electrode electrically connected to a channel layer in the epi layers;
forming a source electrode electrically connected to the channel layer in the epi layers;
coating the drain electrode, the source electrode and a top layer of the epi layers with a removable material;
bonding a carrier wafer to the removable material;
etching away a portion of the substrate under the drain;
depositing dielectric in the etched away portion of the substrate;
depositing backside metal on the substrate and the dielectric; and
removing the carrier wafer and the removable material.

Concept 14. The method of concept 13:
wherein forming the plurality of epi layers on the substrate comprises:
forming a buffer layer on the substrate;
forming the channel layer on the buffer layer;
forming a barrier layer on the channel layer; and
wherein the method further comprises:
forming a source electrode on an opposite end of the barrier layer from the drain electrode;

forming a gate electrode on the barrier layer between the source and drain electrodes; and
coating the source electrode, the drain electrode, the gate electrode and the barrier layer with the removable material.

Concept 15. The method of concept 14 wherein:

forming the buffer layer, forming the channel layer and forming the barrier layer comprise chemical vapor deposition or molecular beam epitaxy; and

etching away a portion of the substrate under the drain comprises plasma etching.

Concept 16. The method of concept 13 further comprising polishing the deposited dielectric before depositing backside metal on the substrate and the dielectric.

Concept 17. The method of concept 13 wherein the substrate comprises silicon.

Concept 18. The method of concept 13 wherein the dielectric comprises benzo-cyclo-butene (BCB).

Concept 19. The method of concept 14 wherein:

the buffer layer comprises a III-nitride material;
the channel layer comprises a III-nitride material;
the barrier layer comprises a III-nitride materials and has a greater energy bandgap than the channel layer.

Concept 20. The method of concept 14 wherein:

the channel layer comprises GaN; and
the barrier layer comprises AlGaN.

Concept 21. The method of concept 13 wherein:

the backside metal comprises AuGe.

Concept 22. The method of concept 14 wherein:

the channel layer has a thickness ranging from 5 nanometers to a two micrometers; and

the barrier layer has a thickness ranging from 5-30 nanometers.

Concept 23. The method of concept 14 wherein:

the plurality of epi layers comprise III-nitride layers.

Concept 24. The method of concept 13 wherein:

the dielectric is on a side of the transistor under the drain electrode.

[0031] Having now described the invention in accordance with the requirements of the patent statutes, those skilled in this art will understand how to make changes and modifications to the present invention to meet their specific requirements or conditions. Such changes and modifications may be made without departing from the scope and spirit of the invention as disclosed herein.

[0032] The foregoing Detailed Description of exemplary and preferred embodiments is presented for purposes of illustration and disclosure in accordance with the requirements of the law. It is not intended to be exhaustive nor to limit the invention to the precise form(s) described, but only to enable others skilled in the art to understand how the invention may be suited for a particular use or implementation. The possibility of modifications and

variations will be apparent to practitioners skilled in the art. No limitation is intended by the description of exemplary embodiments which may have included tolerances, feature dimensions, specific operating conditions, engineering specifications, or the like, and which may vary between implementations or with changes to the state of the art, and no limitation should be implied therefrom. Applicant has made this disclosure with respect to the current state of the art, but also contemplates advancements and that adaptations in the future may take into consideration of those advancements, namely in accordance with the then current state of the art. It is intended that the scope of the invention be defined by the Claims as written and equivalents as applicable. Reference to a claim element in the singular is not intended to mean "one and only one" unless explicitly so stated. Moreover, no element, component, nor method or process step in this disclosure is intended to be dedicated to the public regardless of whether the element, component, or step is explicitly recited in the Claims. No claim element herein is to be construed under the provisions of 35 U.S.C. Sec. 112, sixth paragraph, unless the element is expressly recited using the phrase "means for. . ." and no method or process step herein is to be construed under those provisions unless the step, or steps, are expressly recited using the phrase "comprising the step(s) of. . ."

WHAT IS CLAIMED IS:

1. A transistor comprising:
 - a plurality of epi layers;
 - a drain electrode electrically connected to a channel layer in the epi layers;
 - a source electrode electrically connected to the channel layer;
 - a backside metal layer;
 - a substrate between a first portion of the epi layers and the backside metal layer; and
 - a dielectric between a second portion of the epi layers and the backside metal layer.
2. The transistor of claim 1:
 - wherein the plurality of epi layers comprise:
 - a buffer layer;
 - the channel layer over the buffer layer; and
 - a barrier layer over the channel layer; and
 - wherein the transistor further comprises:
 - a gate electrode on the barrier layer between the source electrode and the drain electrode; and
 - wherein:
 - the substrate is between a first portion of the buffer layer and the backside metal layer; and
 - the dielectric is between a second portion of the buffer layer and the backside metal layer.
3. The transistor of claim 1 wherein the substrate comprises silicon.

4. The transistor of claim 1 wherein the dielectric comprises benzo-cyclo-butene (BCB).
5. The transistor of claim 2 wherein:
 - the buffer layer comprises a III-nitride material;
 - the channel layer comprises a III-nitride material;
 - the barrier layer comprises a III-nitride materials andhas a greater energy bandgap than the channel layer.
6. The transistor of claim 1 wherein the backside metal layer is in electrical contact with the substrate and the dielectric.
7. The transistor of claim 1 wherein the backside metal layer is at a ground voltage.
8. The transistor of claim 2 wherein:
 - the channel layer comprises GaN; and
 - the barrier layer comprises AlGaN.
9. The transistor of claim 1 wherein:
 - the backside metal comprises AuGe.
10. The transistor of claim 2 wherein:
 - the channel layer has a thickness ranging from 5 nanometers to a two micrometers; and
 - the barrier layer has a thickness ranging from 5-30 nanometers.
11. The transistor of claim 1 wherein:
 - the plurality of epi layers comprise III-nitride layers.

12. The transistor of claim 1 wherein:
the dielectric is on a side of the transistor under the drain electrode.
13. A method of fabricating a transistor comprising:
forming a plurality of epi layers on a substrate;
forming a drain electrode electrically connected to a channel layer in the epi layers;
forming a source electrode electrically connected to the channel layer in the epi layers;
coating the drain electrode, the source electrode and a top layer of the epi layers with a removable material;
bonding a carrier wafer to the removable material;
etching away a portion of the substrate under the drain;
depositing dielectric in the etched away portion of the substrate;
depositing backside metal on the substrate and the dielectric; and
removing the carrier wafer and the removable material.
14. The method of claim 13:
wherein forming the plurality of epi layers on the substrate comprises:
forming a buffer layer on the substrate;
forming the channel layer on the buffer layer;
forming a barrier layer on the channel layer; and
wherein the method further comprises:
forming the source electrode on an opposite end of the barrier layer from the drain electrode;
forming a gate electrode on the barrier layer between the source and drain electrodes; and

coating the source electrode, the drain electrode, the gate electrode and the barrier layer with the removable material.

15. The method of claim 14 wherein:

forming the buffer layer, forming the channel layer and forming the barrier layer comprise chemical vapor deposition or molecular beam epitaxy; and

etching away a portion of the substrate under the drain comprises plasma etching.

16. The method of claim 13 further comprising polishing the deposited dielectric before depositing backside metal on the substrate and the dielectric.

17. The method of claim 13 wherein the substrate comprises silicon.

18. The method of claim 13 wherein the dielectric comprises benzo-cyclo-butene (BCB).

19. The method of claim 14 wherein:

the buffer layer comprises a III-nitride material;

the channel layer comprises a III-nitride material;

the barrier layer comprises a III-nitride materials and has a greater energy bandgap than the channel layer.

20. The method of claim 14 wherein:

the channel layer comprises GaN; and

the barrier layer comprises AlGaN.

21. The method of claim 13 wherein:

the backside metal comprises AuGe.

22. The method of claim 14 wherein:

the channel layer has a thickness ranging from 5 nanometers to a two micrometers; and

the barrier layer has a thickness ranging from 5-30 nanometers.

23. The method of claim 14 wherein:

the plurality of epi layers comprise III-nitride layers.

24. The method of claim 13 wherein:

the dielectric is on a side of the transistor under the drain electrode.

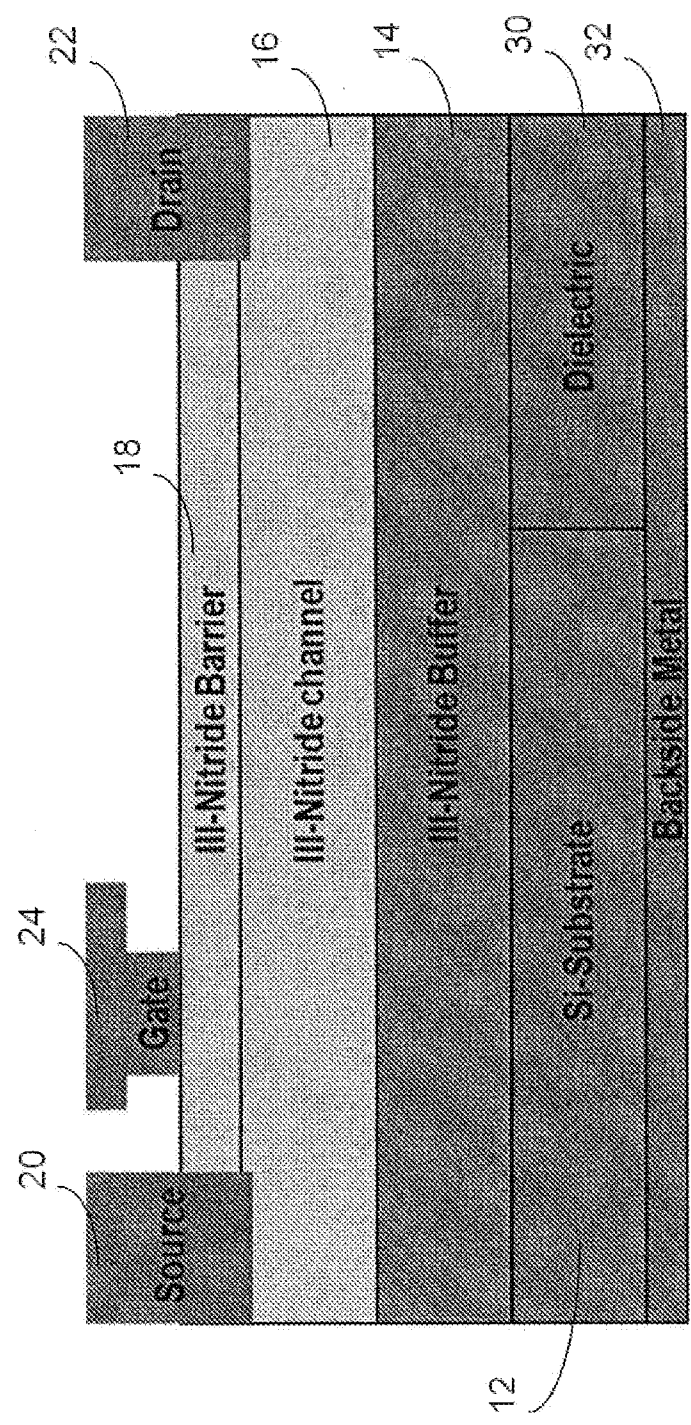


FIG. 1

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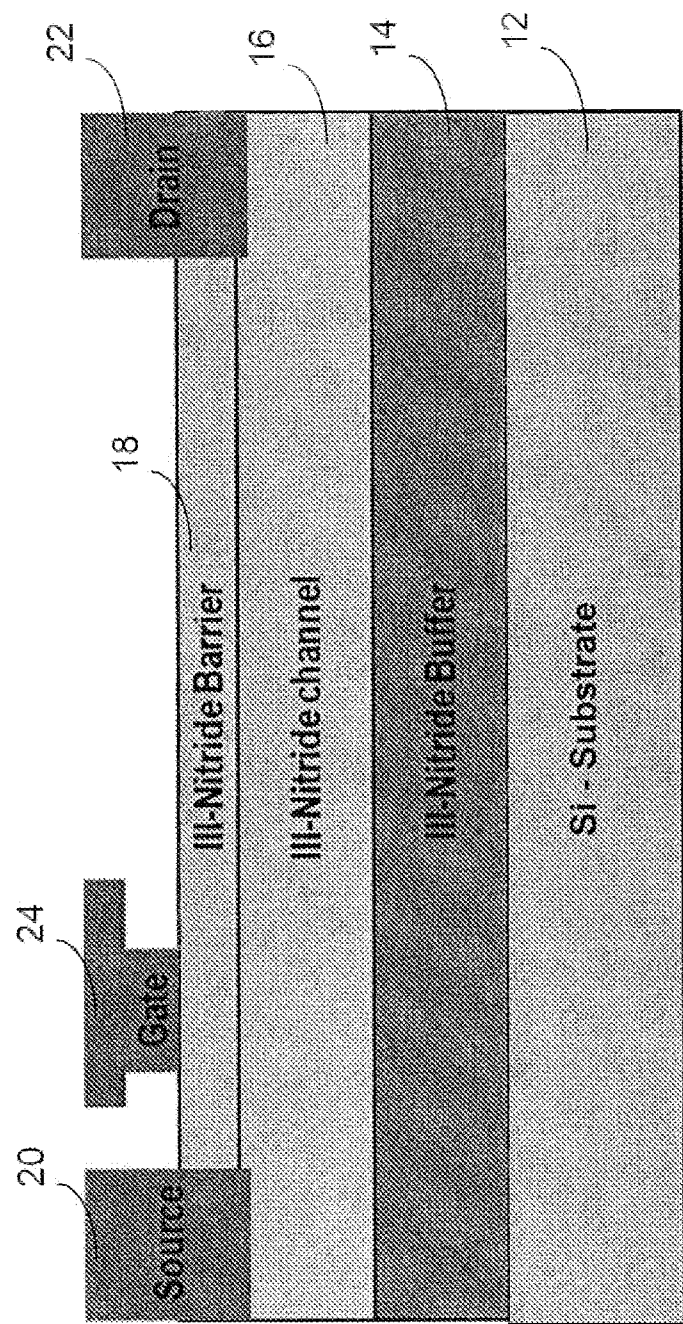


FIG. 2A

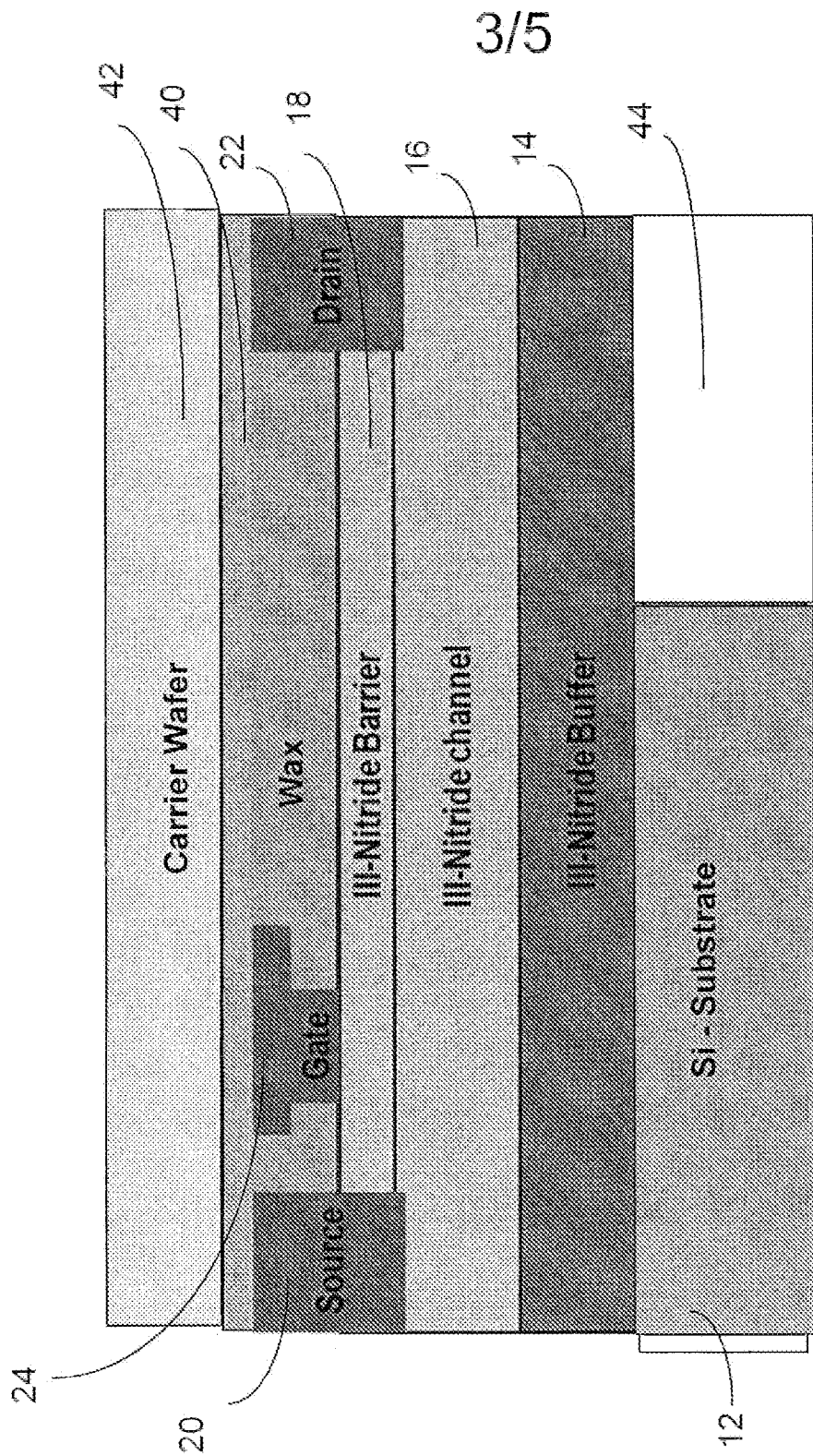


FIG. 2B

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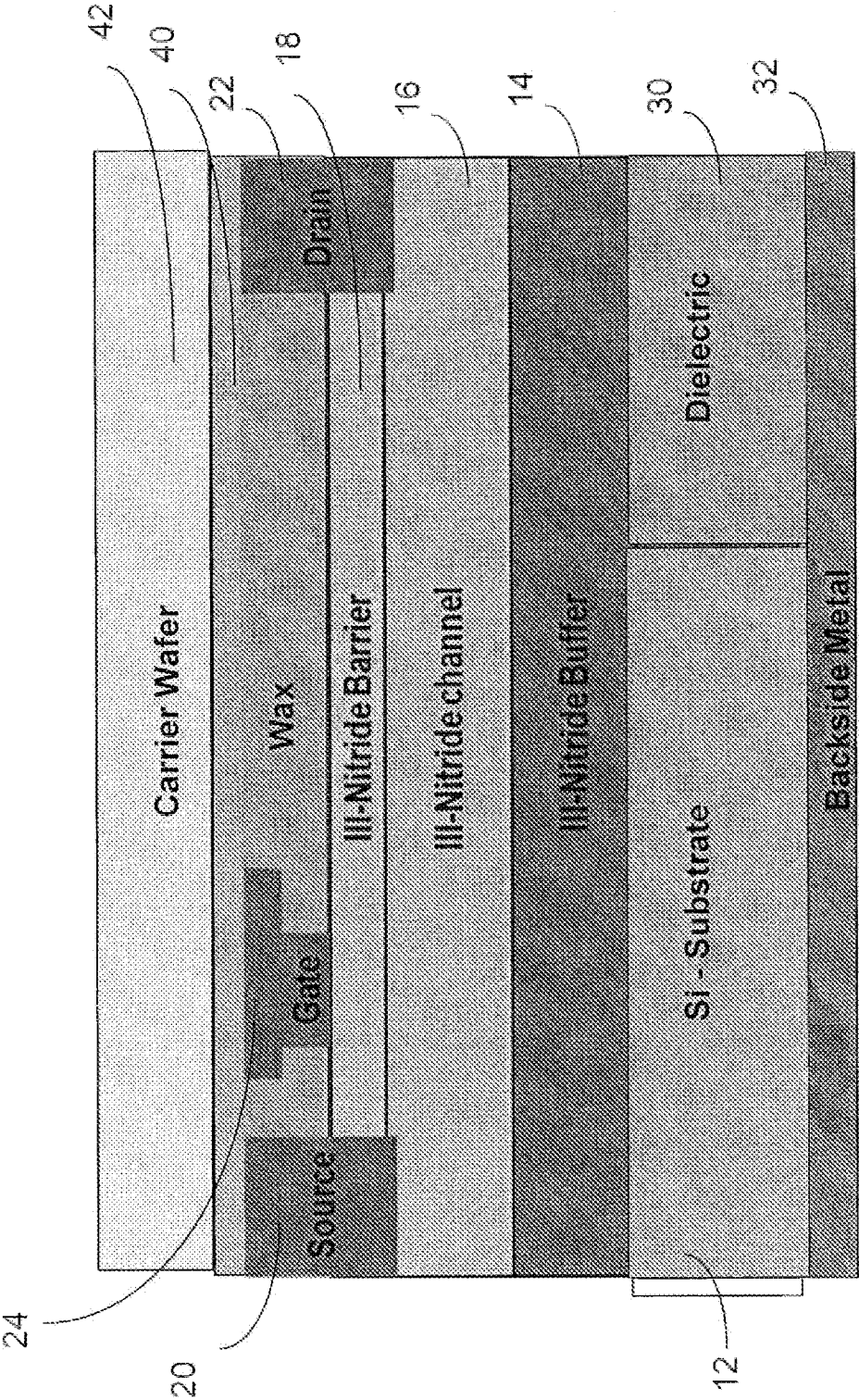


FIG. 2C

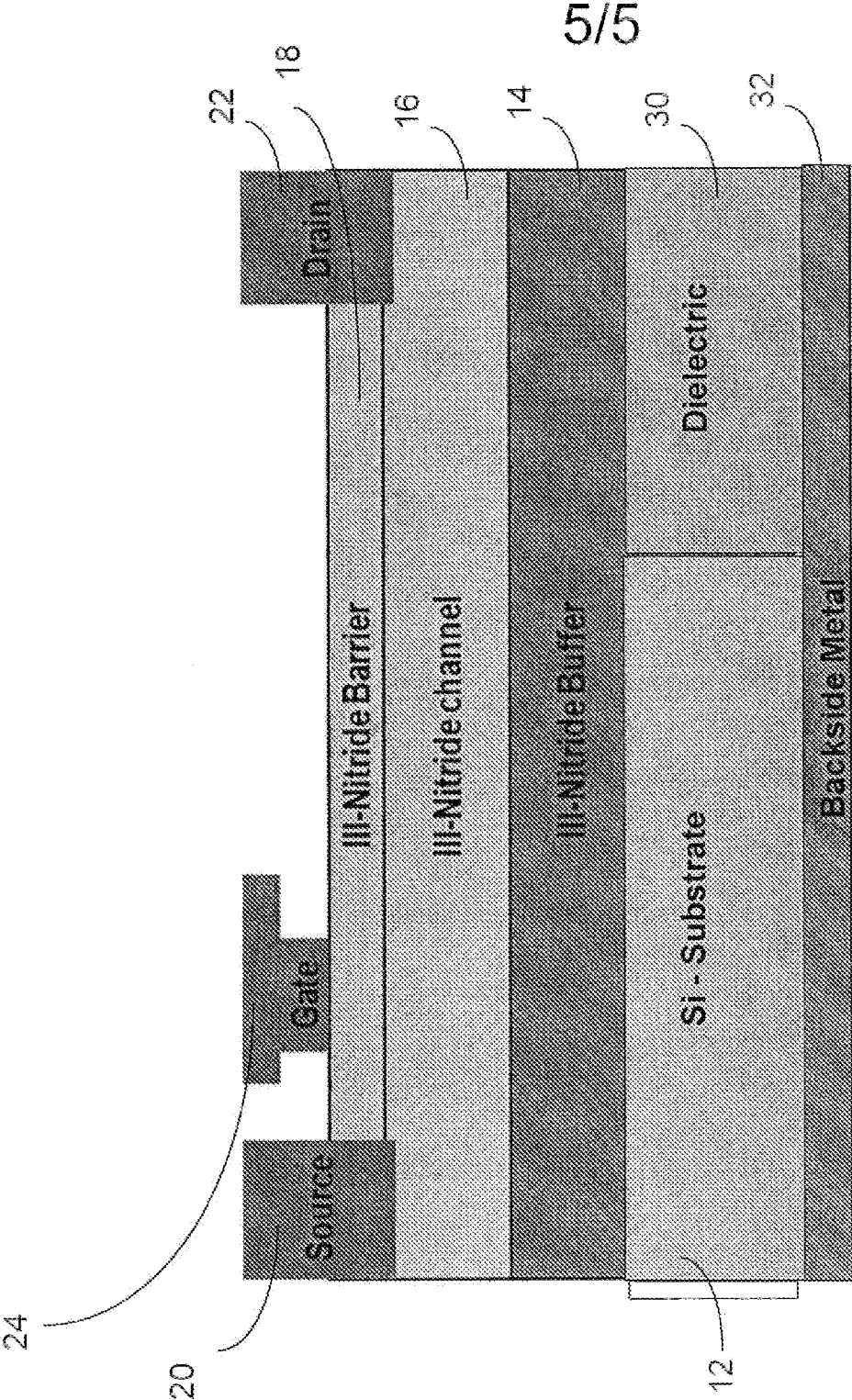


FIG. 2D

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/026776**A. CLASSIFICATION OF SUBJECT MATTER****H01L 29/786(2006.01)i, H01L 21/335(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 29/786; H01L 29/778; H01L 21/331; H01L 31/0312; H01L 29/72; H01L 29/78; H01L 29/40; H01L 29/76; H01L 21/31; H01L 21/335

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: transistor, source, drain, backside metal, dielectric

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	CN 102820325 A (UNIVERSITY OF ELECTRONIC SCIENCE AND TECHNOLOGY OF CHINA) 12 December 2012 See abstract, paragraphs [0029]–[0041], claims 1–10 and figures 1–6.	1–24
A	US 2007–0069216 A1 (JUN KOMIYAMA et al.) 29 March 2007 See abstract, paragraphs [0104]–[0116], claims 1–10 and figure 1.	1–24
A	US 2007–0158692 A1 (TATSUO NAKAYAMA et al.) 12 July 2007 See abstract, paragraphs [0066]–[0085], claims 1–7 and figure 1.	1–24
A	US 2009–0090984 A1 (M. ASIF KHAN et al.) 09 April 2009 See abstract, paragraphs [0029]–[0040], claims 14–24 and figures 1,2	1–24
A	US 2012–0193676 A1 (MADHUR BOBDE et al.) 02 August 2012 See abstract, paragraphs [0046]–[0048], claim 1 and figure 9.	1–24



Further documents are listed in the continuation of Box C.



See patent family annex.

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Date of the actual completion of the international search

30 July 2014 (30.07.2014)

Date of mailing of the international search report

30 July 2014 (30.07.2014)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
CN102820325 A	12/12/2012	None	
US 2007-0069216 A1	29/03/2007	CN 1941405 A FR 2891399 A1 JP 2007-095858 A	04/04/2007 30/03/2007 12/04/2007
US 2007-0158692 A1	12/07/2007	CN 100508212 C CN 101002332 A JP 5084262 B2 US 7859014 B2 WO 2006-001369 A1	01/07/2009 18/07/2007 28/11/2012 28/12/2010 05/01/2006
US 2009-0090984 A1	09/04/2009	US 2013-056796 A1 US 8318562 B2 US 8692293 B2	07/03/2013 27/11/2012 08/04/2014
US 2012-0193676 A1	02/08/2012	CN 102623513 A TW 201232788 A	01/08/2012 01/08/2012