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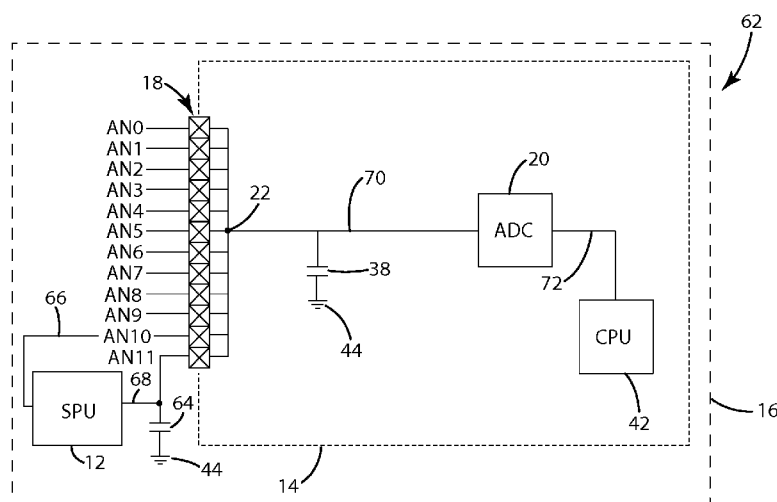
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(54) Title: MICROCONTROLLER MULTIPLEXER PROCESSING



(57) Abstract: Systems and methods for analog signal processing are provided. The systems generally include a microcontroller having a multiplexer and an analog-to-digital converter, and a signal processing unit coupled to the microcontroller and adapted to process the multiplexer output and to provide a processed analog input to the analog-to-digital converter. The methods generally include selecting an analog input signal from among a plurality of analog input signals, processing the selected analog input signal, and converting the processed analog signal into a digital signal. Processing the analog input signal can include sampling, conditioning, filtering, modifying, differentiating, accumulating and combinations thereof. The systems and methods can perform signal processing that might otherwise be performed in digital logic by a microcontroller core processor, simplifying the design of microcontrollers in instances where microcontrollers sample multiple analog signals of the same general type.

MICROCONTROLLER MULTIPLEXER PROCESSING

BACKGROUND OF THE INVENTION

[0001] The present invention relates to systems and methods for signal processing, and in particular, systems and methods for processing analog signals for input to a microcontroller.

[0002] Microcontrollers typically include an analog-to-digital convertor to convert an analog input signal into a digital output signal. The analog input signal can include an analog voltage or an analog current, and the digital output signal can include a digital value proportional to the analog voltage or the analog current for eventual processing by embedded microcontroller software. Many such microcontrollers also include an analog multiplexer for the selection of a desired analog input signal. A typical analog multiplexer can include a data selector that selects one of several analog input signals and forwards the selected analog input signal to the analog-to-digital convertor for processing by embedded microcontroller software.

[0003] In some applications, a microcontroller will sample multiple analog signals of the same type through the analog multiplexer and the analog-to-digital convertor. For example, Fig. 1 illustrates a microcontroller including an analog multiplexer with inputs AN_0 to AN_{11} , an analog-to-digital convertor, and a sample and hold capacitor $C_{S/H}$ coupled between the analog multiplexer and the analog-to-digital convertor. Further by example, Fig. 2 illustrates an analog multiplexer and the analog-to-digital convertor for a PIC16f/LF1824/1828 microcontroller available from Microchip Technology Inc. of Chandler, Arizona. In these examples, the processing of external signals occurs after their conversion into a digital signal by the analog-to-digital convertor. In addition, there is no outside access to the selected analog input signal from either the analog multiplexer or the analog-to-digital convertor. Consequentially, all processing of the external signals is performed by a digital processing unit within the microcontroller.

[0004] There are many applications where multiple analog sensors of the same type need to be sampled and in some cases where it would be very useful to process the analog signal from these sensors where the original analog sensor output is transformed to another value prior to converting to a digital value by the analog-to-digital controller. Examples of this would be filtering, amplifying, differentiating, generating the log of the analog output, etc. It may be possible to do all of these features on the digital signal converted by the analog to digital circuit at the expense of processing by software. Processing by software may not be sufficient or might take too long to adequately process and respond in a sufficient time domain. Therefore utilizing analog processing of these functions using electronic circuits could be beneficial. Often standard industry microcontrollers do not provide access to the output of the analog multiplexer output prior to the input of the analog-to-digital controller as illustrated in Fig. 1 and by specific example Fig. 2.

SUMMARY OF THE INVENTION

[0005] Systems and methods for analog signal processing are provided. In a first aspect of the invention, the system generally includes a microcontroller and a signal processing unit coupled to the microcontroller. The microcontroller includes a multiplexer and an analog-to-digital converter, and the signal processing unit is electrically connected between the multiplexer output and the analog-to-digital converter input. The signal processing unit is adapted to process an analog signal from the multiplexer and is adapted to provide the processed analog signal to the analog-to-digital converter for further processing by the microcontroller.

[0006] In one embodiment, the microcontroller includes a plurality of multiplexer input channels. The signal processing unit is electrically coupled to a selected multiplexer input channel and is adapted to process an electrical output of the selected multiplexer input channel. The processed electrical output is applied to the analog-to-digital converter,

optionally through the multiplexer, to generate a digital output for digital signal processing by a core processing unit associated with the microcontroller.

[0007] In another embodiment, the signal processing unit includes a sampling capacitor, a low pass filter, a high pass filter and/or a band pass filter. The microcontroller optionally includes an amplifier electrically coupled between the plurality of selectable input channels and the output port. Still further optionally, the microcontroller includes a sample and hold capacitor electrically coupled between the analog signal processing unit and the analog-to-digital converter.

[0008] In still another embodiment, the signal processing unit is adapted to provide an analog output based on a comparison between a first multiplexer input and a second multiplexer input. The first and second multiplexer inputs are optionally sampled simultaneously with each other. The signal processing unit can include a differential amplifier having an output coupled to the microcontroller analog-to-digital converter. The analog-to-digital converter provides an output for digital signal processing by a core processing unit associated with the microcontroller.

[0009] In a second aspect of the invention, the method generally includes selecting an analog input signal from among a plurality of analog input signals, processing the selected analog input signal, and converting the processed analog signal into a digital signal. The step of processing the analog input signal is performed by a signal processing unit separate from a microcontroller, which performs the steps of selecting the pre-processed analog input signal and converting the processed analog input signal into a digital signal. The method optionally includes processing the digital signal using a digital signal processor, wherein the multiplexer, the analog-to-digital converter, and the digital signal processor form part of a common microcontroller.

[0010] In one embodiment, processing the selected analog input signal includes sampling, modifying and/or conditioning the selected analog input signal. Further optionally,

processing the analog input signal includes amplifying the selected analog input signal. Still further optionally, processing the selected analog signal includes differentiating the selected analog input signal or signals. Even further optionally, processing the selected analog signal includes generating a log of the selected analog input signal.

[0011] In another embodiment, the method includes providing a microcontroller having a multiplexer and an analog-to-digital converter and providing a signal processing unit separate from the microcontroller. The method further includes simultaneously sampling, using the multiplexer, first and second analog input signals, generating, using the signal processing unit, a differential output signal based on a comparison between the first and second analog input signals, and converting, using the analog-to-digital converter, the differential output signal into a digital signal for further processing by the microcontroller.

[0012] The above systems and methods can therefore perform analog signal processing that might otherwise be performed in digital logic by a microcontroller, for example a microcontroller core processor. In particular, signal processing is instead performed by a signal processing unit external to the microcontroller, freeing the microcontroller to perform other processes and simplifying the design of microcontrollers in instances where microcontrollers sample multiple analog signals of the same general type.

[0013] These and other features and advantages of the present invention will become apparent from the following description of the invention, when viewed in accordance with the accompanying drawings and appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Fig. 1 is a circuit diagram illustrating a first prior art microcontroller including a multiplexer and an analog to digital converter.

[0015] Fig. 2 is a circuit diagram illustrating a second prior art microcontroller including a multiplexer and an analog to digital converter.

[0016] Fig. 3 is a circuit diagram illustrating a signal processing system in accordance with a first embodiment of the invention.

[0017] Fig. 4 is a flow-chart illustrating operation of the signal processing system depicted in Fig. 3.

[0018] Fig. 5 is a circuit diagram illustrating a signal processing system in accordance with a second embodiment of the invention.

[0019] Fig. 6 is a flow-chart illustrating operation of the signal processing system depicted in Fig. 5.

[0020] Fig. 7 is a circuit diagram illustrating a signal processing system in accordance with a third embodiment of the invention.

[0021] Fig. 8 is a first flow-chart illustrating operation of the signal processing system depicted in Fig. 7.

[0022] Fig. 8 is a second flow-chart illustrating operation of the signal processing system depicted in Fig. 7.

[0023] Fig. 10 is a first timing diagram illustrating voltage versus time for the sample and storage capacitor depicted in Fig. 8.

[0024] Fig. 11 is a second timing diagram illustrating voltage versus time for the sample and storage capacitor depicted in Fig. 8.

[0025] Fig. 12 is a timing diagram illustrating voltage versus time for the sample and storage capacitor depicted in Fig. 9.

[0026] Fig. 13 is a circuit diagram illustrating a signal processing system in accordance with a fourth embodiment of the invention.

[0027] Fig. 14 is a circuit diagram illustrating a signal processing system in accordance with a fifth embodiment of the invention.

DETAILED DESCRIPTION OF THE CURRENT EMBODIMENT

[0028] The invention as contemplated and disclosed herein includes systems and methods for analog signal processing. As set forth below, the systems and methods generally include selecting an analog input signal from among a plurality of analog input signals, processing the selected analog input signal, and converting the processed analog signal into a digital signal for further processing by a microcontroller. Selecting an analog signal and converting an analog signal are generally performed by a microcontroller, and the intermediate step of processing the selected analog signal is generally performed by a signal processing unit external to and electrically connected to the microcontroller.

[0029] Referring now to Fig. 3, a signal processing system in accordance with a first embodiment of the present invention is illustrated and generally designated 10. The signal processing system 10 generally includes a signal processing unit 12 and a microcontroller 14. The signal processing unit 12 is generally separate from the microprocessor 14 in the present embodiment, which collectively form part of an integrated circuit 16, for example an application specific integrated circuit (ASIC). In addition, the signal processing unit 12 includes analog or digital circuitry adapted to accept an analog input signal and provide an analog output signal. The analog output signal can include a sampled signal, a conditioned signal, a modified signal, a differentiated signal, an accumulated signal, and/or a filtered signal, optionally for subsequent conversion into a digital signal by an analog-to-digital converter associated with the microcontroller 14.

[0030] As also shown in Fig. 3, the microcontroller 14 includes a multiplexer 18 and an analog-to-digital converter 20. Functionally, the multiplexer 18 is adapted to select an analog input signal from among a plurality of analog input signals, and the analog-to-digital converter 20 is adapted to convert an analog input signal into a digital signal that is representative of the analog input signal. More particularly, the multiplexer 18 includes a plurality of input channels, labeled $AN_0, AN_1 \dots AN_{11}$ in Fig. 3, and an output 22. The

microcontroller 14 additionally includes a first signal path 24 from the multiplexer output 22 to a microcontroller output port 26. The microcontroller output port 26 is coupled to the signal processing unit 12, and in particular, an input terminal 28 of the signal processing unit 12. The microcontroller 14 additionally includes a microcontroller input port 30 coupled to the signal processing unit 12, and in particular, an output terminal 32 of the signal processing unit 12. A second signal path 34 connects the input port 30 to the analog-to-digital converter 20. The microcontroller 14 can include a buffer, for example a unity gain buffer, along the first signal path 24. The microcontroller 14 can further include a sample and hold capacitor 38 or $C_{S/H}$ connected between the second signal path 34 and ground 44. The microcontroller 14 includes a third signal path 40 to electrically connect the analog-to-digital converter output to a core processor 42 associated with the microcontroller 14, the core processor 42 being programmed with a series of instructions that, when executed, cause the core processor 42 to perform desired method steps based ultimately on the multiplexer input.

[0031] Operation of the system of Fig. 3 generally includes a) selecting, using the multiplexer 18, an analog input signal from among a plurality of analog input signals, b) processing, using the signal processing unit 12, the selected analog input signal to generate a processed analog output signal, c) converting, using the analog-to-digital converter, the processed analog output signal into a digital signal that is representative of the processed analog input signal, and d) further processing, using the core processor 42, the digital signal from the analog-to-digital converter 20. As the term is used herein, processing an analog signal includes, without limitation, sampling, modifying, accumulating, conditioning, differentiating, filtering, and/or generating a log plot of the analog signal, optionally for subsequent conversion by an analog-to-digital converter.

[0032] More particularly, and with reference to Fig. 4, operation of the system 10 of Fig. 3 includes deselecting all channels of the analog multiplexer 18 at step 50. The sample and hold capacitor 38 is discharged at step 52 and the desired analog multiplexer channel is

then selected at step 54. At this point, the output of the analog multiplexer 18 is available for processing outside of the microcontroller 14. The output of the analog multiplexer 18 is processed at step 56, where the processing is performed by the signal processing unit 12 using analog or digital circuitry. At step 58, the processed signal is converted by the analog-to-digital converter 20 into a digital signal for further processing by the core processor 42 at step 58. The method then returns to step 50 for a different one of the plurality of the multiplexer input channels. In this regard, the processing of the selected analog signal by external circuitry 12 prior to converting to a digital format can save time and perhaps other processing that is not best suited for software.

[0033] A signal processing system in accordance with a second embodiment of the present invention is illustrated in Fig. 5 and generally designated 62. The signal processing system 62 is functionally similar to the signal processing system of Fig. 3, and is adapted to selectively forward the multiplexer output to the signal processing unit 12 for analog processing or to the analog-to-digital converter 20 for digital processing. In particular, the signal processing system 62 includes a signal processing unit 12 coupled to two of the plurality of multiplexer channels, AN_{10} , AN_{11} , and further includes a sample and storage capacitor 64 or $C_{S/S}$. A first signal path 66 extends between channel AN_{10} and the signal processing unit 12, and a second signal path 68 extends between the signal processing unit 12 and channel AN_{11} of the multiplexer 18. The sample and storage capacitor 64 is connected between the second signal path 68 and ground 44 to temporarily store the processed analog signal. A third signal path 70 extends between the multiplexer output 22 and the analog-to-digital converter 20, and the above mentioned sample and hold capacitor 38 is connected between the third signal path 70 and ground 44. A fourth signal path 72 couples the output of the analog-to-digital converter 20 to the core processor 42. The signal processing system 62 can provided an added degree of flexibility over the signal processing system 10 of Fig. 3 in

that the multiplexer output 22 can be directed through the signal processing unit 12 and can alternatively bypass the signal processing unit 12.

[0034] Operation of the signal processing system 62 can include the following method as generally set forth below in connection with Fig. 6. Beginning at step 72, the multiplexer channels AN_1 , AN_2 ... AN_{11} are deselected. At step 76, the sample and hold capacitor 38 and the sample and storage capacitor 64 are discharged. At step 78, the desired analog multiplexer channel is selected and the corresponding analog signal is forwarded to the sample and hold capacitor 38. Where immediate digital processing is desired, the analog-to-digital converter 20 can convert the analog signal into a digital signal for processing by the core processing unit 42. Where analog pre-processing is desired, the multiplexer channels are deselected and channel AN_{10} is opened to the signal processing unit 12 at step 80. At step 82, the analog value is processed by the signal processing unit 12, and at step 86, the processed analog value is forwarded to the sample and storage capacitor 64. The analog voltage stored to the sample and storage capacitor 64 can be determined according to the formula $V_{s/s} = V_{s/h} * [C_{s/h} / (C_{s/h} + C_{s/s})]$. At step 86, the multiplexer channel associated with the sample and storage capacitor 64 is selected (channel AN_{11}), and the processed analog value is forwarded to the sample and hold capacitor 38. At step 88, the analog-to-digital converter 20 converts the processed analog signal to a digital signal. At step 90, the digital signal is processed in software within the microcontroller, optionally within the core processing unit 42. The method then returns to step 74 for a different one of the plurality of the multiplexer input channels or for the same multiplexer channel a period of time later. In addition, the voltage on the sample and storage capacitor 64 can be discharged on each sample cycle or the voltage on the sample and storage capacitor 64 can be allowed to hold its charge through repeated sampling cycles. Similarly, the signal processing unit 12 can be designed to respond to each sample on each cycle or can be designed to respond to repeated

samples over a longer period, including samples from different ones of the available multiplexer channels.

[0035] A signal processing system in accordance with a third embodiment of the present invention is illustrated in Fig. 7 and generally designated 92. The signal processing system 92 is structurally and functionally similar to the signal processing system of Fig. 5, with the signal processing unit 12 including a low-pass filter coupled between the analog multiplexer 18 and the analog-to-digital converter 20. In particular, the low-pass filter 12 includes a resistor 94 electrically connected in series with the multiplexer channel AN_{11} . In addition, the low-pass filter 12 includes a sample and storage capacitor 96 connected in series with ground 44. In use, the low-pass filter 12 passes low frequency analog signals to the analog-to-digital converter 20 and attenuates higher frequency analog signals, effectively preventing their transfer to the analog-to-digital converter 20. Alternatively, the multiplexer output can bypass the signal processing unit 12 for immediate conversion and digital processing by the microcontroller core processing unit 42, for example when filtering is not desired, substantially as set above in connection with Fig. 5.

[0036] The sequence of sampling a given constant input voltage and performing a resultant conversion using the system of Fig. 7 can include the following method as generally set forth in Fig. 8. At step 98, all multiplexer channels are deselected and at step 100 the sample and hold capacitor 38 and the sample and storage capacitor 96 are discharged. At step 102, the desired multiplexer channel is selected and an analog value is forwarded to the sample and hold capacitor 38. Where immediate digital processing is desired, the analog-to-digital converter 20 can convert the analog signal into a digital signal for processing by the core processing unit 42. Where analog filtering is desired, the multiplexer channels are deselected and channel AN_{10} is opened to the low-pass filter 12 at step 104. The maximum voltage stored to the sample and storage capacitor 96 is determined according to the following formula: $V_{s/s} = V_s/h * [Cs/h / (Cs/h + Cs/s)]$. The maximum voltage that the sample

and storage capacitor 96 can charge to over one sample cycle is equal to $[V_s/h - V_{s/s}] * [1 - e^{-(t/(R * (C_{s/s} || C_{s/h})))}]$ where t is the time that channel AN_{11} is on. At step 106, the multiplexer channels are deselected and step 104 is repeated to allow the sample and storage capacitor 96 to charge up in a desired response time. At step 106, the multiplexer channel associated with the sample and storage capacitor 96 is selected (channel AN_{11}), and the accumulated voltage value is forwarded to the sample and hold capacitor 38. At step 108, the analog-to-digital converter 20 converts the filtered signal into a digital signal. At step 110, the digital signal is processed in software within the microcontroller, optionally within the core processing unit 42. The method then returns to step 98 for a different one of the plurality of the multiplexer input channels or for the same multiplexer channel some time later. Fig. 10 illustrates the effect of the low-pass filter 12 during the cycle time t , as well as the effect of repeated cycles of sampling and storing the analog signal at the sample and storage capacitor 96. Figure 11 similarly illustrates the analog signal voltage at the sample and storage capacitor 96 for an increased low-pass filter resistor value.

[0037] Another sequence of sampling a given constant input voltage and performing a resultant analog-to-digital conversion using the system of Fig. 7 can include the following method as generally set forth in Fig. 9. At step 112, all multiplexer channels $AN_1, AN_2 \dots AN_{11}$ are deselected. At step 114, the sample and hold capacitor 38 and the sample and storage capacitor 96 are discharged. At step 116, the desired multiplexer channel is selected and an analog value is forwarded to the sample and hold capacitor 38. At step 118 the selected multiplexer channel is closed and channel AN_{10} is opened to the low-pass filter 12. The maximum voltage stored to the sample and storage capacitor 96 is determined according to the following formula: $V_{s/s} = V_s/h * [C_{s/h} / (C_{s/h} + C_{s/s})]$. The maximum voltage that the sample and storage capacitor 96 can charge to over one sample cycle is equal to $[V_s/h - V_{s/s}] * [1 - e^{-(t/(R * (C_{s/s} || C_{s/h})))}]$ where t is the time that channel AN_{11} is on. At step 120, multiplexer channel AN_{11} is selected, and the processed voltage value is forwarded to the

sample and hold capacitor 38. At step 122, the analog-to-digital converter converts the processed signal to a digital signal. At step 124, the digital signal is processed in software within the microcontroller, optionally within the core processing unit 42. The method then returns to step 112 for a different one of the plurality of the multiplexer input channels or for the same multiplexer channel.

[0038] In the above sequence, the low-pass filter is permitted to process the analog signal during a time t . Fig. 12 illustrates this sequence where the same channel is repeatedly sampled and converted to a digital value to be processed in software, optionally by the core processor 42. The signal processing unit 12 can additionally or alternatively include circuitry other than low-pass filters. For example, the signal processing unit 12 can include amplifiers, differentiators, log converters, square root extractors, and combinations of the same. The signal processing unit 12 can additionally buffer the sample and storage capacitor output to prevent the analog value from discharging during the processing time (high impedance buffering). In addition, more than one signal processing unit can be implemented. By using available multiplexer channels, multiple processing units can be implemented in which any of the other multiplexer channels can be routed to the relevant sample and storage capacitors. Using multiple sample and storage capacitors, the microcontroller could then performing differential processing of analog input signals.

[0039] A signal processing system in accordance with a fourth embodiment of the present invention is illustrated in Fig. 13 and generally designated 130. The signal processing system 130 of Fig. 13 is structurally and functionally similar to the signal processing system 62 of Fig. 5, with the signal processing system 130 being further adapted to compare the output of any two of the multiplexer input channels $AN_0, AN_1 \dots AN_7$. In particular, the signal processing unit 12 includes a differential amplifier 132 adapted to generate a differential output signal based on a comparison between any two of the multiplexer input channels $AN_0, AN_1 \dots AN_7$ prior to digital signal processing in the core

processor unit 42. In addition, the signal processing system 130 includes a first buffer 134 between the first multiplexer output channel AN_9 and the differential amplifier 132 and a second buffer 136 between the first multiplexer output channel AN_8 and the differential amplifier 132. First and second buffers 134, 136 are shown as unity gain amplifiers in the present embodiment, but can be configured with gain in other embodiments.

[0040] In operation, the selected differential input pair (AN_0/AN_1 , AN_2/AN_3 , AN_4/AN_5 or AN_6/AN_7) is selectively routed to the plus-input sample and storage capacitor ($C_{S/S+}$) 138 and to the minus-input sample and storage capacitor ($C_{S/S-}$) 140. In particular, a first input signal at desired one of multiplexer input channels AN_0 , AN_2 , AN_4 and AN_6 is forwarded to the sample and hold capacitor 38 and then to the plus-input sample and storage capacitor 138 substantially set forth in connection with Fig. 5 above. A second input signal at a desired one of multiplexer input channels AN_1 , AN_3 , AN_5 and AN_7 is forwarded to the sample and hold capacitor 38 and then to the minus-input sample and storage capacitor 140 substantially set forth in connection with Fig. 5 above. Multiplexer channel AN_{10} accepts a buffered signal from the minus-input buffer 134 and multiplexer channel AN_{11} accepts a buffered signal from the plus-input buffer 136. Multiplexer channel AN_{12} , when sampled, includes the output of the differential amplifier 132. As also shown in Fig. 13, the output of the minus-input buffer 134 is the inverting input to the differential amplifier 132 and the output of the plus-input buffer 136 is the non-inverting input of the differential amplifier 132. The signal processing system 130 is therefore adapted to determine a differential input either by determining, in microcontroller digital logic, the difference between the values measured at channel AN_{11} and AN_{10} , or by measuring the analog value at channel AN_{12} . Where the differential input is derived by the microcontroller 14 using the signals at channels AN_{10} and AN_{11} , the differential input can be determined according to the formula $K_1 * AN_{11} - K_2 * AN_{10}$, wherein K_1 and K_2 are the gain values of the first and second buffers 134, 136 and where AN_{11} and AN_{10} are the voltages related to the $C_{S/S+}$ and $C_{S/S-}$ respectively. Where the

differential input is derived by the signal processing unit 12, the differential input can be determined according to the formula $K \cdot (V_{in}^+ - V_{in}^-)$, where K is the gain value of the differential amplifier 132, V_{in}^+ is the voltage at the non-inverting input, V_{in}^- is the voltage at the inverting input, and assuming no gain at the input amplifiers 134, 136.

[0041] A signal processing system in accordance with a fifth embodiment of the present invention is illustrated in Fig. 14 and generally designated 150. The signal processing system 150 of Fig. 14 is structurally and functionally similar to the signal processing system 130 of Fig. 13, with the signal processing system 150 being further adapted to measure simultaneous differential inputs, rather than sequential differential inputs. In particular, the signal processing system 150 is adapted to generate a differential output signal based on a comparison between a first signal at multiplexer input channel AN_{10} , AN_{11} ... or AN_{18} and a second signal at multiplexer input channel AN_{20} , AN_{21} ... or AN_{28} . In addition, the signal processing system 150 includes a microcontroller 14 having first and second sample and hold capacitors 152, 154 and first and second analog-to-digital converters 156, 158 to assist in measuring the difference between the simultaneously sampled signals in digital logic.

[0042] In operation, an input signal from multiplexer input channel AN_{10} , AN_{11} ... or AN_{18} is sampled by the first sample and hold capacitor 152 and an input signal from multiplexer input channel AN_{20} , AN_{21} ... or AN_{28} is sampled by the second sample and hold capacitor 154. The sampling of the selected input signals occurs simultaneously or substantially simultaneously with one another, optionally to improve common mode rejection of signals such as that attributed to electrical noise and changes in temperature, etc.. The sampled signals, e.g., voltage values, are then forwarded through channels AN_{1A} and AN_{29} to the signal processing unit 12. In particular, the sampled signal from the first sample and hold capacitor 152 is routed through channel AN_{1A} to the minus-input sample and storage capacitor ($C_{S/S-}$) 140, and the sampled signal from the second sample and hold capacitor 154

is routed through channel AN_{29} to the plus-input sample and storage capacitor ($C_{S/S+}$) 138. Each stored signal is forwarded through respective buffer amplifiers 134, 136 to the inverting input or non-inverting input of the differential amplifier 132. Multiplexer channel AN_{1B} accepts a buffered signal from the minus-input buffer 134 and multiplexer channel AN_{2A} accepts a buffered signal from the plus-input buffer 136. Multiplexer channel AN_{2A} , when sampled, includes the output of the differential amplifier 132. The signal processing system 130 is adapted to determine the differential input either by determining, in microcontroller digital logic, the difference between the values measured at channels AN_{1B} and AN_{2A} , or by measuring the analog value at channel AN_{2B} .

[0043] To reiterate, the multiplexer 18 includes multiple input channel pairings which, when selected, are simultaneously sampled for comparison in the signal processing unit 12. The channel pairings include minus inputs ($CH0-$, $CH1-$... $CH8-$) and positive inputs ($CH0+$, $CH1+$... $CH8+$), where any one minus input can be paired with any one positive input. The differential input can be derived by measuring the minus and positive inputs separately and then computed by digital signal processing in the microcontroller 14. Alternatively, the differential input can be computed by analog signal processing within the signal processing unit 12. In addition, the channel pairings can be sampled and forwarded directly to the analog-to-digital converters 156, 158, bypassing the signal processing unit 12 where analog signal processing is not desired. In this regard, the present invention provides added versatility by selectively using the external signal processing unit 12 substantially only when beneficial to do so.

[0044] Embodiments of the present invention can be used as a standalone device or embedded into a machine or a system. For example, embodiments of the present invention can be used connection with an electronic device which executes a series of commands representing one or more method steps. The electronic device can be generally programmed with a series of instructions that, when executed, cause the electronic device to perform

certain method steps. The instructions that are performed by the electronic device are generally stored in computer readable media. The computer readable media can be a portable memory device that is readable by the electronic device. Such portable memory devices can include a compact disk, a digital video disk, a flash drive, and any other disk readable by a disk driver embedded or externally connected to a computer, a memory stick, or any other portable storage medium whether now known or hereinafter developed. Alternatively, the computer readable media can be an embedded component of the electronic device, such as a hard disk or a flash drive. In addition, while the signal processing system is described above as including a microcontroller, the signal processing system can be implemented using essentially any controller having a multiplexer and an analog-to-digital converter, whether now known or hereinafter developed. Example controllers include, for example, programmable logic controllers, microprocessors, integrated circuits, field programmable gate arrays, and application specific integrated circuits.

[0045] The above description is that of current embodiments of the invention. Various alterations and changes can be made without departing from the spirit and broader aspects of the invention as defined in the appended claims, which are to be interpreted in accordance with the principles of patent law including the doctrine of equivalents. This disclosure is presented for illustrative purposes and should not be interpreted as an exhaustive description of all embodiments of the invention or to limit the scope of the claims to the specific elements illustrated or described in connection with these embodiments. Any reference to elements in the singular, for example, using the articles “a,” “an,” “the,” or “said,” is not to be construed as limiting the element to the singular.

CLAIMS

1. A microcontroller comprising:
a multiplexer to receive a plurality of analog signals and provide an analog output;
an analog-to-digital converter to provide a signal for digital signal processing; and
an output terminal coupled to the multiplexer analog output and an input terminal coupled to the analog-to-digital converter, wherein the output and input terminals are coupleable to a signal processing unit separate from the microcontroller and adapted to process the multiplexer output and adapted to provide an analog input to the analog-to-digital converter.
2. The microcontroller of claim 1 wherein the multiplexer includes a plurality of channels, the input terminal comprising one of the plurality of multiplexer channels.
3. The microcontroller of claim 1 wherein the multiplexer includes a plurality of channels separate from the input and output terminals.
4. The microcontroller of claim 1 further including an amplifier electrically coupled between the multiplexer and the output terminal.
5. The microcontroller of claim 1 further including a sample and hold capacitor electrically connected between the multiplexer and the analog-to-digital converter.
6. A method for processing an analog signal, the method comprising:
selecting, using a multiplexer, an analog input signal from among a plurality of analog input signals;
processing, using a signal processing unit, the selected analog input signal to generate a processed analog output signal;
converting, using an analog-to-digital converter, the processed analog output signal into a digital signal that is representative of the processed analog output signal; and
processing the digital signal using a digital processor, wherein the multiplexer, the analog-to-digital converter, and the digital processor form part of a microcontroller, and wherein the signal processing unit is external to the microcontroller.

7. The method according to claim 6 wherein processing the selected analog input signal includes filtering the selected analog input signal.

8. The method according to claim 6 wherein processing the selected analog input signal includes amplifying the selected analog input signal.

9. The method according to claim 6 wherein processing the selected analog input signal includes differentiating the selected analog input signal.

10. The method according to claim 6 wherein processing the selected analog input signal includes generating a log of the selected analog input signal.

11. The method according to claim 6 wherein processing the selected analog input signal includes modifying the selected analog input signal.

12. The method according to claim 6 wherein processing the selected analog input signal includes conditioning the selected analog input signal.

13. The method according to claim 6 further including selectively bypassing the signal processing unit to convert a second analog input signal into a second digital signal for processing by the digital processor.

14. A signal processing system comprising:

a signal processing unit; and

a microcontroller including:

a multiplexer,

an analog-to-digital converter,

a first signal path from the multiplexer to the signal processing unit, and

a second signal path from the signal processing unit to the analog-to-digital converter;

wherein the signal processing unit is adapted to process an analog signal from the first signal path and to provide an analog input to second signal path.

15. The signal processing system of claim 14 wherein the signal processing unit includes an analog signal processor.

16. The signal processing system of claim 15 wherein the analog signal processing unit includes a sample and storage capacitor.

17. The signal processing system of claim 15 wherein the analog signal processing unit includes a low pass filter.

18. The signal processing system of claim 15 wherein the analog signal processing unit includes a differential amplifier.

19. The signal processing system of claim 14 wherein the signal processing unit includes a digital signal processor.

20. The signal processing system of claim 14 wherein the first signal path includes at least one of an amplifier and a buffer.

21. A signal processing system comprising:

a multiplexer including a plurality of selectable input channels and an output port electrically coupled to the plurality of selectable input channels;

a signal processing unit electrically coupled to the multiplexer output port, the signal processing unit being adapted to process an analog signal at the multiplexer output port; and

an analog-to-digital converter electrically coupled to the signal processing unit and adapted to generate a digital signal representative of the processed analog signal,

wherein the multiplexer and the analog-to-digital converter are formed on a common microcontroller and wherein the processing unit is separate from the microcontroller.

22. The signal processing system of claim 20 wherein the signal processing unit includes an analog signal processor.

23. The signal processing system of claim 21 wherein the analog signal processing unit includes a sample and storage capacitor.

24. The signal processing system of claim 21 wherein the analog signal processing unit includes a low pass filter.

25. The signal processing system of claim 21 wherein the analog signal processing unit includes a differential amplifier.

26. The signal processing system of claim 20 wherein the signal processing unit includes a digital signal processor.

27. The signal processing system of claim 21 further including an amplifier electrically coupled between the plurality of selectable input channels and the output port.

28. The signal processing system of claim 21 further including a sample and hold capacitor electrically connected between the signal processing unit and the analog-to-digital converter.

29. A signal processing system comprising:

a multiplexer including a plurality of selectable input channels adapted to receive a corresponding plurality of input signals;

a signal processing unit adapted to generate a differential output signal based on two of the plurality of input signals; and

a first analog-to-digital converter electrically coupled to the signal processing unit and adapted to generate a digital signal representative of the differential output signal,

wherein the multiplexer and the analog-to-digital converter are components of a microcontroller and wherein the signal processing unit is separate from the microcontroller.

30. The signal processing system of claim 29 wherein the two of the plurality of input signals are sampled simultaneously with each other.

31. The signal processing system of claim 29 wherein the signal processing unit includes a differential amplifier and first and second sample and storage capacitors.

32. The signal processing system of claim 31 further including first and second buffers coupled between the first and second sample and storage capacitors and the differential amplifier.

33. The signal processing system of claim 29 wherein the microcontroller includes first and second sample and hold capacitors coupled to the multiplexer and adapted to simultaneously sample the two of the plurality of input signals.

34. The signal processing system of claim 33 wherein the differential amplifier includes an output coupled to one of the first and second sample and hold capacitors.

35. A method for processing an analog signal, the method comprising:

providing a microcontroller including a multiplexer and an analog-to-digital converter and providing a signal processing unit separate from the microcontroller;

sampling first and second input signals from among a plurality of multiplexer input signals;

generating, using the signal processing unit, a first differential output signal based on the first input signal and the second input signal; and

converting, using the analog-to-digital converter, the first differential output signal into a first digital signal that is representative of the first differential output signal.

36. The method according to claim 35 wherein the first and second input signals are sampled simultaneously with one another.

37. The method according to claim 35 further including buffering the first and second input signals.

38. The method according to claim 35 further including:

Sampling third and fourth input signals from among the plurality of multiplexer input signals;

generating, using the signal processing unit, a second differential output signal based on the third input signal and the fourth input signal; and

converting, using the analog-to-digital converter, the second differential output signal into a digital signal that is representative of the second differential output signal.

39. The method according to claim 38 wherein the third and fourth input signals are sampled simultaneously with one another.

40. The method according to claim 38 further including buffering the third and fourth input signals.

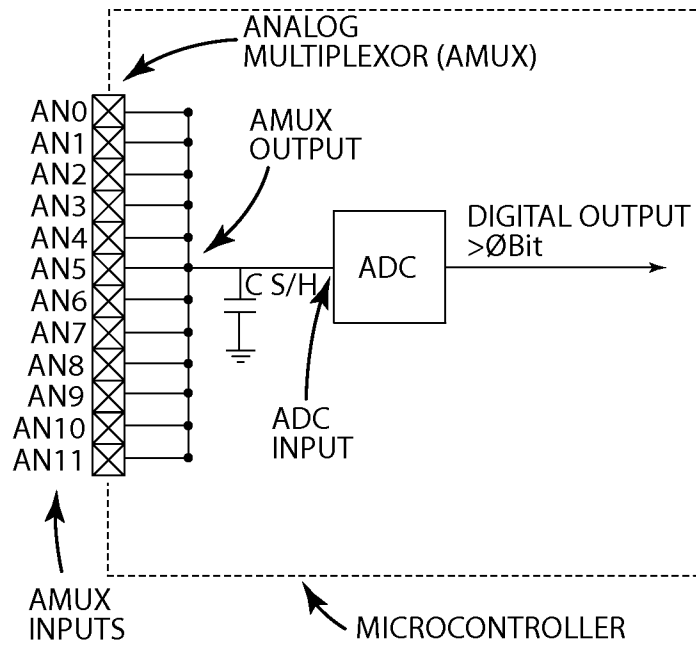


Fig. 1 (Prior Art)

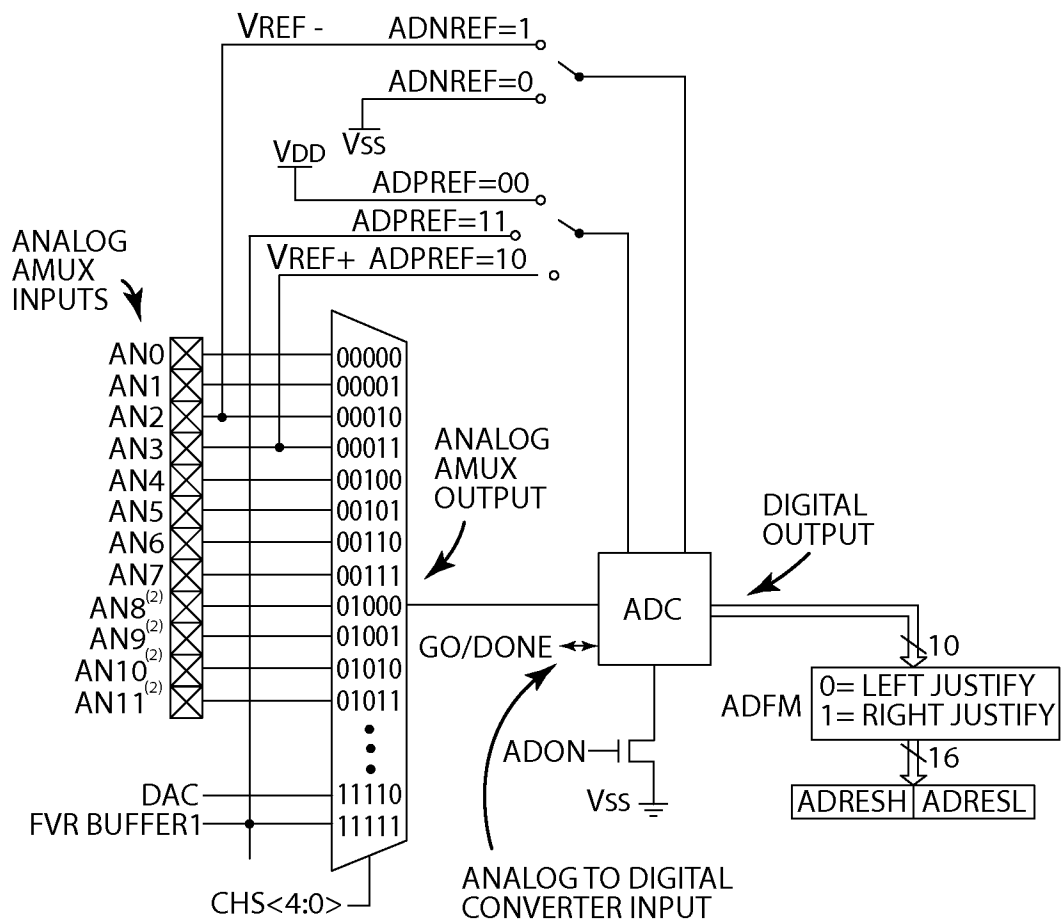
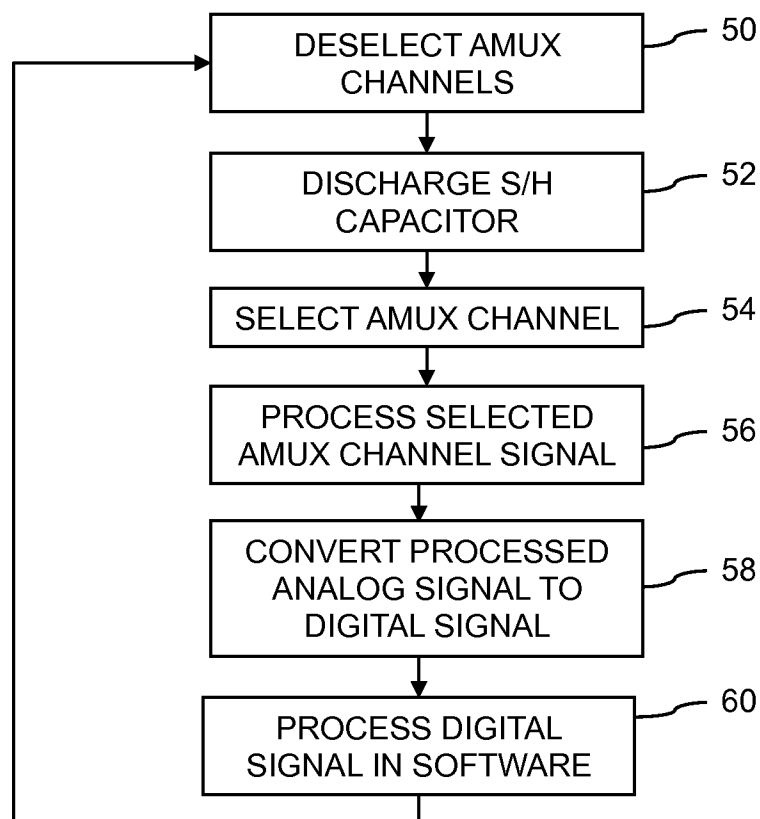
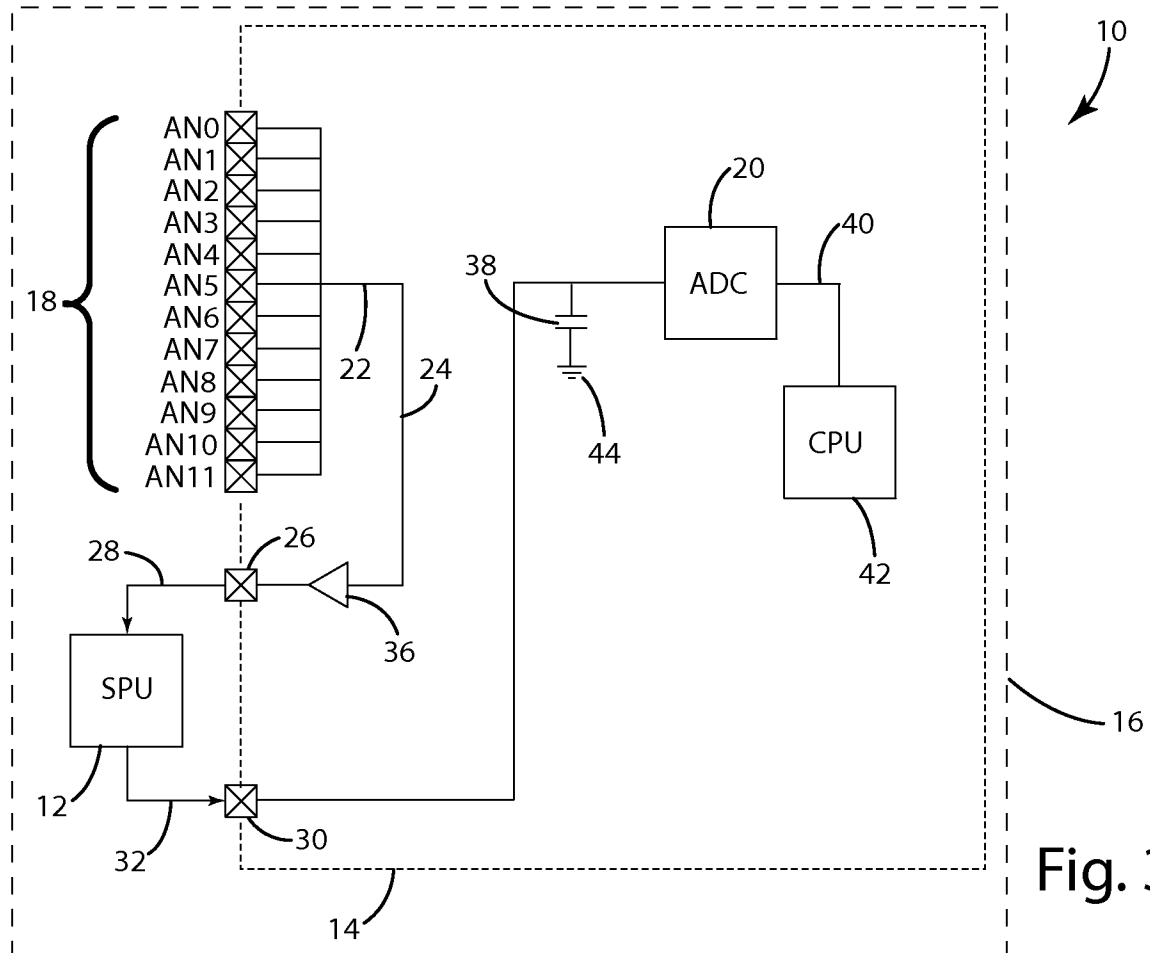
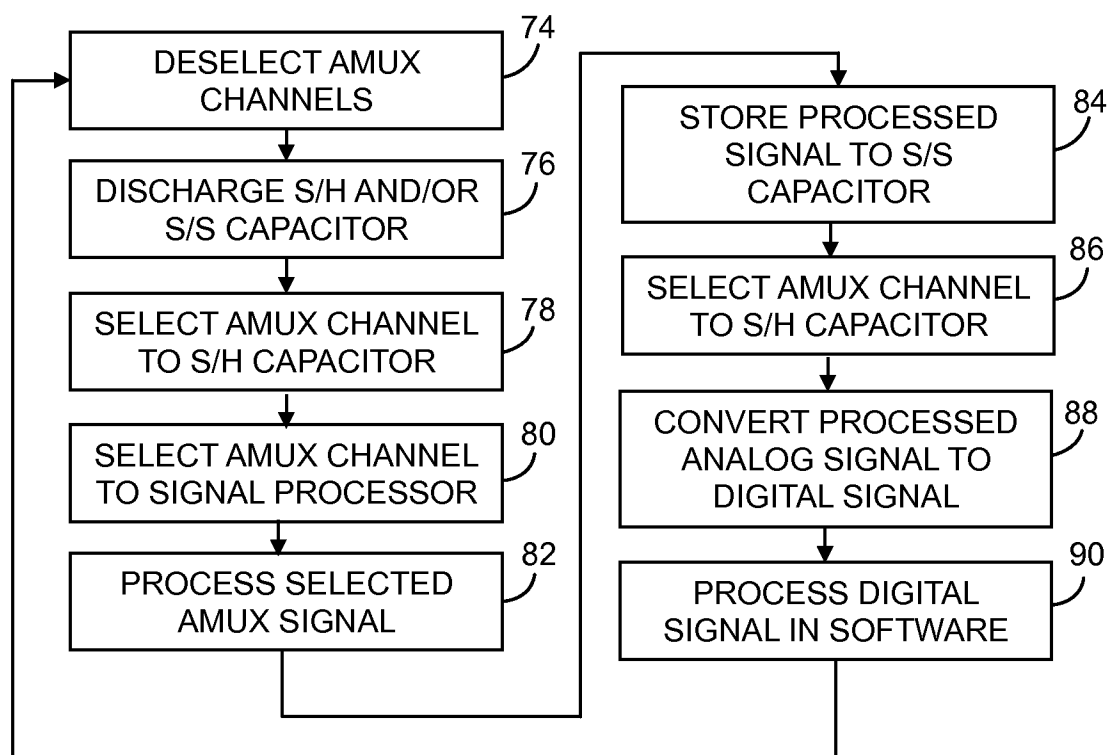
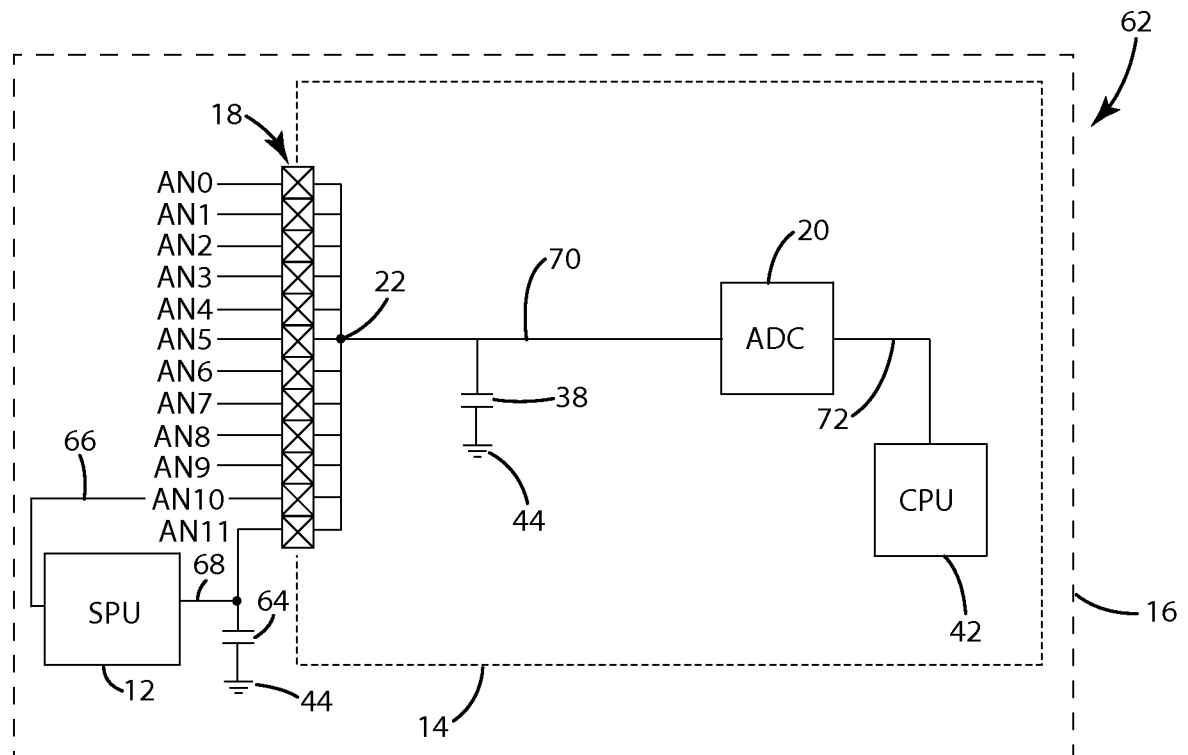


Fig. 2 (Prior Art)





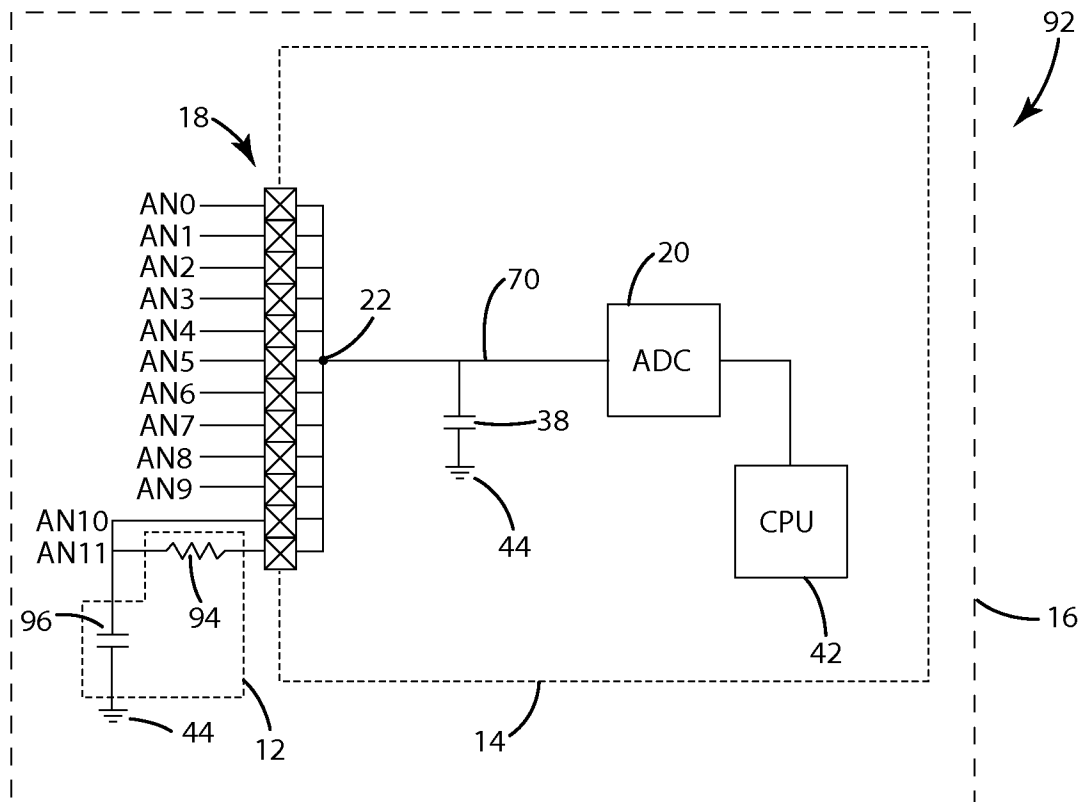


Fig. 7

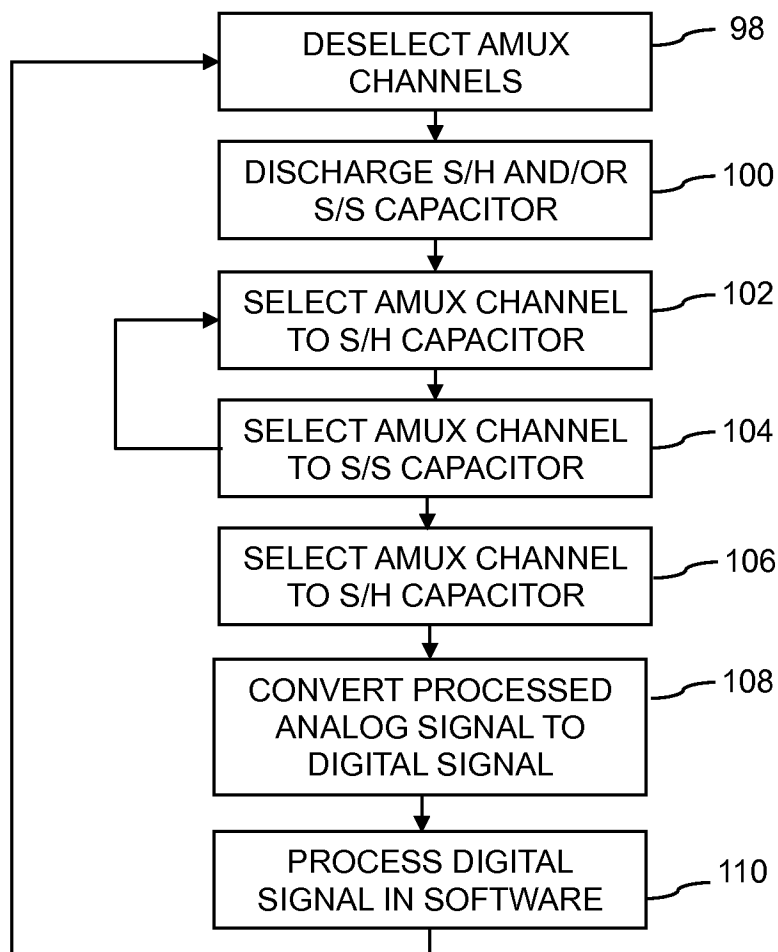


Fig. 8

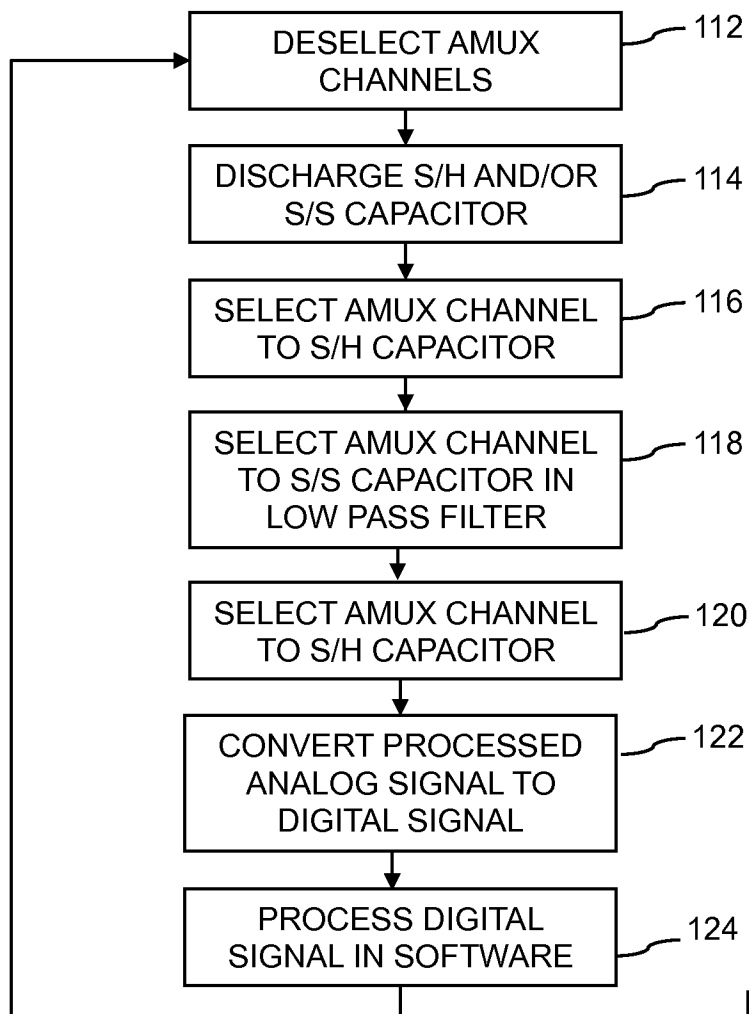


Fig. 9

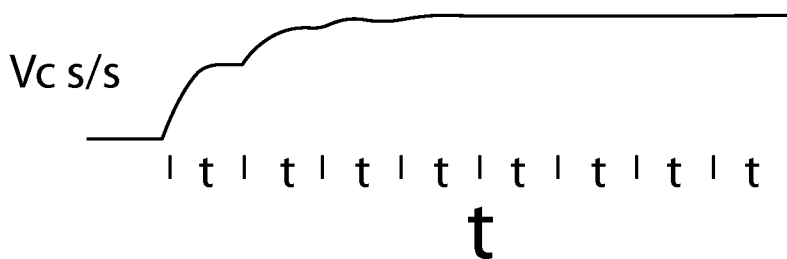


Fig. 10

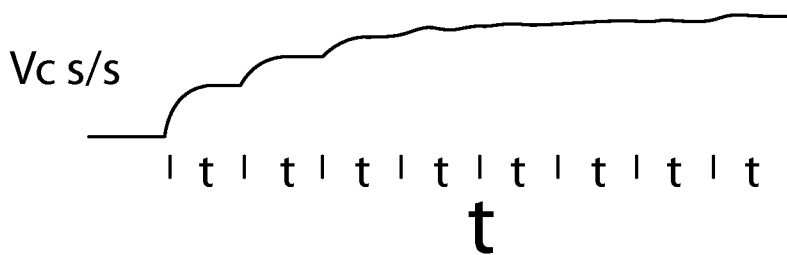


Fig. 11



Fig. 12

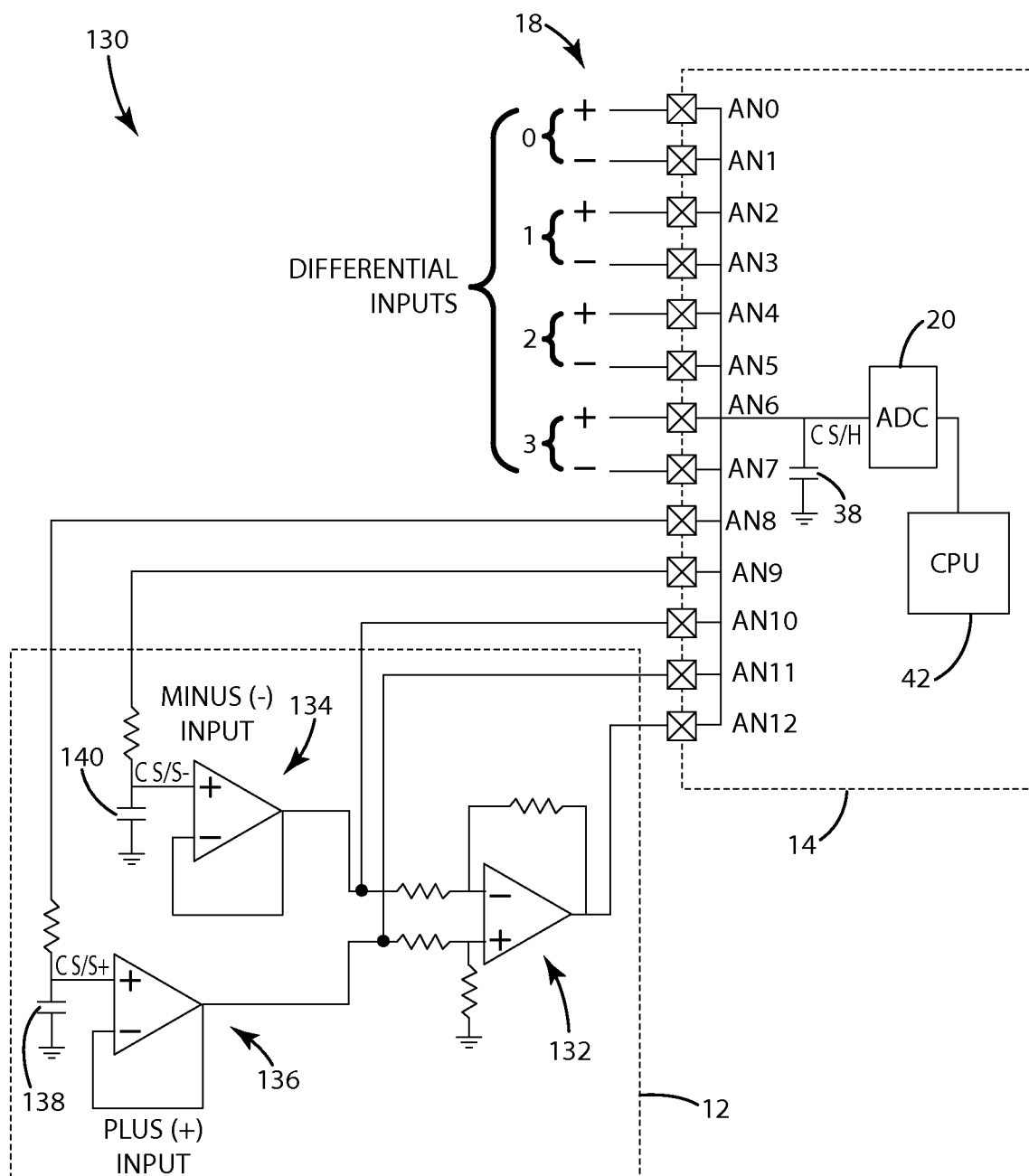


Fig. 13

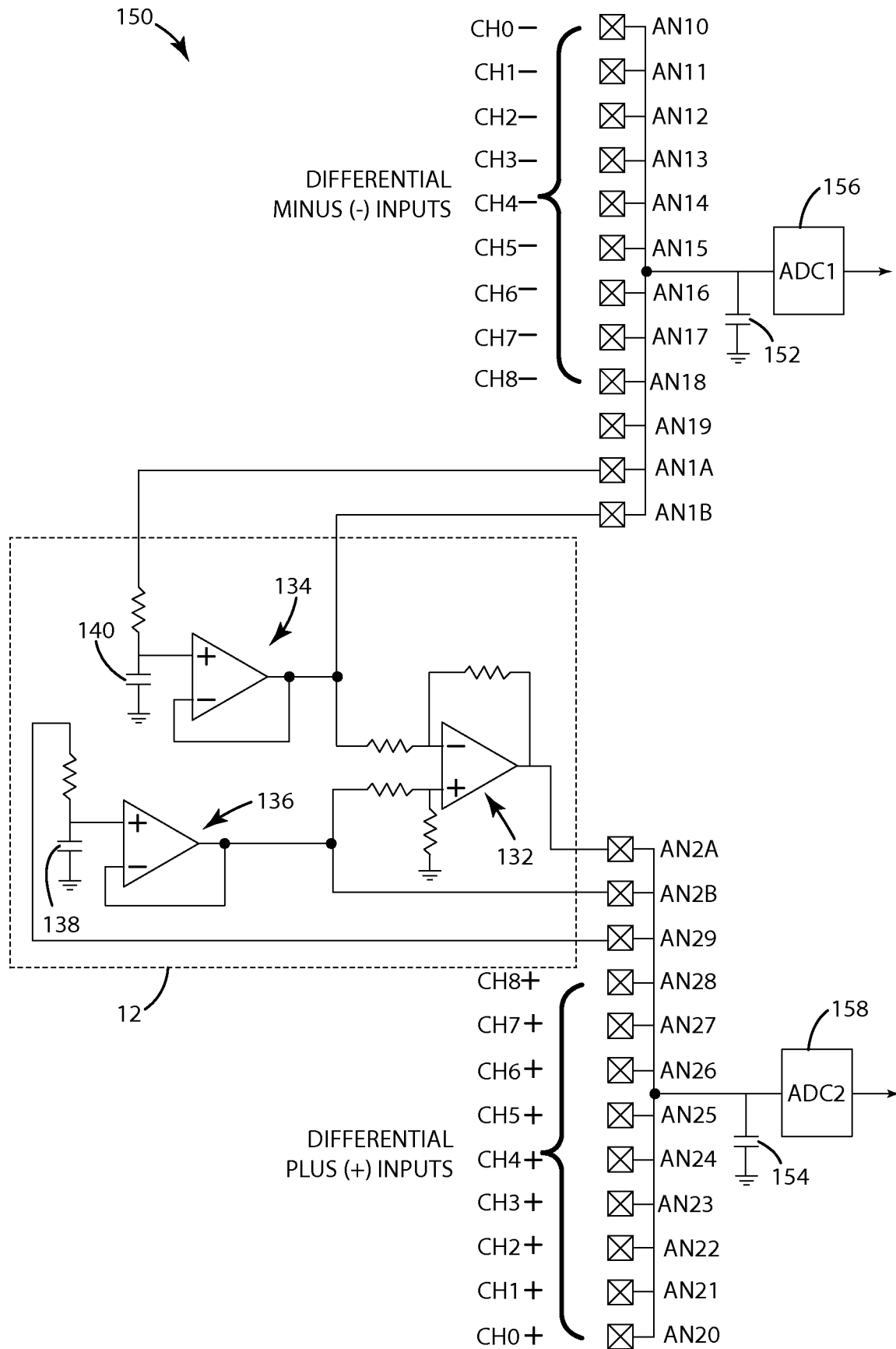


Fig. 14