US 20060261397A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2006/0261397 A1**

**Ahn et al.** (43) **Pub. Date: Nov. 23, 2006**

(54) **LANTHANIDE OXIDE/HAFNIUM OXIDE DIELECTRIC LAYERS**

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(21) Appl. No.: **11/493,074**

(22) Filed: **Jul. 26, 2006**

**Related U.S. Application Data**

(62) Division of application No. 10/931,343, filed on Aug. 31, 2004, which is a division of application No. 10/602,323, filed on Jun. 24, 2003.

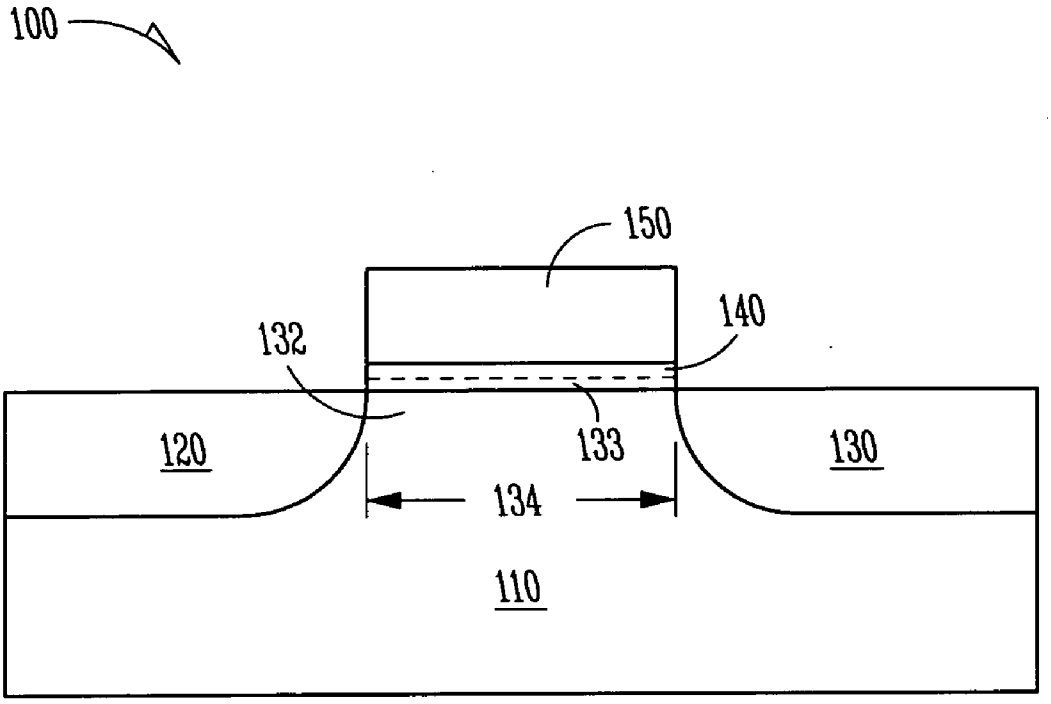
**Publication Classification**

(51) **Int. Cl.**
***H01L 29/94*** (2006.01)

(52) **U.S. Cl.** ..... **257/310**; 257/E21

(57) **ABSTRACT**

Dielectric layers are provided configured with a layer of lanthanide oxide and a layer of hafnium oxide, where the layer of hafnium oxide is structured as one of more monolayers of hafnium oxide. In an embodiment, a dielectric layer may be arranged as a nanolaminate of hafnium oxide and a lanthanide oxide, with the layer of hafnium oxide structured as one of more monolayers of hafnium oxide.



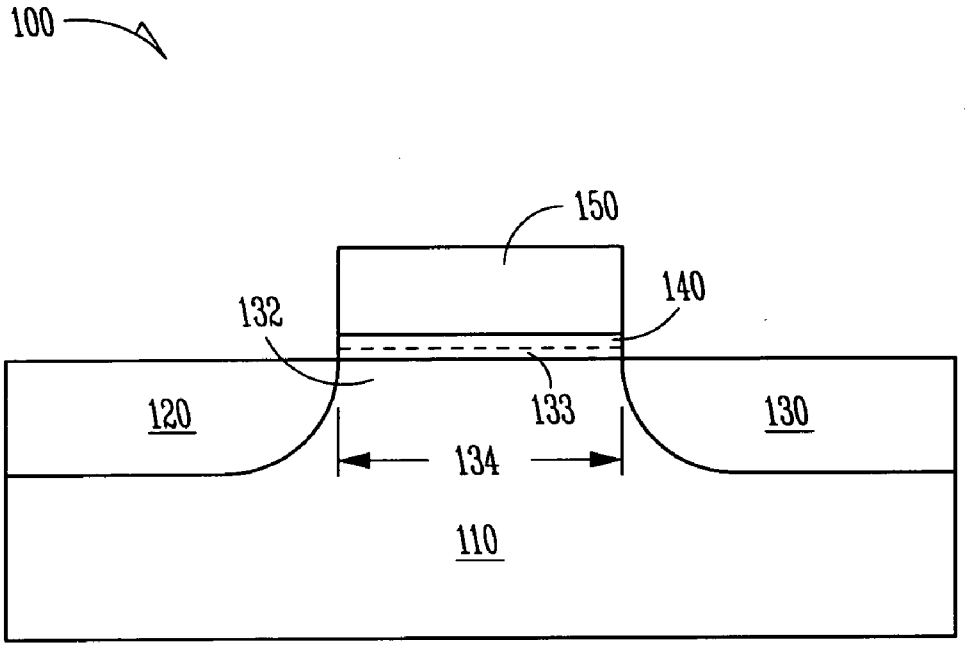



Fig.1

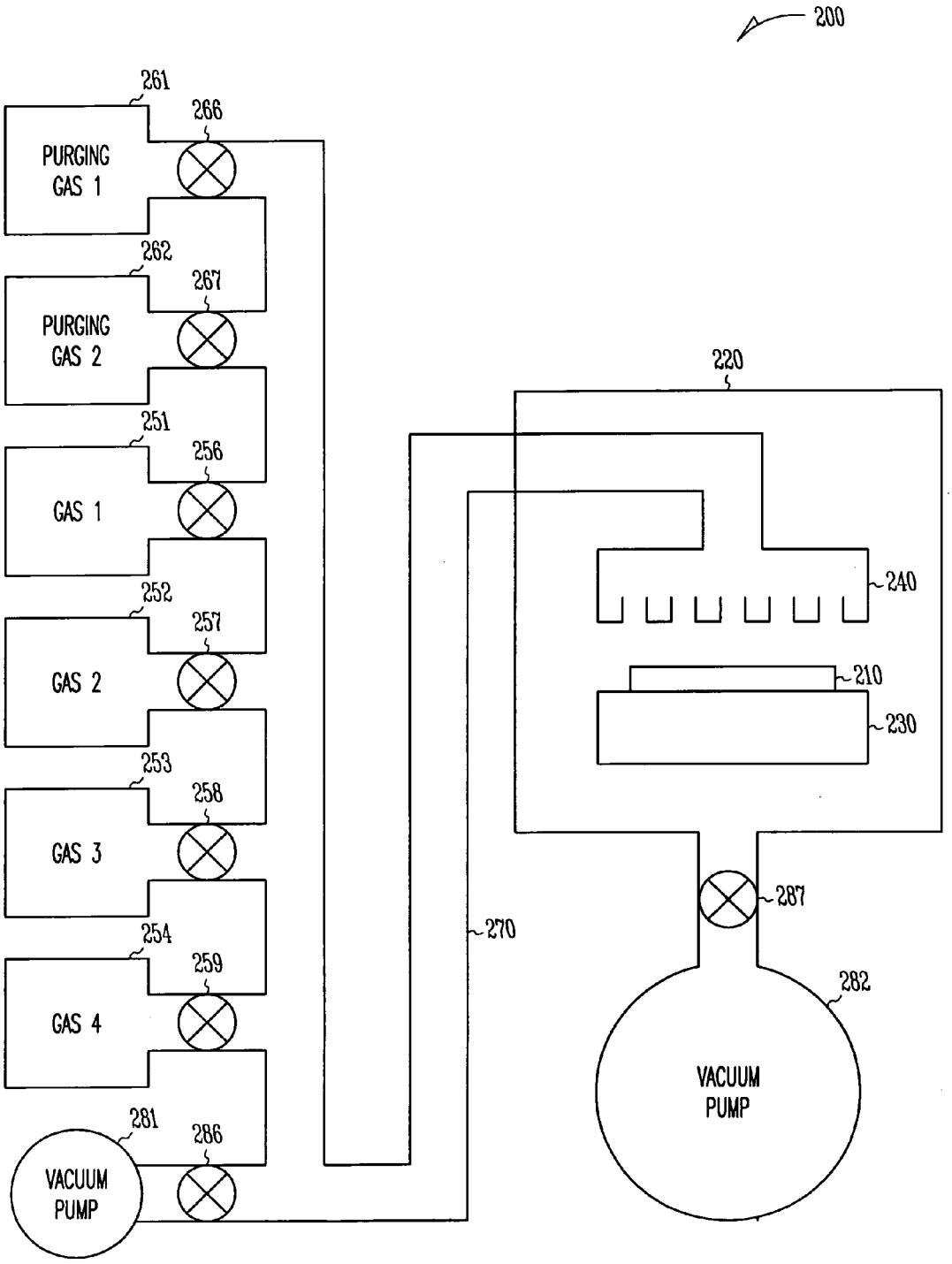

200
261
266
PURGING GAS 1
262
267
PURGING GAS 2
251
256
GAS 1
252
257
GAS 2
253
258
GAS 3
254
259
GAS 4
281
286
VACUUM PUMP
220
240
210
230
270
287
282
VACUUM PUMP

Fig.2A

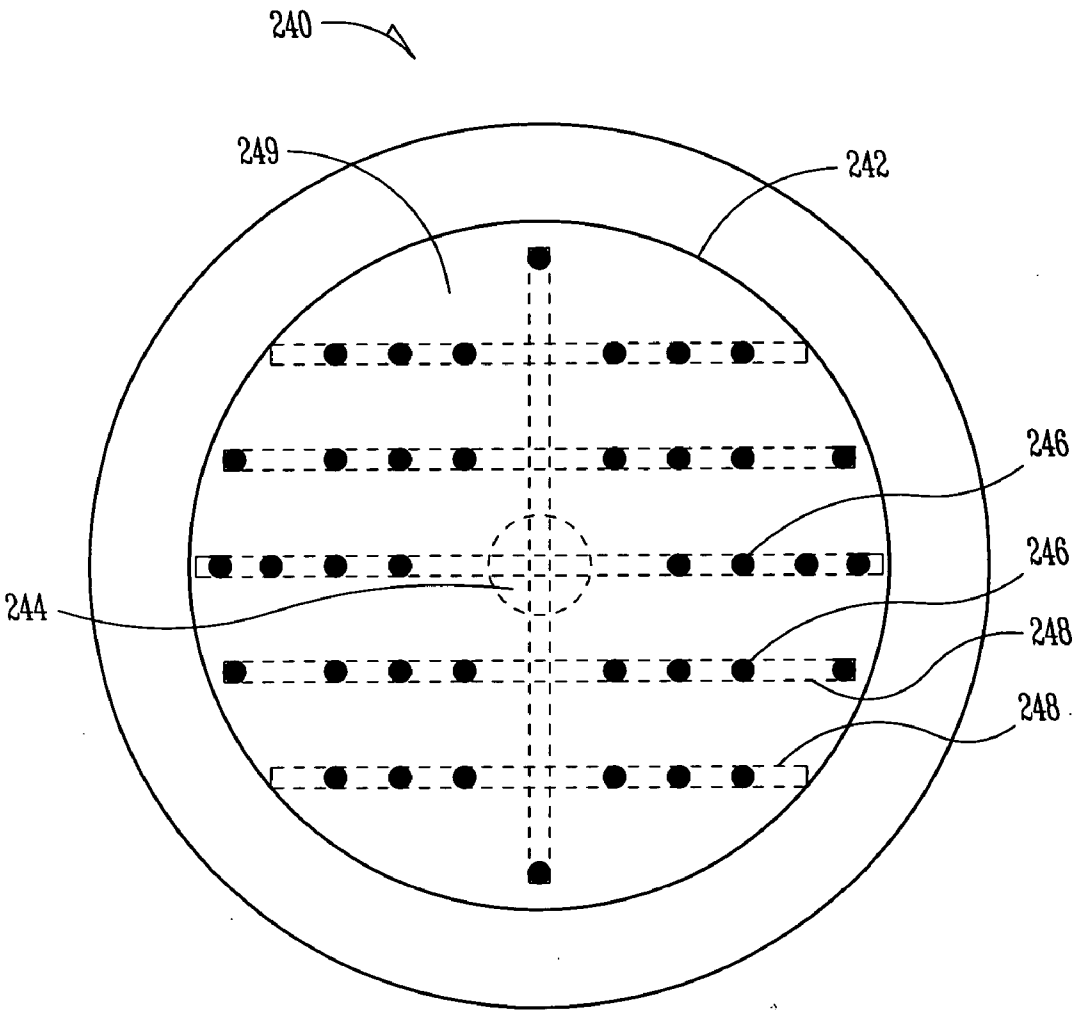
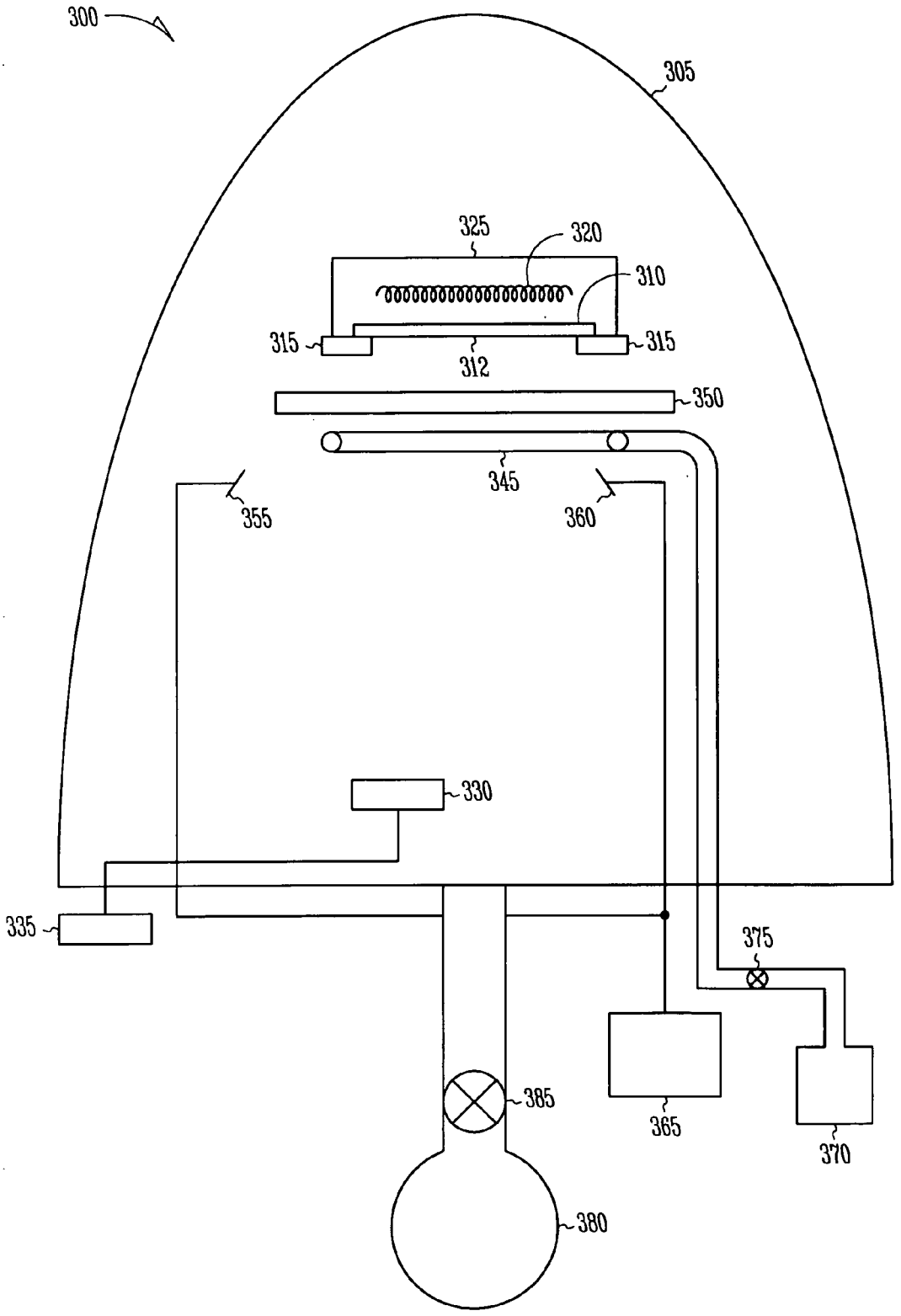



Fig.2B


300
305
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380

Fig.3

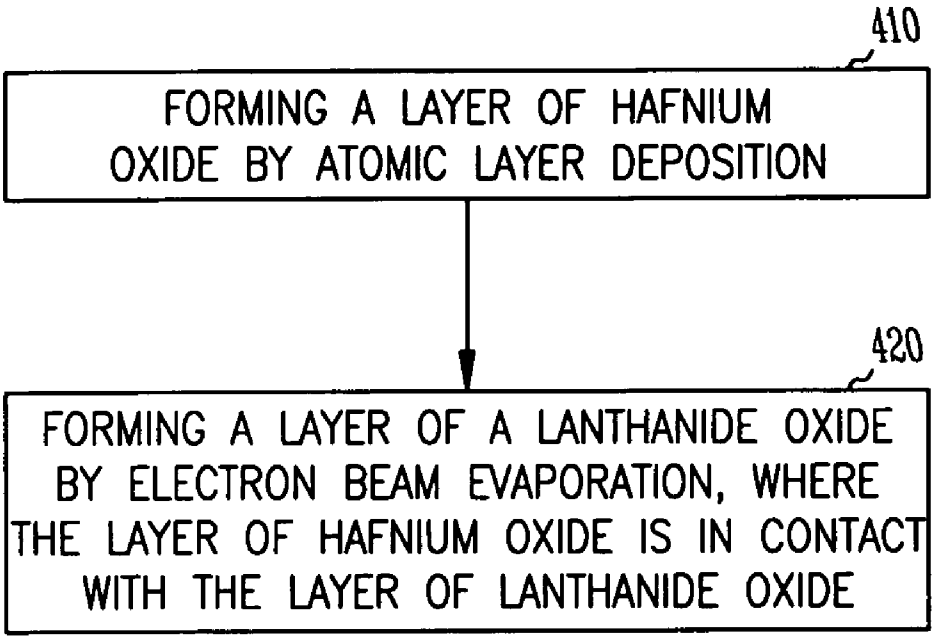
410
FORMING A LAYER OF HAFNIUM OXIDE BY ATOMIC LAYER DEPOSITION
420
FORMING A LAYER OF A LANTHANIDE OXIDE BY ELECTRON BEAM EVAPORATION, WHERE THE LAYER OF HAFNIUM OXIDE IS IN CONTACT WITH THE LAYER OF LANTHANIDE OXIDE

Fig.4

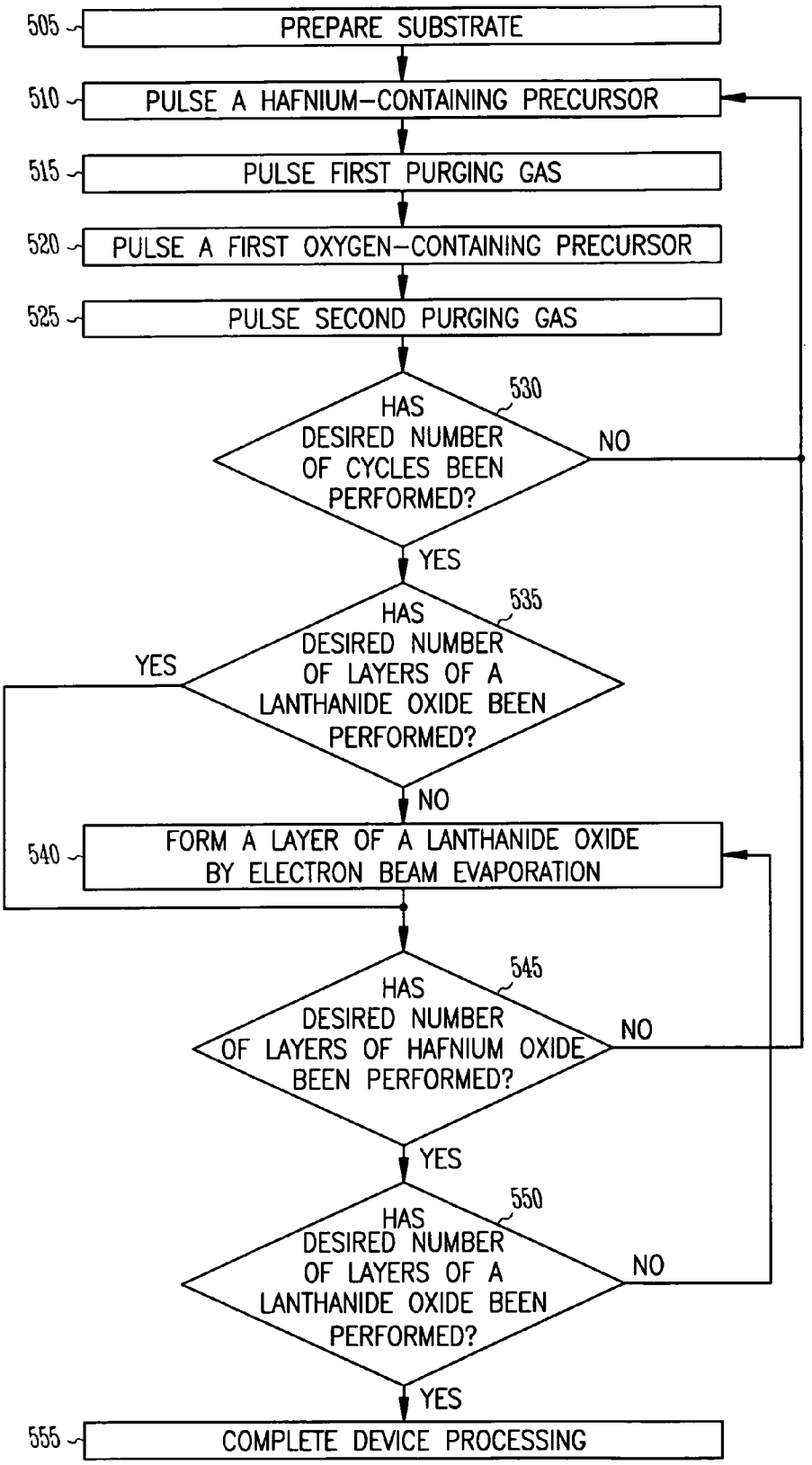
505
PREPARE SUBSTRATE
510
PULSE A HAFNIUM-CONTAINING PRECURSOR
515
PULSE FIRST PURGING GAS
520
PULSE A FIRST OXYGEN-CONTAINING PRECURSOR
525
PULSE SECOND PURGING GAS
530
HAS DESIRED NUMBER OF CYCLES BEEN PERFORMED?
NO
YES
535
HAS DESIRED NUMBER OF LAYERS OF A LANTHANIDE OXIDE BEEN PERFORMED?
YES
NO
540
FORM A LAYER OF A LANTHANIDE OXIDE BY ELECTRON BEAM EVAPORATION
545
HAS DESIRED NUMBER OF LAYERS OF HAFNIUM OXIDE BEEN PERFORMED?
NO
YES
550
HAS DESIRED NUMBER OF LAYERS OF A LANTHANIDE OXIDE BEEN PERFORMED?
NO
YES
555
COMPLETE DEVICE PROCESSING

Fig.5

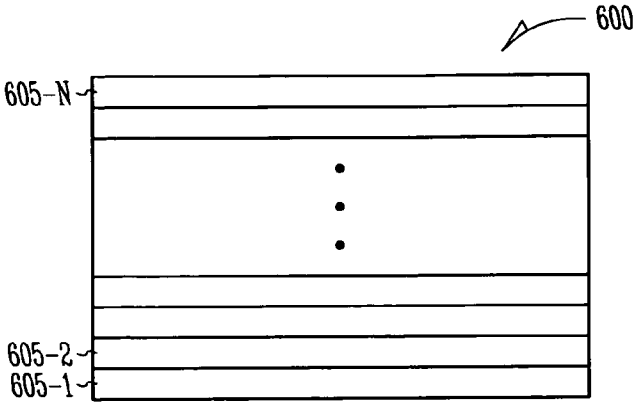


Fig.6

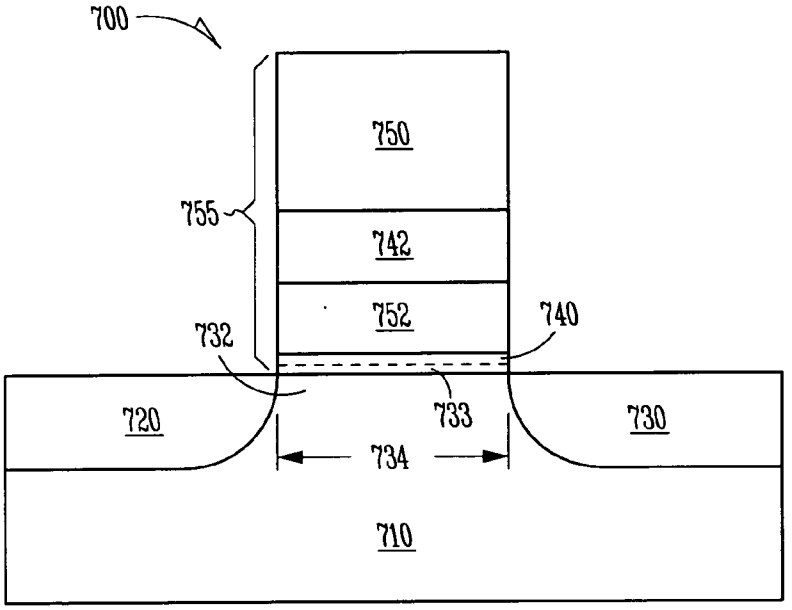


Fig.7

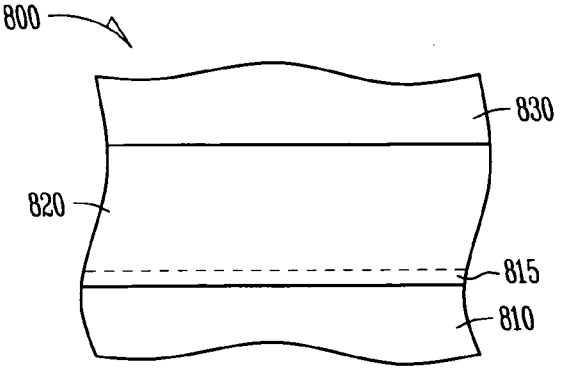


Fig.8

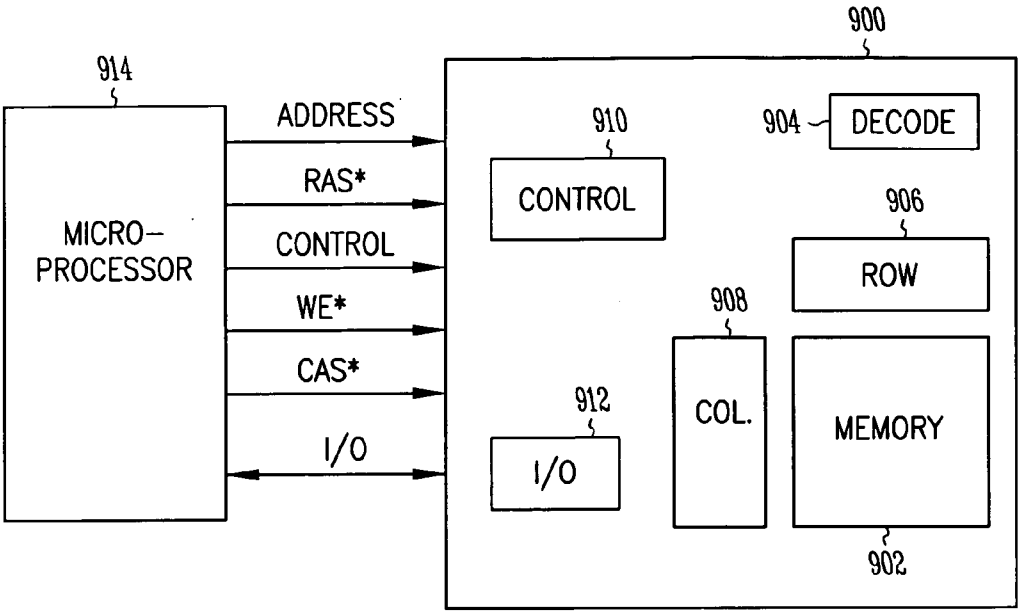
900
914
MICRO–
PROCESSOR
ADDRESS
RAS*
CONTROL
WE*
CAS*
I/O
910
CONTROL
904
DECODE
906
ROW
908
COL.
912
I/O
MEMORY
902

Fig.9

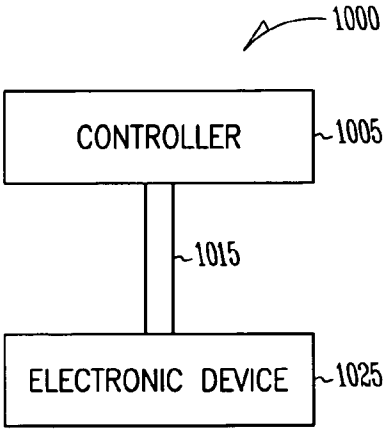
1000
CONTROLLER
1005
1015
ELECTRONIC DEVICE
1025

Fig.10

# LANTHANIDE OXIDE/HAFNIUM OXIDE DIELECTRIC LAYERS

## CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of U.S. application Ser. No. 10/931,343, filed 31 Aug. 2004, which is a divisional of U.S. application Ser. No. 10/602,323, filed 24 Jun. 2003, which applications are incorporated herein by reference in their entirety.

[0002] This application is related to the following commonly assigned U.S. patent applications, which are herein incorporated by reference in their entirety:

[0003] U.S. application Ser. No. 10/602,315, entitled "Lanthanide Oxide/Hafnium Oxide Dielectrics," filed 24 Jun. 2003, now issued as U.S. Pat. No. 7,049,192;

[0004] U.S. application Ser. No. 10/137,058, entitled: "Atomic Layer Deposition and Conversion," filed 2 May 2002;

[0005] U.S. application Ser. No. 10/137,168, entitled: "Methods, Systems, and Apparatus for Atomic-Layer Deposition of Aluminum Oxides in Integrated Circuits," filed 2 May 2002; and

[0006] U.S. application Ser. No. 09/797,324, entitled: "Methods, Systems, and Apparatus for Uniform Chemical-Vapor Depositions," filed 1 Mar. 2001, now issued as U.S. Pat. No. 6,852,167.

## TECHNICAL FIELD

[0007] This application relates generally to semiconductor devices and device fabrication and, more particularly, to dielectric layers and their method of fabrication.

## BACKGROUND

[0008] The semiconductor device industry has a market driven need to improve speed performance, improve its low static (off-state) power requirements, and adapt to a wide range of power supply and output voltage requirements for its silicon based microelectronic products. In particular, there is continuous pressure to reduce the size of devices such as transistors. The ultimate goal is to fabricate increasingly smaller and more reliable integrated circuits (ICs) for use in products such as processor chips, mobile telephones, and memory devices such as dynamic random access memories (DRAMs).

[0009] Currently, the semiconductor industry relies on the ability to reduce or scale the dimensions of its basic devices, primarily, the silicon based metal-oxide-semiconductor field effect transistor (MOSFET). A common configuration of such a transistor is shown in **FIG. 1**. While the following discussion uses **FIG. 1** to illustrate a transistor from the prior art, one skilled in the art will recognize that the present invention could be incorporated into the transistor shown in **FIG. 1** to form a transistor according to the present invention. A transistor **100** is fabricated in a substrate **110** that is typically silicon. Transistor **100** has a source region **120** and a drain region **130**. A body region **132** is located between source region **120** and drain region **130**, where body region **132** defines a channel of the transistor with a channel length **134**. A gate dielectric **140** is located on body region **132** with a gate **150** located over gate dielectric **140**. Gate dielectric **140** is typically an oxide, and is commonly referred to as a gate oxide. Gate **150** may be fabricated from polycrystalline silicon (polysilicon), or other conducting materials such as metal may be used.

[0010] In fabricating transistors to be smaller in size and reliably operate on lower power supplies, one design criteria is gate dielectric **140**. The mainstay for forming the gate dielectric has been silicon dioxide, $SiO_2$. A thermally grown amorphous $SiO_2$ layer provides an electrically and thermodynamically stable material, where the interface of the $SiO_2$ layer with underlying Si provides a high quality interface as well as superior electrical isolation properties. However, increased scaling and other requirements in microelectronic devices have created the need to use other dielectric materials as gate dielectrics.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0011] **FIG. 1** shows a configuration of a transistor having a gate dielectric containing an atomic layer deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, according to various embodiments of the present invention.

[0012] **FIG. 2A** depicts an atomic layer deposition system for processing a layer of hafnium oxide for a dielectric layer containing a hafnium oxide and a lanthanide oxide, according to various embodiments of the present invention.

[0013] **FIG. 2B** depicts a gas-distribution fixture of an atomic layer deposition system for processing a layer of hafnium oxide for a dielectric layer containing a hafnium oxide and a lanthanide oxide, according to various embodiments of the present invention.

[0014] **FIG. 3** depicts an electron beam evaporation system for processing a layer of lanthanide oxide for a dielectric layer containing a hafnium oxide and a lanthanide oxide, according to various embodiments of the present invention.

[0015] **FIG. 4** illustrates a flow diagram of elements for an embodiment of a method to process a dielectric layer containing an atomic layer deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, according to the present invention.

[0016] **FIG. 5** illustrates a flow diagram of elements for an embodiment of a method to process a dielectric layer containing an atomic layer deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, according to the present invention.

[0017] **FIG. 6** depicts an embodiment of a dielectric layer including a nanolaminate of a hafnium oxide layer and a lanthanide oxide layer, according to the present invention.

[0018] **FIG. 7** shows an embodiment of a configuration of a transistor having a dielectric layer containing an atomic layer deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, according to the present invention.

[0019] **FIG. 8** shows an embodiment of a configuration of a capacitor having a dielectric layer containing an atomic layer deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, according to the present invention.

[0020] **FIG. 9** is a simplified block diagram for an embodiment of a memory device with a dielectric layer containing an atomic layer deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, according to the present invention.

[0021] **FIG. 10** illustrates a block diagram for an embodiment of an electronic system having devices with a dielectric layer containing an atomic layer deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, according to the present invention.

## DETAILED DESCRIPTION

[0022] The following detailed description refers to the accompanying drawings that show, by way of illustration, specific aspects and embodiments in which the present invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the present invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The various embodiments disclosed herein are not necessarily mutually exclusive, as some disclosed embodiments can be combined with one or more other disclosed embodiments to form new embodiments.

[0023] The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form an integrated circuit (IC). The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Both wafer and substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art.

[0024] The term "horizontal" as used in this application is defined as a plane parallel to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The term "vertical" refers to a direction perpendicular to the horizontal as defined above. Prepositions, such as "on", "side" (as in "sidewall"), "higher", "lower", "over" and "under" are defined with respect to the conventional plane or surface being on the top surface of the wafer or substrate, regardless of the orientation of the wafer or substrate. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

[0025] In various embodiments, a dielectric layer includes a hafnium oxide layer and a lanthanide oxide layer, where the hafnium oxide layer is formed by atomic layer deposition (ALD) and the lanthanide oxide layer is formed by electron beam evaporation. The lanthanide oxide can be selected from $Pr_2O_3$, $Nd_2O_3$, $Sm_2O_3$, $Gd_2O_3$, and $Dy_2O_3$. In an embodiment, a dielectric layer includes a hafnium oxide/lanthanide oxide nanolaminate.

[0026] The term "nanolaminate" means a composite film of ultra thin layers of two or more materials in a layered stack, where the layers are alternating layers of materials of the composite film. Typically, each layer in a nanolaminate has a thickness of an order of magnitude in the nanometer range. Further, each individual material layer of the nanolaminate can have a thickness as low as a monolayer of the material. A nanolaminate of hafnium oxide and a lanthanide oxide includes at least one thin layer of hafnium oxide, and one thin layer of the lanthanide oxide, which can be written as a nanolaminate of hafnium oxide/lanthanide oxide. Further, a hafnium oxide/lanthanide oxide nanolaminate is not limited to alternating one lanthanide layer after a hafnium oxide layer, but can include multiple thin layers of a lanthanide oxide alternating with multiple thin layers of hafnium oxide. Further, the number of thin layers of lanthanide oxide and the number of thin layers of hafnium oxide can vary independently within a nanolaminate structure. Additionally, a hafnium oxide/lanthanide oxide nanolaminate can include layers of different lanthanide oxides, where each layer is independently selected from $Pr_2O_3$, $Nd_2O_3$, $Sm_2O_3$, $Gd_2O_3$, and $Dy_2O_3$. A dielectric layer containing alternating layers of a lanthanide oxide and a hafnium oxide has an effective dielectric constant related to the series combination of the layers of lanthanide oxide and hafnium oxide, which depends on the relative thicknesses of the lanthanide oxide layers and the hafnium oxide layers. Thus, a dielectric containing a hafnium oxide/lanthanide oxide nanolaminate can be engineered to effectively provide a selected dielectric constant.

[0027] A gate dielectric **140** of **FIG. 1**, when operating in a transistor, has both a physical gate dielectric thickness and an equivalent oxide thickness ($t_{eq}$). The equivalent oxide thickness quantifies the electrical properties, such as capacitance, of a gate dielectric **140** in terms of a representative physical thickness. The equivalent oxide thickness, $t_{eq}$, is defined as the thickness of a theoretical $SiO_2$ layer that would have the same capacitance density as a given dielectric, ignoring leakage current and reliability considerations.

[0028] A $SiO_2$ layer of thickness, t, deposited on a Si surface as a gate dielectric will have a $t_{eq}$ larger than its thickness, t. This $t_{eq}$ results from the capacitance in the surface channel on which the $SiO_2$ is deposited due to the formation of a depletion/inversion region. This depletion/inversion region may result in $t_{eq}$ being from 3 to 6 Angstroms (Å) larger than the $SiO_2$ thickness, t. Thus, with the semiconductor industry driving to scale the gate dielectric equivalent oxide thickness to under 10 Å, the physical thickness for a $SiO_2$ layer used for a gate dielectric would be need to be approximately 4 to 7 Å.

[0029] Additional characteristics for a $SiO_2$ layer depend on the gate electrode used in conjunction with the $SiO_2$ gate dielectric. Using a conventional polysilicon gate results in an additional increase in $t_{eq}$ for the $SiO_2$ layer. This additional thickness could be eliminated by using a metal gate electrode, though metal gates are not currently used in typical complementary metal-oxide-semiconductor field effect transistor (CMOS) technology. Thus, future devices would be designed towards a physical $SiO_2$ gate dielectric layer of about 5 Å or less. Such a small thickness for a $SiO_2$ oxide layer creates additional problems.

[0030] Silicon dioxide is used as a gate dielectric, in part, due to its electrical isolation properties in a $SiO_2$—Si based structure. This electrical isolation is due to the relatively large bandgap of $SiO_2$ (8.9 eV) making it a good insulator from electrical conduction. Signification reductions in its

bandgap would eliminate it as a material for a gate dielectric. As the thickness of a $SiO_2$ layer decreases, the number of atomic layers, or monolayers of the $SiO_2$ decreases. At a certain thickness, the number of monolayers will be sufficiently small that the $SiO_2$ layer will not have a complete arrangement of atoms as in a larger or bulk layer. As a result of incomplete formation relative to a bulk structure, a thin $SiO_2$ layer of only one or two monolayers will not form a full bandgap. The lack of a full bandgap in a $SiO_2$ gate dielectric could cause an effective short between an underlying Si channel and an overlying polysilicon gate. This undesirable property sets a limit on the physical thickness to which a $SiO_2$ layer may be scaled. The minimum thickness due to this monolayer effect is thought to be about 7-8 Å. Therefore, for future devices to have a $t_{eq}$ less than about 10 Å, dielectrics other than $SiO_2$ need to be considered for use as a gate dielectric.

[0031] For a typical dielectric layer used as a gate dielectric, the capacitance is determined as one for a parallel plate capacitance: $C=\kappa\epsilon_0 A/t$, where $\kappa$ is the dielectric constant, $\epsilon_0$ is the permittivity of free space, A is the area of the capacitor, and t is the thickness of the dielectric. The thickness, t, of a material is related to its $t_{eq}$ for a given capacitance, with $SiO_2$ having a dielectric constant $\kappa_0=3.9$, as

$$t=(\kappa/\kappa_{ox})\ t_{eq}=(\kappa/3.9)t_{eq}.$$

Thus, materials with a dielectric constant greater than that of $SiO_2$, 3.9, will have a physical thickness that may be considerably larger than a desired $t_{eq}$, while providing the desired equivalent oxide thickness. For example, an alternate dielectric material with a dielectric constant of 10 could have a thickness of about 25.6 Å to provide a $t_{eq}$ of 10 Å, not including any depletion/inversion layer effects. Thus, a reduced $t_{eq}$ for transistors may be realized by using dielectric materials with higher dielectric constants than $SiO_2$. The thinner $t_{eq}$ for lower transistor operating voltages and smaller transistor dimensions may be realized by a significant number of materials, but additional fabricating characteristics makes determining a suitable replacement for $SiO_2$ difficult.

[0032] The current view for the microelectronics industry is still for Si based devices. Thus, the gate dielectric employed will grow on a silicon substrate or silicon layer, which places significant restraints on the substitute dielectric material. During the formation of the dielectric on the silicon layer, there exists the possibility that a small layer of $SiO_2$ could be formed in addition to the desired dielectric. The result would effectively be a dielectric layer consisting of two sublayers in parallel with each other and the silicon layer on which the dielectric is formed. In such a case, the resulting capacitance would be that of two dielectrics in series. As a result, the $t_{eq}$ of the dielectric layer would be the sum of the $SiO_2$ thickness and a multiplicative factor of the thickness of the dielectric being formed, written as

$$t_{eq}=t_{SiO_2}+(\kappa_{ox}/\kappa)t.$$

Thus, if a $SiO_2$ layer is formed in the process, the $t_{eq}$ is again limited by a $SiO_2$ layer. Thus, use of an ultra-thin silicon dioxide interface layer should be limited to significantly less than ten angstroms. In the event that a barrier layer is formed between the silicon layer and the desired dielectric in which the barrier layer prevents the formation of a $SiO_2$ layer, the $t_{eq}$ would be limited by the layer with the lowest dielectric constant. However, whether a single dielectric layer with a high dielectric constant or a barrier layer with a higher dielectric constant than $SiO_2$ is employed, the layer interfacing with the silicon layer must provide a high quality interface to maintain a high channel carrier mobility.

[0033] One of the advantages for using $SiO_2$ as a gate dielectric has been that the formation of the $SiO_2$ layer results in an amorphous gate dielectric. Having an amorphous structure for a gate dielectric is advantageous because grain boundaries in polycrystalline gate dielectrics provide high leakage paths. Additionally, grain size and orientation changes throughout a polycrystalline gate dielectric may cause variations in the layer's dielectric constant. Many materials having a high dielectric constant relative to $SiO_2$ also have a disadvantage of a crystalline form, at least in a bulk configuration. Thus, the best candidates for replacing $SiO_2$ as a gate dielectric are those with high dielectric constant, a relatively large bandgap, and are able to be fabricated as a thin layer with an amorphous form.

[0034] Materials such as $Ta_2O_3$, $TiO_2$, $A_2O_3$, $HfO_2$, $HfSi_xO_y$, $HfSi_xO_y$, and barium strontium titanate (BST) have been proposed as replacements for $SiO_2$ as gate dielectric materials. Additional materials have been proposed to not only provide a material layer with a dielectric constant greater than silicon dioxide, but also to provide adjustment to the insulating properties of the material. Such materials can be provided as nanolaminates, for example, $Ta_2O_5$/$HfO_2$, $ZrO_2$/$HfO_2$, $Ta_2O_5$/$HfO_2$ nanolaminates. Providing dielectric layers configured as nanolaminates can provide a dielectric layer with relatively low leakage current properties.

[0035] An embodiment for a method for forming a dielectric layer containing a hafnium oxide and a lanthanide oxide includes forming a layer of the hafnium oxide by atomic layer deposition and forming a layer of the lanthanide oxide by electron beam evaporation. The layer of hafnium oxide is adjacent to and in contact with the layer of lanthanide oxide. In an embodiment, a dielectric layer includes a hafnium oxide/lanthanide oxide nanolaminate having an atomic layer deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer.

[0036] Dielectric layers containing an atomic layer deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer have a larger dielectric constant than silicon dioxide. Such dielectric layers provide a significantly thinner equivalent oxide thickness compared with a silicon oxide layer having the same physical thickness. Alternately, such dielectric layers provide a significantly thicker physical thickness than a silicon oxide layer having the same equivalent oxide thickness. Embodiments include structures for capacitors, transistors, memory devices, and electronic systems with dielectric layers containing atomic layer deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer, and methods for forming such structures.

[0037] In an embodiment of the present invention, a dielectric film having an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide allows for the engineering of a dielectric layer with a dielectric constant significantly higher than that of silicon dioxide and a relatively low leakage current characteristic. Using layers of atomic layer deposited $HfO_2$ in various embodiments, provides layers, as compared to $ZrO_2$, that

have a stronger tendency to form a single phase structure, a higher refractive index when deposited at low temperatures, a larger band gap, higher band offsets on silicon, and better thermal stability against silicide formation. Additionally, amorphous lanthanide oxides provide high oxide capacitance, low leakage current, and high thermal stability. Other considerations for selecting the material and method for forming a dielectric layer for use in electronic devices and systems concern the suitability of the material for applications requiring a dielectric layer to have an ultra-thin equivalent oxide thickness, form conformally on a substrate, and/or be engineered to specific thickness and elemental concentrations.

[0038] Another consideration concerns the roughness of the dielectric layer on a substrate. Surface roughness of the dielectric layer has a significant effect on the electrical properties of the gate oxide, and the resulting operating characteristics of the transistor. Leakage current through a physical 1.0 nanometer gate oxide has been found to be increased by a factor of 10 for every 0.1 increase in the root-mean-square (RMS) roughness.

[0039] During a conventional sputtering deposition process stage, particles of the material to be deposited bombard the surface at a high energy. When a particle hits the surface, some particles adhere, and other particles cause damage. High-energy impacts remove body region particles creating pits. The surface of such a deposited layer may have a rough contour due to the rough interface at the body region.

[0040] In an embodiment, a hafnium oxide layer having a substantially smooth surface relative to other processing techniques is formed on a substrate using atomic layer deposition. Further, the ALD deposited hafnium oxide layer provides a conformal coverage on the substrate surface on which it is deposited. A lanthanide oxide layer is then formed on the hafnium oxide layer, where the lanthanide oxide layer is formed by electron beam evaporation.

[0041] ALD, also known as atomic layer epitaxy (ALE), was developed in the early 1970's as a modification of chemical vapor deposition (CVD) and is also called "alternatively pulsed-CVD." In ALD, gaseous precursors are introduced one at a time to the substrate surface mounted within a reaction chamber (or reactor). This introduction of the gaseous precursors takes the form of pulses of each gaseous precursor. Between the pulses, the reaction chamber is purged with a gas, which in many cases is an inert gas, and/or evacuated.

[0042] In a chemisorption-saturated ALD (CS-ALD) process, during the first pulsing phase, reaction with the substrate occurs with the precursor saturatively chemisorbed at the substrate surface. Subsequent pulsing with a purging gas removes precursor excess from the reaction chamber.

[0043] The second pulsing phase introduces another precursor on the substrate where the growth reaction of the desired layer takes place. Subsequent to the layer growth reaction, reaction by-products and precursor excess are purged from the reaction chamber. With favourable precursor chemistry where the precursors adsorb and react with each other on the substrate aggressively, one ALD cycle may be performed in less than one second in properly designed flow type reaction chambers. Typically, precursor pulse times range from about 0.5 sec to about 2 to 3 seconds.

[0044] In ALD, the saturation of all the reaction and purging phases makes the growth self-limiting. This self-limiting growth results in large area uniformity and conformality, which has important applications for such cases as planar substrates, deep trenches, and in the processing of porous silicon and high surface area silica and alumina powders. Thus, ALD provides for controlling layer thickness in a straightforward manner by controlling the number of growth cycles.

[0045] ALD was originally developed to manufacture luminescent and dielectric layers needed in electroluminescent displays. Significant efforts have been made to apply ALD to the growth of doped zinc sulfide and alkaline earth metal sulfide layers. Additionally, ALD has been studied for the growth of different epitaxial II-V and II-VI layers, nonepitaxial crystalline or amorphous oxide and nitride layers and multilayer structures of these. There also has been considerable interest towards the ALD growth of silicon and germanium layers, but due to the difficult precursor chemistry, this has not been very successful.

[0046] The precursors used in an ALD process may be gaseous, liquid or solid. However, liquid or solid precursors must be volatile. The vapor pressure must be high enough for effective mass transportation. Also, solid and some liquid precursors need to be heated inside the reaction chamber and introduced through heated tubes to the substrates. The necessary vapor pressure must be reached at a temperature below the substrate temperature to avoid the condensation of the precursors on the substrate. Due to the self-limiting growth mechanisms of ALD, relatively low vapor pressure solid precursors may be used though evaporation rates may somewhat vary during the process because of changes in their surface area.

[0047] There are several other characteristics for precursors used in ALD. The precursors must be thermally stable at the substrate temperature because their decomposition would destroy the surface control and accordingly the advantages of the ALD method that relies on the reaction of the precursor at the substrate surface. A slight decomposition, if slow compared to the ALD growth, may be tolerated.

[0048] The precursors have to chemisorb on or react with the surface, though the interaction between the precursor and the surface as well as the mechanism for the adsorption is different for different precursors. The molecules at the substrate surface must react aggressively with the second precursor to form the desired solid layer. Additionally, precursors should not react with the layer to cause etching, and precursors should not dissolve in the layer. Using highly reactive precursors in ALD contrasts with the selection of precursors for conventional CVD.

[0049] The by-products in the reaction must be gaseous in order to allow their easy removal from the reaction chamber. Further, the by-products should not react or adsorb on the surface.

[0050] In a reaction sequence ALD (RS-ALD) process, the self-limiting process sequence involves sequential surface chemical reactions. RS-ALD relies on chemistry between a reactive surface and a reactive molecular precursor. In an RS-ALD process, molecular precursors are pulsed into the ALD reaction chamber separately. The metal precursor reaction at the substrate is typically followed by an inert gas

pulse to remove excess precursor and by-products from the reaction chamber prior to pulsing the next precursor of the fabrication sequence.

[0051] By RS-ALD, layers can be layered in equal metered sequences that are all identical in chemical kinetics, deposition per cycle, composition, and thickness. RS-ALD sequences generally deposit less than a full layer per cycle. Typically, a deposition or growth rate of about 0.25 to about 2.00 Å per RS-ALD cycle may be realized.

[0052] The characteristics of RS-ALD include continuity at an interface, conformality over a substrate, use of low temperature and mildly oxidizing processes, freedom from first wafer effects and chamber dependence, growth thickness dependent solely on the number of cycles performed, and ability to engineer multilayer laminate layers with resolution of one to two monolayers. RS-ALD allows for deposition control on the order on monolayers and the ability to deposit monolayers of amorphous layers.

[0053] Herein, a sequence refers to the ALD material formation based on an ALD reaction of a precursor or a precursor with its reactant precursor. For example, forming a metal layer from a precursor containing the metal forms an embodiment of a metal sequence. Additionally, forming a layer of metal oxide from a precursor containing the metal and from an oxygen containing precursor as its reactant precursor forms an embodiment of a metal/oxygen sequence, which may be referred to as the metal oxide sequence. A cycle of a metal sequence includes pulsing a precursor containing the metal and pulsing a purging gas for the precursor. Further, a cycle of a metal oxide sequence includes pulsing a precursor containing the metal, pulsing a purging gas for the precursor, pulsing a reactant precursor, and pulsing a purging gas for the reactant precursor. Additionally, a cycle for a compound metal oxide includes pulsing a precursor containing a first metal, pulsing a purging gas for this precursor, pulsing a reactant precursor for the first metal precursor, pulsing a purging gas for the reactant precursor, pulsing a precursor containing a second metal, pulsing a purging gas for this precursor, pulsing a reactant precursor for the second metal precursor, and pulsing a purging gas for this reactant precursor. The order of the metal precursors can depend on the tendency of the metals to allow diffusion of atoms through the metal to the underlying substrate. The order employed can limit the amount of unwanted atomic diffusion to the substrate surface.

[0054] In an embodiment, a hafnium oxide layer is formed on a substrate mounted in a reaction chamber by ALD using precursor gases individually pulsed into the reaction chamber. Alternately, solid or liquid precursors may be used in an appropriately designed reaction chamber.

[0055] **FIG. 2A** depicts an embodiment of an atomic layer deposition system **200** for processing a layer of hafnium oxide for a dielectric layer containing a hafnium oxide and a lanthanide oxide. The elements depicted are those elements necessary for discussion of embodiments of the present invention such that those skilled in the art may practice various embodiments of the present invention without undue experimentation. A further discussion of the ALD reaction chamber can be found in co-pending, commonly assigned U.S. patent application: entitled "Methods, Systems, and Apparatus for Uniform Chemical-Vapor Depositions," Ser. No. 09/797,324, filed 1 Mar. 2001, incorporated herein by reference.

[0056] In **FIG. 2A**, a substrate **210** is located inside a reaction chamber **220** of ALD system **200**. Also located within reaction chamber **220** is a heating element **230**, which is thermally coupled to substrate **210** to control the substrate temperature. A gas-distribution fixture **240** introduces precursor gases to the substrate **210**. Each precursor gas originates from individual gas sources **251-254** whose flow is controlled by mass-flow controllers **256-259**, respectively. Each gas source, **251-254**, provides a precursor gas either by storing the precursor as a gas or by providing a location and apparatus for evaporating a solid or liquid material to form the selected precursor gas. Furthermore, additional gas sources may be included, one for each metal precursor employed and one for each reactant precursor associated with each metal precursor.

[0057] Also included in the ALD system are purging gas sources **261**, **262**, each of which is coupled to mass-flow controllers **266**, **267**, respectively. Furthermore, additional purging gas sources may be constructed in ALD system **200**, one purging gas source for each precursor gas. For a process that uses the same purging gas for multiple precursor gases less purging gas sources are used in ALD system **200**.

[0058] Gas sources **251-254** and purging gas sources **261-262** are coupled by their associated mass-flow controllers to a common gas line or conduit **270**, which is coupled to the gas-distribution fixture **240** inside reaction chamber **220**. Gas conduit **270** is also coupled to vacuum pump, or exhaust pump, **281** by mass-flow controller **286** to remove excess precursor gases, purging gases, and by-product gases at the end of a purging sequence from gas conduit **270**.

[0059] Vacuum pump, or exhaust pump, **282** is coupled by mass-flow controller **287** to remove excess precursor gases, purging gases, and by-product gases at the end of a purging sequence from reaction chamber **220**. For convenience, control displays, mounting apparatus, temperature sensing devices, substrate maneuvering apparatus, and necessary electrical connections as are known to those skilled in the art are not shown in **FIG. 2A**.

[0060] **FIG. 2B** depicts an embodiment of a gas-distribution fixture **240** of atomic layer deposition system **200** for processing a layer of hafnium oxide for a dielectric layer containing a hafnium oxide and a lanthanide oxide. Gas-distribution fixture **240** includes a gas-distribution member **242**, and a gas inlet **244**. Gas inlet **244** couples gas-distribution member **242** to gas conduit **270** of **FIG. 2A**. Gas-distribution member **242** includes gas-distribution holes, or orifices, **246** and gas-distribution channels **248**. In the illustrated embodiment, holes **246** are substantially circular with a common diameter in the range of 15-20 microns, gas-distribution channels **248** have a common width in the range of 20-45 microns. The surface **249** of gas distribution member **242** having gas-distribution holes **246** is substantially planar and parallel to substrate **210** of **FIG. 2A**. However, other embodiments use other surface forms as well as shapes and sizes of holes and channels. The distribution and size of holes may also affect deposition thickness and thus might be used to assist thickness control. Holes **246** are coupled through gas-distribution channels **248** to gas inlet **244**. Though ALD system **200** is well suited for practicing embodiments of the present invention, other ALD systems commercially available may be used.

[0061] Those of ordinary skill in the art of semiconductor fabrication understand the use, construction and fundamen-

tal operation of reaction chambers for deposition of material layers. Embodiments of the present invention may be practiced on a variety of such reaction chambers without undue experimentation. Furthermore, one of ordinary skill in the art will comprehend the necessary detection, measurement, and control techniques in the art of semiconductor fabrication upon reading and studying this disclosure.

[0062] The elements of ALD system **200** may be controlled by a computer. To focus on the use of ALD system **200** in the various embodiments of the present invention, the computer is not shown. Those skilled in the art can appreciate that the individual elements such as pressure control, temperature control, and gas flow within ALD system **200** may be under computer control. In an embodiment, a computer executes instructions stored in a computer readable medium to accurately control the integrated functioning of the elements of ALD system **200** to form a hafnium oxide layer for a dielectric layer containing a hafnium oxide layer and a lanthanide oxide layer. In an embodiment, following the ALD formation of a hafnium oxide layer, a layer of a lanthanide oxide is formed by electron beam evaporation.

[0063] **FIG. 3** depicts an electron beam evaporation system **300** for processing a layer of lanthanide oxide for a dielectric layer containing a hafnium oxide and a lanthanide oxide. Evaporation system **300** includes a reaction chamber **305** in which is located a substrate **310** having a surface **312** that is to be processed. Substrate **310** rests on substrate holder **315** and its temperature can be raised above room temperature using a heater **320** with its associated reflector **325**. Evaporation system **300** also includes an electron gun device **330** regulated by electron gun controller **335** for depositing material on substrate surface **312**.

[0064] Material evaporated using electron gun device **330** travels to substrate **310** through an ionizer ring **345** and shutter **350**. Ionizer ring **345** provides supplemental oxygen for processes that require additional oxygen due to lost of oxygen in the evaporation of target materials. For target materials substantially void of oxygen, ionizer ring **345** provides initial oxygen to a film deposited on substrate surface **312** that is to undergo a subsequent oxidation process. Shutter **350** is used in conjunction with the control of electron gun device **330** to control the growth rate of a film on substrate **310**. The growth rate is determined using quartz crystal monitors **355**, **360**. The quartz crystal monitors **355**, **360** are coupled to a thickness/rate control **365**, typically located outside reaction chamber **305**.

[0065] Also located outside reaction chamber **305** is an oxygen gas source **370** including a mass-flow controller **375**. In an embodiment, the oxygen gas source is ozone gas. Mass-flow controller **375** controls the flow of the oxygen source into reaction chamber **305**. Further, a vacuum pump **380** with mass flow controller **385** maintains the overall atmosphere of evaporation system **300** at desired levels prior to, during, and after evaporation.

[0066] Electron gun device **330** can include an electron gun and receptacle for a target material that is to be evaporated. Target material placed in the target receptacle of electron gun device **330** is heated by impact from an electron beam from its associated electron gun. The electron beam is generated with an intensity and duration with which to evaporate the material in the target receptacle of electron gun device **330**. The evaporated material then distributes throughout the reaction chamber **305**. The evaporated material and pre-evaporation contaminants are prevented from depositing on substrate surface **312** in an unwanted manner by shutter **350**. Further, electron gun device can be realized using commercially available devices as are known to those skilled in the art.

[0067] Ionizer ring **345** provides oxygen necessary to compensate for loss of oxygen in the evaporated target material, or to add initial oxygen for subsequent oxidation processing. In one embodiment, it includes a ring with a center axis. The ring has a plurality of openings adapted to direct oxygen flowing to ionizer ring **345** from oxygen gas source **370** towards substrate surface **312**. Oxygen is uniformly distributed to substrate surface **312** by ionizer ring **345** positioned generally parallel to substrate **310**.

[0068] The evaporation chamber **300** can be included as part of an overall processing system including ALD system **200** of **FIG. 2A, 2B**. To avoid contamination of the surface of a layer formed by atomic layer deposition, evaporation chamber **300** can be connected to ALD system **200** using sealable connections to maintain the substrate, which is substrate **210** in **FIG. 2** and substrate **310** of **FIG. 3**, in an appropriate environment between ALD processing of a hafnium oxide layer and electron beam evaporation of a lanthanide oxide layer. Other means as are known to those skilled in the art can be employed for maintaining an appropriate environment between different processing procedures.

[0069] **FIG. 4** illustrates a flow diagram of elements for an embodiment of a method to process a dielectric layer containing an atomic layer deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer. This embodiment includes forming a layer of hafnium oxide by atomic layer deposition, at block **410**, and forming a layer of a lanthanide oxide by electron beam evaporation, at block **420**, where the layer of hafnium oxide is adjacent to and in contact with the lanthanide oxide layer. The lanthanide oxide can be selected from $Pr_2O_3$, $Nd_2O_3$, $Sm_2O_3$, $Gd_2O_3$, and $Dy_2O_3$. In an embodiment the method includes forming the layer of hafnium oxide on a substrate and forming the layer of lanthanide oxide on the layer of hafnium oxide. Alternately, a layer of lanthanide oxide is formed on a substrate and a layer of hafnium oxide is formed on the layer of lanthanide oxide. In an embodiment, the method includes controlling the forming of the layer of hafnium oxide and the layer of the lanthanide oxide to form a lanthanide oxide/hafnium oxide nanolaminate. The nanolaminate may have multiple layers of different lanthanide oxides selected from $Pr_2O_3$, $Nd_2O_3$, $Sm_2O_3$, $Gd_2O_3$, and $Dy_2O_3$. For a dielectric layer having a hafnium oxide layer and one or more layers of a lanthanide oxide, the combined thickness of lanthanide oxide layers can be limited to a total thickness between about 2 nanometers and about 10 nanometers. Also, for a dielectric layer having a lanthanide oxide layer and one or more layers of hafnium oxide, the combined thickness of hafnium oxide layers can be limited to a total thickness between about 2 nanometers and about 10 nanometers. In an embodiment, hafnium oxide layers are limited to between 2 nanometers and 5 nanometers. In an embodiment, a dielectric layer includes a hafnium oxide layer and multiple layers of lanthanide oxide, where each layer of lanthanide oxide is limited to a thickness between about 2 nanometers and about 10 nanometers.

[0070] Performing each atomic layer deposition includes pulsing one or more precursors into a reaction chamber for a predetermined period. The predetermined period is individually controlled for each precursor pulsed into the reaction chamber. Further the substrate is maintained at a selected temperature for each pulsing of a precursor, where the selected temperature is set independently for pulsing each precursor. Additionally, each precursor may be pulsed into the reaction under separate environmental conditions. Appropriate temperatures and pressures are maintained dependent on the nature of the precursor, whether the precursor is a single precursor or a mixture of precursors.

[0071] Using atomic layer deposition, the pulsing of the precursor gases is separated by purging the reaction chamber with a purging gas following each pulsing of a precursor. In an embodiment, nitrogen gas is used as the purging gas following the pulsing of each precursor used in a cycle to form a hafnium oxide layer. Additionally, the reaction chamber may also be purged by evacuating the reaction chamber.

[0072] **FIG. 5** illustrates a flow diagram of elements for an embodiment of a method to process a dielectric layer containing an atomic layer deposited hafnium oxide layer and an electronic beam evaporated lanthanide oxide layer. In an embodiment, the method depicted in **FIG. 5** can be used to form a gate dielectric layer for a transistor. This embodiment may be implemented with the atomic layer deposition system **200** of **FIG. 2A**, B, and the electron beam evaporation system of **FIG. 3**.

[0073] At block **505**, substrate **210** is prepared. Substrate **210** used for forming a transistor is typically a silicon or silicon containing material. In other embodiments, germanium, gallium arsenide, silicon-on-sapphire substrates, or other suitable substrates may be used. This preparation process may include cleaning of substrate **210** and forming layers and regions of the substrate, such as drains and sources of a metal oxide semiconductor (MOS) transistor, prior to forming a gate dielectric. In an embodiment, the substrate is cleaned to provide an initial substrate depleted of its native oxide. In an embodiment, the initial substrate is cleaned to provide a hydrogen-terminated surface. In an embodiment, a silicon substrate undergoes a final hydrofluoric acid, HF, rinse prior to ALD processing to provide the silicon substrate with a hydrogen-terminated surface without a native silicon oxide layer.

[0074] In an embodiment, substrate **210** is prepared as a chemical oxide-terminated silicon surface prior to forming a hafnium oxide by atomic layer deposition. This preparation allows for forming an interface layer to provide a structure that may further aid in reducing the leakage current through the dielectric layer.

[0075] The sequencing of the formation of the regions of the transistor being processed follows typical sequencing that is generally performed in the fabrication of a MOS transistor as is well known to those skilled in the art. Included in the processing is the masking of substrate regions to be protected during the gate dielectric formation, as is typically performed in MOS fabrication. In this embodiment, the unmasked region may include a body region of a transistor; however one skilled in the art will recognize that other semiconductor device structures may utilize this process. Additionally, substrate **210** in its ready for processing form is conveyed into a position in reaction chamber **220** for ALD processing.

[0076] At block **510**, a hafnium-containing precursor is pulsed into reaction chamber **220**. In an embodiment, $HfI_4$ is used as a precursor. In other embodiments, a hafnium-containing precursor includes but is not limited to $HfCl_4$, and $Hf(NO_3)_4$. The $HfI_4$ precursor is pulsed into reaction chamber **220** through the gas-distribution fixture **240** to substrate **210**. Mass-flow controller **256** regulates the flow of the $HfI_4$ from gas source **251**, where the $HfI_4$ gas is held at a temperature ranging from about 185° C. to about 195° C. In an embodiment, the substrate temperature is maintained between about 500° C. and about 750° C. In an embodiment, the substrate temperature is maintained at about 300° C. In other embodiments, the substrate may be held at lower temperatures lower than 300° C. The $HfI_4$ reacts with the surface of the substrate **210** in the desired region defined by the unmasked areas of the substrate **210**.

[0077] At block **515**, a first purging gas is pulsed into reaction chamber **220**. In an embodiment, nitrogen with a purity of about 99.999% is used as a purging gas. Mass-flow controller **266** regulates the nitrogen flow from the purging gas source **261** into the gas conduit **270**. Using the pure nitrogen purge avoids overlap of the precursor pulses and possible gas phase reactions.

[0078] A first oxygen-containing precursor is pulsed onto substrate **210**, at block **520**. In an embodiment, molecular oxygen is used as a precursor. In other embodiments, an oxygen-containing precursor for a hafnium/oxygen sequence includes but is not limited to $H_2O$, $H_2O_2$, an $H_2O$—$H_2O_2$ mixture, alcohol (ROH), $N_2O$, or $O_3$. The molecular oxygen precursor is pulsed into reaction chamber **220** through the gas-distribution fixture **240** on substrate **210**. Mass-flow controller **257** regulates the flow of the water vapor from gas source **252**. In an embodiment, the substrate temperature is maintained between about 100° C. and about 150° C. The water vapor reacts with at the surface of substrate **210** in the desired region defined by the unmasked areas of the substrate **210**.

[0079] After pulsing the first oxygen-containing precursor, a second purging gas is pulsed, at block, **525**. In an embodiment, nitrogen is used as the second purging gas. Excess precursor gas and reaction by-products are removed from the system by the purge gas in conjunction with the exhausting of reaction chamber **220** using vacuum pump **282** through mass-flow controller **287**, and exhausting of the gas conduit **270** by the vacuum pump **281** through mass-flow controller **286**. With the conclusion of the second purging gas pulse, a cycle. for forming an atomic layer deposited hafnium oxide is completed.

[0080] In an embodiment using a $HfI_4/O_2$ sequence, the substrate may be held between about 500° C. and about 750° C. by the heating element **230**. In an embodiment, the substrate may be held at 300° C. In other embodiments, the substrate may be held at lower temperatures lower than 300° C. The $HfI_4$ precursor can be pulsed for about 2.0 s. After the $HfI_4$ pulse, the hafnium/$O_2$ sequence continues with a purge pulse followed by a $O_2$ pulse followed by a purge pulse. In an embodiment, the $O_2$ pulse time is about 2.0 sec, and the two nitrogen purging pulse times are each at about 2.0 sec.

[0081] At block **530**, a determination is made as to whether a desired number of cycles has been performed, that is, whether the number of completed cycles is equal to a predetermined number. The predetermined number corre-

sponds to a predetermined thickness for the ALD hafnium oxide layer. The thickness of the hafnium oxide layer is determined by a fixed growth rate for the pulsing periods and precursors used, set at a value such as N nm/cycle. In an embodiment, a hafnium oxide layer may be grown at a rate ranging from about 0.07 nm/cycle to about 0.12 nm/cycle for an oxygen pressure ranging from about 0.1 Torr to about 0.3 Torr. For a desired dielectric layer thickness, t, the ALD process is repeated for t/N total cycles. Once the t/N cycles have completed, no further ALD processing for the current hafnium oxide layer is performed.

[0082] If the number of completed cycles is less than the predetermined number, the hafnium-containing precursor is pulsed into reaction chamber **220**, at block **510**, and the process continues. If the total number of cycles to form the desired thickness for the hafnium oxide layer has been completed, a determination is made as to whether the dielectric layer being formed contains the desired number of layers of a lanthanide oxide, at block **535**. If the desired number of layers of a lanthanide oxide have been made, a determination is made as to whether the desired number of layers of hafnium oxide have been processed, at block **545**. Such a case may occur in embodiments for a dielectric layer having hafnium oxide formed as consecutive layers on a lanthanide oxide layer. If more layers of hafnium oxide are required for the given application, the overall process continues as an atomic layer deposition with the pulsing of a hafnium-containing precursor, at block **510**.

[0083] If it is determined, at block **535**, that the desired number of layers of a lanthanide oxide have not been formed, then a layer of lanthanide oxide is formed on substrate **210**, at block **540**, which may include hafnium oxide layers and other lanthanide oxide layers. Substrate **210** in the ALD system, as illustrated in **FIG. 2**, is moved into the evaporation system depicted in **FIG. 3**, where the substrate **210**, with its formed layers, becomes substrate **310** of **FIG. 3**. To avoid contamination of the surface of a layer formed by atomic layer deposition, evaporation chamber **300** can be connected to ALD system **200** using sealable connections to maintain the substrate in an appropriate environment between ALD processing of a hafnium oxide layer and electron beam evaporation of a lanthanide oxide layer. Other means as are known to those skilled in the art can be employed for maintaining an appropriate environment between different processing procedures.

[0084] Substrate **310**, suitably masked for the given application and process procedures, is moved into evaporation chamber **305**. Electron gun **330** contains a receptacle for a source target on which an electron beam is directed. Electron gun controller **335** regulates the rate of evaporation of material from the target source. Alternatively, evaporation chamber **305** can include multiple electron guns, where each electron gun is directed to different targets containing sources to form selected lanthanide oxides to be used at different times in the process.

[0085] In an embodiment, the target source of electron gun **330** contains a ceramic $Pr_6O_{11}$ source, which is evaporated due to the impact of the electron beam. The evaporated material is then distributed throughout the chamber **305**. A dielectric layer of $Pr_2O_3$ is grown on surface **312** of substrate **310**, which is maintained at a temperature ranging from about 100° C. to about 150° C. The growth rate can vary with a typical rate of 0.1 Å/s. In an embodiment in which a lanthanide is first formed on a substrate prior to forming a hafnium oxide layer, a $Pr_2O_3$ layer may include a thin amorphous interfacial layer separating a crystalline layer of $Pr_2O_3$ from the substrate on which it is grown. This thin amorphous layer may be beneficial in reducing the number of interface charges and eliminating any grain boundary paths for conductance from the substrate. Other source materials can be used for forming a $Pr_2O_3$ layer, as are known to those skilled in the art.

[0086] Alternately, the lanthanide oxide layer formed by electron beam evaporation for a dielectric layer containing an atomic layer deposited hafnium oxide and a lanthanide oxide can be an oxide selected from $Nd_2O_3$, $Sm_2O_3$, $Gd_2O_3$, or $Dy_2O_3$. Further, a dielectric layer may include a number of hafnium oxide layers and a number of lanthanide oxide layers, where the lanthanide oxide layers are different lanthanide oxides. The different lanthanide oxides can be selected from $Pr_2O_3$, $Nd_2O_3$, $Sm_2O_3$, $Gd_2O_3$, and $Dy_2O_3$. The source material for the particular lanthanide oxide is chosen from commercial materials for forming the lanthanide oxide by electron bean evaporation, as is known by those skilled in the art.

[0087] After forming the layer of lanthanide oxide, at block **540**, a determination is made as to whether the desired number of hafnium oxide layers has been formed, at block **545**. If the desired number of hafnium oxide layers has not been formed, substrate **310** is moved back into atomic layer deposition system **200** and a hafnium-containing precursor is pulsed, at block **510** and the process continues. If it is determined that the desired number of hafnium oxide layers have been formed, at block **545**, it is then determined whether the desired number of layers of a lanthanide oxide have been formed, at block **550**. If the desired number of lanthanide oxide layers has not been formed, a layer of lanthanide oxide is formed by electron beam evaporation, at block **540**, and the process continues. If is determined that the desired number of lanthanide oxide layers have been formed, at block **550**, and if the desired number of hafnium oxide layers have been formed, then the substrate is further processed to complete device processing, at block **555**.

[0088] If the dielectric layer containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide has been formed to have the desired thickness, the growth of the dielectric layer is complete. The dielectric layer may be annealed. To avoid the diffusion of oxygen during annealing to the semiconductor substrate surface, annealing may be performed in an oxygen-free environment for short periods of time. An embodiment of an annealing environment may include a nitrogen atmosphere. In addition to limiting or avoiding oxygen diffusion to the semiconductor substrate, the relatively low processing temperatures employed by atomic layer deposition of the hafnium oxide layers and by electron beam evaporation of the lanthanide layers allows for the formation of an amorphous dielectric layer.

[0089] At block **555**, after forming the dielectric film containing atomic layer deposited hafnium oxide and electron beam deposited lanthanide oxide, processing the device having this dielectric layer is completed. In an embodiment, completing the device includes completing the formation of a transistor. In an embodiment, completing the device

includes completing the formation of a capacitor. In an embodiment, completing the process includes completing the construction of a memory device having an array with access transistors formed with gate dielectrics containing atomic layer deposited hafnium oxide and electron beam deposited lanthanide oxide. In an embodiment, completing the process includes the formation of an electronic system including an information handling device that uses electronic devices with transistors formed with dielectric layers having an atomic layer deposited hafnium oxide and an electron beam deposited lanthanide oxide.

[0090] Upon reading and comprehending this disclosure, it can be appreciated by those skilled in the art that the elements of a method for forming a dielectric layer containing atomic layer deposited hafnium oxide and electron beam deposited lanthanide oxide in the embodiment of **FIG. 5** may be performed under various environmental conditions, including various pressures and temperatures, and pulse periods depending on the dielectric layer to be formed for a given application and the systems used to fabricate such a dielectric layer. Determination of the environmental conditions, precursors used, purging gases employed, pulse periods for the precursors and purging gases, and electron beam target materials may be made without undue experimentation.

[0091] The elements for a method for forming a dielectric layer containing an atomic layer deposited hafnium oxide and an electron beam deposited lanthanide oxide as illustrated in **FIG. 5** can vary and include numerous permutations. In an embodiment, an atomic layer deposited hafnium oxide layer is formed on a substrate and an electron beam evaporated lanthanide oxide layer is formed on the hafnium oxide layer. Alternately, an electron beam evaporated lanthanide oxide layer is formed on a substrate and an atomic layer deposited hafnium oxide layer is deposited on the lanthanide oxide layer. A hafnium oxide layer may be formed as multiple layers of atomic layer deposited hafnium oxide. Similarly, a lanthanide oxide layer may be formed as multiple layers of an electron beam evaporated lanthanide oxide. Additionally, a dielectric layer may contain multiple layers of lanthanide oxide, where two or more layers contain different lanthanide oxides selected from $Pr_2O_3$, $Nd_2O_3$, $Sm_2O_3$, $Gd_2O_3$, and $Dy_2O_3$.

[0092] In an embodiment, a dielectric containing hafnium oxide and lanthanide oxide is formed as a nanolaminate. The nanolaminate may have multiple layers of different lanthanide oxides selected from $Pr_2O_3$, $Nd_2O_3$, $Sm_2O_3$, $Gd_2O_3$, and $Dy_2O_3$. For a dielectric layer having a hafnium oxide layer and one or more layers of a lanthanide oxide, the combined thickness of lanthanide oxide layers can be limited to a total thickness between about 2 nanometers and about 10 nanometers. Also, for a dielectric layer having a lanthanide oxide layer and one or more layers of hafnium oxide, the combined thickness of hafnium oxide layers can be limited to a total thickness between about 2 nanometers and about 10 nanometers. In an embodiment, hafnium oxide layers are limited to between 2 nanometers and 5 nanometers. In an embodiment, a dielectric layer includes a hafnium oxide layer and multiple layers of lanthanide oxide, where each layer of lanthanide oxide is limited to a thickness between about 2 nanometers and about 10 nanometers. In an embodiment, a dielectric layer includes a lanthanide oxide layer and multiple layers of hafnium oxide, where each layer of hafnium oxide is limited to a thickness between about 2 nanometers and about 10 nanometers. In an embodiment, a dielectric layer containing an atomic layer deposited hafnium oxide layer and an electron beam evaporated lanthanide oxide layer has a thickness ranging from about 2 nanometers to about 20 nanometers.

[0093] A dielectric layer containing an atomic layer deposited hafnium oxide and an electron beam deposited lanthanide oxide may be processed in an atomic layer deposition system such as ALD system **200** and evaporation system **300** under computer control to perform various embodiments, and operated under computer-executable instructions to perform these embodiments. Instructions stored in a computer readable medium are executed by a computer to accurately control the integrated functioning of the elements of atomic layer deposition system **200** and evaporation system **300** to form a dielectric layer containing hafnium oxide and a lanthanide oxide, according to various embodiments. The computer-executable instructions may be provided in any computer-readable medium. Such computer-readable medium may include, but is not limited to, floppy disks, diskettes, hard disks, CD-ROMS, flash ROMS, nonvolatile ROM, and RAM.

[0094] Dielectric layers containing hafnium oxide layers and lanthanide oxide layers can have a wide range of dielectric constants determined by the series configuration and relative thickness of the hafnium oxide layers and the lanthanide oxide layers. In bulk form, $HfO_2$ has a dielectric constant of about 25. Bulk $Pr_2O_3$ has a dielectric constant of about 31, while the dielectric constants for $Nd_2O_3$, $Sm_2O_3$, $Gd_2O_3$, and $Dy_2O_3$, in bulk form, are generally also in the range of 25-30. Consequently, a dielectric layer containing bulk layers of hafnium oxide and lanthanide oxide could be expected to have a dielectric constant engineered in the range from about 25 to about 31. Such a dielectric layer would have a $t_{eq}$ that is about one-sixth to one-eight smaller than a silicon oxide layer of the same thickness.

[0095] However, a thin dielectric layer with an interfacial layer formed between the surface of the substrate and the first layer of a hafnium oxide or a lanthanide oxide will have a $t_{eq}$ that is based on an interfacial layer physically in parallel with the dielectric layer equivalently forming a series configuration of electrical structures. Thus, the dielectric layer formed having an interfacial layer between it and the substrate on which it is grown can have an effective dielectric constant considerably less than a dielectric constant associated with the combination of hafnium oxide and lanthanide oxide layers.

[0096] Effective dielectric constants associated with thin layers of $Pr_2O_3$, $Nd_2O_3$, $Sm_2O_3$, $Gd_2O_3$, and $Dy_2O_3$ oxides on silicon have been reported to have dielectric constants in the range of 11 to 15 with interfacial regions having a thickness in the of about 0.5 nm to about 1.1 nm. See J. Sanghun et al., *Technical Digest of International Electron Devices Meetings* 2001, pp. 471-474 (2001). Similarly, $HfO_2$ also has been reported to have an effective dielectric constant reduced from its bulk value to a value in the range of 12 to 16 when formed as a thin layer on a silicon substrate with an interfacial layer. See K. Kukli et al., *Journal of Applied Physics,* vol. 92: no. 10, pp. 5698-5703 (2002). The effective dielectric constants for thin dielectric layers containing any of these materials and/or combinations of these

materials may be reduced from their bulk value depending on the thickness and material composition of any interfacial layer that may be formed.

[0097] Further, for those cases in which a dielectric layer containing hafnium oxide and lanthanide oxide is formed with little or no interfacial layer, the dielectric layer may be subject to a thin film effect related to the abrupt termination of the film. A planar bulk or thick film can be considered as a bulk region with two surface regions. Due to the termination of the thick film, the properties of the two surface regions can vary from that of the bulk region. In a thick film, the effective properties of the film are dominated by the bulk region. In a thin film, including nanolaminates, the properties of the thin film are effectively controlled by two surface regions. See K. Natori et al., *Applied Physics Letters,* vol. 73: no. 5, pp. 632-634 (1998). Thus, thin films of hafnium oxide and lanthanide oxide may have effective dielectric constants reduced from their bulk values without being formed in a structure with interfacial regions. Without a size effect, dielectric layers containing hafnium oxide and lanthanide oxide may have a dielectric constant in the range of about 25 to about 31. With a size effect, dielectric layers containing hafnium oxide and lanthanide oxide may have dielectric constants in the range from about 11 to about 16.

[0098] The embodiments described herein provide a process for growing a dielectric layer containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide having a wide range of useful equivalent oxide thickness, $t_{eq}$. The relatively large dielectric constant for such a dielectric layer ranges from about 11 to about 31, depending on the presence of an interfacial layer and/or on a size effect. Forming a dielectric layer according to various embodiments with a thickness ranging from 2 nanometers to 20 nanometers allows for the engineering of dielectric layers achieving a $t_{eq}$ in the range of about 0.7 nanometers to about 7 nanometers. Without an interfacial layer and without a size effect, the $t_{eq}$ for such a dielectric layer may range from about 0.25 nanometers to about 2.5 nanometers. A dielectric layer containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide may be formed for applications with a $t_{eq}$ between 10 Å and 20 Å, or less than 10 Å.

[0099] Dielectric layers containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide using embodiments of the present invention may be engineered with various structures and compositions including an amorphous structure. Embodiments using low processing temperatures tend to provide an amorphous structure, which is better suited for reducing leakage current than structures exhibiting a polycrystalline structure or a partial polycrystalline structure.

[0100] **FIG. 6** depicts a nanolaminate structure **600** for an embodiment of a dielectric structure including atomic layer deposited hafnium oxide and electron beam evaporated lanthanide oxide. Nanolaminate structure **600** includes a plurality of layers **605-1** to **605**-N, where each layer contains atomic layer deposited hafnium oxide or electron beam evaporated lanthanide oxide. The sequencing of the layers depends on the application. The effective dielectric constant associated with nanolaminate structure **600** is that attributable to N capacitors in series, where each capacitor has a thickness defined by the thickness of the corresponding electron beam evaporated lanthanide oxide or atomic layer deposited hafnium oxide layer. By selecting each thickness and the composition of each layer, electron beam evaporated lanthanide oxide or atomic layer deposited hafnium oxide layer, a nanolaminate structure can be engineered to have a predetermined dielectric constant.

[0101] Embodiments for forming a dielectric layer including ALD processing of a hafnium oxide and processing of an lanthanide oxide by electron beam evaporation may be implemented to form transistors, capacitors, memory devices, and other electronic systems including electro-optic devices, microwave devices, and information handling devices. With careful preparation and engineering of the dielectric layer limiting the size of interfacial regions, a $t_{eq}$ less than about 10 Å for these devices is anticipated.

[0102] A transistor **100** as depicted in **FIG. 1** may be constructed by forming a source region **120** and a drain region **130** in a silicon based substrate **110** where source and drain regions **120**, **130** are separated by a body region **132**. Body region **132** defines a channel having a channel length **134**. A dielectric layer is disposed on substrate **110** formed as a layer containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide. The resulting dielectric layer forms gate dielectric **140**.

[0103] A gate **150** is formed over gate dielectric **140**. Typically, forming gate **150** may include forming a polysilicon layer, though a metal gate may be formed in an alternative process. An interfacial layer **133** may form between body region **132** and gate dielectric **140**. Interfacial layer **133** may be limited to a thickness less than 1 nanometer, or to a thickness significantly less than 1 nanometer as to be effectively eliminated. Forming the substrate, the source and drain regions, and the gate is performed using standard processes known to those skilled in the art. Additionally, the sequencing of the various elements of the process for forming a transistor is conducted with standard fabrication processes, also as known to those skilled in the art.

[0104] The method for forming a dielectric layer containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide in various embodiments may be applied to other transistor structures having dielectric layers. **FIG. 7** shows an embodiment of a configuration of a transistor **700** having a dielectric layer containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide. Transistor **700** includes a silicon based substrate **710** with a source **720** and a drain **730** separated by a body region **732**. Body region **732** between source **720** and drain **730** defines a channel region having a channel length **734**. Located above body region **732** is a stack **755** including a gate dielectric **740**, a floating gate **752**, a floating gate dielectric **742**, and a control gate **750**. Gate dielectric **740** includes a dielectric containing an atomic layer deposited hafnium oxide layer and an electron beam evaporated lanthanide oxide layer as described herein with the remaining elements of the transistor **700** formed using processes known to those skilled in the art. Alternately, both gate dielectric **740** and floating gate dielectric **742** may be formed as dielectric layers containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide in various embodiments as described herein. An interfacial layer **733** may form between body region **732**

and gate dielectric **740**. Interfacial layer **733** may be limited to a thickness less than 1 nanometer, or to a thickness significantly less than 1 nanometer as to be effectively eliminated.

[**0105**] The embodiments of methods for forming dielectric layers containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide may also be applied to forming capacitors in various integrated circuits, memory devices, and electronic systems. In an embodiment for forming a capacitor **800** illustrated in **FIG. 8**, a method includes forming a first conductive layer **810**, forming a dielectric layer **820** containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide on first conductive layer **810**, and forming a second conductive layer **830** on dielectric layer **820**. An interfacial layer **815** may form between first conductive layer **810** and dielectric layer **820**. Interfacial layer **815** may be limited to a thickness less than 1 nanometer, or to a thickness significantly less than **1** nanometer as to be effectively eliminated.

[**0106**] Transistors, capacitors, and other devices dielectric layers containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide using methods described herein may be implemented into memory devices and electronic systems including information handling devices. Such information devices may include wireless systems, telecommunication systems, and computers. It will be recognized by one skilled in the art that several types of memory devices and electronic systems including information handling devices utilize embodiments of the present invention.

[**0107**] **FIG. 9** is a simplified block diagram of a memory device **900** using an embodiment of a dielectric containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide. Memory device **900** includes an array of memory cells **902**, address decoder **904**, row access circuitry **906**, column access circuitry **908**, control circuitry **910**, and Input/Output (I/O) circuit **912**. The memory is operably coupled to an external microprocessor **914**, or memory controller for memory accessing. Memory device **900** receives control signals from processor **914**, such as WE*, RAS* and CAS* signals, which can be supplied on a system bus. Memory device **900** stores data that is accessed via I/O lines. Each memory cell in a row of memory cell array **902** is coupled to a common word line. The word line is coupled to gates of individual transistors, where at least one transistor has a gate coupled to a gate dielectric containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide in accordance with the methods and structure previously described herein. Additionally, each memory cell in a column is coupled to a common bit line. Each cell in memory array **902** may include a storage capacitor and an access transistor as is conventional in the art. It will be appreciated by those skilled in the art that additional circuitry and control signals can be provided, and that the memory device of **FIG. 9** has been simplified to focus on embodiments of the present invention.

[**0108**] It will be understood that the above description of a memory device is intended to provide a general understanding of the memory and is not a complete description of all the elements and features of a specific type of memory, such as DRAM (Dynamic Random Access Memory). Further, embodiments are equally applicable to any size and type of memory circuit and are not intended to be limited to the DRAM described above. Other alternative types of devices include SRAM (Static Random Access Memory) or Flash memories. Additionally, the DRAM could be a synchronous DRAM commonly referred to as SGRAM (Synchronous Graphics Random Access Memory), SDRAM (Synchronous Dynamic Random Access Memory), SDRAM II, and DDR SDRAM (Double Data Rate SDRAM), as well as Synchlink or Rambus DRAMs and other emerging DRAM technologies.

[**0109**] **FIG. 10** illustrates a block diagram for an electronic system **1000** having devices with an embodiment for a dielectric layer containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide. Electronic system **1000** includes a controller **1005**, a bus **1015**, and an electronic device **1025**, where bus **1015** provides electrical conductivity between controller **1005** and electronic device **1025**. In various embodiments, controller **1005** and/or electronic device **1025** include an embodiment for a dielectric layer containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide as previously discussed herein. In an embodiment, electronic system **1000** includes a plurality of electronic devices using an embodiment for a dielectric layer containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide according to the present invention. Electronic system **1000** may include, but is not limited to, information handling devices, wireless systems, telecommunication systems, fiber optic systems, electro-optic systems, and computers.

## CONCLUSION

[**0110**] A dielectric layer containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide, using methods described herein, provides a reliable dielectric layer having an equivalent oxide thickness thinner than attainable using $SiO_2$. Forming dielectric layers containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide in relatively low processing temperatures may allow for dielectric layers that are amorphous and conformally layered on a substrate surface. Further, the formation of these dielectric layers provides for enhanced dielectric and electrical properties relative to those attained with an amorphous $SiO_2$ layer. These properties of dielectric layers containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide allow for application as dielectric layers in numerous devices and systems.

[**0111**] Capacitors, transistors, electro-optic devices, higher level ICs or devices, and electronic systems are constructed utilizing various embodiments for forming a dielectric layer containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide structured to provide an ultra thin equivalent oxide thickness, $t_{eq}$. Dielectric layers containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide are formed having a dielectric constant substantially higher than that of silicon dioxide, where such dielectric layers are capable of a $t_{eq}$ thinner than 10 Å, thinner than the expected limit for $SiO_2$ gate dielectrics. The thinner $t_{eq}$ of these dielectric layers allows for a higher

capacitance than $SiO_2$ gate dielectrics, which provides further effective scaling for microelectronic devices and systems. At the same time, the physical thickness of the dielectric layer containing an atomic layer deposited hafnium oxide and an electron beam evaporated lanthanide oxide is much larger than the $SiO_2$ thickness associated with the $t_{eq}$ limit of $SiO_2$. Forming the larger thickness aids in the manufacturing process for gate dielectrics and other dielectric layers.

[0112] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments will be apparent to those of skill in the art upon reviewing the above description. The scope of the present invention includes any other applications in which the above structures and fabrication methods are used. The scope of the present invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.

What is claimed is:

**1**. An electronic device comprising:

a first conductive region disposed on a substrate;

a dielectric layer disposed on the first conductive region, the dielectric layer including a hafnium oxide layer in contact with a lanthanide oxide layer, the hafnium oxide layer structured as one or more monolayers of hafnium oxide; and

a first conductive region disposed on the dielectric layer, wherein the first conductive region, the dielectric layer, and the second conductive region are structured in a capacitor or in a transistor.

**2**. The electronic device of claim 1, wherein the lanthanide oxide layer is disposed as an electron beam evaporated lanthanide oxide layer.

**3**. The electronic device of claim 1, wherein the hafnium oxide layer and the lanthanide oxide layer are arranged as a hafnium oxide/lanthanide oxide nanolaminate.

**4**. The electronic device of claim 1, wherein the lanthanide oxide layer has a thickness essentially between 2 nanometers and 10 nanometers.

**5**. The electronic device of claim 1, wherein the lanthanide oxide layer includes $Pr_2O_3$.

**6**. The electronic device of claim 1, wherein the dielectric layer includes $Nd_2O_3$.

**7**. The electronic device of claim 1, wherein the dielectric layer includes $Sm_2O_3$.

**8**. The electronic device of claim 1, wherein the dielectric layer includes $Gd_2O_3$.

**9**. The electronic device of claim 1, wherein the dielectric layer includes $Dy_2O_3$.

**10**. A capacitor, comprising:

a first conductive layer disposed on a substrate;

a dielectric layer disposed on the first conductive layer, the dielectric layer including a hafnium oxide layer in contact with a lanthanide oxide layer, the hafnium oxide layer structured as one or more monolayers of hafnium oxide, the hafnium oxide layer and lanthanide oxide layer disposed in a hafnium oxide/lanthanide oxide nanolaminate, the nanolaminate having one or more lanthanide oxide layers; and

a second conductive layer disposed on the dielectric layer, wherein the lanthanide layers of the nanolaminate have a combined thickness ranging from about 2 nanometers to about 10 nanometers.

**11**. The capacitor of claim 10, wherein the lanthanide oxide layer includes an electronic beam evaporated lanthanide oxide layer.

**12**. The capacitor of claim 10, wherein the hafnium oxide layer is disposed in contact with the first conductive layer.

**13**. The capacitor of claim 10, wherein hafnium oxide/lanthanide oxide nanolaminate includes an electron beam evaporated lanthanide oxide layer disposed in contact with the first conductive layer.

**14**. The capacitor of claim 10, wherein the lanthanide oxide layer includes one or more of $Pr_2O_3$, $Nd_2O_3$, $Sm_2O_3$, $Gd_2O_3$, or $Dy_2O_3$.

**15**. A transistor comprising:

a body region in a substrate between a source region and a drain region;

a dielectric layer disposed on the body region, the dielectric layer including a hafnium oxide layer in contact with a lanthanide oxide layer, the hafnium oxide layer structured as one or more monolayers of hafnium oxide; and

a gate coupled to the dielectric layer.

**16**. The transistor of claim 15, wherein the lanthanide oxide layer dielectric layer includes an electron beam evaporated lanthanide oxide layer.

**17**. The transistor of claim 15, wherein the hafnium oxide layer and the lanthanide oxide layer are layers in a lanthanide oxide/hafnium oxide nanolaminate.

**18**. The transistor of claim 15, wherein the dielectric layer contains multiple electron beam evaporated lanthanide oxide layers with a combined thickness of the multiple electron beam evaporated lanthanide oxide layers ranging from about 2 nanometers and about 10 nanometers.

**19**. The transistor of claim 15, wherein the dielectric layer contains multiple hafnium oxide layers, the hafnium oxide layers structured as one or more monolayers of hafnium oxide, the multiple hafnium oxide layers having a combined thickness of the multiple hafnium oxide layers ranging from about 2 nanometers and about 10 nanometers.

**20**. The transistor of claim 15, wherein the hafnium oxide layer and the lanthanide oxide layer are layers in a lanthanide oxide/hafnium oxide nanolaminate having multiple layers of lanthanide oxide, each layer of lanthanide oxide limited to a thickness of between about 2 nanometers and about 10 nanometers.

**21**. The transistor of claim 15, wherein the lanthanide oxide layer includes a combination of lanthanide oxides, the oxides selected from the group of $Pr_2O_3$, $Nd_2O_3$, $Sm_2O_3$, $Gd_2O_3$, and $Dy_2O_3$.

**22**. A memory comprising:

a number of transistors, each transistor including a gate coupled to a dielectric layer, the dielectric layer disposed on a body region in a substrate between a source region and a drain region, the dielectric layer including

a hafnium oxide layer in contact with a lanthanide oxide layer, the hafnium oxide layer structured as one or more monolayers of hafnium oxide; and

a number of bit lines, each bit line coupled to one of the number of transistors.

**23**. The memory of claim 22, wherein the dielectric layer includes a hafnium oxide/lanthanide oxide nanolaminate such that a combined thickness of the lanthanide oxide layers in the nanolaminate ranges from a thickness of 2 nanometers to 10 nanometers.

**24**. The memory of claim 22, wherein the transistor is a transistor in a flash memory and the dielectric layer is an inter-gate dielectric of the transistor.

**25**. The memory of claim 22, wherein the dielectric layer is structured as a nanolaminate.

**26**. The memory of claim 22, wherein the dielectric layer includes a hafnium oxide/lanthanide oxide nanolaminate having a combined thickness of hafnium oxide layers ranging from about 2 nanometers to about 10 nanometers.

**27**. The memory of claim 22, wherein the lanthanide oxide layer includes an electron beam evaporated lanthanide oxide layer having one or more $Pr_2O_3$, $Nd_2O_3$, $Sm_2O_3$, $Gd_2O_3$, or $Dy_2O_3$.

**28**. An electronic system comprising:

a controller; and

an electronic device coupled to the controller, wherein at least one of the controller and the electronic device includes a dielectric layer, the dielectric layer including a hafnium oxide layer in contact with a lanthanide oxide layer, the hafnium oxide layer structured as one or more monolayers of hafnium oxide.

**29**. The electronic system of claim 28, where the lanthanide oxide layer includes an electron beam evaporated lanthanide oxide layer.

**30**. The electronic system of claim 28, wherein the hafnium oxide layer and the lanthanide oxide layer are layers in a lanthanide oxide/hafnium oxide nanolaminate.

**31**. The electronic system of claim 28, wherein the dielectric layer contains multiple electron beam evaporated lanthanide oxide layers with a combined thickness of the multiple electron beam evaporated lanthanide oxide layers ranging from about 2 nanometers and about 10 nanometers.

**32**. The electronic system of claim 28, wherein the dielectric layer contains multiple hafnium oxide layers with a combined thickness of the multiple hafnium oxide layers ranging from about 2 nanometers and about 10 nanometers.

**33**. The electronic system of claim 28, wherein the lanthanide oxide layer includes $Pr_2O_3$.

**34**. The electronic system of claim 28, wherein the lanthanide oxide layer includes one or more of $Nd_2O_3$ or $Sm_2O_3$.

**35**. The electronic system of claim 28, wherein the lanthanide oxide layer includes one or more of $Gd_2O_3$ or $Dy_2O_3$.

**36**. The electronic system of claim 28, wherein the electronic system includes an information handling device.

**37**. The electronic system of claim 28, wherein the electronic system includes a wireless system.

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