July 13, 1948. L. E. FLORY 2,445,215

ELECTRONIC COMPUTER

Filed Oct. 21, 1943 3 Sheets-Sheet 1

Fig. 1.

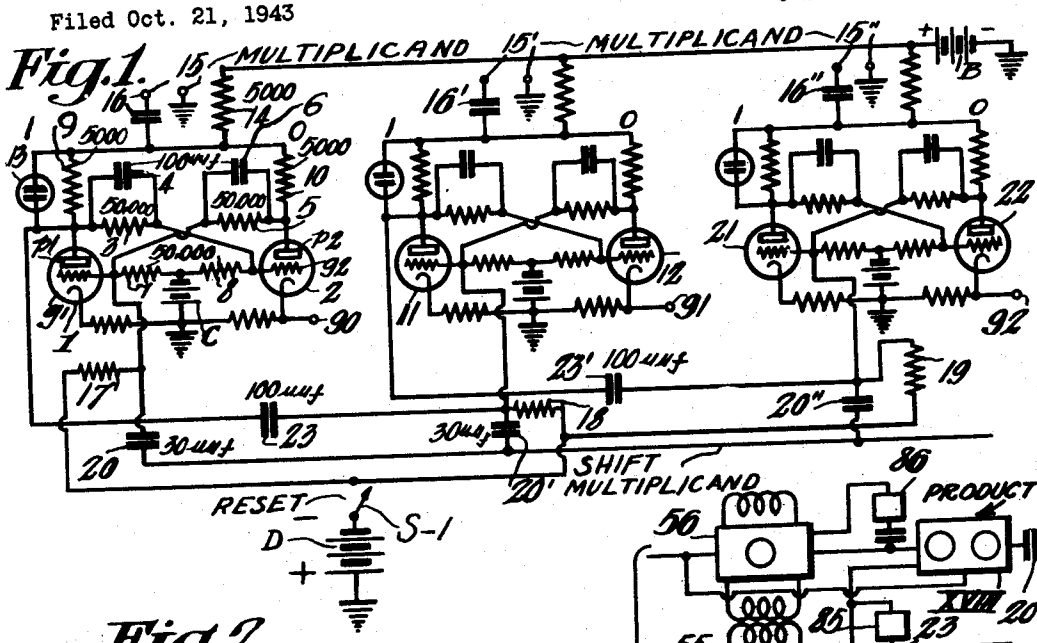


Fig. 2.

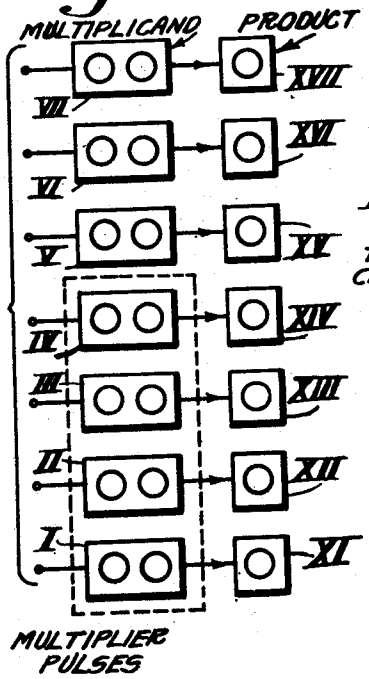
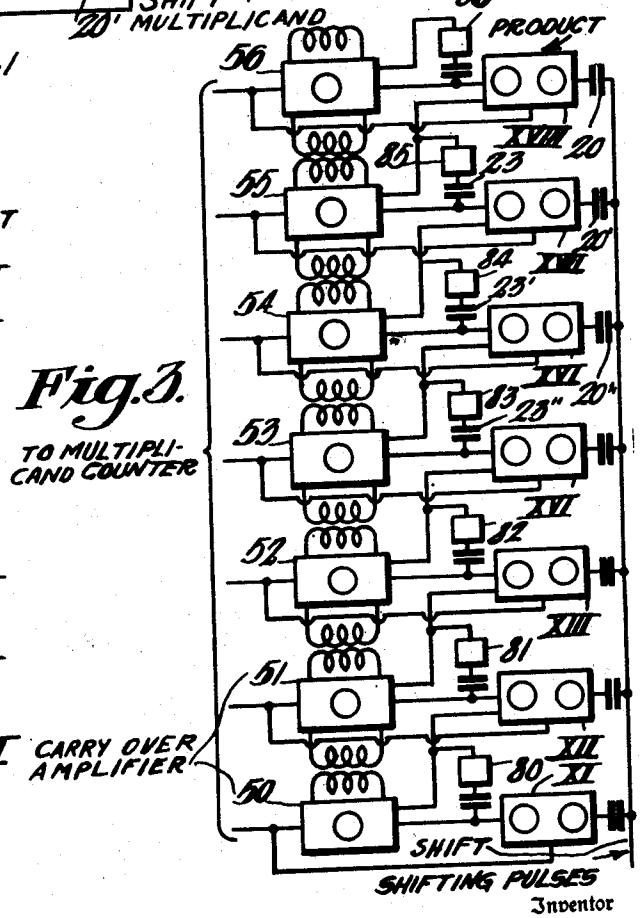


Fig. 3.



Inventor

Leslie E. Flory

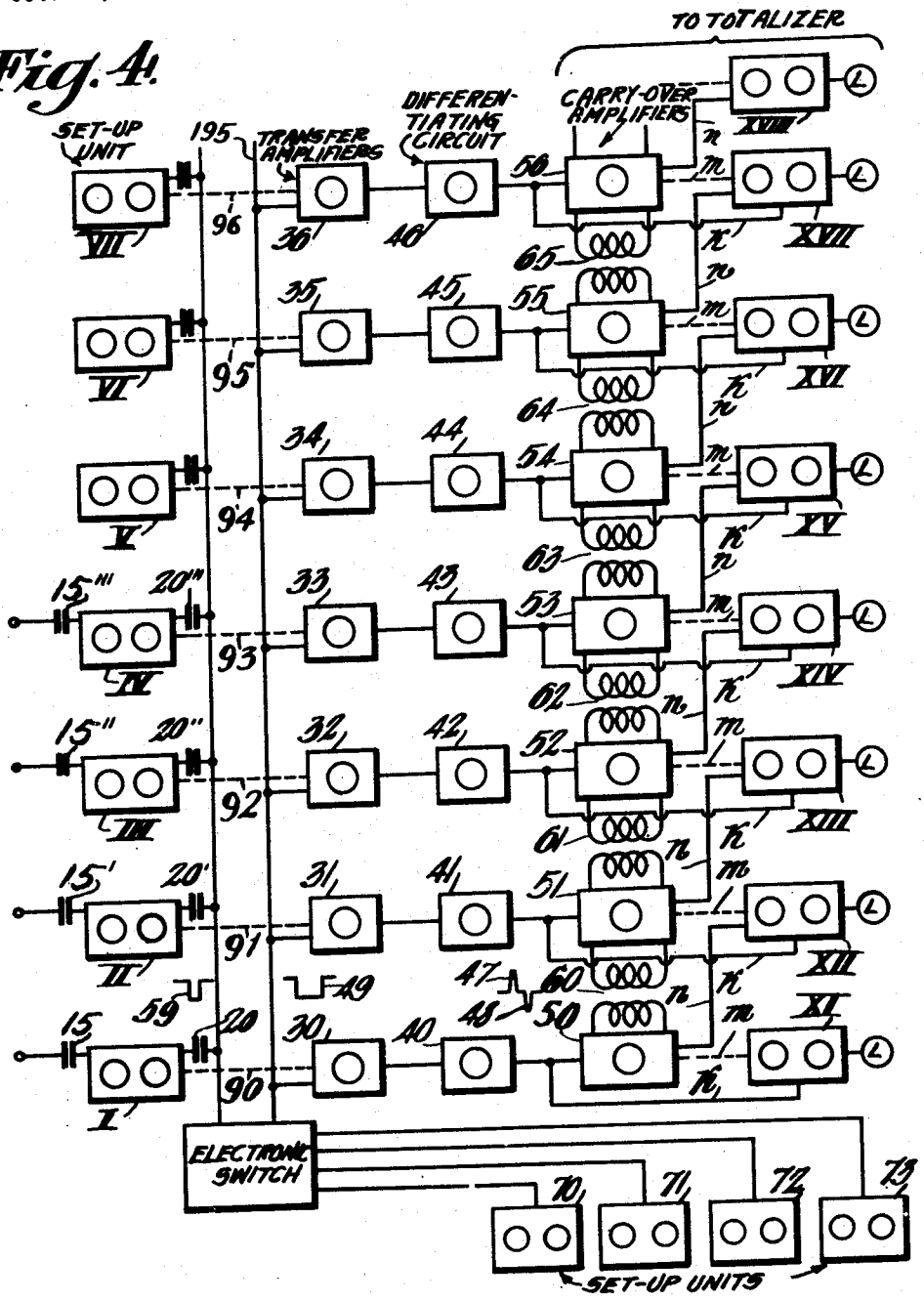
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July 13, 1948. L. E. FLORY 2,445,215

ELECTRONIC COMPUTER

Filed Oct. 21, 1943 3 Sheets-Sheet 2

Fig. 4.



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July 13, 1948. L. E. FLORY 2,445,215

ELECTRONIC COMPUTER

Filed Oct. 21, 1943 3 Sheets-Sheet 3

Fig. 5.

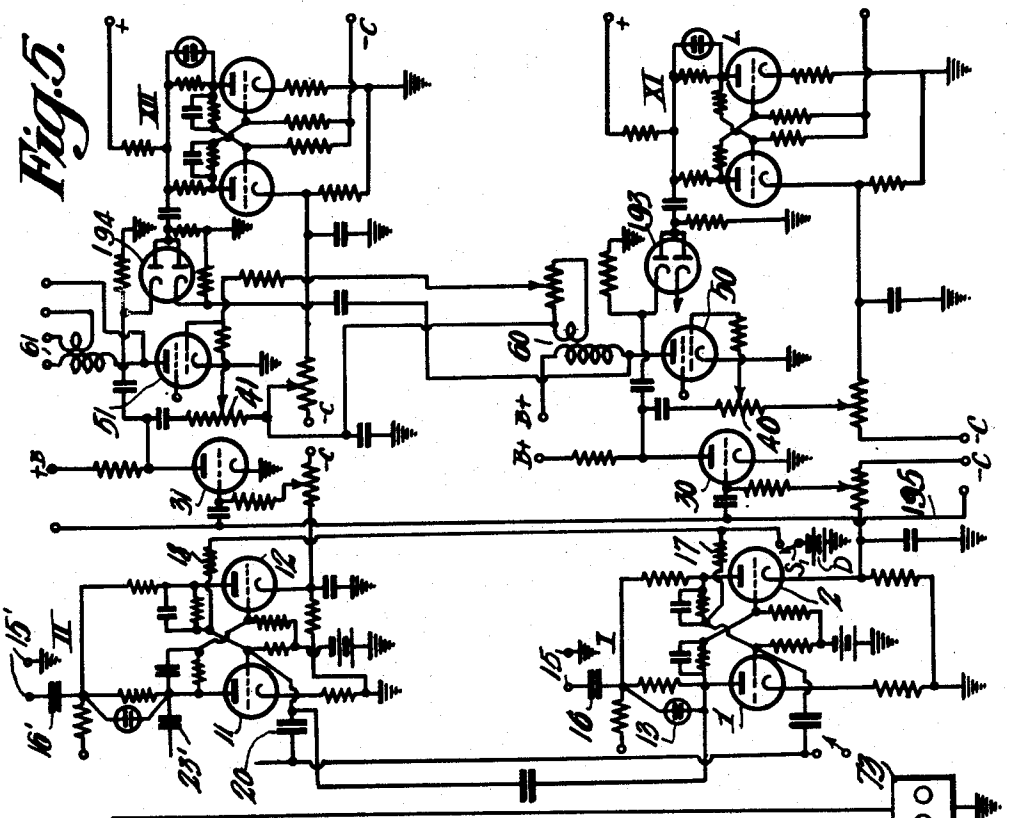
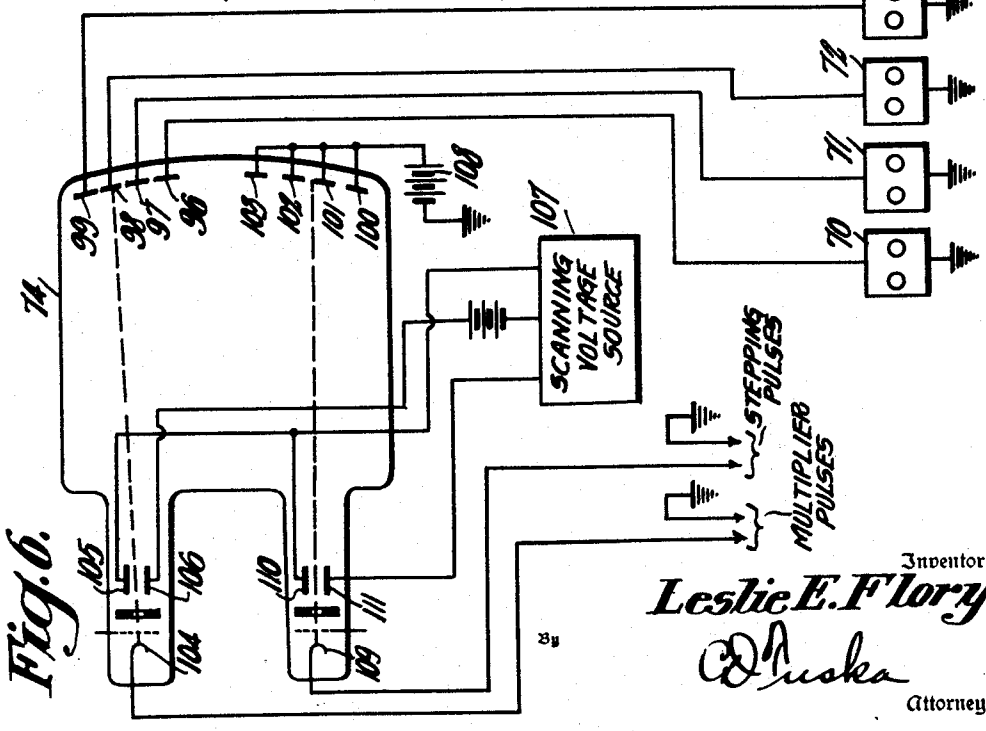


Fig. 6.



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UNITED STATES PATENT OFFICE

2,445,215

ELECTRONIC COMPUTER

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Application October 21, 1943, Serial No. 507,131

12 Claims. (Cl. 235—61)

1

This invention relates generally to electronic computers and particularly to electronic apparatus for counting voltage pulses and for deriving the product of quantities represented by groups of such pulses.

The present application is a continuation-in-part of an application Serial No. 467,229, filed November 28, 1942, now abandoned.

The basic circuit utilized in adapting the invention herein to the various circuits to be described is the well known "trigger" circuit of the general type described in "Theory and Application of Vacuum Tubes" by Herbert J. Reich. In one of its simplest forms, this trigger circuit includes two triodes in which the grid of the first triode is coupled to the anode of the second triode through a network comprising a parallel connected resistor and capacitor, and the grid of the second triode is similarly coupled to the anode of the first triode through a similar coupling network. The cathodes of both triodes are grounded, either directly, or through suitable cathode resistors. Grid and anode potentials are applied to the respective electrodes through separate resistors. If desired, a gaseous discharge tube may be connected across one of the anode resistors to indicate circuit operation.

In operation, if a negative voltage is applied to the grid of the first triode, the anode current of the triode will be reduced and the anode potential will become more positive. Due to the connection through the coupling resistor, the grid potential of the second triode will become more positive, causing an increase in the anode current of the second triode, with a resultant decrease in the second triode anode potential. This decrease in anode potential will, in turn, cause the grid potential of the first triode to become more negative. This action will continue, because of the difference in the potential charges on the coupling capacitors, until the anode current of the first triode is cut off. The first triode will remain cut off, and the second triode will remain conducting, until a positive potential is applied to the grid of the first triode or a negative potential is applied to the grid of the second triode. In either latter instance, the tube operating conditions will be reversed and the first triode will become conducting and the anode current of the second triode will be cut off.

One of the features of the instant invention is the utilization of such trigger circuits in cascade arrangement, whereby a predetermined change in the polarization or activization of one triode of the trigger circuit will generate a pulse to

2

trigger or activate a succeeding trigger circuit in the cascade arrangement. As many trigger circuits as desired may be connected in cascade. The instant invention is a modification of that disclosed in the copending U. S. application of George A. Morton and Leslie E. Flory, Serial No. 459,404, filed September 23, 1942, now Patent No. 2,442,403, granted June 1, 1948, which describes a cascade trigger circuit arrangement for counting voltage pulses to derive a sum in the scale of 10. It is also an improvement on the invention of another copending U. S. application of George A. Morton and Leslie E. Flory, Serial No. 464,292, filed November 2, 1942, now Patent No. 2,409,689, granted October 22, 1946, and entitled "Electronic computing devices." The instant invention, however, is adapted to the direct multiplication of two binary numbers which are applied to the apparatus in the form of groups of potentials. In addition, provision is made for deriving directly the binary product of two or more binary numbers represented by succeeding series of voltage pulses.

In the last mentioned copending application, multiplication is accomplished by deriving the binary sum of a binary multiplicand added to itself a number of items which is equal to the multiplier. In the instant invention, multiplication is accomplished by deriving the binary sum of a binary multiplicand added to the same multiplicand once for each occurrence of a binary 1 in the multiplier, and in which successively added numbers are stepped over one step for each term in the multiplier.

The binary system of computation is particularly suited to electronic computers since a complete binary term of a binary number may be expressed in terms of either the conducting condition or the cut-off condition of the anode circuit of a conventional vacuum tube. A saving in the number of tubes required for a given number is also possible in a ratio of 3 to 1 over the scale of 10 system. A more complete discussion of the binary system of computation may be found in "Elementary Number Theory" by Uspenski and Heaslet.

In order to operate a computer utilizing the binary system, it is necessary to adapt the conventional trigger circuit described heretofore to effect a reversal in polarization or activization by succeeding applied pulses of a similar nature. Some of the circuits to be described hereinafter are adapted to this purpose by applying in a symmetrical manner negative operating pulses to the anode circuits of the trigger tubes.

Among the objects of the invention are to provide a new and improved means for counting voltage pulses. Another object of the invention is to provide improved means for utilizing conventional trigger circuits in a novel cascade arrangement for deriving the product of quantities represented by the numbers of pulses in successive series of voltage pulses. Still another object is to provide an improved means for connecting conventional trigger circuits in cascade arrangement to provide a continuous computer. A further object is to provide improved means for clearing the computer after each operation thereof, for conditioning the circuit for counting succeeding applied pulses. Another object is to provide an improved means for deriving the binary product of two or more binary numbers represented by successive groups of potentials applied to a thermionic tube trigger circuit. Still another object is to provide a new and improved means for deriving the binary product of the binary sums of succeeding series of voltage pulses wherein the multiplicand and multiplier are applied as binary numbers to separate series of cascaded trigger circuits.

The invention will be described by reference to the accompanying drawings, of which Fig. 1 is a schematic circuit diagram of the binary shifting circuit, Fig. 2 is a partial block circuit diagram of one embodiment of the invention, Fig. 3 is a partial block circuit diagram of a second embodiment of the invention, Fig. 4 is a block circuit diagram of the complete embodiment partially shown, in Fig. 2, Fig. 5 is a wiring diagram of a part of the computing system of Fig. 4, and Fig. 6 illustrates the electronic switch through which multiplier and stepping pulses are applied to the computing system of Fig. 4. Similar reference numerals are applied to similar elements throughout the drawings.

Referring to the drawings, Fig. 1 comprises a trigger circuit of the general type described heretofore, which is adapted to the displacement of the multiplicand for successive terms of the binary multiplier. The grid *g1* of a first triode 1 is connected to the anode *p2* of a second triode 2 through a network comprising the parallel connected resistor 5 and capacitor 6. The anode *p1* of the first triode 1 is connected to the grid *g2* of the second triode 2 through a second network comprising the parallel connected resistor 3 and capacitor 4. The cathodes of the first and second triodes 1, 2 are grounded through separate resistors. A source of negative bias potential *c* is connected to the grid *g1* of the first tube 1 through a grid resistor 7, and to the grid *g2* of the second triode 2 through a second grid resistor 8. The positive terminal of the bias source *c* is grounded. Anode potential from a source B is applied to the anode *p1* of the first tube 1 through an anode coupling resistor 9, and to the anode *p2* of the second tube 2 through a second anode coupling resistor 10. The negative terminal of the anode potential source B is grounded.

A gaseous indicator tube 13, which may be a conventional neon tube, is connected across the second anode resistor 9 to indicate when the anode current exceeds a predetermined value, characteristic of the anode current conducting condition of the second tube 2. A choking resistor 14 is connected in series with the positive anode power supply lead to the common terminals of the anode resistors 9 and 10. Negative input control pulses are applied to the input teminals 15 between ground and the common terminal of the anode resistors 9 and 10, through an input coupling capacitor 16.

In operation, if it is assumed that the first tube 1 initially is drawing anode current, the second tube 2 will be biased off. A negative pulse applied to the input terminals 15 will appear on the anode *p2* of the tube 2 and on the grid *g1* of the first tube 1 which will, in turn, reduce the anode current in the first tube 1. This, in turn, will make the potential on the anode *p1* of the first tube 1 more positive, and degenerate simultaneously any of the original negative pulses applied at *p1*. A positive pulse will be applied to the grid *g2* of the tube 2, causing the tube 2 to become conducting. This effect will increase and continue, because of the difference in the potential charges on the capacitors 4 and 6, until the first tube 1 is cut off, and the second tube 2 becomes completely conducting. A subsequent negative pulse applied to the input terminals 15 will cause the stable conditions of the trigger tubes 1, 2 to be reversed since the circuit is completely symmetrical.

The indicator tube 13 will be illuminated when the first tube 1 is conducting, since only under this condition is there an appreciable voltage drop across the anode coupling resistor 9. If it is assumed that the conducting condition of the first tube *p1* represents one, and the conducting condition of the second tube 2 represents zero, the result is a binary set-up system in which zero is indicated on the indicator tube 13 when the tube is extinguished, and one is indicated when the tube is illuminated. The second pulse applied to the input terminals 15 will cut off the second trigger tube 2 and cause the first tube 1 again to become conducting. In order to indicate that two pulses have occurred instead of none, it is essential that a carryover system be employed which will provide a second indication representative of the second term of the binary total. This feature will be described hereinafter in connection with the product computer circuit of Fig. 4. If a carryover circuit is desired for the multiplicand set-up system, it may be of the type described in the second copending application mentioned heretofore. However, to simplify the present description, it is assumed that a binary multiplicand is directly set up on the multiplicand set-up system, through the separate input terminals 15, 15', 15''.

It will be seen that the circuit of Fig. 1 employs three identical trigger circuits connected in a novel cascade arrangement whereby three terms of a binary number may be set up as a binary multiplicand. As illustrated, the circuit comprises three trigger circuits of the general type described heretofore, but it should be understood that as many such circuits as are required for the multiplicand may be connected in cascade arrangement in a similar manner. The first and second trigger tubes 1 and 2, comprising the trigger circuit I and the first indicator tube 13 correspond to the first term of the binary number. The subsequent trigger circuits II and III correspond respectively to the second and third terms of the binary multiplicand. The grids of the tubes 1 and 11 are connected respectively through suitable choking resistors 17 and 18 to a fixed contact of a reset switch S—1. The movable contact of the reset switch S—1 is connected to the negative terminal of a potential source D to provide cut-off grid bias for the tubes 1 and 11 when the switch is closed. The positive terminal of the bias potential source D is grounded.

To accomplish the multiplicand shifting, the shift pulses are applied to the grid *g1* of the first

tube of each of the trigger circuits I, II and III through capacitors 20, 20' and 20'', respectively, which have a capacity of the order of 20 mmf. A coupling capacitor 23, which has a capacity of the order of 100 mmf., connects the anode p1 of the first tube 1 of the trigger circuit I to the grid of the first tube 11 of the second trigger circuit II. A similar capacitor 23' couples the anode of tube 11 to the grid of tube 21.

Assuming the reset switch s1 to be open and the tube 2 to be conducting, the application of a negative pulse at the terminals 15 causes current to be transferred from the tube 2 to the tube 1, thereby illuminating the indicator 13. A second negative impulse similarly applied transfers current from the tube 1 to the tube 2. Negative pulses applied to terminals 15' and 15'' similarly affect the units II and III.

The multiplicand shifting operation of the circuit, in response to shift pulses derived from each term of the binary multiplier, may be described as follows: Assume that the grids of the trigger tubes 1 and 11 are at positive potential and that the grid of the trigger tube 21 is at negative potential. This will mean that the condition of the circuit may represent the binary number 011. A negative shift pulse is applied to the grids of all three of the trigger tubes 1, 11 and 21 through the respective capacitors 20, 20' and 20''. The anode current of the tube 1 will be cut off, thereafter indicating binary 0, and a positive pulse will be applied to the grid of tube 11 through the capacitor 23. The negative shift pulse will also start to make the tube 11 non-conducting, thereby causing a positive pulse to be applied from its anode through the relatively large capacitor 23' to the grid of the tube 21 and making this tube conductive. The tube 11 does not reach a stable conducting condition, however, due to a positive impulse which is applied to it from the anode of the tube 1 when this tube becomes non-conducting. Therefore, the circuit condition will now represent the binary number 110, or, in other words, the number 011 has been moved one digital position to the left. This method is applied, as described hereinafter, to shift the multiplicand, or the product.

One method of multiplying two binary numbers is schematically illustrated in Fig. 2. A binary multiplicand is set up, in any known manner, on the trigger circuits I, II, III, IV of the multiplicand set-up system, which comprises a plurality of trigger circuits connected as described in Fig. 1. A multiplier pulse is derived from a multiplier set-up system for each binary 1 term therein. A shift pulse is also derived from the multiplier set-up system for each term in the multiplier.

The multiplier pulses are transmitted to a product totalizer including the trigger circuits XI, XII, XIII, XIV, XV, XVI and XVII for each term of the multiplicand which happens to be binary 1. The means for accomplishing this is described in detail in the second copending application referred to heretofore and is included hereinafter under the description of Fig. 4.

As each term of the multiplier, from the lowest to the highest, either delivers a multiplier pulse or fails to do so, depending upon the binary value of the term, a second or shift pulse is derived which is applied to the circuit described in Fig. 1 to shift the multiplicand one place for each term in the multiplier. It will therefore be seen that the product totalizer will provide the sum of the multiplicand transferred a number of times and occupying places which correspond to the number and place occurrence of binary 1 terms in the multiplier.

The operation of Fig. 3 is similar to Fig. 2 with the exception that the shift pulses are applied to the product totalizer. In this arrangement, trigger circuits XI, XII, XIII, XIV, XV, XVI and XVII, which are interconnected as described in Fig. 1, are used in the product totalizer instead of in the multiplicand set-up system, as in Fig. 2. Carryover amplifiers 50, 51, 52, 53, 54, 55, and 56, described hereinafter, in Fig. 4, are interconnected between successive trigger circuits of the totalizer.

The multiplier shift pulses are applied to the product totalizer through the capacitors 20, 20', 20'' to shift the intermediate product back one place between each successive multiplier pulse, or absence of a pulse, corresponding to successively higher terms in the multiplier.

In order to prevent a short circuit of product carryover pulses due to by-passing the carryover amplifiers 50, 51, 52, 53, 54, 55, 56 by the capacitors 23, 23', 23'', etc. of the shifting circuit, amplifiers 85, 84, 83, etc. are inserted in series with the capacitors 23, 23', 23'', etc. respectively. These amplifiers are normally biased below cut-off, but are connected to the source of shifting pulses, which pulses reduce the amplifier bias just to cut-off during the duration of the shift pulse. Since the multiplier pulses are interspersed between the shifting pulses, the amplifiers present a high impedance shunt circuit to the carryover pulses. A similar arrangement could be used in the multiplicand trigger circuits if these circuits are also to be used as a set-up system for establishing the binary multiplicand from a source of pulses.

Fig. 4 comprises a block diagram of an electronic multiplying system wherein a multiplicand is set up as a binary number on a series of cascaded trigger circuits of the general type described heretofore. The binary multiplicand is then transferred to a second binary totalizer upon which the binary product is derived. The circuits to be described hereinafter accomplish both the direct transfer of the multiplicand to the product totalizer and the carryover operation required as each element of the product totalizer changes from one to zero in the binary system. Each of the trigger circuits I, II, III, IV, V, VI and VII of the multiplicand set up system is connected, through leads 90, 91, 92, etc., to a corresponding transfer amplifier 30, 31, 32, 33, 34, 35 and 36, respectively, in such a manner that when the set-up system trigger circuit is in the binary zero condition, the amplifier tube is biased well beyond cut-off and when the set-up system is in the binary 1 condition, the corresponding amplifier is biased just to the anode current cut-off condition.

Pulses are applied as described heretofore, to the input terminals 15, 15', 15'', 15''' of the multiplicand binary set-up system to establish the multiplicand as a binary quantity on, for example, the trigger circuits I, II, III and IV. Pulses which correspond to the presence of binary 1 terms of the binary multiplier are successively applied simultaneously to all of the respective grid circuits of the transfer amplifiers 30, 31, 32, 33, 34, 35 and 36. Means for deriving the pulses 40 from a binary multiplier will be described hereinafter. The multiplier pulses will be transmitted by only the transfer amplifiers which are biased to cut-off and which are connected to the corre-

sponding multiplicand trigger circuits in the binary 1 condition. The pulses transmitted by the respective transfer amplifiers are next applied to separate differentiating circuits 40, 41, 42, 43, 44, 45 and 46, respectively, from which are derived a positive pulse 47 and a negative pulse 48, separated by the width of the multiplier pulses 49. These pulses are next applied directly to the product binary totalizer comprising the trigger circuits XI, XII, XIII, XIV, XV, XVI, XVII and XVIII, respectively. The positive pulse 47 is utilized to accomplish the carryover operation between successive product totalizer trigger circuits whenever it is applied to one of the trigger circuits which is in the binary 1 condition. The negative pulse 48 is utilized to trigger the corresponding product binary trigger circuit to the next binary number. Both negative and positive pulses 48 and 47, respectively, are applied to the input of a second group of transfer amplifiers 50, 51, 52, 53, 54, 55 and 56, respectively, which are connected to the corresponding product trigger circuits. The second transfer amplifiers are connected by the leads *m* so that they are inoperative when the corresponding product trigger circuit is in the binary zero condition, and are just cut off when the corresponding trigger circuit is in the binary 1 condition. The outputs of the second transfer amplifiers are connected by the leads *n* to trigger the next succeeding trigger circuits of the product counter. It will therefore be seen that if the first product trigger circuit XI is in the binary 1 condition, the transfer amplifier 50 will be just cut off. The positive pulses 47, applied to the input of the transfer amplifier, will therefore provide a negative pulse in the lead *n* to the second product trigger circuit XII. The negative pulse 48, which immediately follows the positive pulse 47, will then trigger the first product trigger circuit XI to the binary zero condition by means of the directly transmitted pulse over the connection *k*.

A condition may arise, for example, where successive carryover pulses are applied to successive circuits in which no positive or negative pulses 47, 48 exist due to the fact that the corresponding term in the multiplicand is binary zero, and the corresponding product trigger circuit is initially also in the binary zero condition. This condition is now considered in connection with Fig. 5, which is identical with Fig. 3 of the aforesaid copending application Serial No. 464,292 and has its corresponding parts indicated by the same reference numerals as those of the previous figures. As pointed out in Serial No. 464,292, the function of the diodes 193 and 194 is to transmit impulses to the totalizer units XI and XII and to prevent reaction on preceding trigger circuits due to pulses in subsequent binary term trigger circuits. Other functions performed by the circuit of Fig. 5 will be understood from the previous explanation and from the following statement of its operation.

It is assumed as a starting condition that the unit I is in a binary one condition and the units II, XI and XII are in a binary zero condition. Under these conditions, the transfer amplifier 30 is biased to cut off and the amplifiers 31, 50 and 51 are biased beyond cut off.

The first multiplier pulse (applied through lead 195) operates through 193 to change the unit XI to a binary one condition and to bias the amplifier 50 to cut off.

The second multiplier pulse operates through 50 and 194 to change the unit XII to a binary one

condition and to bias the amplifier 51 to cut off and through 193 to change the unit XI to a binary zero condition, the count now being 10 or 2 in the decimal system.

The third multiplier pulse operates through 193 to change the unit XII to a binary one condition and to bias the amplifier 50 to cut off, the count now being 11 or 3 in the decimal system.

The fourth multiplier pulse operates through the transformer 60 and the amplifier 51 to change the unit XIII to a binary one condition, through 194 to change the unit XII to a binary zero condition and through 193 to change the unit XI to a binary zero condition, the count now being 100 or 4 in the decimal system.

Further steps in the operation of the computing system will be understood without detailed explanation.

The number of trigger circuits utilized in the multiplicand set up system will be equal to the sum of the numbers of binary terms in the multiplicand and the multiplier. The number of trigger circuits required in the product totalizer will be one more than the sum of the number of binary terms in the multiplicand and multiplier, respectively. Indicator lamps may be connected in the anode circuits of the individual trigger circuits of the product totalizer in the same manner as described heretofore in Figure 1 for the individual trigger circuits of the multiplicand set-up system. Likewise, the anode circuits of the product totalizer may be connected to apply the binary product directly to other utilization circuits.

The multiplier, which may be in the form of potentials representative of a binary number, is applied directly to a multiplier set-up system comprising a plurality of trigger circuits 70, 71, 72, 73, of the type described in Fig. 1, with the exception that the capacitors 20, 20', 20'' and 23, 23', 23'' are omitted. Potentials indicative of either the binary 0 or the binary 1 conditions of the individual multiplier trigger circuits 70, 71, 72, 73 are applied to stationary contacts of an electronic switch or distributor 74. The switch 74 and its various connections is shown by Fig. 6. It includes a plurality of fixed contacts 96 to 99 which have their respective potentials controlled by the multiplier units 70 to 73 and which receive a beam of electrons from a cathode 104, the position of this beam being determined by the potentials applied to the deflecting electrodes 105—106 from a scanning voltage source 107. Multiplier pulses thus derived are applied to the transfer amplifiers 30 to 36 of Fig. 4.

The switch 74 also includes fixed contacts 100 to 103 which are subjected to the potential of a source 108 and which cooperate with a cathode 109 and deflectors 110 and 111 (connected to the source 107) to generate stepping pulses which are applied to the units I to VII of Fig. 4 for stepping the multiplicand one step along the multiplicand set-up system after the application of each multiplier pulse to the transfer amplifiers. The scanning may be accomplished by applying scanning potentials of any desired frequency to beam deflecting elements. The switch should preferably be so arranged that one scanning beam slightly leads the other scanning beam, in order that two separate distinctive pulses may be derived from each multiplier trigger circuit, followed by additional pairs of pulses derived from each of the succeeding multiplier trigger circuits. A negative multiplying pulse 49, which is preferably of square wave form, is thereby derived from one beam of

the electronic switch 74 each time a contact connected to a multiplier trigger circuit in the binary 1 condition is scanned.

In addition, stepping pulses 58, also preferably of square wave form, are derived from the other beam of the electronic switch each time this beam passes over the individual contacts of the second group. Thus, as the switch covers the contacts connected to the individual multiplier trigger circuits, a multiplying pulse is derived, providing the multiplier term is binary 1, for keying the transfer amplifiers 30 to 36 which happen to be unblocked by the respective multiplicand trigger circuits. Immediately thereafter, and irrespective of the condition of the particular multiplier trigger circuit, a second pulse 58 is derived from the switch, and applied to all of the multiplicand trigger circuits I, II, III, IV, V, VI, VII to step the multiplicand along the multiplicand counter. After the beams of the switch 74 have scanned all of the switch contacts, no more pulses 49, 58 are derived until a new multiplier is set up on the multiplier counter.

Any other well known electronic or mechanical sequential switching means may be employed, providing two separate and distinctive pulses may be obtained for each term of the multiplier in proper sequence to provide both transfer and shifting of the multiplicand as described heretofore.

All trigger circuits may be cleared after each multiplying operation is completed by applying a high negative bias simultaneously to all binary 1 tubes in the manner which is described in Fig. 1.

Thus the invention described comprises an electronic multiplying device in which the multiplicand is applied to a cascaded binary counter and transferred to a second or product binary totalizer, a number of times corresponding to the binary 1 terms in the multiplier, while simultaneously the multiplicand is shifted a number of times equal to the number of terms in the multiplier. Provision may be made in both the setup and totalizing systems to accomplish binary carry-over operations where required, and to segregate the carryover operation from the direct application of the multiplicand to the product totalizer.

I claim as my invention:

1. The combination of means for producing potentials representative of a multiplicand, a totalizer for establishing potentials representative of a product, means for applying pulses representative of a multiplier, amplifier means biased to conditions dependent on said multiplicand-representative potentials and responsive to said pulses for transferring said multiplicand to said totalizer once for each occurrence of a predetermined digit in said multiplier, and means for changing the relation between said multiplicand and product potentials by one digital position once for each digital position of said multiplier.

2. The combination of means for producing potentials representative of a multiplicand, a totalizer for establishing potentials representative of a product, means for establishing potentials representative of a multiplier, means including a capacitor and a resistor responsive to said multiplicand and multiplier potentials for transferring said multiplicand to said totalizer once for each occurrence of a predetermined digit in said multiplier, and means for shifting said multiplicand potentials by one digital position once for each digital position of said multiplier.

3. The combination of means for producing potentials representative of a multiplicand, a totalizer for establishing potentials representative of a product, means for establishing potentials representative of a multiplier, means including a capacitor and a resistor responsive to said multiplicand and multiplier potentials for transferring said multiplicand to said totalizer once for each occurrence of a predetermined digit in said multiplier, and means for shifting said product potentials by one digital position once for each digital position of said multiplier.

4. The combination of means for producing potentials representative of a multiplicand, a totalizer for establishing potentials representative of a product, means for establishing potentials representative of a multiplier, means including an amplifier biased to cutoff and beyond cutoff in response to potentials representing a digit 1 and a digit 0 of said multiplicand for transferring said multiplicand to said totalizer once for each occurrence of one of said digits in said multiplier, and means for changing the relation between said multiplicand and product potentials by one digital position once for each digital position of said multiplier.

5. The combination of means for producing potentials representative of a multiplicand, a totalizer for establishing potentials representative of a product, means for establishing potentials representative of a multiplier, and means including an electronic switch for transferring said multiplicand to said totalizer once for each occurrence of a predetermined digit in said multiplier and for changing the relation between said multiplicand and product potentials by one digital position once for each digital position of said multiplier.

6. The combination of a plurality of successive units each including a pair of electron discharge devices having anode and control electrodes and each operable to produce potentials representative of either of two digits, means for polarizing said units to provide successive potentials representative of the successive digits of a number, and means connected between the anode electrode of one of said units and the corresponding control electrode of a succeeding one of said units for shifting said digital representative potentials by one digital position.

7. The combination of a plurality of successive units each including a pair of electron discharge devices having anode and control electrodes and each operable to produce potentials representative of either of two digits, means for polarizing said units to provide successive potentials representative of the successive digits of successive numbers, carry over means connected between said units for totalizing said numbers, and means connected between the anode electrode of one of said units and the control electrode of a corresponding device of a succeeding one of said units for shifting said digital representative potentials by one digital position.

8. The combination of means for producing potentials in sets each representative of a different number, amplifying means biased to cut-off in response to the occurrence of one digit in the first of said numbers and beyond cut-off in response to the occurrence of another digit in said first number, means for applying to said amplifying means one after the other the potentials of that set which is representative of the second of said numbers, and means for shifting by one digital position that set of potentials which is representative of said first number.

9. The combination of means for producing po-

tentials in sets each representative of a different number, amplifying means biased to cut-off in response to the occurrence of one digit in the first of said numbers and beyond cut-off in response to the occurrence of another digit in said first number, means for applying to said amplifying means one after the other the potentials of that set which is representative of the second of said numbers, and means for changing by one digital position the relation between that set of potentials which is representative of said first number and that set of potentials which is representative of the third of said numbers.

10. The combination of a plurality of trigger circuits each including a pair of electron discharge devices having a cathode and anode and an electrode for controlling the current between said cathode and anode, means for establishing in successive ones of said circuits potentials representative of the successive digits of a number, and means coupling the anode of the electron discharge device of one trigger circuit to the control electrode of the corresponding electron discharge device of a succeeding one of said trigger circuits for shifting said digital representative potentials by one digital position.

11. The combination of a plurality of trigger circuits each including a pair of electron discharge devices having a cathode and anode and an electrode for controlling the current between said cathode and anode, means for establishing

in successive ones of said circuits potentials representative of the successive digits of a number, and means including a capacitor coupling the anode of the electron discharge device of one trigger circuit to the control electrode of the corresponding electron discharge device of a succeeding one of said trigger circuits for shifting said digital representative potentials by one digital position.

12. The combination of a plurality of successive units each including a pair of elements having anode and control electrodes and each operable to produce either of two potentials, means for polarizing said units to provide potentials representative of different digits in a series of numbers, and means connected between the anode electrode of one of said units and the corresponding control electrode of a succeeding one of said units for shifting said potentials by one digital position.

LESLIE E. FLORY.

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