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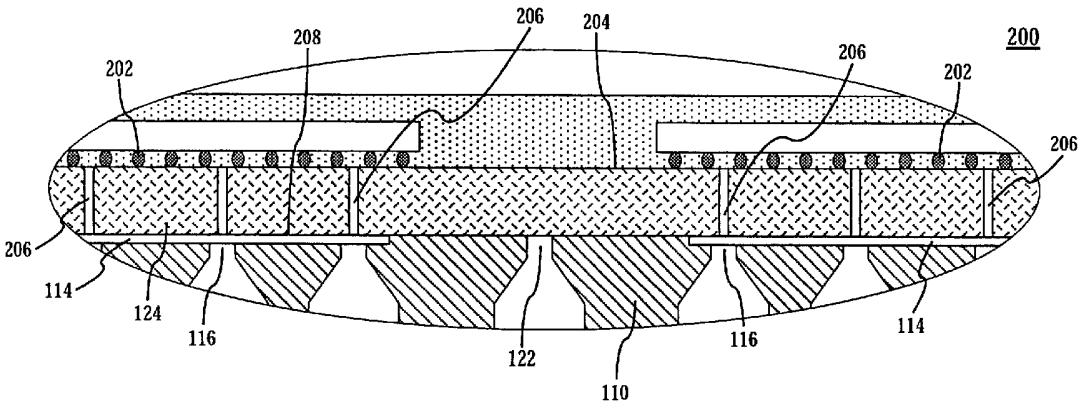
(54) Title: METHOD AND APPARATUS FOR FORMING A FLIP CHIP SEMICONDUCTOR PACKAGE AND METHOD FOR PRODUCING A SUBSTRATE FOR THE FLIP CHIP SEMICONDUCTOR PACKAGE



(57) Abstract: Specifications of a flip chip package and mold compound for a package are provided to a mold flow simulator and locations of void formation in the package during molding, identified. Subsequently, a substrate (124) for the package is designed with vias (206) at the locations of void formation. During molding, air pockets at the locations of void formation escape through the vias (206) and vents (116) in the lower cavity bar (110), as mold compound flows between the die and the substrate (124) and forces the air out. In addition, the lower cavity bar (110) has a down set central location (114), which allows air to pass from the vias (206) to the vents (116). In addition, as the diameter of a via (206) is between 20-30 microns, more area on the lower surface of the substrate (124) is available for terminals arranged in an array.

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METHOD AND APPARATUS FOR FORMING A FLIP CHIP SEMICONDUCTOR PACKAGE AND METHOD FOR PRODUCING A SUBSTRATE FOR THE FLIP CHIP SEMICONDUCTOR PACKAGE

Field of the Invention

The present invention relates to forming a flip chip semiconductor package and a substrate therefor, and more particularly to molding a flip chip semiconductor package with the substrate.

Background of the Invention

As is known, a flip chip semiconductor package is one where a bumped semiconductor die is flipped over with its pattern of pads directly connected by the bumps, after reflow, to a corresponding pattern of terminals on a substrate. The assembly of die, bumps or interconnects and substrate is then molded on the substrate to encapsulate the die and bumps in mold compound. The molded package protects the die and the bumps, and allows the package to be conveniently handled. In addition, the molded package must withstand a range of operating conditions including operating at elevated temperatures.

A difficulty when molding flip chip packages is the formation of voids between the die and the substrate. Voids are pockets of air that are trapped when the mold compound flows between the die and the substrate and between the bumps, and, as is known to one skilled in the art, can adversely affect the reliability of a molded semiconductor package. There aren't any universally accepted criteria for measuring voids, however, based on a particular package and the requirements of the user of that package, a ratio of area covered by voids to total area between the die and substrate is sometimes specified as a criteria.

A method of molding a flip chip semiconductor package with a view to reducing the formation of voids is disclosed by Weber in US Patent No. 6,038,136, assigned to Hestia Technologies, Inc. of the USA. Weber teaches a mold having upper and lower cavity bars between which a flip chip package is molded on a substrate. The substrate has a single vent hole therethrough, which is centrally located; and the lower cavity bar, on which the substrate is held, has an overflow channel that is aligned with the vent hole in the substrate. The upper cavity bar has a cavity in which the flipped semiconductor die, mounted on the substrate, is enclosed when the upper and lower cavity bars come together. During molding, mold compound is injected into the cavity, and the mold compound fills the cavity surrounding the semiconductor die, and is forced into the gap between the semiconductor die and the substrate. The mold compound then flows radially inwards from each of the edges of the semiconductor die until it reaches the vent hole. The mold compound then passes through the vent hole and into the overflow channel, filling the overflow channel and forming an overflow bead on the lower surface of the substrate. The vent hole allows air between the semiconductor die and the substrate to escape as the mold compound is forced therebetween. This is intended to prevent air pockets from becoming trapped between the semiconductor die and the substrate, and thereby reducing the formation of voids. In addition, Weber teaches the use of multiple vent holes in the substrate.

When molding a particular flip chip semiconductor package, for example one having a particular semiconductor die size and a particular number of interconnects, it has been found that voids are formed relatively consistently at particular locations as the mold compound flows between the semiconductor die and the substrate. A possible cause of such void formation may be that air pockets are trapped against the sides of interconnects as the mold compound flows around the interconnects.

Hence, a disadvantage of Weber's method is that air pockets trapped around the interconnects that are located close to the vent hole can escape through the vent hole, and air pockets that are not located close to the vent hole remain trapped between the semiconductor die and the substrate.

Another disadvantage of the Weber method is the formation of the overflow bead on the lower surface of the substrate. The overflow bead consumes precious surface area of the substrate, reducing the available area for ball or pin grid array terminals for mounting and coupling the molded semiconductor package, as required by the growing densities of package inputs and outputs.

Yet another disadvantage of Weber is the relatively large size of the vent hole with a diameter in the range of 152 to 500 micrometers or microns ($1X10^{-6}$ meters). Again, the large dimension of the vent hole consumes substrate real estate that can otherwise be used for inputs and outputs on a molded semiconductor package.

A still further disadvantage of Weber is the need for a lower cavity bar having the overflow channel therein, and the complexities and cost of fabricating and using a variety of lower cavity bars for a variety of molded semiconductor packages, as the vent holes in the substrate and the overflow channel in the lower cavity bar must be aligned.

Brief Summary of the Invention

The present invention seeks to provide a method and apparatus for forming a flip chip semiconductor package and method and apparatus for producing a substrate for the flip chip semiconductor package, which overcomes, or at least reduces, the abovementioned problems of the prior art.

Accordingly, in one aspect, the present invention provides at least one mold piece for molding at least one semiconductor package, the at least one mold piece comprising:

a molding surface for receiving a substrate, the substrate having at least on via therethrough, and the substrate having at least one semiconductor die flip chip mounted thereto; and

at least one vent therein which extends from the molding surface, the at least one vent for pneumatically coupling to the at least one via.

In another aspect the present invention provides a method for molding at least one flip chip semiconductor package, the method comprising the steps of;

a) providing at least one substrate having a plurality of vias therethrough, the plurality of vias being at predetermined locations;

b) flip chip mounting at least one semiconductor die to the substrate;

c) providing at least one mold piece having a molding surface for receiving the substrate, the at least one mold piece having a plurality of vents extending from the molding surface;

d) disposing the substrate with the at least one semiconductor die thereon on the molding surface;

e) enclosing the substrate in a mold cavity formed by another molding surface of at least another mold piece; and

f) injecting mold compound into the mold cavity, and thereby expressing air from between the at least one substrate and the at least one semiconductor die through at least some of the plurality of vias and at least some of the plurality of vents.

In yet another aspect the present invention provides a method for producing a substrate for forming at least one flip chip semiconductor package, the method comprising the steps of:

a) simulating molding the at least one flip chip semiconductor package to produce simulation results indicating locations of void formation within the at least one flip chip semiconductor package;

b) selecting some of the locations of void formation; and

c) fabricating the substrate with vias at the selected locations of void formation.

Brief Description of the Drawings

An embodiment of the present invention will now be fully described, by way of example, with reference to the drawings of which:

FIG. 1 shows a side sectional view of a molding apparatus in accordance with the present invention;

FIG. 2 shows an enlarged view of a portion of the molding apparatus in FIG.1;

FIG. 3 shows a plan view of the lower cavity bar I FIG. 1;

FIG. 4 shows a plan view of the upper cavity bar I FIG. 1;

FIG. 5 shows a flowchart of a molding process using the molding apparatus in FIG. 1;

FIG. 6 shows the flow of mold compound within the mold cavity of the molding apparatus in FIG. 1;

FIG. 7 shows a flowchart of a process for producing the substrate in FIG. 1; and

FIG. 8 shows results of a simulation in accordance with the flowchart in FIG. 7.

Detail Description of the Drawings

For a particular molded semiconductor package, the specifications of the package and the mold for forming the package are provided to a mold flow simulator that identifies the locations of void formation in the package. Subsequently, a substrate for the particular package is

designed with vias at the locations of void formation. During molding, air pockets at the locations of void formation escape through the vias and vents in the lower cavity bar, as mold compound flows between the die and the substrate and forces the air out. In addition, the lower cavity bar has a down set central location coupled to the vent, hence avoiding the need to align the vias in the substrate with the vent as the down set allows air to pass from the vias to the vent wherever the vias are located within the downset area. Further, a lower cavity bar with a particular downset may be used for a variety of substrates of the same size but having different via locations. In addition, as the lower cavity bar does not have an overflow channel, as in the prior art, and the diameter of a via is between 20 –30 microns, more area on the lower surface of the substrate is available for terminals arranged in an array.

FIG. 1 shows a portion of a molding apparatus 100 comprising an upper mold piece or upper cavity bar 105 and a lower mold piece or lower cavity bar 110. As is known by one skilled in the art, the upper cavity bar 105 is mounted to an upper portion of a press (not shown), and the lower cavity bar 110 is mounted to a lower portion of a press (not shown). In a conventional molding press, the upper portion is not movable and the lower portion moves in a vertical direction between an upper molding position and a lower open position. Consequently, the lower mold piece 110 is moved vertically between a lower open position and a raised molding position. The raise molding position is shown.

The lower cavity bar 110 has an upper surface 112, with downset portions 114, one for each of the semiconductor packages being formed. The downset portions are 15-20 microns recessed in the upper surface 112 of the lower cavity bar 110. Each of the downset portions 114 has a number of vents 116 that extend from the downset portions 114 through the lower cavity bar 110, to a channel 118. The channel 118 is, in turn, coupled to an outlet 120. In addition, vacuum

inlets 122 in the upper surface of the lower cavity bar 110 are coupled to a vacuum source (not shown) to secure a substrate 124 on the lower cavity bar 110. It will be appreciated that here the vents 116 and the vacuum inlets 122 are coupled to the channel 118. Consequently, a vacuum is applied to the vacuum inlets and the vents 116. In an alternative embodiment of the present invention, only the vacuum inlets 122 may be coupled to apply a vacuum, while the vents 116 are not coupled to apply a vacuum. The vents may be left open to ambient air pressure or coupled to an alternative vacuum source to apply a different vacuum force than that applied at the vacuum inlets 122. On the substrate 124 are three semiconductor dies 126 that are flip-chip mounted thereto. A more detailed description of the flip chip mounting will be provided later. The package that is being molded here is similar to what is referred to as a quad-flat-non-leaded (QFN), where a number of semiconductor dies are encapsulated in a single molding, and subsequently singulated to produce individual semiconductor packages.

The upper cavity bar 105 has a lower surface 128 that forms a molding cavity 130 with the substrate 124, when the upper and lower cavity bars 105 and 110 are in the molding position. The lower surface 128 also includes a gate 132, which lies between a cull 134 and the cavity 130. In the molding position, the three semiconductor dies 126 are enclosed in the cavity 130. A plunger 138 moves in a vertical direction to force mold compound in the cull 134 into the cavity 130. A location 136 opposite the gate 132, includes a vent at the end of the cavity 130 as is known in the art, and no further details are provided herein.

FIG. 2 shows an enlarged view of a portion 200 of the upper and lower cavity bars 105 and 110. Interconnects 202 mount the semiconductor dies 126, and electrically couple the pads (not shown) on the flipped dies 126 to terminals (not shown) on the upper surface 204 of the substrate 130. The interconnects 202 are sometimes

referred to as bumps, and are typically formed on the pads of the semiconductor dies 126. The dies 126 are then flipped over and the bumps 126 aligned with the terminals before the dies are placed on the substrate 124. A subsequent reflow process causes the bumps 202, typically made of solder, to melt and couple the pads to the terminals. The bumps may be made of a variety of materials, and a layer of solder is usually incorporated into the structure of the bump.

As mentioned above, the vents 116 are coupled to the downset portions 114, and the substrate 124 has vias 206 that extend from the upper surface 204 of the substrate to the lower surface 208, which is within the downset portions 114. The vias 206 are located between the interconnects 202 at predetermined locations, hence when vacuum is applied at the predetermined locations through the vias, the vacuum advantageously removes pockets of air and reduces the formation of voids at the predetermined locations.

FIG. 3 shows the lower cavity bar 110 indicating the downset portions 114 with outlines 302 of the semiconductor dies 126 overlaid. The downset portions 114 are made smaller than the outlines 302 of the semiconductor dies 126 to ensure sufficient support for the portion of the substrate 124 below the semiconductor dies 126.

FIG. 4 show the upper cavity bar 105 with outlines 402 of the semiconductor dies 126 overlaid, indicating the position of the semiconductor dies 126 within the cavity 130.

With additional reference now to FIG. 5, a process 500 for molding a semiconductor package in accordance with the present invention, starts 505 with disposing 510 bumped semiconductor dies 126 on the substrate 124 having the corresponding pattern of pads thereon and the vias 206 at the predetermined locations. The semiconductor dies 126 and the substrate 124 are then reflowed 515 in a reflow chamber causing the bumps to form the interconnects 202. The assembly of the substrate 124 and the semiconductor dies 126 is then disposed 520 on the upper surface 112 of the lower cavity bar

110. Both the upper and lower cavity bars 105 and 110 are preheated and maintained at an elevated molding temperature. There will of course be the necessary alignment features such as locating pins on the upper surface 112, and corresponding apertures in the substrate 124 to ensure proper location of the substrate 124.

Next, the upper and lower cavity bars 105 and 110 are brought 525 together, enclosing the semiconductor dies 126 in the molding cavity 130 formed by the molding surface 128 of the upper cavity bar 105, and the substrate 124. With a deposit of mold compound in the cull 134, the plunger 138 moves upwards compressing the mold compound, and under the imposed heat and pressure, the mold compound changes to a molten liquefied state. The molten compound is injected 530 from the cull 134 through the gate 132 and into the cavity 130. With reference to FIG. 6, the arrows show the flow of the mold compound within the cavity 130. The flow of the mold compound exhibits what is sometimes called a wrapping effect. This is where the mold compound flows around the semiconductor dies 126 and then, after surrounding the semiconductor dies 126, begins flowing inwardly between the semiconductor dies 126 and the substrate 124, thus filling 535 the gap between the semiconductor dies 126 and the substrate 124.

Air in air pockets 605 trapped between the semiconductor dies 126 and the substrate 124 are gradually forced out through the vias 202 by the flow of mold compound, through the downset portions 114 and the vents 116. Where a vacuum is employed, the flow of the mold compound and the displacement of the air in the air pockets 605 is further enhanced. Thus, advantageously facilitating the flow of the mold compound between the semiconductor dies 126 and the substrate 124, and reducing the formation of voids. The mold compound continues to flow between the semiconductor dies 126 and the substrate 124 and then into the vias 116. The mold compound can

flow through the vias 116 and form dimples at the opening of the vias on the lower surface of the substrate 124.

The mold compound is then allowed 540 some time to set, as determined by a variety of parameters including the type of mold compound that is used. The upper and lower cavity bars 105 and 110 are subsequently separated 545 and the molded semiconductor packages, now being a part of a single molding, is removed 550 from the lower cavity bar 110, and the molding process 500 ends 555. As is known a singulation process follows to produce the individual semiconductor packages.

With reference to FIG. 7 a process 700 for fabricating a substrate with the vias at the predetermined locations starts 705 with simulating 710 molding the particular semiconductor package using a computer program to determine the mold flow pattern when molding that package using the upper and lower cavity bars 105 and 110, and a particular mold compound. Examples of such simulation software applications are C-MOLD by Exicad Corporation of the USA, and MOLD-FLOW of Australia. From the simulation results, the next step is to determine 715 the locations of voids in the package, and determine 720 the fillet size of the particular mold compound, for example 10-20 microns. It will be appreciated by one skilled in the art that voids are discernible from the simulation results, as the primary purpose of such simulation programs is determining the location of voids. The fillet size of the mold compound on the other hand is a part of the specification of the mold compound, and is readily determined from the manufacturer. FIG. 8 shows the results of a simulation indicating the locations of voids 805. There is a tendency for the voids to occur in central locations between the semiconductor dies 126 and the substrate 124.

The location of the voids provide an indication of the locations, sometimes referred to as target locations, where vias are required in the substrate; while the fillet size of the mold compound will

determine the size of the vias e.g. the diameter. With this information, the substrate is then fabricated 730 using conventional processes to form the vias having the required dimensions at the target locations, and the process 700 ends 735.

Although the simulation results indicate the locations of the voids, there are compromises that need to be made when actually selecting the location of the vias. Considerations that have to be made are, the tolerance of the simulation results, the availability of space on the substrate for the vias, the layout of runners in the substrate, the size of the voids, the number of vias required, and the costs of adding the vias to a substrate. There is also a limit to the number of vias that may be provided for each semiconductor package as vias are openings in the package that can allow moisture into the package and adversely affect the reliability of the package. Hence, the size of the die and the type of semiconductor package also affect the number and size of vias on a substrate in a semiconductor package. With a die size of 11.8 square millimeters (mm^2), two to three vias are required for each die, and the vias each have a diameter of 20-30 microns.

Hence, the present invention, as described, provides a method of molding a flip chip semiconductor package that reduces the formation of voids in the semiconductor package.

This is accomplished by simulating the molding of the semiconductor package to determine the locations of void formation, and then fabricating a substrate for the semiconductor package with vias at the locations of void formation. In addition, a mold piece for molding the semiconductor package is made with vents that allow air at the locations of void formation. When the semiconductor package is formed using the substrate and the mold piece, air from the locations of void formation flows through the vias to the vents, during molding.

The present invention therefore provides a method and apparatus for forming a flip chip semiconductor package and method

for producing a substrate for the flip chip semiconductor package, which overcomes, or at least reduces, the abovementioned problems of the prior art.

It will be appreciated that although only one particular embodiment of the invention has been described in detail, various modifications and improvements can be made by a person skilled in the art without departing from the scope of the present invention.

Claims

1. At least one mold piece for molding at least one semiconductor package, the at least one mold piece comprising:

a molding surface for receiving a substrate, the substrate having at least on via therethrough, and the substrate having at least one semiconductor die flip chip mounted thereto; and

at least one vent therein which extends from the molding surface, the at least one vent for pneumatically coupling to the at least one via.

2. At least one mold piece in accordance with claim 1, wherein the at least one via comprises a plurality of vias at predetermined locations of the substrate, wherein the at least one vent comprises a plurality of vents, and wherein at least some of the plurality of vias at predetermined locations of the substrate are pneumatically coupled to at least some of the plurality of vents.

3. At least one mold piece in accordance with claim 1 wherein at least a portion of the molding surface is downset, and wherein the at least one vent is located within the downset portion.

4. At least one mold piece in accordance with claim 3 wherein the at least one via comprises a plurality of vias and at least some of the plurality of vias are located on the substrate to pneumatically couple to the downset portion.

5. At least one mold piece in accordance with claim 1 wherein the at least one mold piece comprises at least another one vent therein which extends from the molding surface, the at least one vent for securing the substrate to the molding surface.

6. At least one mold piece in accordance with claim 1 wherein the at least one mold piece further comprises at least one pneumatic pathway coupled to the at least one vent.

7. At least one mold piece in accordance with claim 6 wherein the at least one pneumatic pathway further comprises at least one outlet.

8. At least one mold piece in accordance with claim 6 wherein at least one outlet is adapted for coupling to a vacuum source.

9. A method for molding at least one flip chip semiconductor package, the method comprising the steps of;

a) providing at least one substrate having a plurality of vias therethrough, the plurality of vias being at predetermined locations;

b) flip chip mounting at least one semiconductor die to the substrate;

c) providing at least one mold piece having a molding surface for receiving the substrate, the at least one mold piece having a plurality of vents extending from the molding surface;

d) disposing the substrate with the at least one semiconductor die thereon on the molding surface;

e) enclosing the substrate in a mold cavity formed by another molding surface of at least another mold piece; and

f) injecting mold compound into the mold cavity, and thereby expressing air from between the at least one substrate and the at least one semiconductor die through at least some of the plurality of vias and at least some of the plurality of vents.

10. A method in accordance with claim 9 wherein step (a) comprises the steps of:

a1) determining locations of void formation within the at least one flip chip semiconductor package; and

a2) fabricating the at least one substrate with the plurality of vias at the predetermined locations.

11. A method in accordance with claim 9 wherein step (b) comprises the steps of:

b1) bumping the at least one semiconductor die;

b2) mounting the bumped at least one semiconductor die on the at least one substrate; and

b3) reflowing the assembly of the bumped at least one semiconductor die and the at least one substrate.

12. A method in accordance with claim 9 wherein step (c) comprises the steps of:

c1) providing specifications of the at least one substrate and the predetermined locations of the plurality of vias; and

c2) fabricating the at least one mold piece having the plurality of vents extending from the molding surface particular for molding the at least one substrate with the plurality of vias at the predetermined locations.

13. A method in accordance with claim 9 wherein step (d) comprises the steps of:

d1) locating the at least one substrate on the molding surface; and

d2) securing the at least one substrate to the molding surface.

14. A method in accordance with claim 9 wherein step (e) comprises the steps of:

e1) bringing the another mold piece and the at least one mold piece together; and

e2) keeping the another mold piece and the at least one mold piece together until after the mold compound has cured.

15. A method for producing a substrate for forming at least one flip chip semiconductor package, the method comprising the steps of:

a) simulating molding the at least one flip chip semiconductor package to produce simulation results indicating locations of void formation within the at least one flip chip semiconductor package;

b) selecting some of the locations of void formation; and

c) fabricating the substrate with vias at the selected locations of void formation.

16. A method in accordance with claim 15 wherein step (a) comprises the step of using a molding simulation program on a computer.

17. A method in accordance with claim 15 wherein step (b) comprises selecting the locations of void formation where relatively larger voids tend to form.

18. A method in accordance with claim 15 wherein step (b) comprises the step of selecting the locations of void formations where locating a via will not interfere with existing features of the at least one substrate.

19. A method in accordance with claim 15 wherein step (b) comprises the step of selecting the minimal number of vias to avoid adversely affecting reliability of the at least one flip chip semiconductor package.

20. A method in accordance with claim 15, prior to step (c), comprises the steps of:

determining fillet size of mold compound to be used for forming the at least one flip chip semiconductor package; and

setting the size of each of the vias to a size not substantially greater than the fillet size.

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AMENDED CLAIMS

[received by the International Bureau on 17 February 2003 (17.02.03);
original claims 1-20 replaced by amended claims 1-20 (5 pages)

1. At least one mold piece for molding at least one semiconductor package, the at least one mold piece comprising:

a molding surface for receiving a substrate, the substrate having at least on via therethrough, and the substrate having at least one semiconductor die flip chip mounted thereto;

at least one vent therein which extends from the molding surface, the at least one vent for pneumatically coupling to the at least one via; and

at least another one vent therein which extends from the molding surface for securing the substrate to the molding surface.

2. At least one mold piece in accordance with claim 1, wherein the at least one via comprises a plurality of vias at predetermined locations of the substrate, wherein the at least one vent comprises a plurality of vents, and wherein at least some of the plurality of vias at predetermined locations of the substrate are pneumatically coupled to at least some of the plurality of vents.

3. At least one mold piece in accordance with claim 1 wherein at least a portion of the molding surface is downset, and wherein the at least one vent is located within the downset portion.

4. At least one mold piece in accordance with claim 3 wherein the at least one via comprises a plurality of vias and at least some of the plurality of vias are located on the substrate to pneumatically couple to the downset portion.

5. (Canceled)

6. At least one mold piece in accordance with claim 1 wherein the at least one mold piece further comprises at least one pneumatic pathway coupled to the at least one vent.

7. At least one mold piece in accordance with claim 6 wherein the at least one pneumatic pathway further comprises at least one outlet.

8. At least one mold piece in accordance with claim 6 wherein at least one outlet is adapted for coupling to a vacuum source.

9. A method for molding at least one flip chip semiconductor package, the method comprising the steps of;

a) providing at least one substrate having a plurality of vias therethrough, the plurality of vias being at predetermined locations;

b) flip chip mounting at least one semiconductor die to the substrate;

c) providing at least one mold piece having a molding surface for receiving the substrate, the at least one mold piece having a plurality of vents extending from the molding surface;

d) disposing the substrate with the at least one semiconductor die thereon on the molding surface;

e) enclosing the substrate in a mold cavity formed by another molding surface of at least another mold piece;

f) injecting mold compound into the mold cavity, and thereby expressing air from between the at least one substrate and the at least one semiconductor die through at least some of the plurality of vias and at least some of the plurality of vents;

g) determining locations of void formation within the at least one flip chip semiconductor package; and

h) fabricating the at least one substrate with the plurality of vias at the predetermined locations.

10. (Canceled)

11. A method in accordance with claim 9 wherein step (b) comprises the steps of:

b1) bumping the at least one semiconductor die;

b2) mounting the bumped at least one semiconductor die on the at least one substrate; and

b3) reflowing the assembly of the bumped at least one semiconductor die and the at least one substrate.

12. A method in accordance with claim 9 wherein step (c) comprises the steps of:

c1) providing specifications of the at least one substrate and the predetermined locations of the plurality of vias; and

c2) fabricating the at least one mold piece having the plurality of vents extending from the molding surface particular for molding the at least one substrate with the plurality of vias at the predetermined locations.

13. A method in accordance with claim 9 wherein step (d) comprises the steps of:

d1) locating the at least one substrate on the molding surface; and

d2) securing the at least one substrate to the molding surface.

14. A method in accordance with claim 9 wherein step (e) comprises the steps of:

e1) bringing the another mold piece and the at least one mold piece together; and

e2) keeping the another mold piece and the at least one mold piece together until after the mold compound has cured.

15. A method for producing a substrate for forming at least one flip chip semiconductor package, the method comprising the steps of:

a) simulating molding the at least one flip chip semiconductor package to produce simulation results indicating locations of void formation within the at least one flip chip semiconductor package;

b) selecting some of the locations of void formation; and

c) fabricating the substrate with vias at the selected locations of void formation.

16. A method in accordance with claim 15 wherein step (a) comprises the step of using a molding simulation program on a computer.

17. A method in accordance with claim 15 wherein step (b) comprises selecting the locations of void formation where relatively larger voids tend to form.

18. A method in accordance with claim 15 wherein step (b) comprises the step of selecting the locations of void formations where locating a via will not interfere with existing features of the at least one substrate.

19. A method in accordance with claim 15 wherein step (b) comprises the step of selecting the minimal number of vias to avoid adversely affecting reliability of the at least one flip chip semiconductor package.

20. A method in accordance with claim 15, prior to step (c), comprises the steps of:

determining fillet size of mold compound to be used for forming the at least one flip chip semiconductor package; and

setting the size of each of the vias to a size not substantially greater than the fillet size.

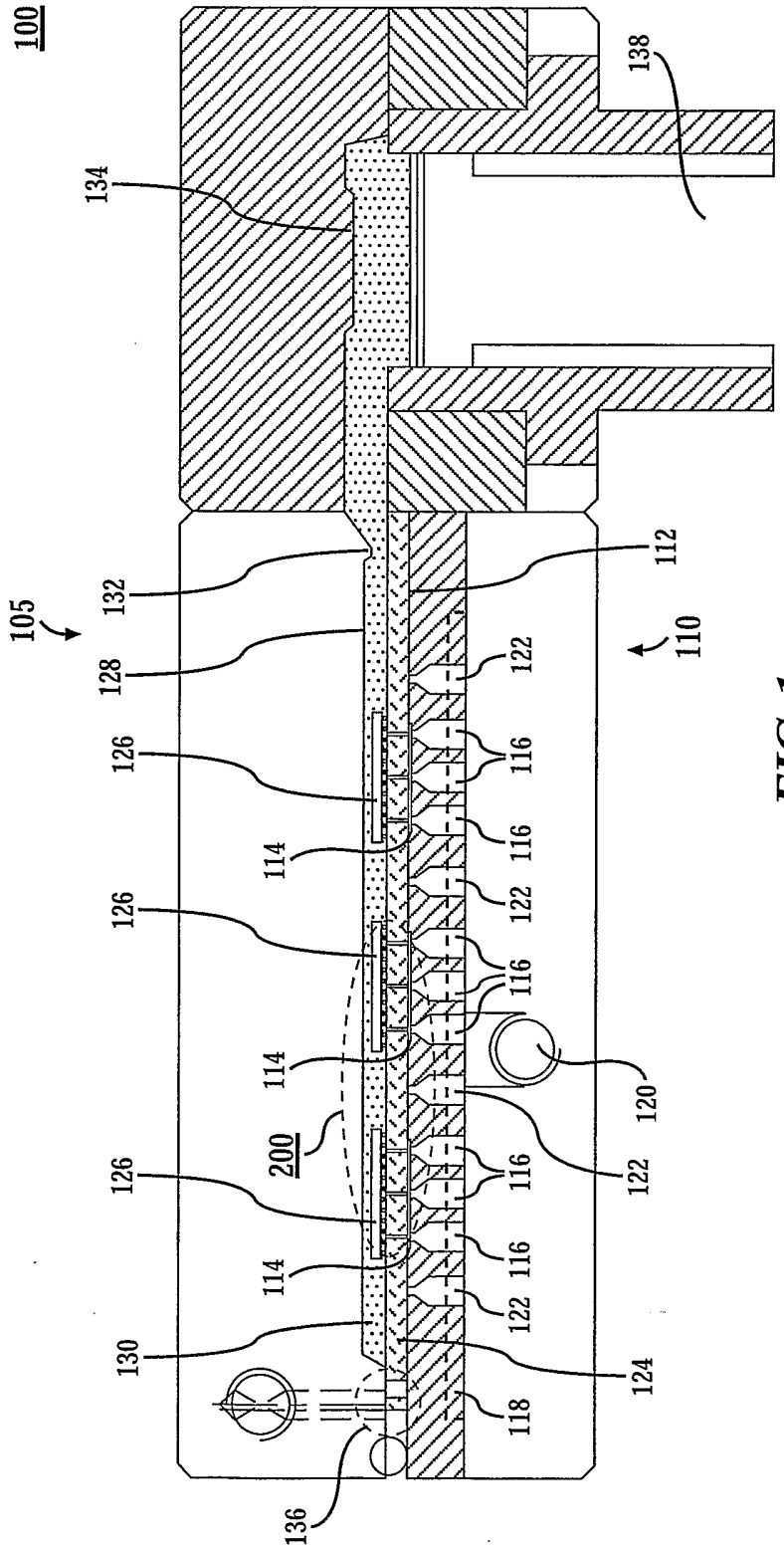
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FIG. 1

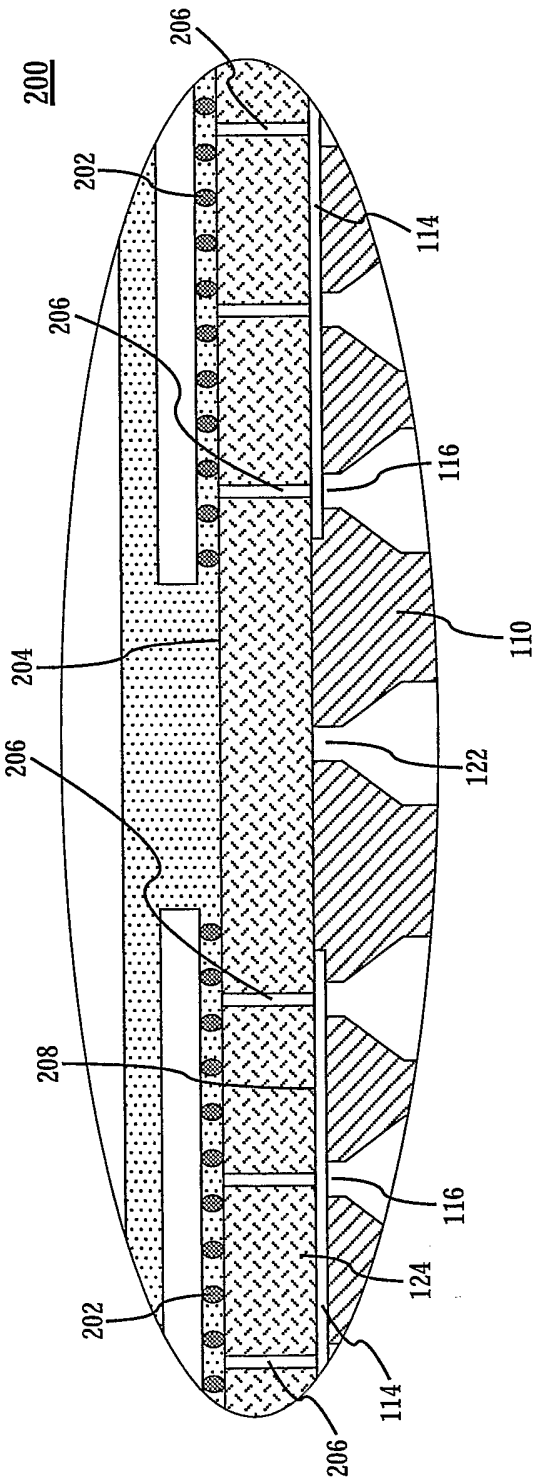

FIG. 2

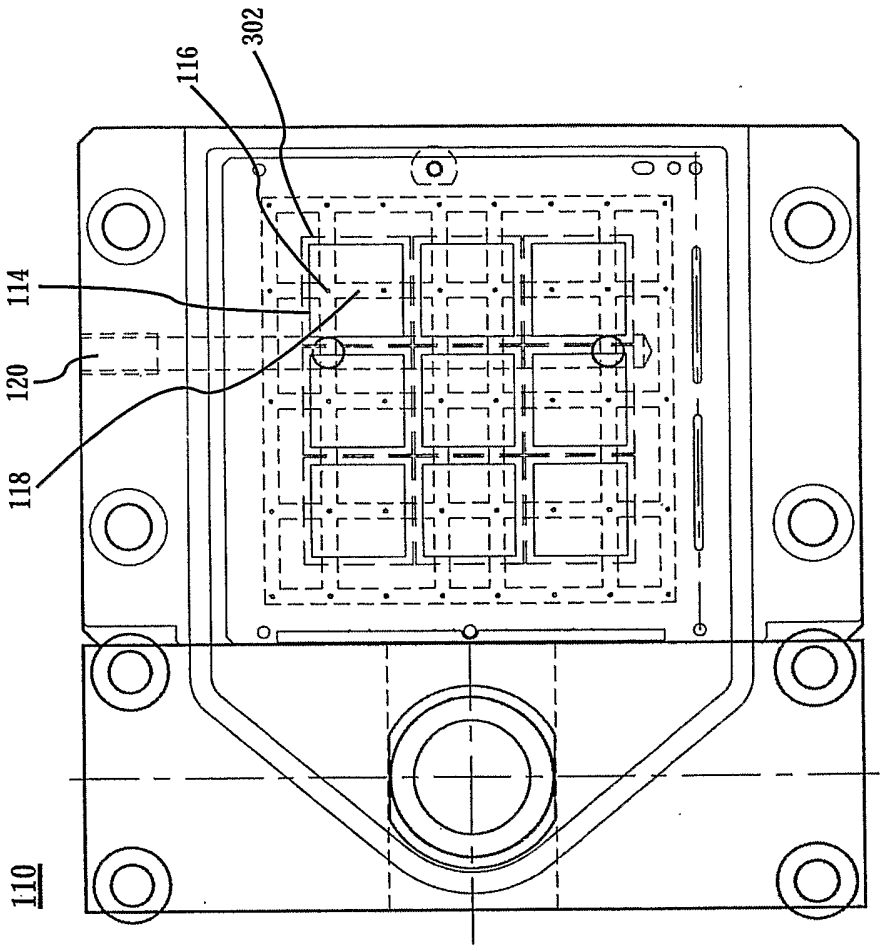

FIG. 3

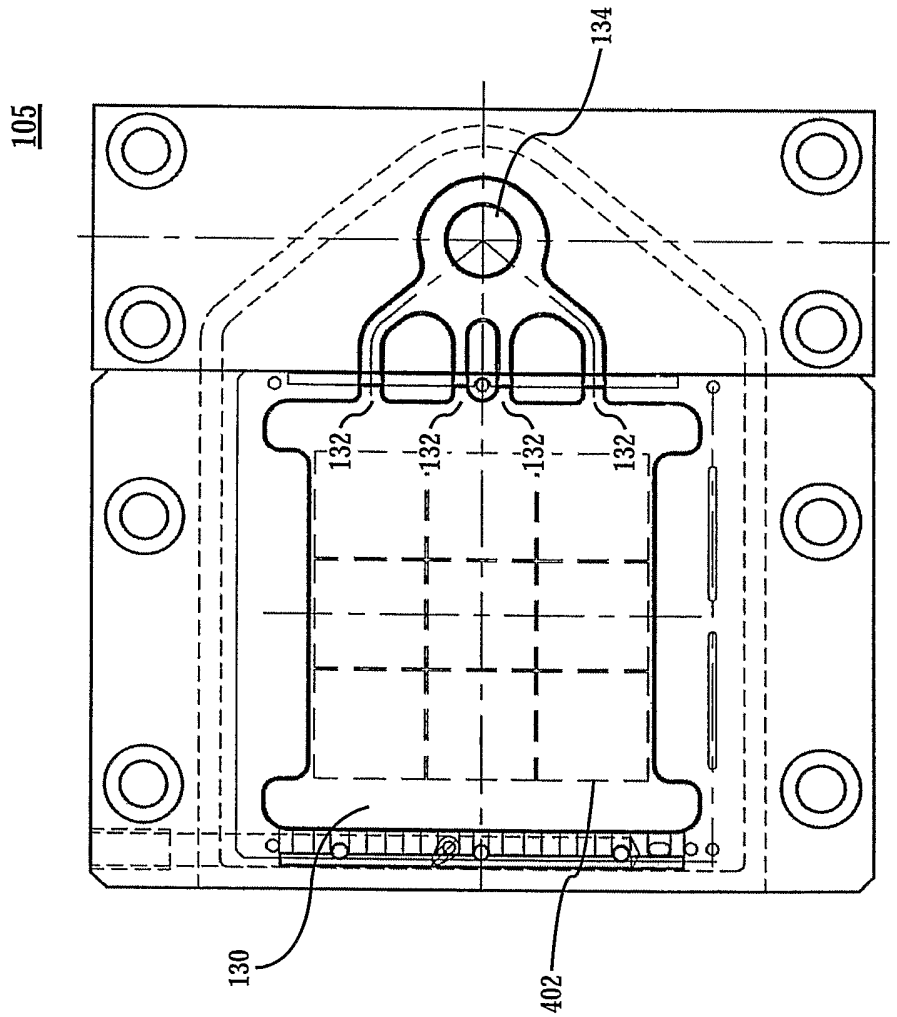

FIG. 4

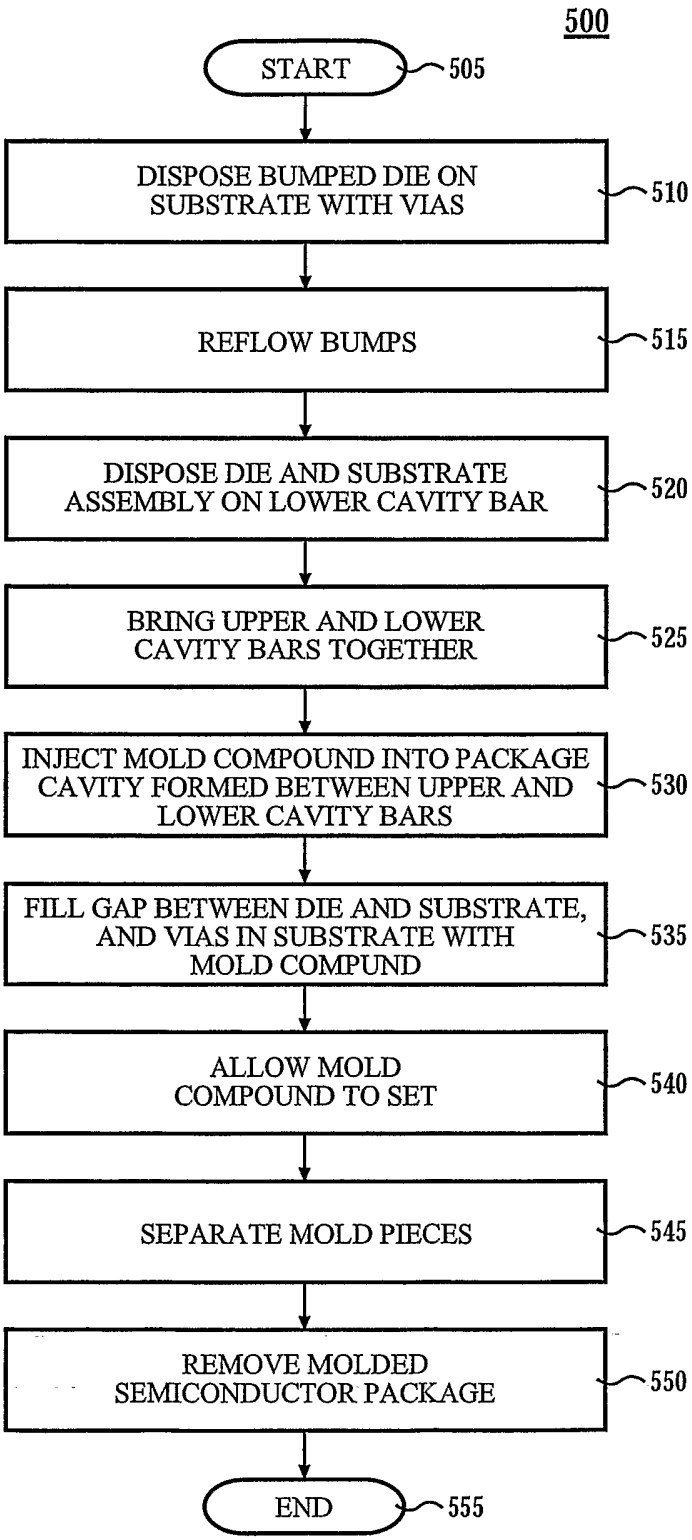
500
START
505
DISPOSE BUMPED DIE ON SUBSTRATE WITH VIAS
510
REFLOW BUMPS
515
DISPOSE DIE AND SUBSTRATE ASSEMBLY ON LOWER CAVITY BAR
520
BRING UPPER AND LOWER CAVITY BARS TOGETHER
525
INJECT MOLD COMPOUND INTO PACKAGE CAVITY FORMED BETWEEN UPPER AND LOWER CAVITY BARS
530
FILL GAP BETWEEN DIE AND SUBSTRATE, AND VIAS IN SUBSTRATE WITH MOLD COMPUND
535
ALLOW MOLD COMPOUND TO SET
540
SEPARATE MOLD PIECES
545
REMOVE MOLDED SEMICONDUCTOR PACKAGE
550
END
555

FIG. 5

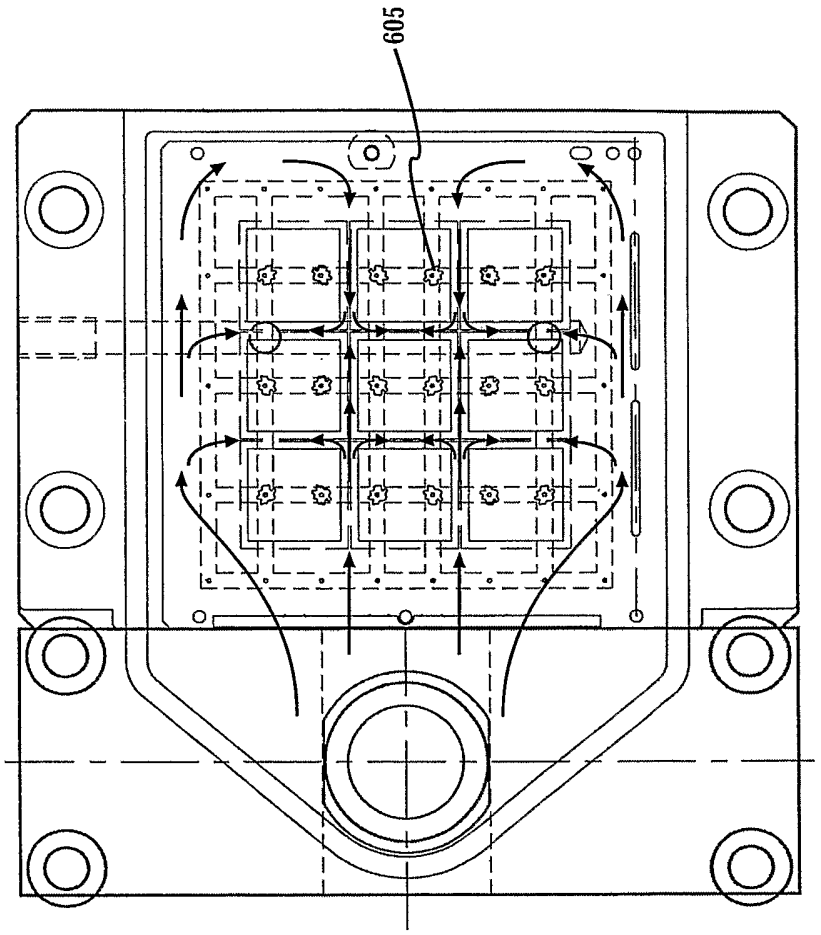

FIG. 6

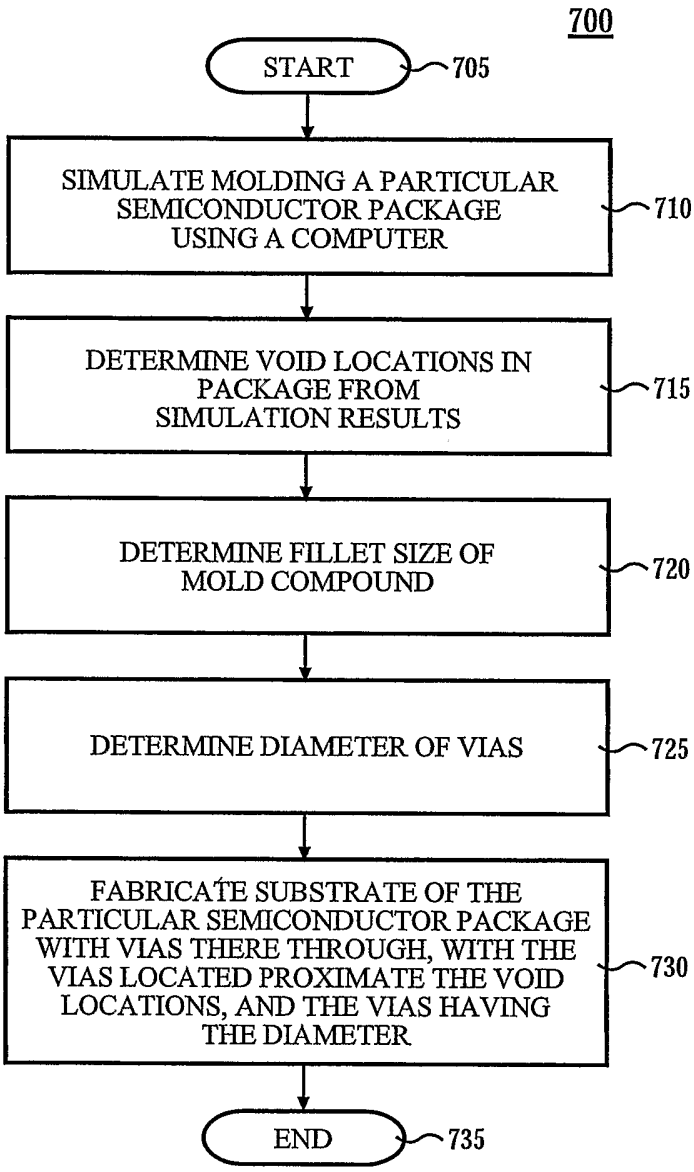
700
START
705
SIMULATE MOLDING A PARTICULAR SEMICONDUCTOR PACKAGE USING A COMPUTER
710
DETERMINE VOID LOCATIONS IN PACKAGE FROM SIMULATION RESULTS
715
DETERMINE FILLET SIZE OF MOLD COMPOUND
720
DETERMINE DIAMETER OF VIAS
725
FABRICATE SUBSTRATE OF THE PARTICULAR SEMICONDUCTOR PACKAGE WITH VIAS THERE THROUGH, WITH THE VIAS LOCATED PROXIMATE THE VOID LOCATIONS, AND THE VIAS HAVING THE DIAMETER
730
END
735

FIG. 7

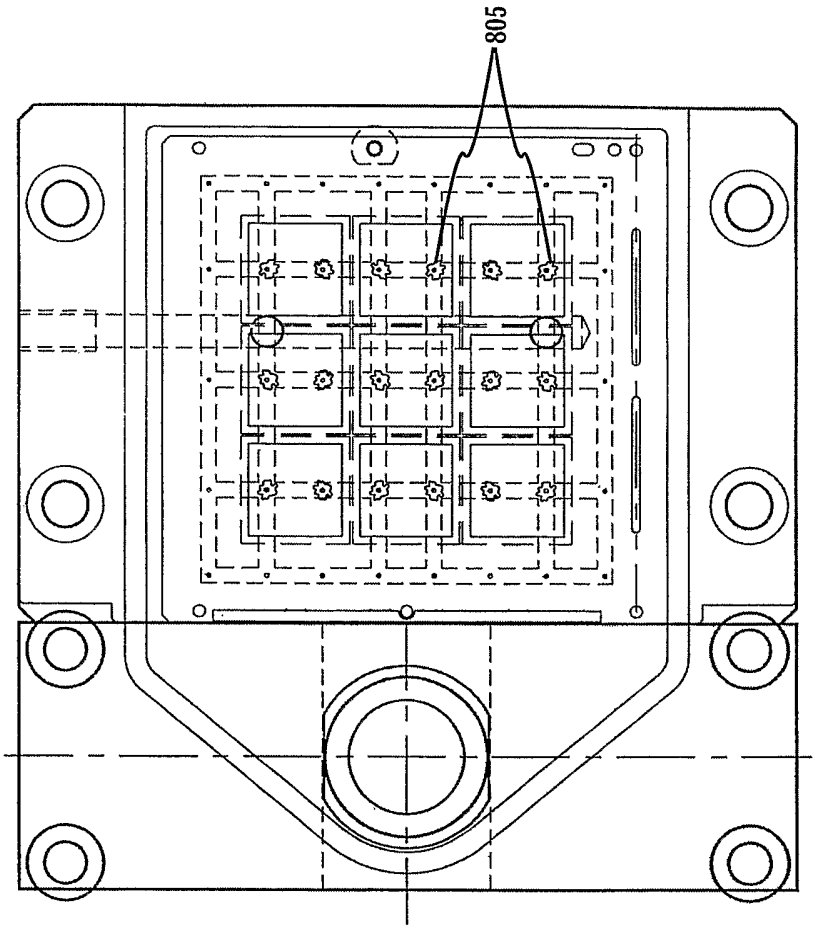

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG02/00257

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl. [7]: H01L 23/31, 21/56, B29C 45/34

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Refer electronic data base consulted

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DWPI, JAPIO: IPC H01L/-, B29C 33/-, 43/-, 45/- & keywords: semiconductor, integrated circuit, IC, flip chip; board, substrate; via, hole, opening, aperture, channel, passage; mo(u)ld, die, underfill, encapsulat+, seal+; vent, path+, outlet, duct; air, void, pocket, gap, space, bubble; void (w) (form+, generat+, occur+); simulat+; program+, computer

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P, X	US 6383846 B1 (SHEN at al.) 7 May 2002 See the whole document, in particular, Fig. 6; column 4 line 38 - column 5 line 19	1-4, 6-9, 11-14
X	JP 2001-267345 A (APIC YAMADA CORP) 28 September 2001 See machine translation:[online], [retrieved on 2002-12-09]. Retrieved from the Internet <URL:http://www6.ipdl.jpo.go.jp/Tokujitu/PAJdetail.ipdl?N0000=60&N0120=01&N2001=2&N3001=2001-267345> See in particular, Figs. 1-2; abstract; [Description of Drawings]	1-4, 6-9, 11-14

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 December 2002	16 DEC 2002
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	Authorized officer **RAJEEV DESHMUKH** Telephone No : (02) 6283 2145

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG02/00257

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	Patent Abstracts of Japan, JP 10-012646 A (OKI ELECTRIC IND CO LTD) 16 January 1998 See abstract; Figs. 1-4	1-4, 6-9, 12-14
X	Derwent Abstract Accession No. 2002-252698/30, Class U11, TW 432648 A (ADVANCED SEMICONDUCTOR ENG INC) 1 May 2001 See abstract	1, 2, 6, 7, 9, 11-14
X	Derwent Abstract Accession No. 2002-302545/34, Class U11, TW 448547 A (ADVANCED SEMICONDUCTOR ENG INC) 1 August 2001 See abstract	1, 2, 6, 7, 9, 11-14
A	US 6038136 A (WEBER) 14 March 2000 See the whole document, in particular, Figs. 6-8	1-20
A	US 5920768 A (SHINTAI) 6 July 1999 See the whole document, in particular, Figs. 3-6 & 8	1-20

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG02/00257

Box I Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos :

because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos :

because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos :

because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a)

Box II Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

See separate sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims

2. ☒ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG02/00257

Supplemental Box
(To be used when the space in any of Boxes I to VIII is not sufficient)

Continuation of Box No: II

The International Searching Authority has found that there are two inventions:

(1) Claims 1-14 directed to a mold piece/method for molding a flip chip semiconductor package, characterised by at least one via through the substrate, and at least one vent on the lower mold piece pneumatically coupled to the at least one via through the substrate.

(2) Claims 15-20 directed to a method for fabricating a substrate (for forming a flip chip semiconductor package) with vias at selected locations of void formation, characterised by simulating molding the flip chip semiconductor package to produce simulation results indicating locations of void formation.

The feature common to the two groups of claims is a substrate (for forming a flip chip semiconductor package) with at least one via therethrough. However, **this common feature is known in the art**. See for example, the applicant cited prior art at page 2 of the specification (US 6038136). Consequently the common feature does not constitute "a special feature" since it makes no contribution over the prior art. Since there exists no other common feature which can be considered as a special technical feature, no technical relationship between the different inventions can be seen. Consequently it appears that **a posteriori**, the claims do not satisfy the requirement that they relate to one invention only.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/SG02/00257

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	6383846	NONE					
JP	2001267345	NONE					
JP	10012646	NONE					
TW	432648	NONE					
TW	448547	NONE					
US	6038136	EP	1190448	WO	200070678	US	6324069
		US	2002043721	US	6157086	US	2001038166
		WO	200143518				
US	5920768	JP	10178030				

END OF ANNEX