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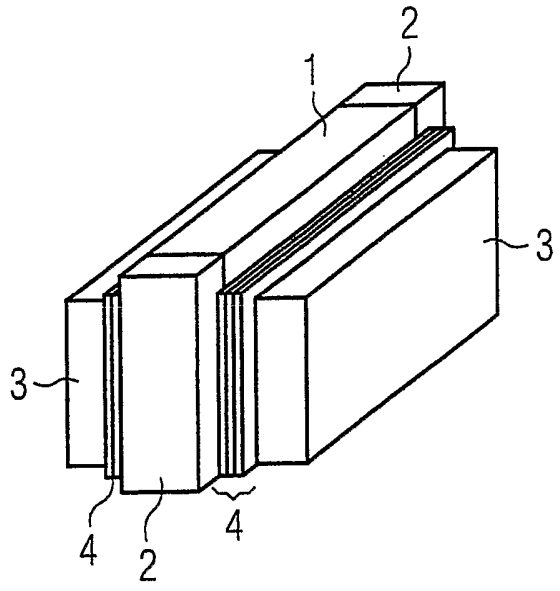
(54) **Title:** CHARGE-TRAPPING MEMORY CELL AND CHARGE-TRAPPING MEMORY DEVICE



(57) **Abstract:** The memory cell is arranged in a ridge of semiconductor material forming a fin with sidewalls and a channel region between source and drain regions . Memory layer sequences provided for charge-trapping are applied to the sidewalls, and gate electrodes are arranged on both sides of the ridge. A plurality of ridges at a distance parallel to one another and have sidewalls facing a neighboring ridge form an array of charge-trapping memory cells. Wordlines are arranged between the ridges, sections of the wordlines forming the gate electrodes. This arrangement enables a double gate operation of the cells and thus allows for a storage of four bits of information in every single memory cell structure.

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Description

Charge-trapping memory cell and charge-trapping memory device

Technical field

The present invention concerns charge-trapping memory cells, especially memory cells of the SONOS or NROM type, and memory devices comprising arrays of such memory cells.

Background of the invention

Non-volatile memory cells that are electrically programmable and erasable can be realized as charge-trapping memory cells which comprise a memory layer sequence of dielectric materials with a memory layer between confinement layers of dielectric material having a larger energy bend gap than the memory layer. This memory layer sequence is arranged between a channel region within a semiconductor layer or substrate and a gate electrode, which is provided to control the channel by means of an applied electric voltage. The programming of the cell is performed by the acceleration of charge carriers, especially electrons, in the channel region to generate charge carriers of sufficient kinetic energy (channel hot electrons) to penetrate the confinement layer and to be trapped in the memory layer. Source and drain regions are provided at both ends of the channel region to apply the accelerating electric voltage.

The threshold voltage of the transistor structure is sensed when the programmed state of the memory cell is read. It is

possible to store bits at both channel ends by the application of reverse operating voltages. This means that two bits can be programmed in each charge-trapping memory cell. Examples of charge-trapping memory cells are the SONOS memory cells, in which each confinement layer is an oxide of the semiconductor material and the memory layer is a nitride of the semiconductor material, usually silicon.

The memory layer can be substituted with another dielectric material, provided the energy band gap is smaller than the energy band gap of the confinement layers. When using silicon dioxide as confinement layers, the memory layer may be tantalum oxide, cadmium silicate, titanium oxide, zirconium oxide or aluminum oxide. Also intrinsically conducting (non-doped) silicon may be used as the material of the memory layer.

A publication by B. Eitan et al., "NROM: a Novel Localized Trapping, 2-Bit Nonvolatile Memory Cell" in IEEE Electron Device Letters, volume 21, pages 543 to 545 (2000), describes a charge-trapping memory cell with a memory layer sequence of oxide, nitride and oxide which is especially adapted to be operated with a reading voltage that is reverse to the programming voltage (reverse read). The oxide-nitride-oxide layer sequence is especially designed to avoid the direct tunneling regime and to guarantee the vertical retention of the trapped charge carriers. The oxide layers are specified to have a thickness of more than 5 nm.

A type of field effect transistor is formed in a so-called finfet structure, in which the channel region and the source and drain regions are arranged in a ridge or fin at a surface of a semiconductor substrate. The gate electrode is applied to the fin either on the top, at a sidewall or in bridge-like

fashion across the fin; and the direction of the channel is parallel to the longitudinal extension of the fin.

Summary of the invention

It is an object of the present invention to increase the storage capacity of charge-trapping memory devices.

It is a further object of the present invention to disclose a memory device with high storage density that is easily produced with standard semiconductor technology.

It is still a further object of the present invention to disclose production methods that are especially adapted to the device structure according to this invention.

The charge-trapping memory cell according to this invention comprises a ridge of semiconductor material forming a fin with sidewalls. Memory layer sequences provided for charge-trapping are applied to the sidewalls, and gate electrodes are arranged on both sides of the ridge above the memory layer sequences. The gate electrodes are arranged so as to control a channel region located within the ridge between doped regions which are provided as source and drain and which are arranged at a distance from one another within the ridge. A plurality of ridges which are arranged at a distance parallel to one another and have sidewalls facing a neighboring ridge, form an array of charge-trapping memory cells that are arranged along rows and columns. Wordlines are arranged between the ridges, sections of the wordlines that are adjacent to the channel region forming the gate electrodes. This arrangement enables a double gate operation of the cells and

thus allows for a storage of four bits of information in every single memory cell structure.

The preferred production method makes use of a dopant glass or other doped material suitable for the diffusion of doping atoms, which is filled in trenches that are etched across the direction of the ridges. The source and drain regions are formed by an outdiffusion of dopant from this material. After the formation of the ridges, a layer sequence of dielectric materials suitable for charge-trapping memory layer sequences is applied all over the surface, including the sidewalls of the ridges. Between the ridges, an electrically conductive material like doped polysilicon or tungsten is filled to form the wordlines comprising the gate electrodes of the individual memory cells.

The source and drain regions are preferably contacted on the top by means of local interconnects that are arranged above in such a manner that each local interconnect contacts two subsequent source/drain regions of the same ridge. In order to obtain alternating connections of the interconnects to the bitlines, it is preferable to have additional connections between the bitlines and the local interconnects so that the bitlines can be arranged slightly deviating from the symmetry axis between subsequent source and drain regions. This enables a separate addressing of both parts of each memory cell by means of the two separate gate electrodes. In this manner, four bits can be stored in every memory cell.

These and other objects, features and advantages of the invention will become apparent from the following brief description of the drawings, detailed description and appended claims and drawings.

Brief description of the drawings

Figure 1 is a perspective view showing the principal structure of the memory cell.

Figure 2 is a top view of a memory device showing the arrangement of wordlines and ridges.

Figure 3 is a perspective view of an example of the connection of a memory cell to the bitline.

Figure 4 is a top view of a memory device showing bitlines, local interconnects, and connections to the local interconnects.

Figure 5A is a top cross section of a single memory cell showing the programmable bits.

Figure 5B is a circuit scheme of the memory cell according to figure 5A.

Figure 6 is a circuit diagram of a memory cell array, showing examples of voltages to be applied during a write operation.

Figure 7 is an energy band diagram corresponding to the write operation.

Figure 8 is a perspective cross-section of an intermediate product of a preferred production method.

Figure 9 shows the cross-section according to figure 8 after the application of a dopant material.

Figure 10 shows the cross-section according to figure 9 after the formation of ridges and source and drain regions.

Figure 11 is the cross-section according to figure 10, regarded in the direction from right to left and showing the arrangement of a dielectric layer sequence.

Figure 12 shows the view according to figure 11 after the formation of wordlines.

Figure 13 shows a perspective cross-section of an intermediate product corresponding to figure 9 after the formation of diffusion regions.

Figure 14 shows the cross-section according to figure 13 after the removal of the doping material.

Figure 15 shows the cross-section according to figure 14 after the application of an electrically insulating filling.

Figure 16 shows the cross-section according to figure 15 after the formation the ridges.

Figure 17 shows a cross-section of an intermediate product along a ridge after the formation of local interconnects.

Figure 18 shows the cross-section according to figure 17 after the formation of connections to the local interconnects.

Figure 19 shows the cross-section according to figure 18 after the formation of bitlines.

Detailed description

Figure 1 shows a perspective view of the principal structure of a memory cell according to the invention, isolated from the memory device. This memory cell comprises a fin 1, which can be part of a ridge of semiconductor material. At the longitudinal ends of the fin 1, source/drain regions 2 are formed as doped regions. The fin preferably comprises a basic doping, for example of p-conductivity. The source/drain regions 2 are doped for the opposite conductivity type and with a higher concentration of doping atoms. On both sidewalls of the fin 1, there are gate electrodes 3, which are electrically insulated from the semiconductor material by memory layer sequences 4. The memory layer sequences 4 comprise a memory layer provided for the trapping of charge carriers and arranged between confinement layers of higher energy band gap. The memory layer sequence 4 can be formed of any sequence of dielectric materials which is suitable as charge-trapping memory layer sequence. The memory layer sequence 4 may especially be an oxide-nitride-oxide layer sequence.

Figure 2 shows a top view onto an array of memory cells and wordlines of a memory device comprising memory cells according to figure 1. The wordlines WL_n are arranged at a distance to one another between the ridges comprising the fins 1. At the longitudinal ends of the fins, with respect to the direction of the wordlines, there are source/drain regions 2, which are formed as doped regions. The wordlines are arranged at the same level with the ridges that comprise the fins, and

the memory layer sequence 4, which is not shown in detail in figure 2, is arranged between the ridges and the wordlines, forming the storage means between the fins 1 and the gate electrodes 3 that are formed by sections of the wordlines.

Figure 3 shows the arrangement of two subsequent memory cells in the same ridge and the electric connection to a bitline that is arranged above. The section shown in figure 3 encompasses two fins 1 that are adjacent in the same ridge of semiconductor material. At the longitudinal ends of the fins, there are source/drain regions 2. Every two subsequent source/drain regions 2 which belong to subsequent fins are together connected to a local interconnect 5, which is arranged as a local contact on the two subsequent source/drain regions 2. The source/drain regions 2 are covered by the local interconnect 5 in figure 3 so that only the source/drain regions 2 at the opposite ends of the two represented fins are shown. These source/drain regions 2 are also connected to local interconnects, which in turn also contact a further source/drain region 2 of those fins 1 that follow next in both directions along the ridge. The bitlines can be arranged immediately above the local interconnects 5. Instead, as shown in figure 3, contacts 6 to the interconnects can be provided to facilitate the relative arrangement of the bitlines with respect to the local interconnects 5 and the location of all the source/drain regions 2 that are to be connected by the same bitline. The bitlines BL are formed by conductor tracks 7 electrically connected to the local interconnects 5, eventually via the contacts 6. The bitlines can be doped polisilicon or, preferably, metal conductor tracks, and the wordlines can also be formed of metal, for example tungsten, or of doped polysilicon.

Figure 4 shows a top view onto an array of memory cells, which are contacted with local interconnects and connected by bitlines. The arrangement corresponds to the top view of figure 2, with the wordlines WL running from the top to the bottom of the figure and the bitlines BL from left to right. The local interconnects and contacts to the interconnects can be of any geometrical shape that is suitable for the purpose. To improve the readability of figure 4, all local interconnects 5 are represented by oval contacts, and all contacts 6 between the local interconnects and the conductor tracks 7 forming the bitlines are represented by circles, indicating a cylindrical shape. The hidden contours of the wordlines WL, the local interconnects 5, and the contacts 6 to the interconnects are represented by broken lines. In this top view of figure 4, the bitlines are arranged uppermost, the contacts 6 follow at the next level, the local interconnects 5 are arranged between the semiconductor ridges and the contacts 6, and the ridges comprising the fins 1 and the wordlines are at the lowest level which is shown in figure 4. The source/drain regions 2 are shown in figure 4 as small rectangular areas which are also drawn with broken lines.

It is clear from figure 4 that the local interconnects 5 are arranged above pairs of source/drain regions 2 that are subsequent along the semiconductor ridges. Each pair of source/drain regions 2 which are connected in this way by the same local interconnect 5 belong to two immediately subsequent memory cells of the same ridge. This means that the fins 1 are mainly situated in the areas between the local interconnects. Each of the wordlines WL is provided to address the memory cells of two neighboring ridges. Therefore, it is important that the source/drain regions 2 of the memory cells that are adjacent to the same wordline on opposite sides of

the wordline are connected to different bitlines. By choosing one bitline in figure 4 and following this bitline from left to right, it is easily seen that the sequence of local interconnects that are electrically connected to this bitline are arranged on every second ridge. One of the two immediately neighboring bitlines is connected to local interconnects which are arranged on the same ridges as those of the chosen bitline. The other neighboring bitline, on the other side of the chosen bitline, is connected to local interconnects that are situated on the intermediate ridges, in order to address the memory cells of the intermediate ridges. This preferable arrangement can better be characterized in the following way.

Suppose a consecutive enumeration of the ridges in one direction, for example from left to right in figure 4, is given. Furthermore, the bitlines can be thought to be grouped into disjoint pairs of neighboring bitlines, these pairs being also consecutively enumerated along one direction parallel to the wordlines. Then memory cells located in even-numbered ridges are connected to even-numbered pairs of bitlines, and memory cells located in odd-numbered ridges are connected to odd-numbered pairs of bitlines. Whether the numbers are even or odd obviously depends on the given enumeration, and the ridges and pairs of bitlines can instead be numbered in such a way that memory cells in even-numbered ridges are connected to odd-numbered pairs of bitlines.

The essential feature here is that there are pairs of bitlines which are provided to connect source/drain regions of memory cells in every second ridge. Two neighboring pairs of bitlines are provided to connect memory cells in even-numbered and odd-numbered ridges, respectively, which means that all pairs of bitlines only connect memory cells of every sec-

ond ridge. The memory cells that are subsequent within the same ridge are addressed by one bitline of the same pair of bitlines and by the nearest bitline of the next but one pair of bitlines. If the bitlines represented in figure 4 are, for example, numbered from 1 to 7 from top to bottom of the figure, the source/drain regions of the memory cells that are located in the first ridge on the left side of figure 4, for instance, are addressed by bitlines 1 and 2, 2 and 5, and 5 and 6. Bitlines number 3, 4 and 7 do not address any memory cell in the first ridge.

Figures 5A and 5B show a top cross-section of one memory cell and an appertaining circuit diagram to explain the location of the programmed bits. Figure 5A shows a fin 1, source/drain regions 2 at both longitudinal ends of the fin 1, and gate electrodes 3 on both sides of the fin, which are electrically insulated from it by memory layer sequences 4. The gate electrodes 3 are part of wordlines WL extending along the semiconductor ridge. As the charge-trapping memory cells enable the programming of bits at both ends of the channel, there are in total four possible bit positions 8, in which a bit of information can be stored.

The circuit diagram in figure 5B shows the electric connection of the wordlines to the gate electrodes of the memory cell according to figure 5A, and the electric connection of the bitlines to the source/drain regions of the transistor structures. The circuit diagram shows that each memory cell is equivalent to the arrangement of two transistor structures that are arranged opposite to one another and comprise a common transistor body. The channels are located adjacent to the sidewalls of the fin 1, which are covered with the memory layer sequences 4. Therefore, the transistor structure shown

in figure 5A is equivalent to the structure of two devices, one of which is turned upside down and which are combined rear to rear.

Figure 6 shows a circuit diagram representing an array of memory cells that are connected to wordlines WL_1, WL_2, WL_3 and bitlines BL_1, BL_2, BL_3, BL_4, BL_5, BL_6. The diagram of figure 6 explains the operation of the array according to figure 4. The location where one bit of information is to be stored is indicated as bit position 8. The gate electrode 3 of the corresponding memory cell transistor is connected to wordline WL_1. The source/drain regions of this transistor are connected to bitlines BL_2 and BL_3. The source/drain regions at the channel end where the bit position 8 is located is connected to a higher voltage than the opposite source/drain region. In the example shown in figure 6, a voltage of 5 volt is applied. Electrons are accelerated in the channel by this voltage to enable channel hot electron injection at the indicated bit position 8.

The channel is opened by a positive electric potential of typically about 5 volt, for example; it is applied to the gate electrode 3 via wordline WL_1. A negative electric potential, typically about -2 volt, for example, is applied to the opposite gate electrode of the same memory cell via wordline WL_2, in order to switch off the second transistor structure that is present in the same memory cell, i. e. in the same fin. Figure 6 also shows the arrangement of electric connections of the bitlines, forming disjoint pairs of bitlines, for example BL_2 and BL_3, or BL_4 and BL_5. Bitlines BL_2 and BL_3 are provided to address the memory cells in the second and forth columns of the section of the array that is shown in figure 6, while bitlines BL_4 and BL_5 are provided to address

the memory cells in the first and third columns. The memory cell that is left to the memory cell marked with the bit position 8, for instance, is addressed via bitlines BL_1 and BL_4.

Figure 7 shows an energy band diagram for the programming operation. The gate electrode of the transistor that is to be programmed (gate 1, on the right side of the diagram) is on a high (positive) potential (+), and the second gate electrode (gate 2, on the left side of the diagram) is on a low (negative) potential (-). Between the gate electrodes, there are the transistor body (Si-FIN) and the memory layer sequences (ONO) arranged on opposite sidewalls. In the channel that is controlled by gate 1, channel hot electrons (CHE) are generated by the application of an accelerating voltage between source and drain. These electrons acquire a high kinetic energy which enables them to penetrate the oxide confinement layer, indicated in the diagram by the arrow pointing upwards, and to enter the nitride memory layer, indicated by the curved arrow, to be trapped there. The position of the induced channel formed by an inversion layer is marked IL. This energy diagram is represented for the sake of a better understanding of the write operation, but a thorough explanation of the programming mechanism is not necessary, because charge-trapping memory cells are known per se.

A memory device comprising a memory cell array of memory cells according to this invention will be described by examples of preferred production methods. First, as shown in the perspective cross-section of figure 8, a substrate 10 of semiconductor material is provided with a plurality of first trenches 11, which are etched into a main surface of the substrate. The first trenches 11 are arranged at a distance from

one another and parallel to one another. They are preferably one unit F of the minimal technology dimension wide and are preferably spaced 3F apart, as indicated in figure 8.

Next, as shown in figure 9, the first trenches 11 are filled with a doped material that is suitable to form doped regions by outdiffusion of doping atoms, for example a dopant glass 12.

Figure 10 shows the perspective cross-section according to figure 9 after the formation of second trenches 14 in a direction perpendicular to the direction of the first trenches 11, thereby forming ridges 15. As indicated in figure 10, the second trenches 14 and the ridges 15 are preferably one unit of the minimal dimension F wide. A dielectric layer sequence provided for the memory layer sequence is applied all over the surface of the ridges and second trenches. The dielectric layer sequence is not shown in figure 10 in order not to cover the other details.

Diffusion regions 13 are subsequently formed by a diffusion of doping atoms out of the remaining parts of the dopant glass 12. This is promoted by an elevation of the temperature (furnace diffusion). The diffusion regions 13 are indicated with broken lines in figure 10.

Figure 11 shows a perspective cross-section which is seen from a direction that is at an angle to the line of view of figure 10. In figure 11, the dielectric layer sequence 16 is also shown. The ridges 15 comprise the fins that are provide for the memory cells and still contain the remaining parts of the dopant glass 12, surrounded by the produced diffusion regions 13. It is preferable to apply the dielectric layer 16,

before the temperature step to promote the diffusion is performed.

Figure 12 shows the cross-section according to figure 11, after the second trenches 14 have been filled with an electrically conducting material 17, which is provided for the wordlines. This material can be doped polysilicon, for example, or a metal like tungsten. After the deposition of this material, the surface can be planarized, for example by CMP (chemical mechanical polishing). This planarization stops on the top of the ridges, where the dielectric layer sequence 16 is preferably completely removed. The electrically conducting material 17 is recessed, and the recesses are filled with an electrically insulating cover 18, for instance nitride, which is preferably also slightly recessed.

In an alternative method, starting from the intermediate product of figure 9, a diffusion of doping atoms to form the diffusion regions 13, according to figure 13, takes place first. The doping material, which can be a dopant glass 12, is then removed, as shown in figure 14. The opened first trenches are then again filled, this time by a deposition of an electrically insulating filling 19, which may be an oxide or nitride.

Then, as shown in figure 16, the second trenches 14 are etched to form the ridges 15, rendering a structure comparable to that of figure 10. The position of the fins 1 within the ridges 15 and the source/drain regions 2 are indicated in figure 16. The application of a dielectric layer sequence follows to obtain an intermediate product corresponding to the product shown in figure 11. The electrically conducting material 17 and the insulating cover 18 can be applied as

well to obtain an intermediate product according to figure 12.

Figure 17 is a cross-section of a further intermediate product, taken along a wordline. This intermediate product is obtained proceeding from the intermediate product according to figure 12 by the application of local interconnects 5, which can be formed of metal like tungsten. The interspaces are filled with a dielectric layer 20. This can be done by a standard technology, for example by applying a dielectric layer and forming contact holes in the dielectric layer, which are then filled with electrically conductive material, for instance tungsten, the fillings forming the local interconnects 5.

The local interconnects 5 are applied in electric contact to pairs of source/drain regions 2. The wordlines comprising the gate electrodes 3 can be arranged slightly recessed to a distance from the edge of the ridges so that the fins 1 and/or memory layer sequences 4 more or less exceed the top of the wordlines.

Figure 18 shows the further intermediate product after the production of contacts 6 to the local interconnects 5, in order to facilitate the electric connection to the bitlines.

Figure 19 shows the cross-section according to figures 17 and 18 with an arrangement of bitlines formed as conductor tracks 7 in a further dielectric layer 21. The passing bitlines 9 are connected to contacts 6 that belong to the neighboring ridges before and behind the plane of drawing. The arrangement of local interconnects 5, contacts 6, and conductor tracks 7 can be produced by a standard damascene process,

which is known per se. The dielectric layers 20 and 21 may be any intermetal dielectric, for example an oxide or BPSG (borophosphorus silicate glass).

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

List of reference numerals

1 fin
2 source/drain region
3 gate electrode
4 memory layer sequence
5 local interconnect
6 contact to interconnect
7 conductor track
8 bit position
9 passing bitline
10 substrate
11 first trench
12 dopant glass
13 diffusion region
14 second trench
15 ridge
16 dielectric layer sequence
17 electrically conducting material
18 insulating cover
19 insulating filling
20 dielectric layer
21 further dielectric layer
$BL_{[k]}$ bitline
$WL_{[n]}$ wordline

We claim:

1. Charge-trapping memory cell, comprising:
a substrate provided with a ridge of semiconductor material having sidewalls and forming a fin structure;
source and drain regions formed as doped regions at a distance from one another in said ridge;
memory layer sequences of dielectric materials arranged on said sidewalls and comprising a memory layer provided for charge-trapping between confinement layers; and
gate electrodes arranged on said memory layer sequences adjacent to a region of said ridges between said source and said drain regions and provided as a channel region.

2. Charge-trapping memory cell as claimed in claim 1, further comprising:
said ridge being laterally delimited by two parallel trenches; and
said gate electrodes being arranged within said trenches.

3. Charge-trapping memory cell as claimed in claim 1 or 2, further comprising:
local interconnects of electrically conducting material being arranged above said source and drain regions.

4. Charge-trapping memory device, comprising:
a substrate provided with ridges arranged at a distance parallel to one another and having sidewalls facing a neighboring ridge;
said ridges comprising semiconductor material, in which a plurality of source and drain regions are formed as doped regions adjacent to sections of said ridges that are provided as channel regions;

memory layer sequences of dielectric materials arranged on said sidewalls and comprising a memory layer provided for charge-trapping between confinement layers;
gate electrodes arranged on said memory layer sequences adjacent to said channel regions in spaces between neighboring ones of said ridges;
wordlines provided to electrically connect said gate electrodes along said ridges;
local interconnects provided to electrically contact said source and drain regions; and
conductor tracks provided as bitlines to electrically connect pluralities of said interconnects that are arranged along rows across said wordlines.

5. Charge-trapping memory device as claimed in claim 4, further comprising:
said wordlines being arranged in spaces between neighboring ones of said ridges and comprising sections forming said gate electrodes.

6. Charge-trapping memory device as claimed in claim 4 or 5, further comprising:
said gate electrodes each being provided for two channel regions located on opposite sides in neighboring ridges.

7. Charge-trapping memory device as claimed in claim 4 or 5, further comprising:
said ridges comprising sections, each of which comprises one of said channel regions, adjacent ones of said source and drain regions, memory layer sequences on both of said sidewalls, and gate electrodes on both of said memory layers sequences;

said sections forming memory cells provided for the storage of four bits; and
said local interconnects being provided for the electric connection of two subsequent ones of said source and drain regions belonging to two subsequent ones of said memory cells.

8. Charge-trapping memory device as claimed in claim 4 or 5, further comprising:
said bitlines each being electrically connected to a plurality of said interconnects that are provided for an electric connection of said source and drain regions of every second of said memory cells along one of said rows.

9. Charge-trapping memory device as claimed in claim 8, further comprising:
said bitlines being arranged in one metalization layer and being grouped into disjoint pairs of neighboring bitlines; given a consecutive enumeration of said pairs of bitlines in a direction along the ridges, and a consecutive enumeration of said ridges in one direction, memory cells located in even-numbered ridges being connected to even-numbered pairs of bitlines, and memory cells located in odd-numbered ridges being connected to odd-numbered pairs of bitlines, or vice versa.

10. Charge-trapping memory device as claimed in claim 9, further comprising:
both bitlines belonging to an even-numbered pair and one of the bitlines of the previous or next even-numbered pair being connected to two subsequent ones of said memory cells along said ridges; and
both bitlines belonging to an odd-numbered pair and one of the bitlines of the previous or the next odd-numbered pair

being connected to two subsequent ones of said memory cells along said ridges.

11. Method for producing a charge-trapping memory device, comprising:
providing a substrate of semiconductor material with a plurality of first trenches that are arranged parallel and at a distance from one another at a main surface of said substrate;
filling said first trenches with dopant glass or another doped material suitable for a diffusion of doping atoms;
diffusing the dopant to form doped regions provided for source and drain;
removing said dopant glass or doped material;
filling said first trenches with electrically insulating material;
etching second trenches in a direction perpendicular to the first trenches into said main surface to form ridges arranged parallel at a distance from one another and comprising sidewalls facing a neighboring one of said ridges;
applying a dielectric layer sequence provided for a memory layer sequence;
filling said second trenches with an electrically conductive material provided for wordlines;
recessing said electrically conducting material and filling an electrically insulating material to cover said electrically conducting material;
applying a metalization to form interconnects that electrically contact said doped regions provided for source and drain; and
applying conductor tracks provided as bitlines.

12. Method for producing a charge-trapping memory device, comprising:
providing a substrate of semiconductor material with a plurality of first trenches that are arranged parallel and at a distance from one another at a main surface of said substrate;
filling said first trenches with dopant glass or another doped material suitable for a diffusion of doping atoms;
etching second trenches in a direction perpendicular to the first trenches into said main surface to form ridges arranged parallel at a distance from one another and comprising sidewalls facing a neighboring one of said ridges;
applying a dielectric layer sequence provided for a memory layer sequence;
diffusing the dopant to form doped regions provided for source and drain;
filling said second trenches with an electrically conducting material provided for wordlines;
recessing said electrically conducting material and filling an electrically insulating material to cover said electrically conducting material;
removing said dopant glass or doped material and filling an electrically insulating material instead;
applying a metalization to form interconnects that electrically contact said doped regions provided for source and drain; and
applying conductor tracks provided as bitlines.

13. Method for producing a charge-trapping memory device as claimed in claim 11 or 12, further comprising:
said interconnects being applied to pairs of doped regions provided for source and drain.

FIG 1

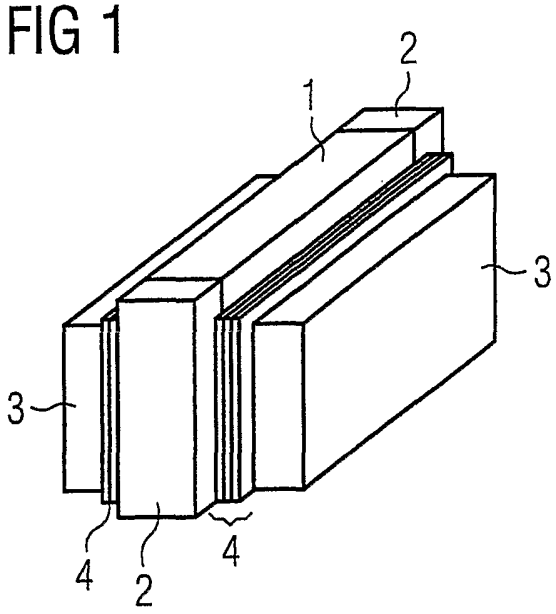

FIG 2

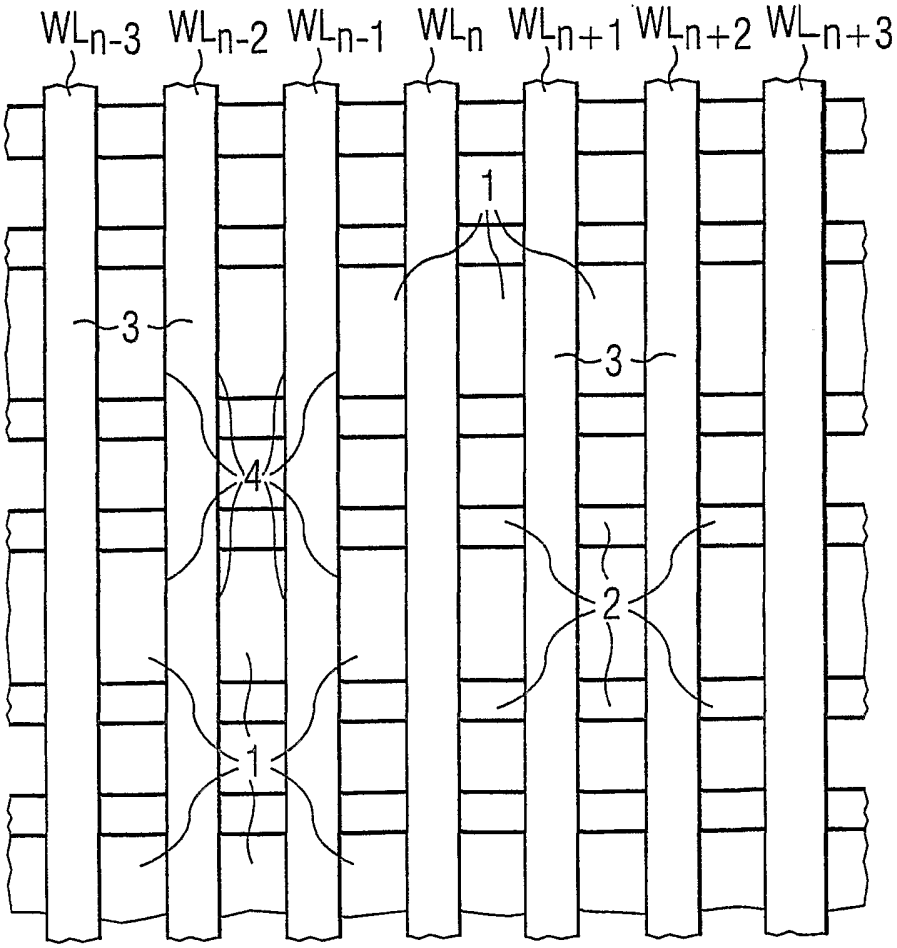

FIG 3

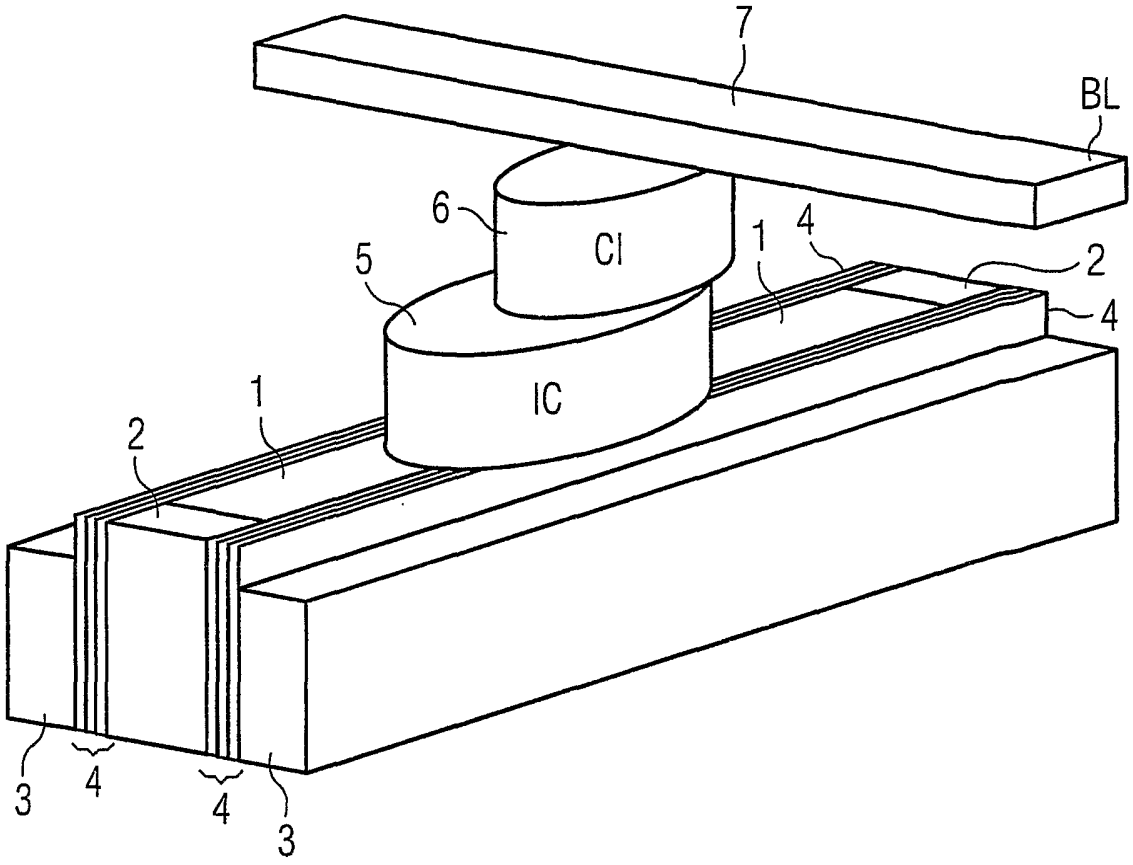

FIG 4

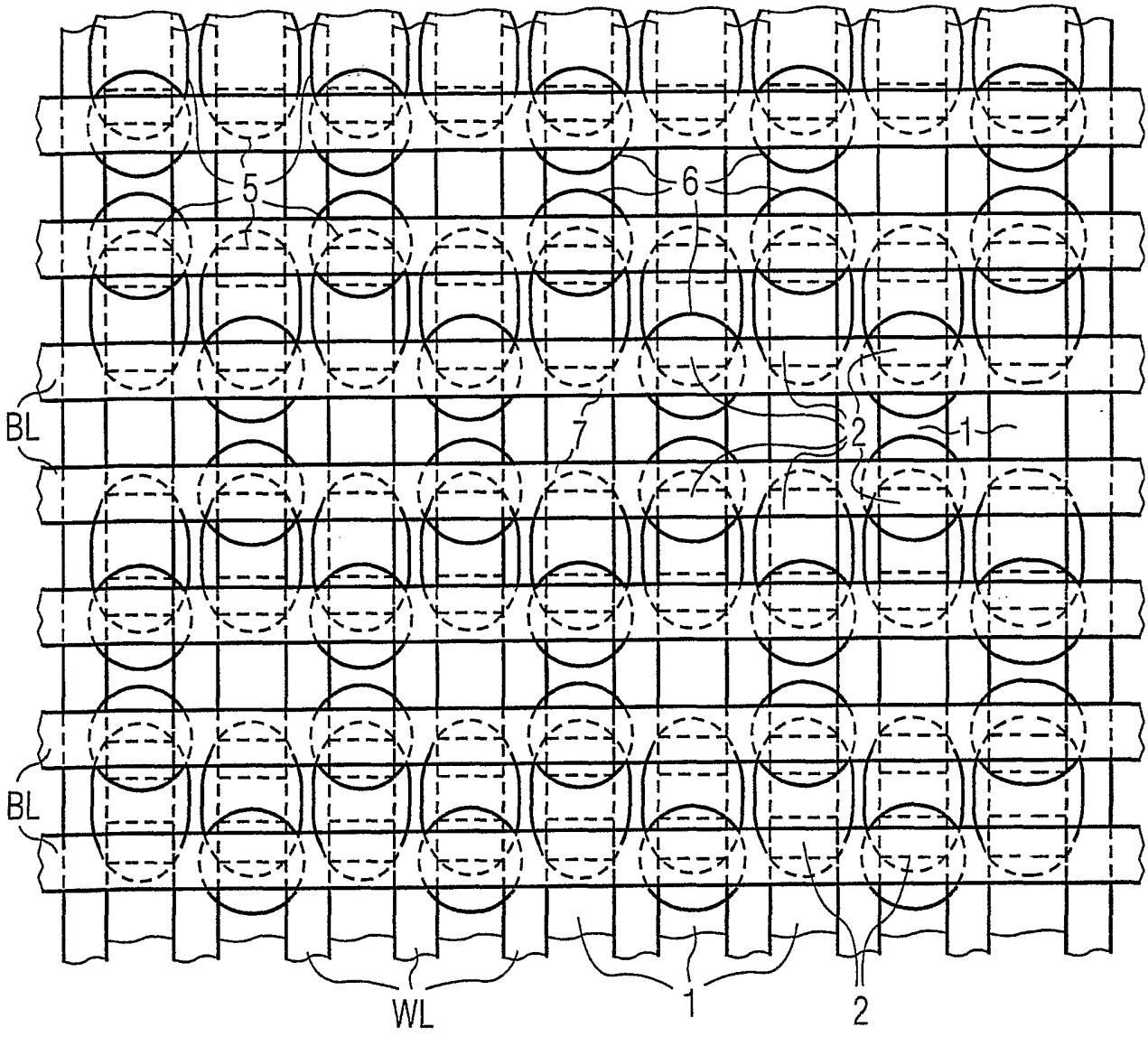

FIG 5A

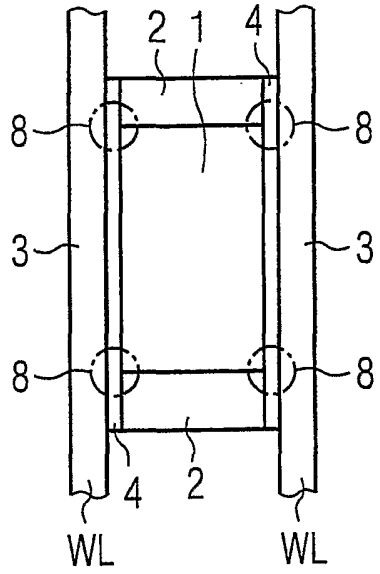

FIG 5B

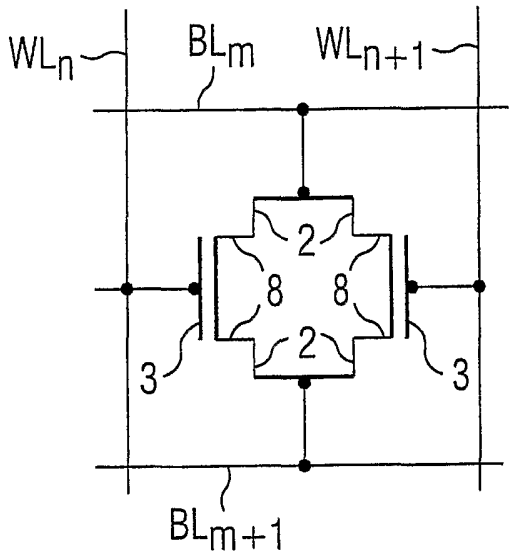

FIG 6

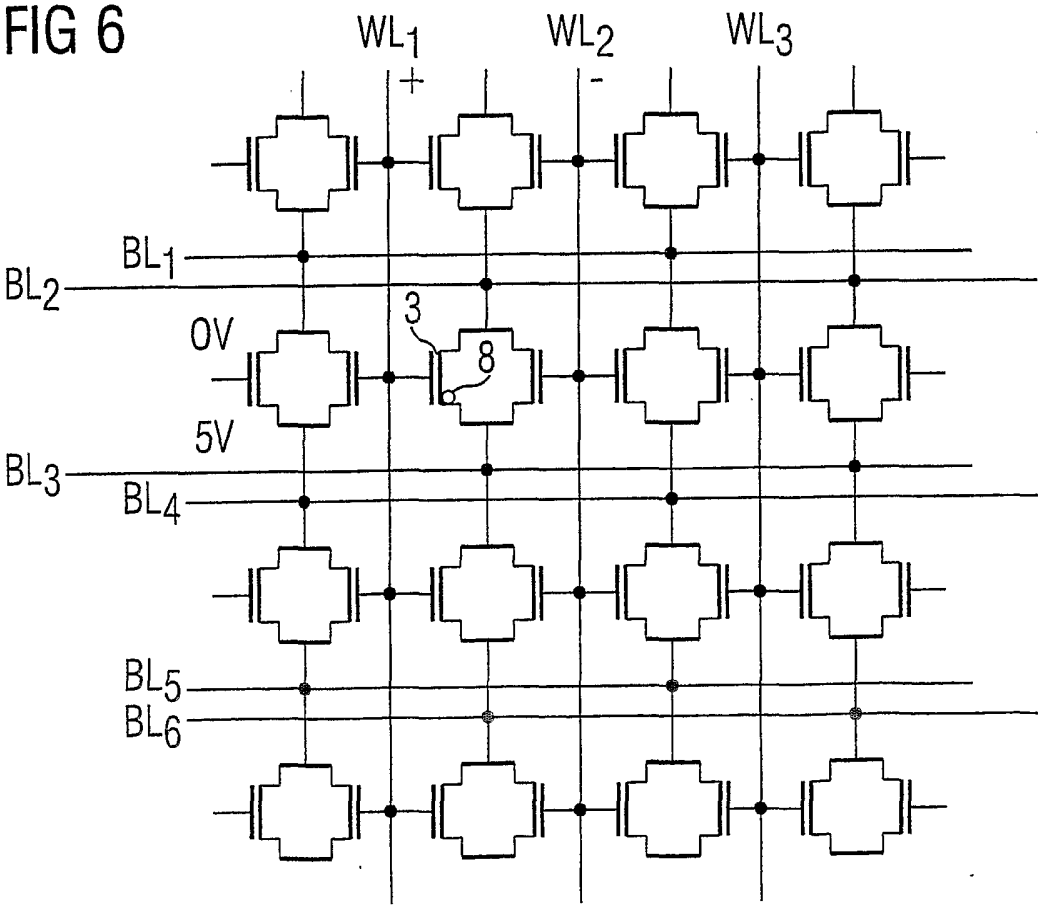

FIG 7

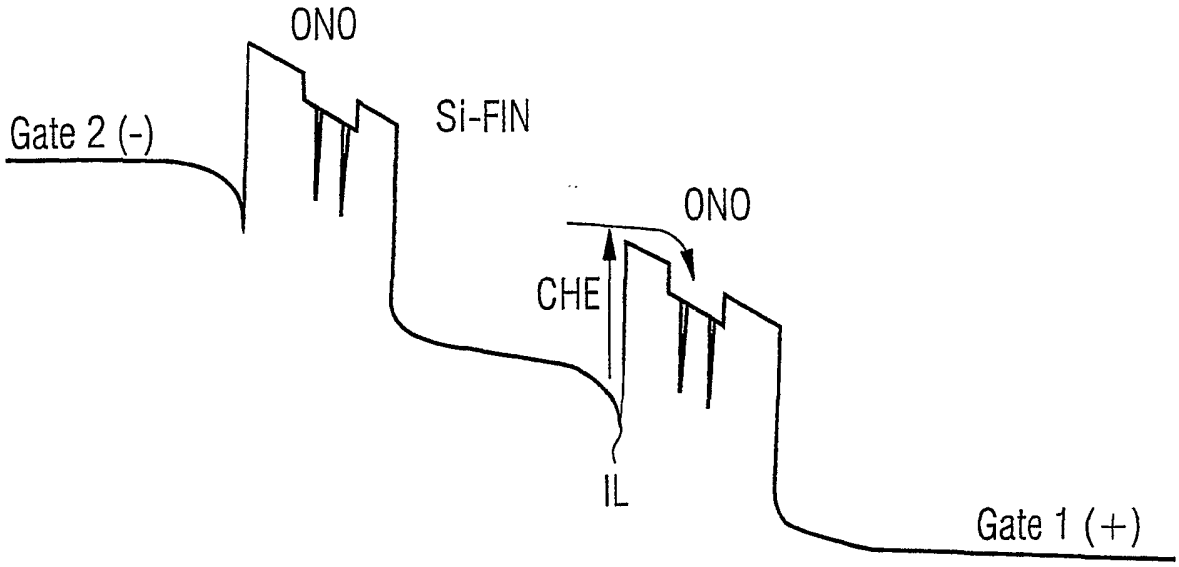

FIG 8

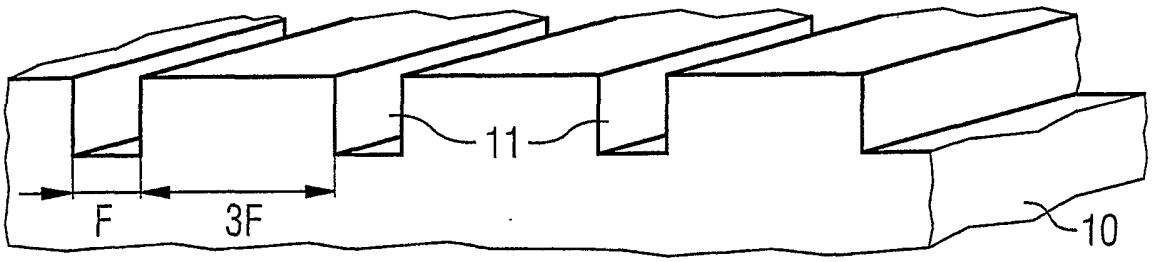

FIG 9

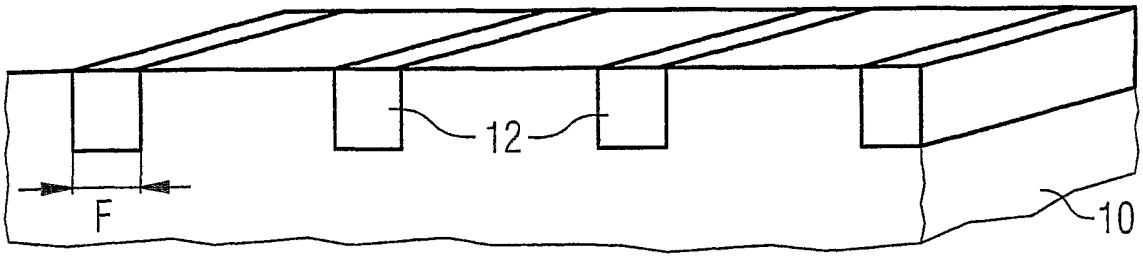

FIG 10

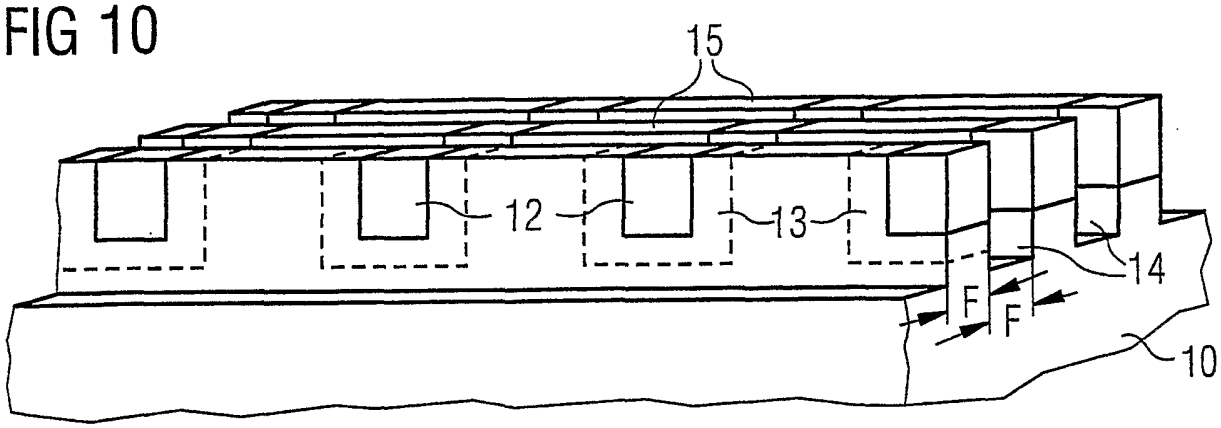

FIG 11

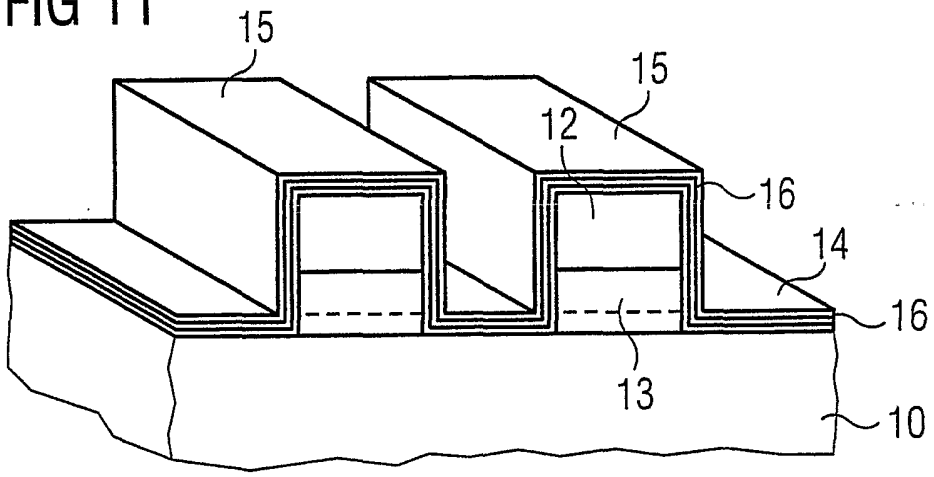

FIG 12

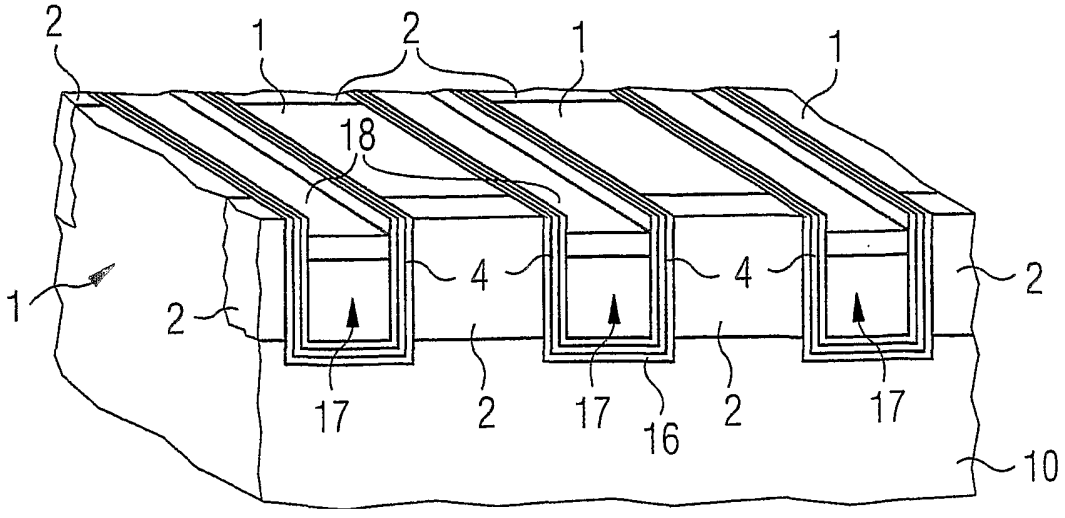

FIG 13

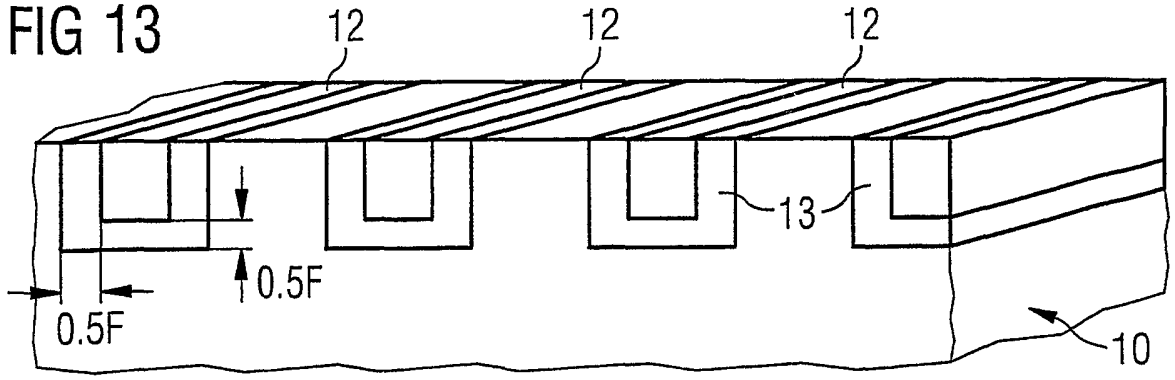

FIG 14

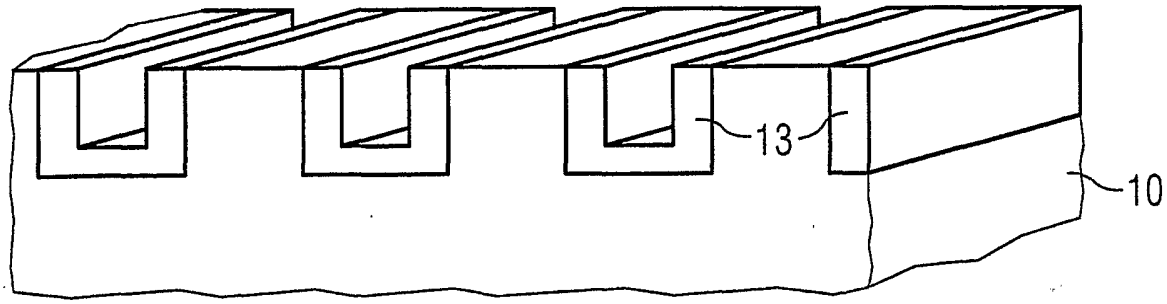

FIG 15

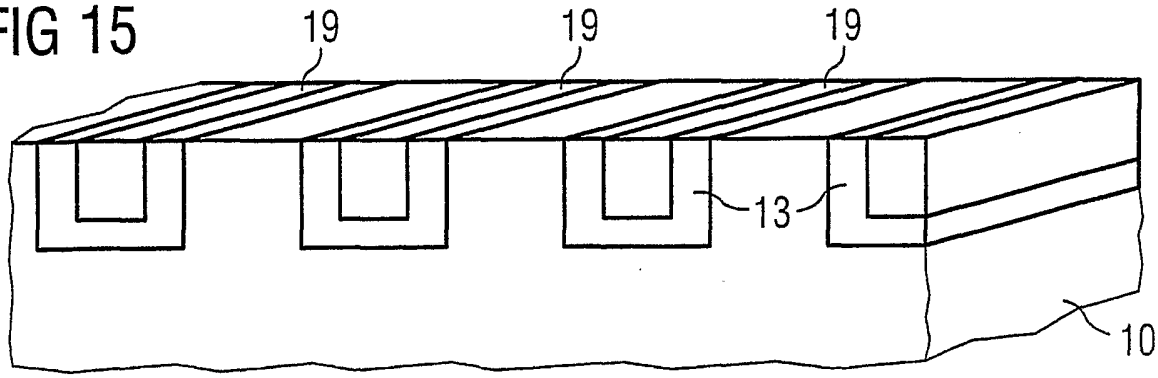

FIG 16

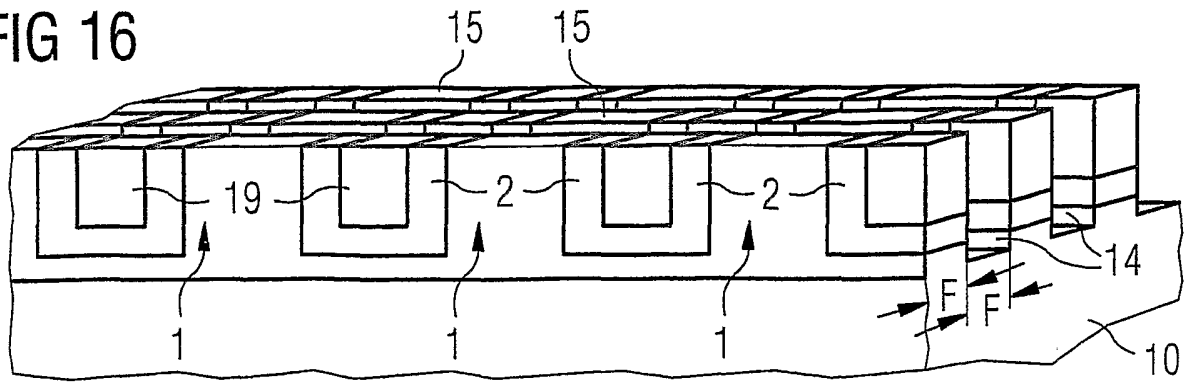

FIG 17

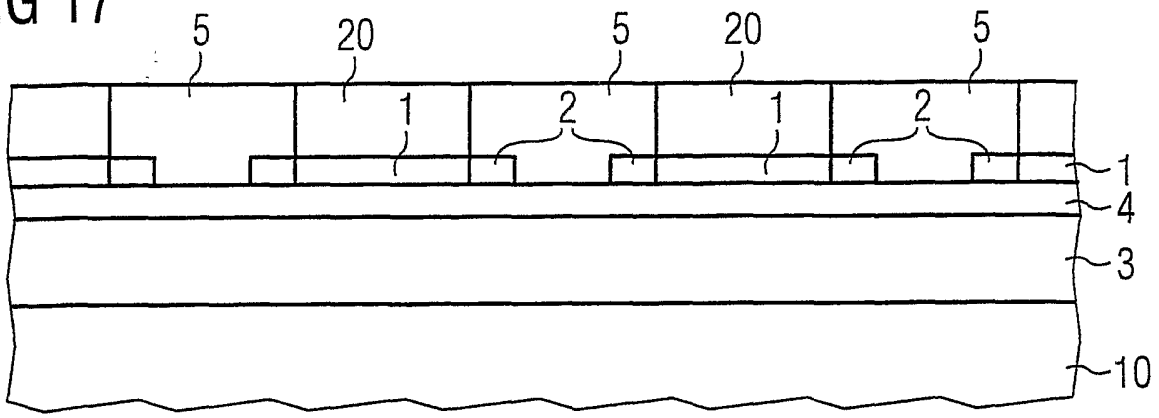

FIG 18

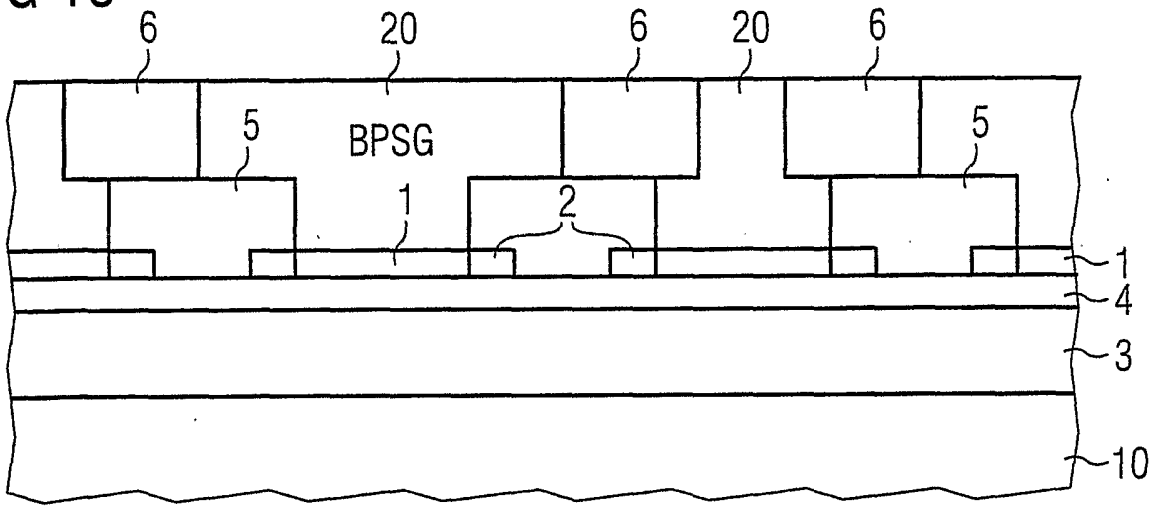

FIG 19