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(54) **SEMICONDUCTOR SUBSTRATE AND TEST PATTERN FOR THE SAME**

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(57) **ABSTRACT**

A test pattern used for testing an electrical characteristic of a semiconductor substrate, includes: a first conductive pattern formed on a lower surface of the semiconductor substrate; a second conductive pattern formed on an upper surface of the semiconductor substrate; first and second electrodes formed on the second conductive pattern, the electrodes being connected to test probes; and a first test via-hole formed through the semiconductor substrate to connect the first and second conductive pattern electrically to each other.

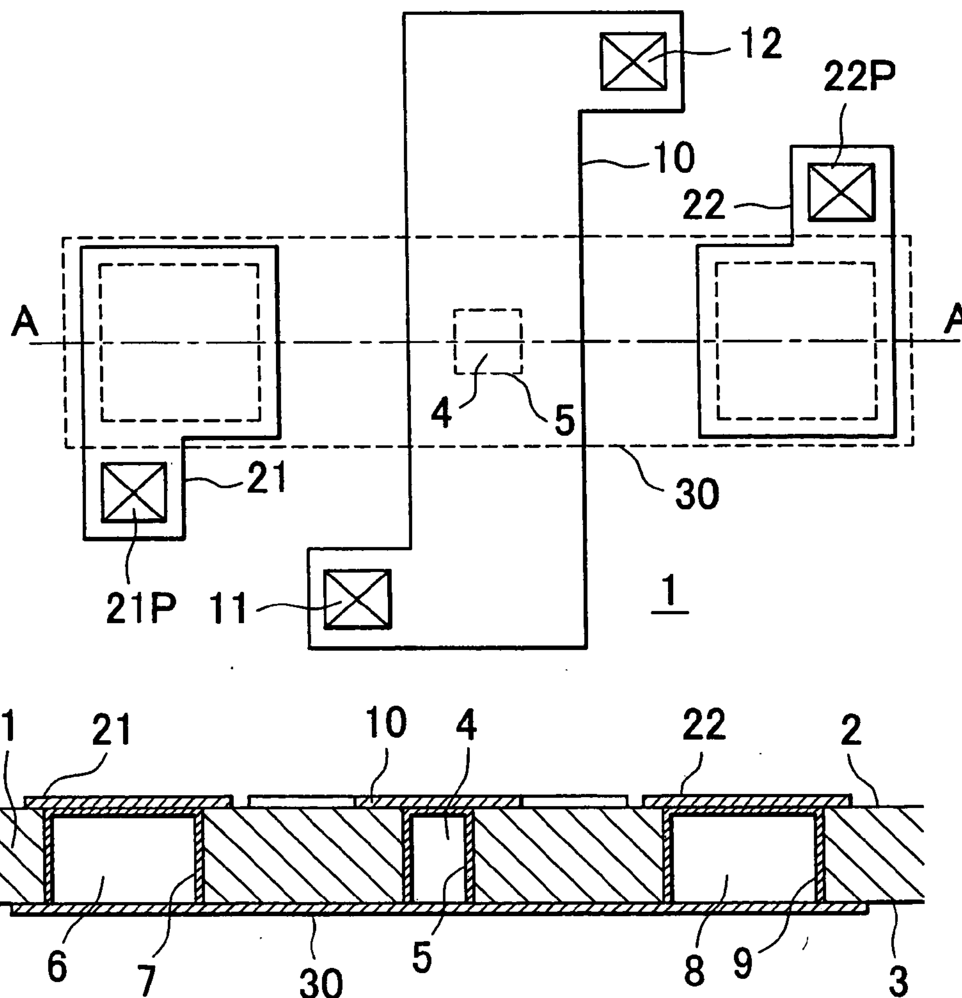


FIG. 1A

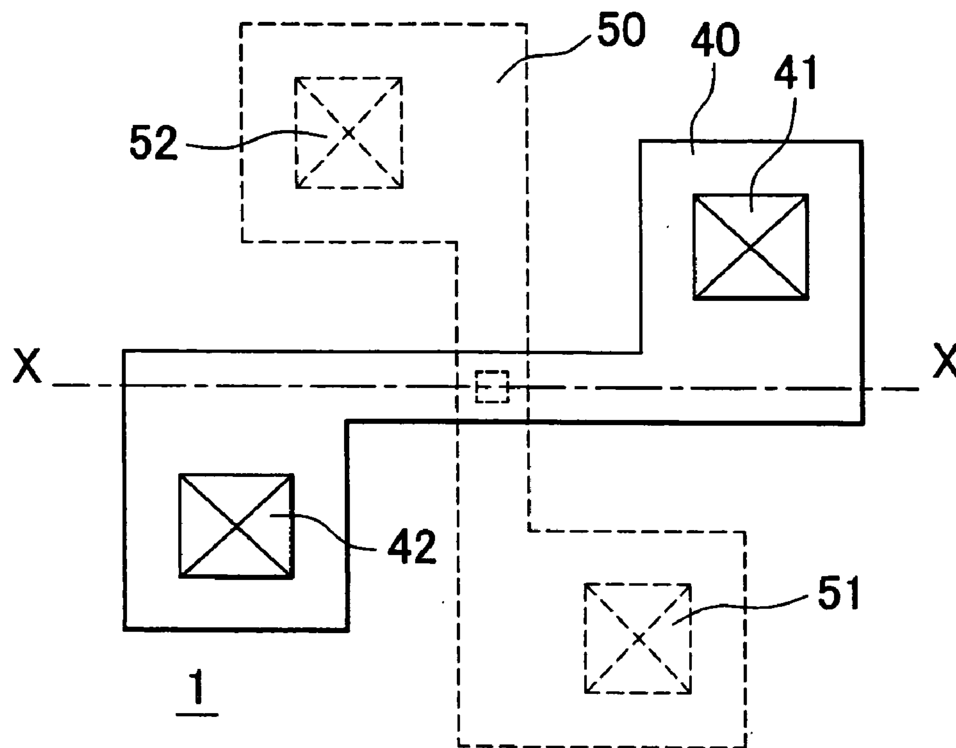
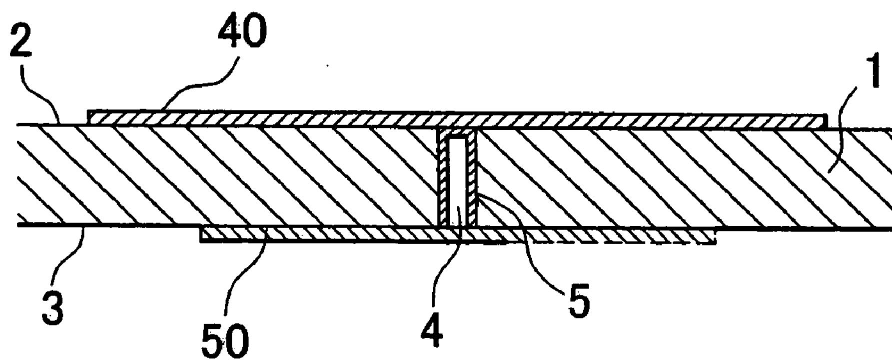



FIG. 1B



# FIG. 2

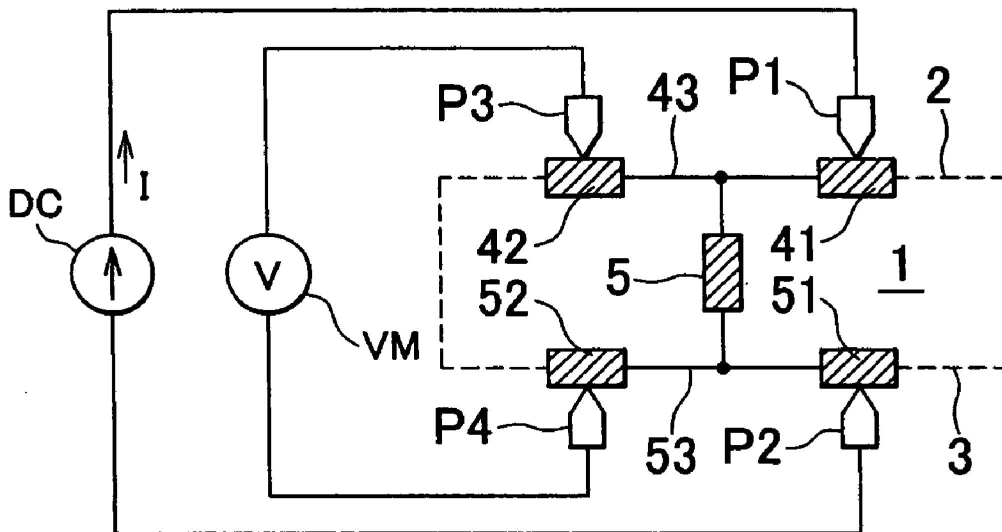


FIG. 3A

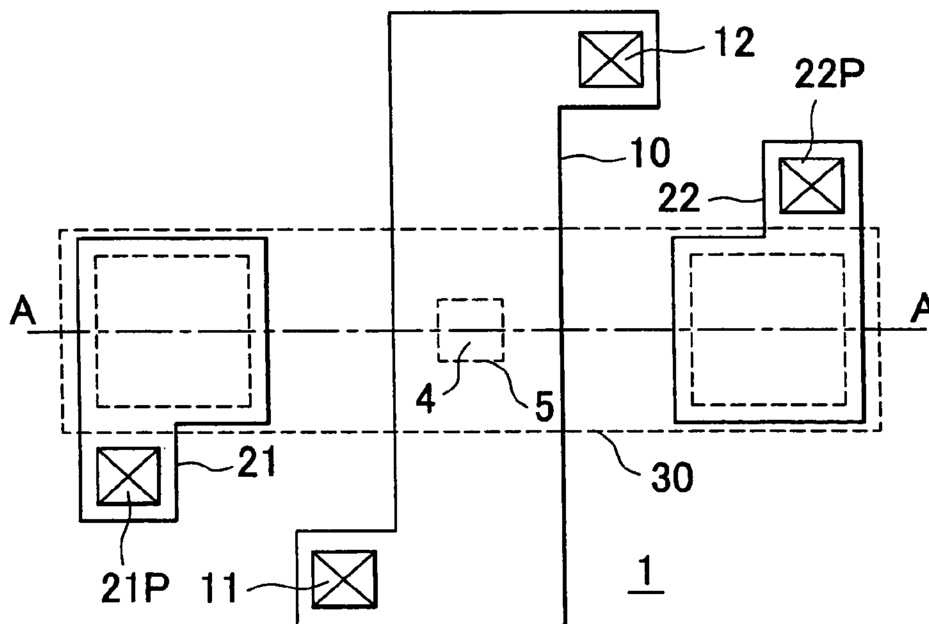



FIG. 3B

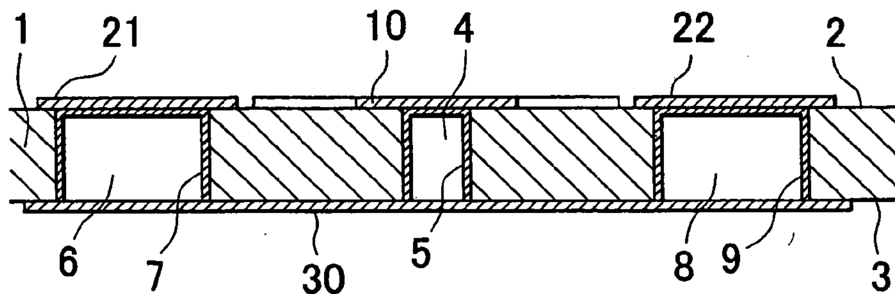
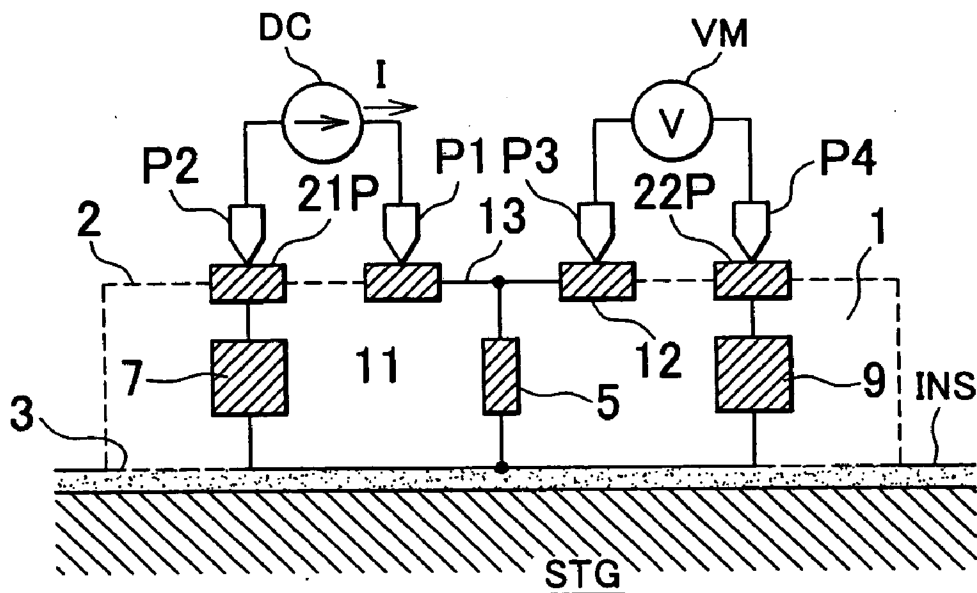
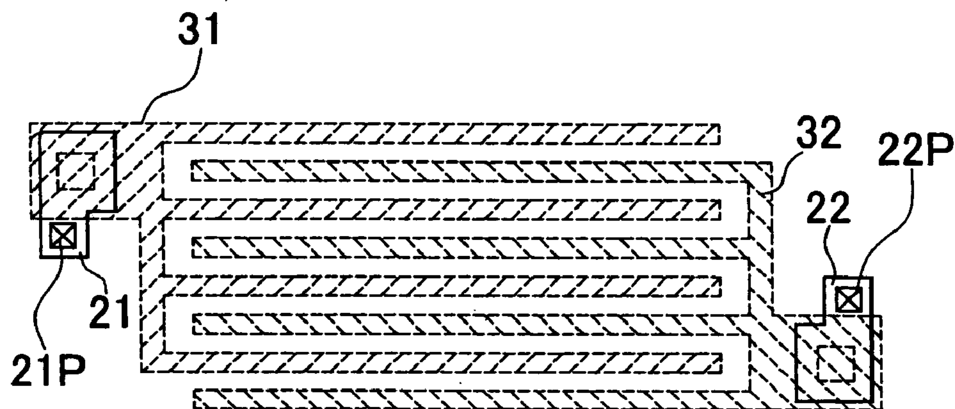


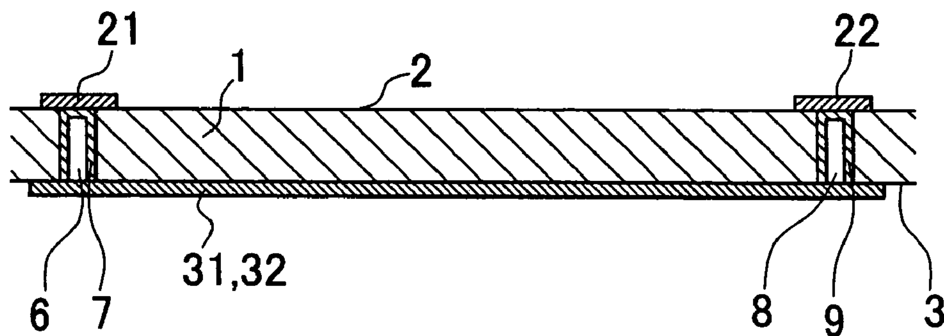
FIG. 4



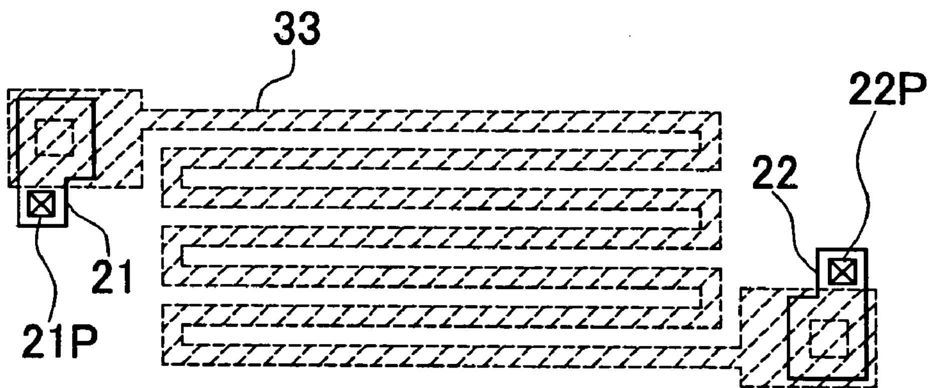
# FIG. 5A



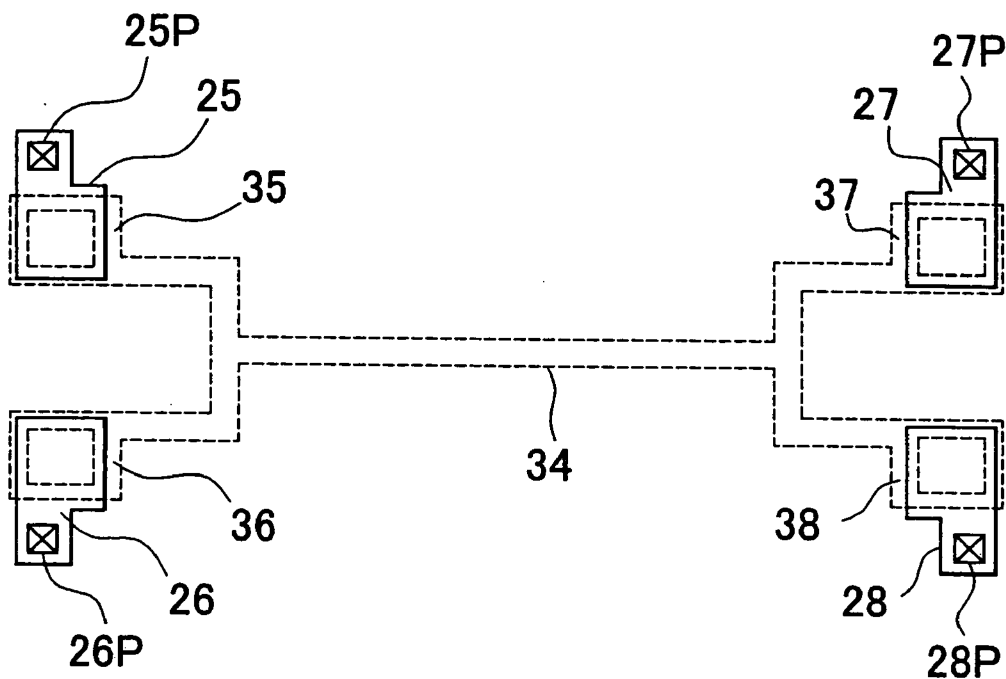

# FIG. 5B



# FIG. 6



# FIG. 7



# SEMICONDUCTOR SUBSTRATE AND TEST PATTERN FOR THE SAME

## CROSS REFERENCE TO RELATED APPLICATION

**[0001]** This application claims the priority of Application No. 2002-150534, filed May 24, 2002 in Japan, the subject matter of which is incorporated herein by reference.

## TECHNICAL FIELD OF THE INVENTION

**[0002]** This invention relates to a test pattern formed on a semiconductor substrate.

## BACKGROUND OF THE INVENTION

**[0003]** **FIG. 1A** is a plane view showing a conventional test pattern used for measuring a contact resistance of a via-hole formed in a semiconductor substrate. **FIG. 1B** is a cross-sectional view taken on line X-X in **FIG. 1A**.

**[0004]** The conventional test pattern (conductive pattern or wiring patter) is used for measuring a contact resistance of a conductive material **5** formed inside a via hole **4**, formed in a semiconductor substrate **1**. The semiconductor substrate **1** includes an upper surface **2** and a lower (or bottom) surface **3**. The via hole **4** is formed to pass through the semiconductor substrate **1**.

**[0005]** The test pattern includes an upper wiring pattern **40** formed on the upper surface **2** of the semiconductor substrate **1** and a lower (or bottom) wiring pattern **50** formed on the lower surface **3** of the semiconductor substrate **1**.

**[0006]** The upper wiring pattern **40** includes a pad (electrode) **41** to be in contact with a current supply probe, a pad **42** to be in contact with a voltage supply probe, and a contact pattern **43** to electrically connect the pads **41** and **42** to the conductive material **5**. The pads **41** and **42** and contact pattern **43** is formed in united body on the upper surface **2** of the semiconductor substrate **1**.

**[0007]** The lower wiring pattern **50** includes a pad (electrode) **51** to be in contact with a current supply probe, a pad **52** to be in contact with a voltage supply probe, and a contact pattern **53** to electrically connect the pads **51** and **52** to the conductive material **5**. The pads **51** and **52** and contact pattern **53** is formed in united body on the lower surface **3** of the semiconductor substrate **1**.

**[0008]** **FIG. 2** is circuit diagram of the conventional test pattern, shown in **FIGS. 1A and 1B**.

**[0009]** As shown in **FIG. 3**, the pads **41** and **51** are in contact with probes P1 and P2, respectively, so that a predetermined amount of electric current I is supplied from a direct power supply (DC) to the pads **41** and **51**. The current I flows along a path formed by the probe P1, the pad **41**, the conductive pattern **43**, the conductive material **5**, the conductive pattern, the pad **51** and the probe P2 in this order. As a result, a voltage, calculated by multiplying the current I and the contact resistance of the conductive material **5**, is applied between the ends of the conductive material **5**.

**[0010]** On the other hand, the pads **42** and **52** are in contact with probes P3 and P3, respectively. The voltage (potential) V applied between the pads **42** and **45** is measured by a voltage meter VM.

**[0011]** The voltage meter VM should have a high sensitivity so that the voltage V can be assumed to be the same as a voltage applied over the ends of the conductive material **5**. Therefore, the contact resistance R of the conductive material **5** is calculated by the following equation: R=V/I

**[0012]** However, according to the above-described conventional test pattern, the pads **41** and **42** are arranged on the upper surface **2** of the semiconductor substrate **1** while the pads **51** and **52** are arranged on the lower surface **3** of the semiconductor substrate **1**; and therefore, the probes P1 to P4 are required to be arranged and in contact to the pads **41**, **42**, **51** and **52** from the both sides of the semiconductor substrate **1**. As a result, it is required to use a specially-designed device for measuring or testing electrical characteristics of the semiconductor substrate **1**.

## OBJECTS OF THE INVENTION

**[0013]** Accordingly, an object of the present invention is to provide a test pattern with which electrical characteristics of a semiconductor substrate may be easily measured or tested.

**[0014]** Additional objects, advantages and novel features of the present invention will be set forth in part in the description that follows, and in part will become apparent to those skilled in the art upon examination of the following or may be learned by practice of the invention. The objects and advantages of the invention may be realized and attained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

## SUMMARY OF THE INVENTION

**[0015]** According to an aspect of the present invention, a test pattern used for testing an electrical characteristic of a semiconductor substrate, includes: a first conductive pattern formed on a lower surface of the semiconductor substrate; a second conductive pattern formed on an upper surface of the semiconductor substrate; first and second electrodes formed on the second conductive pattern, the electrodes being connected to test probes; and a first test via-hole formed through the semiconductor substrate to connect the first and second conductive pattern electrically to each other.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0016]** **FIG. 1A** is a plane view showing a conventional test pattern used for measuring a contact resistance of a via-hole formed in a semiconductor substrate.

**[0017]** **FIG. 1B** is a cross-sectional view taken on line X-X in **FIG. 1A**.

**[0018]** **FIG. 2** is circuit diagram of the conventional test pattern, shown in **FIGS. 1A and 1B**.

**[0019]** **FIG. 3A** is a plane view showing a test pattern, according to a first preferred embodiment of the present invention, used for measuring a contact resistance of a via-hole formed in a semiconductor substrate.

**[0020]** **FIG. 3B** is a cross-sectional view taken on line A-A in **FIG. 3A**.

**[0021]** **FIG. 4** is circuit diagram of the test pattern according to the first preferred embodiment, shown in **FIGS. 3A and 3B**.

[**0022**] **FIG. 5A** is a plane view showing a test pattern, according to a second preferred embodiment of the present invention, used for measuring an insulation resistance of a semiconductor substrate.

[**0023**] **FIG. 5B** is a cross-sectional view of **FIG. 5A**.

[**0024**] **FIG. 6** is a plane view showing a test pattern, according to a third preferred embodiment of the present invention, used for measuring a wiring resistance of a semiconductor substrate.

[**0025**] **FIG. 7** is a plane view showing a test pattern, according to a fourth preferred embodiment of the present invention, used for measuring a wiring resistance of a semiconductor substrate.

## DETAILED DISCLOSURE OF THE INVENTION

[**0026**] In the following detailed description of the preferred embodiments, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific preferred embodiments in which the inventions may be practiced. These preferred embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other preferred embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present inventions. The following detailed description is, therefore, not to be taken in a limiting sense, and scope of the present inventions is defined only by the appended claims.

[**0027**] **FIG. 3A** is a plane view showing a test pattern, according to a first preferred embodiment of the present invention, used for measuring a contact resistance of a via-hole formed in a semiconductor substrate. **FIG. 3B** is a cross-sectional view taken on line A-A in **FIG. 3A**.

[**0028**] The test pattern (conductive pattern or wiring patter) is used for measuring a contact resistance of a conductive material **5** formed inside a via hole **4**, formed in a semiconductor substrate **1**. The semiconductor substrate **1** includes an upper surface **2** and a lower (or bottom) surface **3**. The via hole **4** is formed to pass through the semiconductor substrate **1**.

[**0029**] The test pattern includes an upper wiring pattern **10** formed on the upper surface **2** of the semiconductor substrate **1** and a lower (or bottom) wiring pattern **30** formed on the lower surface **3** of the semiconductor substrate **1**.

[**0030**] The upper wiring pattern **10** includes a pad (electrode) **11** to be in contact with a current supply probe, a pad **12** to be in contact with a voltage supply probe, and a contact pattern **13** to electrically connect the pads **11** and **12** to the conductive material **5**. The pads **11** and **12** and contact pattern **13** is formed in united body on the upper surface **2** of the semiconductor substrate **1**.

[**0031**] The test pattern further includes other upper patterns **21** and **22**, which are not overlapped with the wiring pattern **10** on the upper surface **2** of the semiconductor substrate **1**. The upper patterns **21** and **22** are electrically connected to the lower wiring pattern **30** thought via holes **6** and **8**, respectively. The upper patterns **21** and **22** are provided thereon with pads **21P** and **22P**, which are to be in contact with a current supply probe and a voltage-measuring probe, respectively.

[**0032**] The lower wiring pattern **30** is shaped to extend and to connect the conductive material **5** to test via-holes **6** and **8**. The test via-holes **6** and **8** are provided with conductive inner layers **7** and **9**, which are electrically connected to the pattern **21** and **22** on the upper surface **2**, respectively.

[**0033**] **FIG. 4** is circuit diagram of the test pattern according to the first preferred embodiment, shown in **FIGS. 3A and 3B**. Now a method for measuring a contact resistance of the conductive material **5** is described in connection with **FIG. 4**.

[**0034**] First, an insulating material INS, for example, paper or quartz is arranged on a test stage STG. Next, the semiconductor substrate **1** is placed on the insulation material INS so that the upper surface **2** faces up.

[**0035**] Subsequently, current supply probes **P1** and **P2** are contacted to the pad **11** on the upper wiring pattern (upper circuit pattern) **10** and the pad **21** on the upper test pattern **21**, respectively. A direct current supply DC supplies a constant current I to the probes **P1** and **P2**. On the other hand, voltage measuring probes **P3** and **P4** are contacted to the pads **12** and **22**, respectively, so that a voltage is measured by a voltage meter VM.

[**0036**] When the constant current I is supplied to the probes **P1**, the current flows along the path formed by the pad **11**, the connection pattern **13**, the conductive material (inside wall) **5**, the lower wiring pattern **30**, the conductive material (inside wall) **7**, the pad **21P** and the probe **P2**, in this order. As a result, a voltage, calculated by multiplying the current I and the contact resistance of the conductive material **5**, is applied between the ends of the conductive material **5**.

[**0037**] On the other hand, the pad **P3** is applied with a voltage at an upper side of the conductive material **5** through the connection pattern **13** and the pad **12**. The pad **P4** is applied with a voltage at a lower side of the conductive material **5** through the lower wiring pattern **30**, the conductive material **9** and the pad **22P**. The voltage (potential) V applied between the pads **12** and **22** is measured by the voltage meter VM.

[**0038**] The voltage meter VM should have a high sensitivity so that the voltage V can be assumed to be the same as a voltage applied over the ends of the conductive material **5**. Therefore, the contact resistance R of the conductive material **5** is calculated by the following equation: $R=V/I$

[**0039**] As described above, according to the first preferred embodiment, all the pads **11**, **12**, **21P** and **22P** used for test are formed on the upper surface **2** of the semiconductor substrate **1**. Therefore, an electrical characteristic of the semiconductor substrate **1** can be performed easily.

[**0040**] **FIG. 5A** is a plane view showing a test pattern, according to a second preferred embodiment of the present invention, used for measuring an insulation resistance of a semiconductor substrate. **FIG. 5B** is a cross-sectional view of **FIG. 5A**.

[**0041**] The test pattern shown in **FIGS. 5A and 5B** is used for measuring an insulation resistance of the semiconductor substrate. The pattern includes upper patterns **21** and **22** and lower wiring patterns **31** and **32**. The lower wiring patterns **31** and **32** are shaped to be comb-branched patterns, which

are arranged to be opposed and nested or interlocked but not to be in contact to each other.

[**0042**] The semiconductor substrate **1** includes a couple of via holes **6** and **8**, which are provided with conductive inner materials **7** and **9**. The lower wiring pattern **31** is electrically connected to the upper pattern **21** through the conductive material **7** in the via hole **6**. A pad **21**P is formed on the upper pattern **21** so that a test probe is in contact therewith.

[**0043**] The lower wiring pattern **32** is electrically connected to the upper pattern **22** through the conductive material **9** in the via hole **8**. A pad **22**P is formed on the upper pattern **22** so that a test probe is in contact therewith.

[**0044**] In a measurement process, first, an insulating material, for example, paper or quartz is arranged on a test stage. Next, the semiconductor substrate **1** is placed on the insulation material so that the upper surface **2** faces up. Subsequently, the probes are contacted to the pads **21**P and **22**P and a resistance between those pads is measured.

[**0045**] As described above, according to the second preferred embodiment, both the pads **21**P and **22**P used for test are formed on the upper surface **2** of the semiconductor substrate **1**. As a result, the upper surface **2**, on which a micro-designed circuit is formed, is not in contact with a test stage; and therefore, an electrical characteristic of the semiconductor substrate **1** can be performed easily. Further, the upper surface **2** of the semiconductor substrate **1** is prevented from being damaged and having particles thereon.

[**0046**] **FIG. 6** is a plane view showing a test pattern, according to a third preferred embodiment of the present invention, used for measuring a wiring resistance of a semiconductor substrate.

[**0047**] The test pattern shown in **FIG. 6** is used for measuring a wiring resistance of the semiconductor substrate. The pattern includes upper patterns **21** and **22** and a lower wiring pattern **33**. The lower wiring pattern **33** is wound or shaped to be zigzag path.

[**0048**] The semiconductor substrate **1** includes a couple of via holes, which are provided with conductive inner materials, in the same manner as the above described second preferred embodiment. One end of the wiring pattern **33** is electrically connected to the upper pattern **21** through the via hole. A pad **21**P is formed on the upper pattern **21** so that a test probe is in contact therewith.

[**0049**] The other end of the wiring pattern **33** is electrically connected to the upper pattern **22** through the via hole. A pad **22**P is formed on the upper pattern **22** so that a test probe is in contact therewith.

[**0050**] In a measurement process, first, an insulating material, for example, paper or quartz is arranged on a test stage. Next, the semiconductor substrate **1** is placed on the insulation material so that the upper surface **2** faces up. Subsequently, the probes are contacted to the pads **21**P and **22**P and a resistance between those pads is measured.

[**0051**] As described above, according to the second preferred embodiment, both the pads **21**P and **22**P used for test are formed on the upper surface **2** of the semiconductor substrate **1**. As a result, the upper surface **2**, on which a micro-designed circuit is formed, is not in contact with a test stage; and therefore, an electrical characteristic of the semiconductor substrate **1** can be performed easily. Further, the upper surface **2** of the semiconductor substrate **1** is prevented from being damaged and having particles thereon.

[**0052**] **FIG. 7** is a plane view showing a test pattern, according to a fourth preferred embodiment of the present invention, used for measuring a wiring resistance of a semiconductor substrate.

[**0053**] The test pattern shown in **FIG. 7** is used for measuring a wiring resistance of the semiconductor substrate. The pattern includes upper patterns **25**, **26**, **27** and **28** and a lower wiring pattern (**34**, **35**, **36**, **37** and **38**). The lower wiring pattern **34** is shaped to have a center portion **34** extending straight and terminal portions **35**, **36**, **37** and **38**. The terminal portions **35** and **36** are arranged at one end of the center portion **34**, while the terminal portions **37** and **38** are arranged at the other end of the center portion **34**. The center portion **34** and the terminal portions **35-38** are formed in one united body.

[**0054**] The semiconductor substrate **1** includes four via holes, which are provided with conductive inner materials, in the same manner as the above described second and third preferred embodiment. The terminal portions **35-38** are electrically connected to the patterns **25-28**, respectively, through the via holes. Pads **25**P, **26**P, **27**P and **28**P are formed on the upper patterns **25-28**, respectively, so that test probes are contacted thereto.

[**0055**] In a measurement process, first, an insulating material, for example, paper or quartz is arranged on a test stage. Next, the semiconductor substrate **1** is placed on the insulation material so that the upper surface **2** faces up. Subsequently, current supply probes are contacted to the pads **25**P and **27**P, and voltage measuring probes are contacted to the pads **25**P and **28**P.

[**0056**] Next, a constant current I is supplied between the pads **25**P and **27**P, and a voltage V applied between the pads **26**P and **28**P is measured. Therefore, the wiring resistance R is calculated by the following equation: $R=V/I$

[**0057**] As described above, according to the second preferred embodiment, all the pads **25**P to **28**P used for test are formed on the upper surface **2** of the semiconductor substrate **1**. As a result, the upper surface **2**, on which a micro-designed circuit is formed, is not in contact with a test stage; and therefore, an electrical characteristic of the semiconductor substrate **1** can be performed easily. Further, the upper surface **2** of the semiconductor substrate **1** is prevented from being damaged and having particles thereon.

[**0058**] Wiring patterns formed on the upper and lower surfaces **2** and **3** of the semiconductor substrate are not limited by the above described embodiments.

[**0059**] The invention may be applied to a measurement of any of electric characteristics, for example, capacitance and inductance, in addition to insulation resistance and wiring resistance.

**1-22**. (canceled)

**23**. A test pattern used for testing a resistance of a subject pattern of a semiconductor substrate, comprising:

a lower wiring pattern as the subject pattern, formed on a lower surface of the substrate and shaped to follow a zigzag path;

first and second upper patterns formed on an upper surface of the substrate, first and second electrodes formed respectively on the first and second upper patterns for connection to respective first and second test probes; and

a first via-hole formed through the substrate to connect electrically to each other one end of the lower wiring pattern and the first upper pattern; and

a second via-hole formed through the substrate to connect electrically to each other the other end of the lower wiring pattern and the second upper pattern.

**24**. A test pattern according to claim 23, wherein conductive inner materials are provided in the first and second via holes.

* * * * *