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(54) Title: FLATTENING PROCESS FOR BONDED SEMICONDUCTOR SUBSTRATES		
(57) Abstract Process for the preparation of a substrate having a semiconductor layer of a target thickness, T_t. In the process, two wafers are bonded face to face to form a substrate wherein one of the wafers has a known thickness, T_{known}, and a total thickness variation of less than about 0.75 micrometers and the second wafer comprises a layer of semiconductor material. The substrate is thinned in a first stock removal step to reduce the thickness of the semiconductor layer. The distance between the front and back surfaces of the thinned substrate at discrete positions on said front surface is measured to generate thickness profile data. Additional stock is removed from the front surface of the thinned substrate in a second stock removal step to reduce the thickness of the semiconductor layer to the target thickness, T_t, with the amount of stock being removed at each of said discrete positions being determined after taking into account the thickness profile data, T_t, and T_{known}.		

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FLATTENING PROCESS FOR BONDED SEMICONDUCTOR SUBSTRATESBackground of the Invention

The present invention relates to a process for flattening the surface of a semiconductor substrate which comprises two or more bonded semiconductor wafers. In particular, the present invention provides a means to obtain bonded substrates having a uniform and specified thickness and to populations of bonded substrates resulting from this process.

Semiconductor on insulator ("SOI") substrates are finding increasing application in the semiconductor industry. These substrates generally comprise a thin silicon or other semiconductor layer commonly referred to as the device layer, an insulating layer, and a wafer bulk or support layer. The insulating layer, which typically comprises silicon dioxide silicon nitride or another dielectric material, electrically isolates the device layer from the support layer.

SOI substrates have been prepared by bonding two silicon wafers together. In general, an insulating layer is formed on the polished face of one or both of the wafers, and the two wafers are bonded together with the insulating layer(s) being at the bonding interface. The thickness of one of the bonded wafers is then reduced by various means to produce a thin device layer on the insulating layer.

One method which has been suggested for producing SOI substrates is the bond and etch back method which is schematically depicted in Fig. 1. The starting materials for this method are a handle wafer 1 and a device wafer 2. The handle wafer 1 has a bulk silicon layer 3 and an oxide layer 4. The device wafer 2 has an epitaxially grown device layer 5 of silicon, an epitaxially grown layer 6 of very heavily doped silicon, and a bulk silicon layer 7. The wafers are then joined to form a bonded

substrate 8 with the device layer 5 being bonded to the oxide layer 4. Bulk silicon layer 7 is removed by etching, or by a combination of mechanical grinding followed by etching to expose heavily doped silicon layer 6. Heavily doped silicon layer 6 is then removed with a preferential etch solution to yield an SOI substrate 9 having an exposed device layer 5 overlying an insulating layer 4 and a support layer 3. See, for example, European Patent Application, Publication No. 0 520 216 A2.

While the bond and etch back method can be used to produce high quality SOI substrates, it is relatively complex to execute and is subject to a variety of constraints. For example, epitaxial growth is generally carried out at lower temperatures to minimize doping of the device layer, which has the effect of reducing epitaxial growth rate and thus, throughput for an installed base of epitaxial reactors. For this same reason, the insulating oxide layer is typically grown on the handle wafer instead of the device wafer.

Another method which has been suggested for reducing the thickness of one of the joined wafers is plasma assisted chemical etching ("PACE") which is schematically depicted in Fig. 2. In this method, a SOI substrate 8' is formed by bonding a handle wafer 1 having a silicon layer 3 and an oxide layer 4 to a silicon device wafer 2. The substrate 8' is then thinned in two stock removal steps. In the first step, silicon stock is rapidly, but not necessarily uniformly, removed from surface 10 by conventional grinding, chemo-mechanical polishing or other gross stock removal means to produce a film 2' having an intermediate thickness, T_{int} , which is in excess of the final target thickness, T_t , of the device layer. To reduce the nonuniformity introduced in the first stock removal step, the thickness profile of film 2' is measured using an ellipsometer, a high frequency acoustic

wave device, or a full surface interferometer. The profile data representing point-by-point thickness of the film 2' is then processed to yield a dwell time versus position map for the entire surface of the film 2'. This map is used to control the movement of a material removal tool (such as a plasma puck) over the film 2' to locally remove additional stock from the surface 10' of layer 2' to produce an SOI wafer 9 having a device layer 5 which has a thickness, T_t . See, for example, U.S. Patent No. 5,254,830.

One advantage of the PACE method is that it produces an SOI substrate having a device layer with very little total thickness variation ("TTV") about a target thickness, e.g., about 10 nanometers of TTV. Significantly, however, this method relies upon an optical thickness measurement of the device layer which requires that the operating wavelength of the thickness profile measurement device be within the transparency range of the device layer. At the wavelengths which are typically used, therefore, this method may not be used to measure device layers which are greater than about 7 micrometers in thickness nor can it be used to measure the thickness of highly doped or other optically opaque layers. Furthermore, only the TTV of device layer is controlled in this approach; any TTV which exists in the support layer is ignored and "printed into" the SOI substrate. This effect is schematically depicted in Fig. 3 which illustrates in exaggerated detail an SOI substrate prepared using a handle wafer having considerable TTV; the result is an SOI substrate having little or no TTV in device layer 5, but considerable TTV in silicon layer 3 and in the substrate 9.

Summary of the Invention

Among the several objects of this invention, therefore, may be noted the provision of a process for the preparation of a substrate which is not unduly
5 complex, a process which enables an insulating layer to be formed on the handle wafer, the device wafer or both prior to bonding, a process which has no thermal processing constraints, a process which enables the use of optically opaque layers, and a process which enables
10 TTV control of the substrate and not just the device layer.

Briefly, therefore, the present invention is directed to a process for the preparation of a substrate having a semiconductor layer of a target thickness, T_t .
15 The process comprises bonding two wafers face to face to form a substrate wherein one of the wafers has a known thickness, T_{known} , and a total thickness variation of less than about 0.75 micrometers and the second wafer comprises a layer of semiconductor material. The
20 substrate is thinned in a first stock removal step to reduce the thickness of the semiconductor layer. The distance between the front and back surfaces of the thinned substrate at discrete positions on said front surface is measured to generate thickness profile data.
25 Additional stock is then removed from the front surface of the thinned substrate in a second stock removal step to reduce the thickness of the semiconductor layer to the target thickness, T_t , with the amount of stock being removed at each of said discrete positions being
30 determined after taking into account the thickness profile data, T_t , and T_{known} .

The present invention is also directed to a population of substrates, prepared by bonding two or more wafers. The population consists of at least 10
35 substrates having an average total thickness variation for the substrate which does not exceed about 0.2

micrometers and an average total thickness variation for the semiconductor layer which does not exceed about 0.5 micrometers.

Other objects and features will be in part apparent and in part pointed out hereinafter.

Brief Description of the Drawings

Fig. 1 is a schematic cross-sectional view of a bonded SOI substrate prepared in accordance with a first prior art method;

Fig. 2 is a schematic cross-sectional view of a bonded SOI substrate prepared in accordance with a second prior art method;

Fig. 3 is a schematic cross-sectional view of a bonded SOI substrate prepared in accordance with the second prior art method using a handle wafer having substantial total thickness variation; and

Fig. 4 is a schematic cross-sectional view of a bonded SOI substrate prepared in accordance with the process of the present invention.

Corresponding reference characters indicate corresponding parts throughout the several views of the drawings.

Description of the Preferred Embodiments

Referring now to the Figures, and more particularly to Fig. 4, the process of the present invention employs, as a starting material, a handle wafer 1. In general, handle wafer 1 may be patterned or unpatterned and it may have any diameter and target thickness which is appropriate for a semiconductor application; for example, the diameter may be from 4 to 8 inches (100 to 200 mm) or greater and the thickness may be from 475 to 725 micrometers or greater, with the thickness typically increasing with increasing diameter.

In the first process step, handle wafer 1 is flattened to form an ultra-flat wafer of known thickness. Preferably, the flattened wafer has a TTV of less than 1 micrometer, more preferably a TTV of less than about 0.75 micrometers, still more preferably a TTV of less than about 0.5 micrometers, most preferably a TTV of less than about 0.2 micrometers, and optimally a TTV of less than about 0.1 micrometers. Wafers meeting this TTV criteria may be prepared, for example, using the PACE-based technology disclosed in U.S. Patent Nos. 4,668,366, 5,254,830, 5,291,415, 5,375,064, 5,376,224, and 5,491,571. Precision wafer shaping equipment using this technology is commercially available from IPEC/Precision (Bethel, Connecticut) under the PWS-200 trademark.

In general, wafers having a surface roughness (rms) of less than about 0.1 nm over an area of $25\ \mu\text{m} \times 25\ \mu\text{m}$ are bondable. Plasma wafer-thinning processes, however, will typically leave the surface of the silicon wafer with a significant amount of surface roughness (rms) as measured, for example, with an Atomic Force Microscope (AFM). Thus, it is preferred that the roughness of the plasma thinned handle wafer surfaces be reduced to a value which is less than that level of roughness. This is conveniently done by a light polishing process referred to as a "kiss" polish. The algorithm to determine the amount of removal is as follows: (1) determine the peak ("p") to valley ("v") roughness of the plasma thinned surface, $r(p-v)$; (2) design the polishing process to remove approximately $3r(p-v)$ to $4r(p-v)$ using a finishing type slurry (e.g., diluted Glanzox); and (3) conventional RCA type cleaning. Removing this small amount of silicon does not detract from the TTV of the wafer.

Taking into the account the need to control TTV, handle wafer 1 comprises any material which mechanically supports the other layers, enables handling and

processing of the structure and does not constitute a source of contaminants for the device layer. Such materials include, for example, an elemental semiconductor material, a compound semiconductor material, polycrystalline silicon, a glass material such as quartz, or a ceramic material such as aluminum oxide, aluminum nitride or silicon carbide. Silicon is a preferred material for the handle wafer 1 with the conductivity type and resistivity not being critical.

Referring again to Fig. 4, handle wafer 1 is processed in a manner to form an insulating layer 4 comprising a dielectric material of known thickness on the surface of silicon layer 3. The thickness of the insulating layer 4 is generally between about 5 Å (0.5 nm) and about 5 micrometers, preferably about 0.4 to about 2 micrometers, with thicknesses in the range of about 300 to about 500 Å being typical. Silicon dioxide, silicon nitride or combinations thereof are preferred dielectric materials. Although the insulating layer is preferably formed by thermal growth processes, other techniques such as chemical vapor deposition and plasma enhanced deposition may also be suitable.

After the insulating layer is formed, handle wafer 1 is bonded to a similarly treated or untreated device wafer 2 to form a substrate 8'. More specifically, the insulating layer 4 of handle wafer 1 is bonded to the exposed surface of the device wafer 2. Bonding is done according to methods known in the art. Preferably, a direct bonding method is employed wherein the bonding surfaces are cleaned in a manner which leaves them hydrophilic, precisely aligned and bonded at room temperature. The substrate 6 is then annealed at an elevated temperature to increase the bond strength.

Referring again to Fig. 4, substrate 8' is thinned in a first stock removal step to produce a film 2' having an intermediate thickness, T_{int} . In general, this step is

a gross removal step in which stock is rapidly, but not necessarily uniformly, removed from the substrate. It may be carried out by a variety of conventional thinning techniques, such as grinding, chemomechanical polishing, or etching (plasma or chemical). Accordingly, the intermediate thickness, T_{int} resulting from this first removal step will be the target device layer thickness, T_t , plus an amount which is roughly about two-times the value of the TTV which was introduced during the first stock removal step. In general, conventional mechanical thinning methods will introduce about 1 to 5 micrometers of TTV and thus, the difference between T_{int} and T_t will generally be less than about 20 micrometers, preferably is less than about 10 micrometers and most preferably is less than about 5 micrometers.

If substrate 8' exhibits voids, bubbles and other delaminations as a result of non-uniform bonding at the edges of the handle and device wafers, the edge margin of layer 2' may be removed by mechanical means such as grinding or polishing or by etching (plasma or chemical) to eliminate these features which detract from the desirability of the substrates. Typically, this edge-stripping step, if carried out at all, will be carried out between the first and second stock removal steps.

After the first stock removal step, point-by-point thickness profile data is generated for the thinned substrate and mapped as a function of position on the surface of substrate 8' with data being generated at a sufficient number of discrete positions to assure full surface coverage for substrate 8'. The number of discrete positions, therefore, is at least 2, preferably at least 10, more preferably at least about 100, still more preferably at least about 1000 and, for some applications, most preferably at least about 5,000. The thickness measurement tool used to generate this data may be a capacitance, optical interference, FTIR, or

mechanical (e.g., micrometer) thickness measurement tool. Preferably, however, it is determined using a capacitance thickness measurement tool having a resolution of at least about 0.5 micrometers and more preferably a resolution of at least about 0.1 micrometers. A capacitance measurement tool having a resolution of about 0.1 to about 0.2 micrometers is commercially available from ADE Corporation (Newton, MA) under the ADE 7200 trademark. In operation, the introduction of a silicon wafer in the airgap of a parallel plate capacitor of these tools causes a change in capacitance. This capacitance change can be related to the thickness of the wafer and its effective dielectric constant. If the wafer is layered with materials of different dielectric constants, the effective dielectric constant can be extracted by modeling the layered structure as capacitances in series. For example, in the case of SOI layers where the buried oxides are uniform and thin (less than about $2\mu\text{m}$), the deviation caused by the differences in material is minimal and in any case can be precisely calculated if the buried oxide thickness is precisely known.

Significantly, because the thickness of the support layer 3 and the oxide layer 4 are known and because these layers are ultra-flat, the thickness and thickness variation of layer 2' can be calculated using an algorithm which operates on the thickness profile data, the known thickness of the handle wafer, T_{known} , and the target thickness value, T_t . For example, the amount of material to be removed to achieve the target thickness, T_t , can be determined by subtracting the known thickness of the handle wafer, T_{known} , from the thickness profile data at each discrete position. The difference between these numbers is then compared to the target thickness, T_t , for device layer 5 with the difference between the two values constituting the amount of stock which must be

removed at each position to achieve the target thickness, T_t .

Once the amount of material to be removed from each position in layer 2' is determined, this information is processed and converted to a dwell time versus position map which is used to control a stock removal tool during a second stock removal step. This second stock removal step may be executed using any tool which is capable of locally and precisely removing stock from small regions of layer 2' to produce device layer 5. The tool may be, for example, a chemomechanical polishing tool having micropolishing heads. Preferably, however, it is a PACE removal tool of the type described in U.S. Patent Nos. 4,668,366, 5,254,830, 5,291,415, 5,375,064, 5,376,224, and 5,491,571, which are commercially available from IPEC/Precision, Inc. under the PWS-200 trademark.

After the second stock removal step, substrate 8' has a TTV of less than 1 micrometer, more preferably a TTV of less than about 0.75 micrometers, still more preferably a TTV of less than about 0.5 micrometers, most preferably a TTV of less than about 0.2 micrometers, and optimally a TTV of less than about 0.1 micrometers. In general, device layer 5 has a TTV which is about twice the value of the TTV of the substrate 8'. Thus, device layer 5 has a TTV of less than 2 micrometers, more preferably a TTV of less than about 1.5 micrometers, still more preferably a TTV of less than about 1 micrometer, most preferably a TTV of less than about 0.4 micrometers, and optimally a TTV of less than about 0.2 micrometers. The final TTV values for the substrate and the device layer are achieved by starting with an ultra-flat handle wafer, accurately mapping the thickness of the substrate, and precision thinning the substrate using this map in the second stock removal step. Since the handle wafer is ultra-flat, the TTV which exists in the substrate prior to the second stock removal step is

substantially attributable to the nonuniformity (TTV) of the device layer. In addition, accurate mapping and precision thinning of the substrate enables the preparation of a device layer having a TTV which, after the second stock removal step, is comparable to the TTV of the substrate.

Substrate 8' may be optionally be subjected to a "kiss" polish to reduce the surface roughness (rms) after the second stock removal step to a value of about 1 Å over an area of 25 μm^2 . In general, about 1 to about 300 nanometers of silicon will be removed in this polish step. The polishing may be carried out in a chemical/mechanical polishing process using, for example, a dilute ammonia stabilized colloidal silica slurry and conventional polishing equipment. A preferred ammonia stabilized colloidal silica slurry is Glanzox 3900, which is commercially available from Fujimi Incorporated of Aichi Pref. 452, Japan. Glanzox 3900 has a silica content of from about 8 to about 10% and a particle size of from about 0.025 to about 0.035 μm . If the ammonia stabilized silica slurry is not diluted prior to use, the polished wafer will not be as smooth as a wafer treated with a diluted slurry. A dilution of about one part silica slurry to about 10 parts deionized water is preferred. After polishing, the substrate is subjected to a cleaning step using a standard cleaning solution such as H_2O - H_2O_2 - NH_4OH .

The process of the present invention offers particular advantages in the preparation of SOI substrates having relatively thick semiconductor layers, i.e., thicknesses of at least 1 micrometer, 3 micrometers, 5 micrometers, 7 micrometers, 10 micrometers, or even greater thicknesses. The process of the present invention also offers particular advantages in the preparation of SOI substrates having layers or regions which are optically opaque. This advantage

arises from the measurement technique used in this process. In the present invention, thickness measurements are taken using the backside of the support layer as the reference plane with measurement tools which do not require that the substrate be transparent to light of any wavelength. The backside of the support layer can be used as the reference plane because the support layer is derived from an ultra-flat handle wafer which introduces little TTV to the substrate.

10 As illustrated in Fig. 4, insulating layer 4 is formed on handle wafer 1. In practice, however, the insulating layer may be formed on the handle wafer, the device wafer or both prior to bonding so long as the two wafers are bonded together with the oxide layer(s) being at the bonding interface.

While the present invention has been described in the context of SOI substrates, its application is not limited to substrates comprising an insulating layer. It has general application to any semiconductor substrate prepared from two or more wafers in which one of the wafers is an ultra-flat wafer. Thus, for example, it may be used in applications in which each of the bonded wafers comprise semiconductor layers which may be patterned or unpatterned. It may also be used in applications where more than two wafers are bonded.

Furthermore, the wafer bonding and flattening process of the present invention enables the preparation of a population of semiconductor substrates having a tight distribution of TTV. That is, a population of at least about 10 substrates, preferably at least about 25 substrates, can be prepared having an average TTV for the substrate which does not exceed about 0.2 micrometers and an average TTV for the semiconductor layer which does not exceed about 0.5 micrometers.

In view of the above, it will be seen that the several objects of the invention are achieved and other advantageous results attained.

5 As various changes could be made in the above constructions and processes without departing from the scope of the invention, it is intended that all matter contained in the above description or shown in the accompanying drawings shall be interpreted as illustrative and not in a limiting sense.

CLAIMS:

WHAT IS CLAIMED IS:

1. A process for the preparation of a substrate having a semiconductor layer with a target thickness value, T_t , the process comprising
 - 5 bonding first and second wafers together face to face to form a substrate, the first wafer having a known thickness value, T_{known} , and a total thickness variation of less than about 0.75 micrometers, the second wafer comprising a semiconductor material, said substrate having front and back surfaces defined by unbonded faces
 - 10 of the first and second wafers, an interface between said front and back surfaces defined by bonded faces of the first and second wafers, a support layer between the back surface and the interface, and a semiconductor layer located between the front surface and the interface which
 - 15 comprises the semiconductor material,
 - thinning the substrate by removing stock from the front surface in a first stock removal step to reduce the thickness of the semiconductor layer to an intermediate thickness value, T_{int} , which is greater than T_t ,
 - 20 generating thickness profile data for the thinned substrate, said thickness profile data generation comprising measuring the distance between the front and back surfaces of the substrate at discrete positions on said front surface,
 - 25 determining the amount of stock to be removed at each of said discrete positions to reduce the thickness of the semiconductor layer to the target thickness value, T_t , said determination comprising use of an algorithm operating on the thickness profile data, T_t , and T_{known} , and
 - 30 removing stock from the front surface of the thinned substrate in a second stock removal step to reduce the thickness of the semiconductor layer to T_t , the amount of stock being removed at each of said discrete positions being based upon said determination.

2. The process of claim 1 wherein the process additionally comprises the step of flattening the first wafer to reduce the total thickness variation of the first wafer to a value of no more than about
5 0.75 micrometers prior to the bonding step.

3. The process of claim 2 wherein the process additionally comprises the step of polishing the first wafer after the flattening step and prior to the bonding step.

4. The process of claim 1 wherein the process additionally comprises the step of flattening the first wafer to reduce the total thickness variation of the first wafer to a value of no more than about
5 0.5 micrometers prior to the bonding step.

5. The process of claim 4 wherein the process additionally comprises the step of polishing the first wafer after the flattening step and prior to the bonding step.

6. The process of claim 1 wherein the process additionally comprises the step of flattening the first wafer to reduce the total thickness variation of the first wafer to a value of no more than about
5 0.2 micrometers prior to the bonding step.

7. The process of claim 6 wherein the process additionally comprises the step of polishing the first wafer after the flattening step and prior to the bonding step.

8. The process of claim 1 wherein the first wafer has a total thickness variation of less than about 0.5 micrometers.

9. The process of claim 1 wherein the first wafer has a total thickness variation of less than about 0.2 micrometers.

10. The process of claim 1 wherein the substrate contains a silicon dioxide layer having a thickness of at least about 300 Å which is between the semiconductor layer and the support layer.

11. The process of claim 1 wherein T_{int} is greater than T_t by no more than about 10 micrometers.

12. The process of claim 1 wherein T_{int} is greater than T_t by no more than about 5 micrometers.

13. The process of claim 1 wherein the substrate is polished after the second stock removal step.

14. The process of claim 1 wherein the thickness profile data is generated by measuring the capacitance of the substrate at said discrete positions.

15. A process for the preparation of a substrate having a semiconductor layer with a target thickness value, T_t , of at least about 1 micrometer, the process comprising

5 bonding first and second wafers together face to face to form a substrate, the first wafer having a known thickness value, T_{known} , and a total thickness variation of less than about 0.75 micrometers, the second wafer comprising a semiconductor material, at least one of said
10 first and second wafers comprising a layer of a dielectric material, said substrate having front and back surfaces defined by unbonded faces of the first and second wafers, an interface between said front and back

surfaces defined by bonded faces of the first and second
15 wafers, a support layer between the back surface and the
interface, a semiconductor layer located between the
front surface and the interface which comprises the
semiconductor material, and an insulating layer which
comprises the layer of dielectric material between the
20 semiconductor layer and the support layer,

thinning the substrate by removing stock from the
front surface in a first stock removal step to reduce the
thickness of the semiconductor layer to an intermediate
thickness value, T_{int} , which is greater than T_t ,

25 generating thickness profile data for the thinned
substrate, said thickness profile data generation
comprising measuring the distance between the front and
back surfaces of the substrate at discrete positions on
said front surface,

30 determining the amount of stock to be removed at
each of said discrete positions to reduce the thickness
of the semiconductor layer to the target thickness value,
 T_t , said determination comprising use of an algorithm
operating on the thickness profile data, T_t , and T_{known} , and

35 removing stock from the front surface of the thinned
substrate in a second stock removal step to reduce the
thickness of the semiconductor layer to T_t , the amount of
stock being removed at each of said discrete positions
being based upon said determination.

16. The process of claim 15 wherein the thickness
profile data is generated by measuring the capacitance of
the substrate at said discrete positions.

17. The process of claim 16 wherein the process
additionally comprises the step of flattening the first
wafer to reduce the total thickness variation of the
first wafer to a value of no more than about
5 0.2 micrometers.

18. The process of claim 17 wherein the process additionally comprises the step of polishing the first wafer after the flattening step and prior to the bonding step.

19. The process of claim 18 wherein the substrate is polished after the second stock removal step.

20. The process of claim 15 wherein the first wafer has a total thickness variation of less than about 0.2 micrometers.

21. The process of claim 15 wherein the first wafer has a total thickness variation of less than about 0.2 micrometers and the thickness profile data is generated by measuring the capacitance of the substrate
5 at said discrete positions.

22. The process of claim 15 wherein the dielectric layer is a silicon dioxide layer having a thickness of at least about 300 Å.

23. The process of claim 15 wherein the substrate is polished after the second stock removal step.

24. The process of claim 15 wherein the first wafer has a total thickness variation of less than about 0.2 micrometers, the thickness profile data is generated by measuring the capacitance of the substrate at said
5 discrete positions and the substrate is polished after the second stock removal step.

25. A process for the preparation of a substrate having a semiconductor layer with a target thickness value, T_t , of at least about 1 micrometer, the process comprising

5 flattening a first silicon wafer to reduce the total thickness variation of the wafer to a value of no more than about 0.5 micrometers, the flattened first silicon wafer having a known thickness value, T_{known} ,

 polishing the flattened wafer to reduce the surface
10 roughness (rms) of a face of the flattened wafer to a value of no more than about 0.1 nm over an area of $25\ \mu\text{m} \times 25\ \mu\text{m}$,

 forming a silicon dioxide layer on the polished face
15 of the first wafer or upon a face of a second silicon wafer,

 bonding the first and second wafers together face to
face to form a substrate, said substrate having front and back surfaces defined by unbonded faces of the first and second wafers, an interface between said front and back
20 surfaces defined by bonded faces of the two wafers, a support layer between the back surface and the interface, a silicon layer located between the front surface and the interface, and a dielectric layer between the support layer and the semiconductor layer which comprises said
25 silicon dioxide layer,

 thinning the substrate by removing stock from the front surface in a first stock removal step to reduce the thickness of the semiconductor layer to an intermediate thickness value, T_{int} , which is greater than T_t by no more
30 than about 10 micrometers,

 generating thickness profile data for the thinned substrate, said thickness profile data generation comprising measuring the distance between the front and back surfaces of the substrate at discrete positions on
35 said front surface using a capacitance measurement tool,

 determining the amount of stock to be removed at each of said discrete positions to reduce the thickness of the semiconductor layer to the target thickness value, T_t , said determination comprising use of an algorithm
40 operating on the thickness profile data, T_t , and T_{known} , and

removing stock from the front surface of the thinned substrate in a second stock removal step by etching the front surface with a plasma to reduce the thickness of the semiconductor layer to T_t , the amount of stock being
45 removed at each of said discrete positions being based upon said determination.

26. A population of substrates, each of which comprises bonded second and first wafers having front and back surfaces, an interface between said front and back surfaces defined by bonded faces of the two wafers, a
5 support layer between the back surface and the interface, a semiconductor layer located between the front surface and the interface which comprises a semiconductor material, and a dielectric layer between the support layer and the semiconductor layer, the population
10 consisting of at least 10 substrates having an average total thickness variation for the substrate which does not exceed about 0.2 micrometers and an average total thickness variation for the semiconductor layer which does not exceed about 0.5 micrometers.

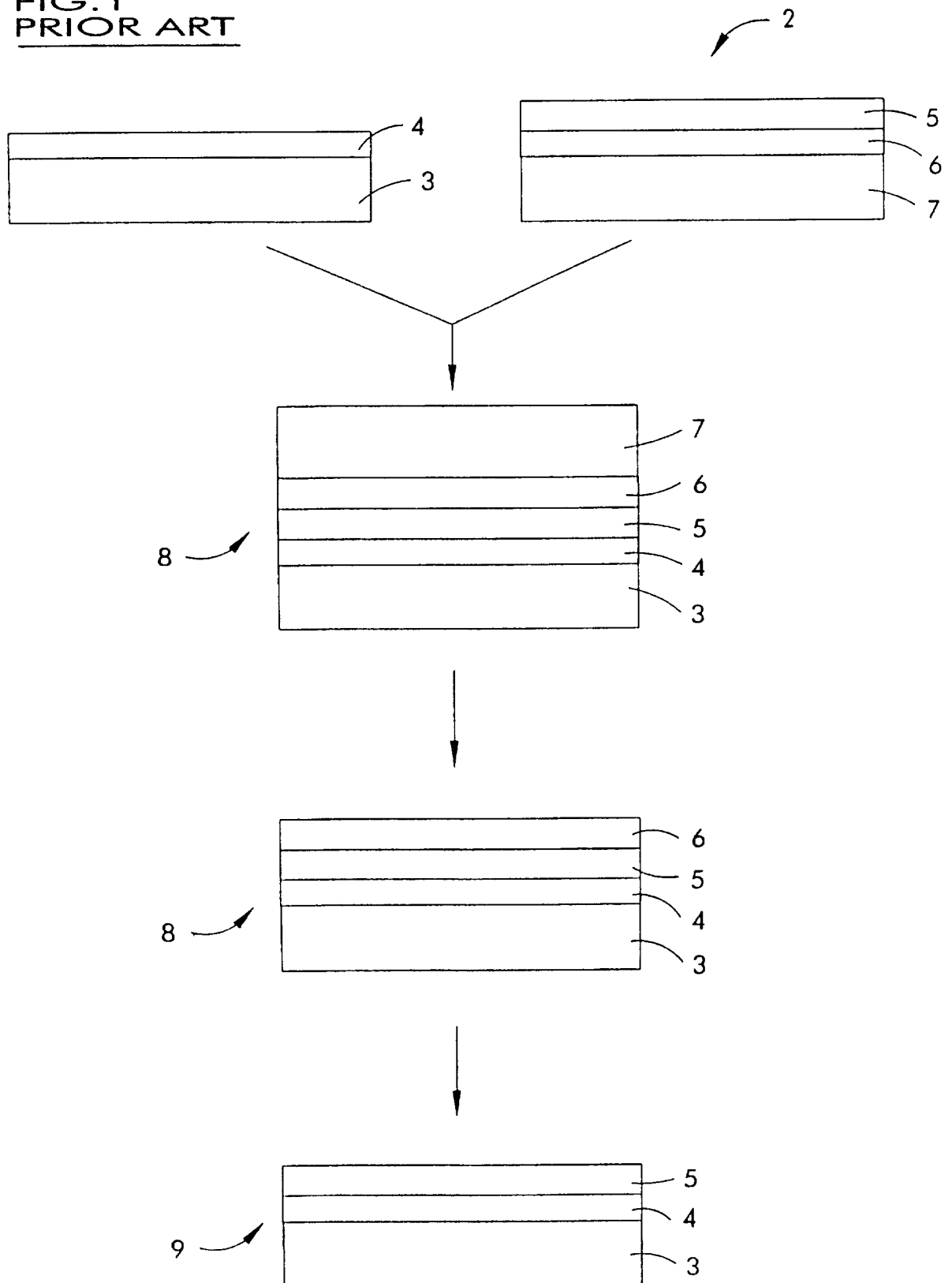
27. The population of wafers of claim 26 wherein the population consists of at least about 25 wafers.

28. The population of wafers of claim 26 wherein the dielectric layer of each of the wafers in the population comprises a layer of silicon dioxide of at least about 300 Å in thickness.

29. The population of wafers of claim 26 wherein the semiconductor layer of each of the wafers in the population comprises a layer of silicon of at least about 1 micrometer in thickness.

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FIG. 1
PRIOR ART



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FIG. 2
PRIOR ART

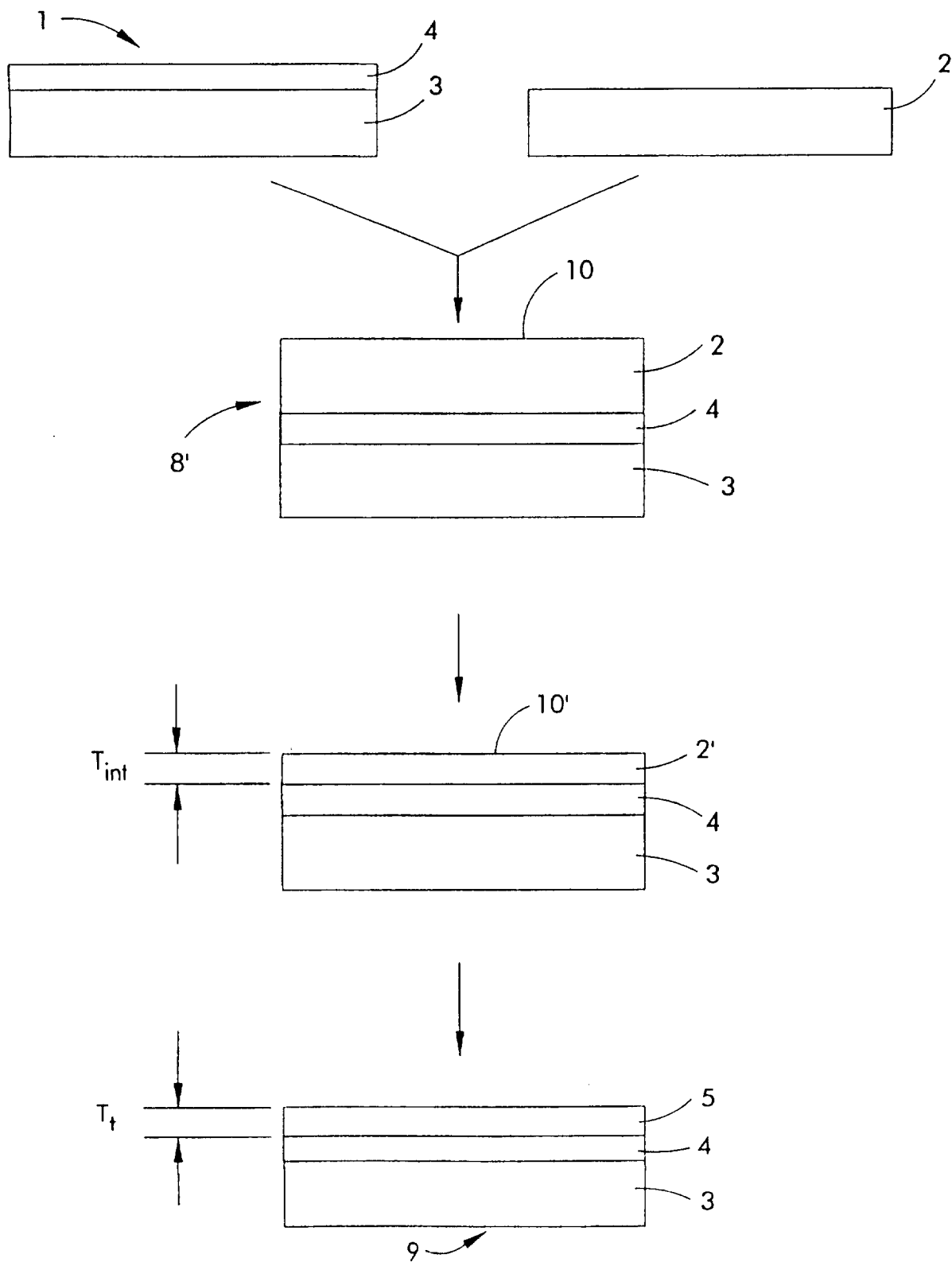
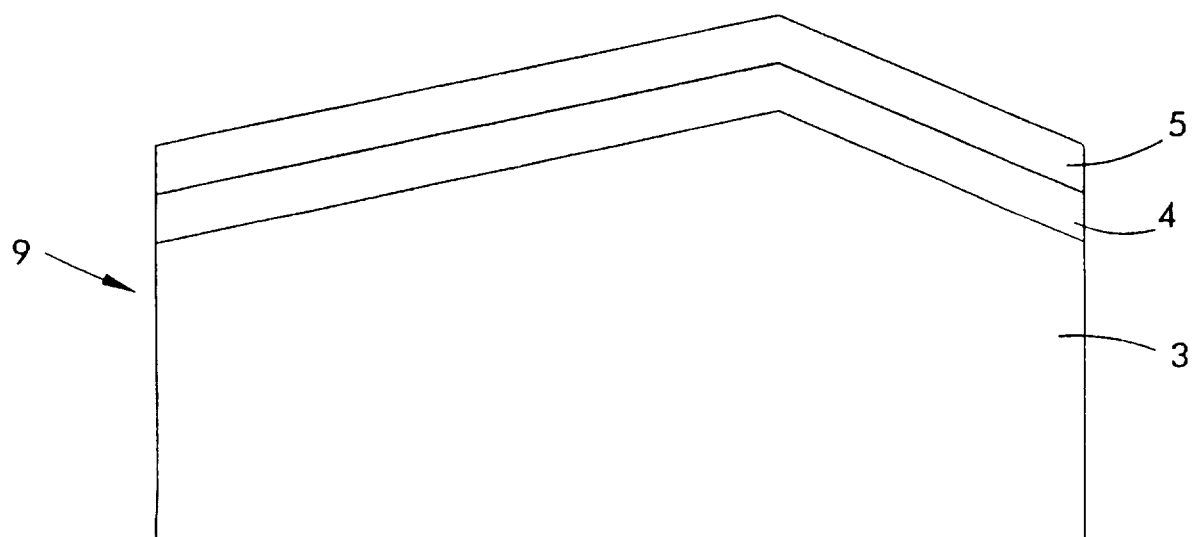
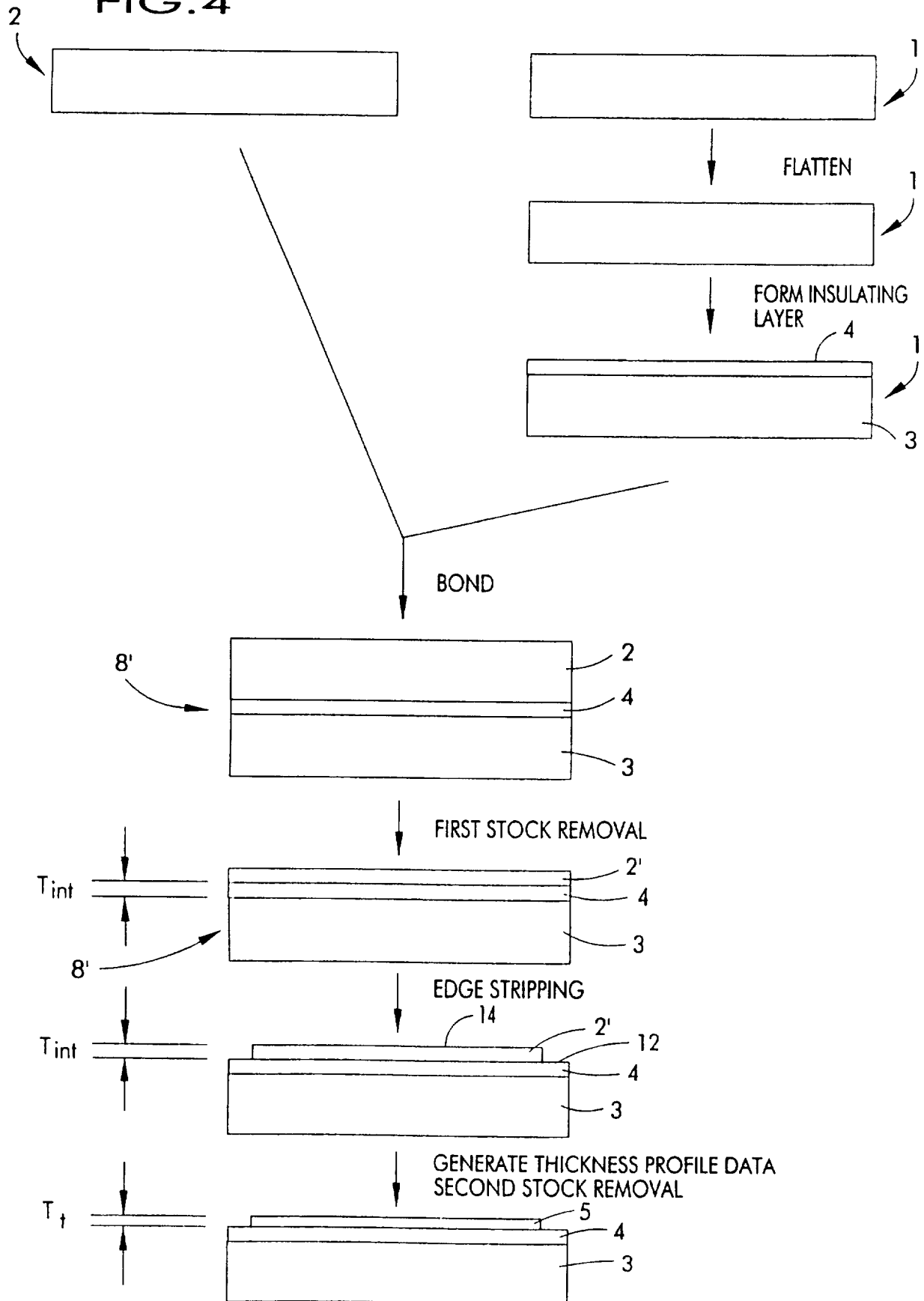


FIG.3
PRIOR ART



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FIG. 4



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/13069

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : B31F 1/22

US CL : 156/345,646,643,625,626,636,209,657,627; 219/43,54,59121

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 156/345,646,643,625,626,636,209,657,627; 219/43,54,59121

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,218,213 A (GAUL et al) 08 June 1993, col 1, lines 55-col 2, line 49	1,8-14,20-25
Y	US 5,494,849 A (LYER et al) 27 February 1996, col 4, lines 10-30	8, 9 12,13,14,20,22,24,23



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
A document defining the general state of the art which is not considered to be of particular relevance	*X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
E earlier document published on or after the international filing date	*Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	*A* document member of the same patent family
O document referring to an oral disclosure, use, exhibition or other means	
P document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

04 NOVEMBER 1997

Date of mailing of the international search report

04 DEC 1997

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INTERNATIONAL SEARCH REPORT**International application No.**
PCT/US97/13069**C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,254,830 A (ZAROWIN et al) 19 October 1993, col 3, lines 35-60	2-7,17,18,19