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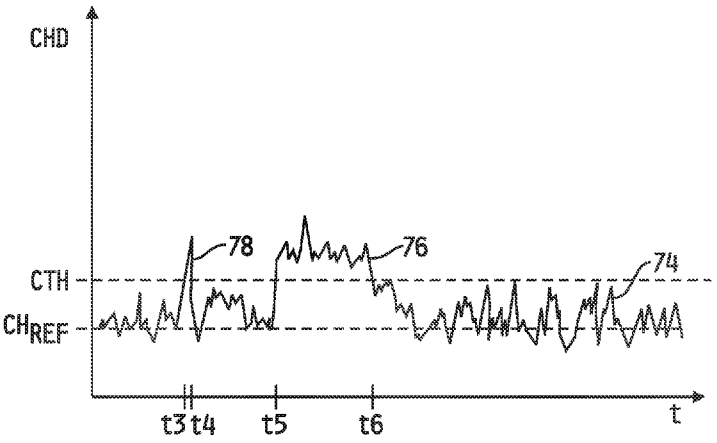


FIG. 5B

(57) Abstract: A system for trapping ions for measurement thereof may include an electrostatic linear ion trap (ELIT), a source of ions to supply ions to the ELIT, a processor operatively coupled to ELIT, and a memory having instructions stored therein executable by the processor to produce at least one control signal to open the ELIT to allow ions supplied by the source of ions to enter the ELIT, determine an ion inlet frequency corresponding to a frequency of ions flowing from the source of ions into the open ELIT, generate or receive a target ion charge value, determine an optimum threshold value as a function of the target ion charge value and the determined ion inlet frequency, and produce at least one control signal to close the ELIT when a charge of an ion within the ELIT exceeds the optimum threshold value to thereby trap the ion in the ELIT.

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APPARATUS AND METHOD FOR CAPTURING IONS IN AN ELECTROSTATIC LINEAR ION TRAP

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of and priority to U.S. Provisional Patent Application Ser. No. 62/680,296, filed June 4, 2018, the disclosure of which is incorporated herein by reference in its entirety.

GOVERNMENT RIGHTS

[0002] This invention was made with government support under CHE1531823 awarded by the National Science Foundation. The United States Government has certain rights in the invention.

TECHNICAL FIELD

[0003] The present disclosure relates generally to charge detection mass spectrometry instruments, and more specifically to performing mass and charge measurements with such instruments.

BACKGROUND

[0004] Mass Spectrometry provides for the identification of chemical components of a substance by separating gaseous ions of the substance according to ion mass and charge. Various instruments and techniques have been developed for determining the masses of such separated ions, and one such technique is known as charge detection mass spectrometry (CDMS). In CDMS, ion mass is determined as a function of measured ion mass-to-charge ratio, typically referred to as "m/z," and measured ion charge.

[0005] High levels of uncertainty in m/z and charge measurements with early CDMS detectors has led to the development of an electrostatic linear ion trap (ELIT) detector in which ions are made to oscillate back and forth through a charge detection cylinder. Multiple passes of ions through such a charge detection cylinder provides for multiple measurements for each ion, and it has been shown that the uncertainty in charge measurements decreases with $n^{1/2}$, where n is the number of charge measurements. However, spurious, extraneous and/or other charges picked up on the charge detector can present challenges to distinguishing valid and detectable charges from charge detector noise, and this effect becomes even more pronounced as charge signal levels approach the noise floor of the charge detector. Accordingly, it is desirable to seek improvements in ELIT design and/or operation which extend

the range of valid, detectable charge measurements over those obtainable using current ELIT designs.

SUMMARY

[0006] The present disclosure may comprise one or more of the features recited in the attached claims, and/or one or more of the following features and combinations thereof. In a first aspect, a system for trapping ions for measurement thereof may comprise an electrostatic linear ion trap (ELIT), a source of ions configured to supply ions to the ELIT, a processor operatively coupled to the ELIT, and a memory having instructions stored therein which, when executed by the at least one processor, cause the at least one processor to (i) produce at least one control signal to open the ELIT to allow ions supplied by the source of ions to enter the ELIT, (ii) determine an ion inlet frequency corresponding to a frequency of ions flowing from the source of ions into the open ELIT, (iii) generate or receive a target ion charge value, (iv) determine an optimum threshold value as a function of the target ion charge value and the determined ion inlet frequency, and (v) produce at least one control signal to close the ELIT when a charge of an ion within the ELIT exceeds the optimum threshold value to thereby trap the ion in the ELIT.

[0007] In a second aspect, a method is provided for trapping in an electrostatic linear ion trap (ELIT) ions supplied by a source of ions for measurement thereof. The method may comprise (i) producing, with a processor, at least one control signal to open the ELIT to allow ions supplied by the source of ions to enter the ELIT, (ii) determining, with the processor, an ion inlet frequency corresponding to a frequency of ions flowing from the source of ions into the open ELIT, (iii) generating or receiving, with the processor, a target ion charge value, (iv) determining, with the processor, an optimum threshold value as a function of the target ion charge value and the determined ion inlet frequency, and (v) producing, with the processor, at least one control signal to close the ELIT when a charge of an ion within the ELIT exceeds the optimum threshold value to thereby trap the ion in the ELIT.

[0008] In a third aspect, a system for separating ions may comprise the ion trapping system described in either of the above aspects, wherein the source of ions is configured to generate ions from a sample, and at least one ion separation instrument configured to separate the generated ions as a function of at least one molecular characteristic, wherein ions exiting the at least one ion separation instrument are supplied to the ELIT.

[0009] In a fourth aspect, a system for separating ions may comprise an ion source configured to generate ions from a sample, a first mass spectrometer configured to separate the generated ions as a function of mass-to-charge ratio, an ion dissociation stage positioned

to receive ions exiting the first mass spectrometer and configured to dissociate ions exiting the first mass spectrometer, a second mass spectrometer configured to separate dissociated ions exiting the ion dissociation stage as a function of mass-to-charge ratio, and the system described above in the third aspect coupled in parallel with and to the ion dissociation stage such that the system of the third aspect can receive ions exiting either of the first mass spectrometer and the ion dissociation stage, wherein the system of the third aspect is a charge detection mass spectrometer (CDMS), wherein masses of precursor ions exiting the first mass spectrometer are measured using the CDMS, mass-to-charge ratios of dissociated ions of precursor ions having mass values below a threshold mass are measured using the second mass spectrometer, and mass-to-charge ratios and charge values of dissociated ions of precursor ions having mass values at or above the threshold mass are measured using the CDMS.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a simplified diagram of an ion mass detection system including an embodiment of an electrostatic linear ion trap (ELIT) with control and measurement components coupled thereto.

[0011] FIG. 2A is a magnified view of the ion mirror M1 of the ELIT illustrated in FIG. 1 in which the mirror electrodes of M1 are controlled to produce an ion transmission electric field therein.

[0012] FIG. 2B is a magnified view of the ion mirror M2 of the ELIT illustrated in FIG. 1 in which the mirror electrodes of M2 are controlled to produce an ion reflection electric field therein.

[0013] FIG. 3 is a simplified diagram of an embodiment of the processor 16 illustrated in FIG. 1.

[0014] FIGS. 4A – 4C are simplified diagrams of the ELIT of FIG. 1 demonstrating sequential control and operation of the ion mirrors and of the charge generator to capture at least one ion within the ELIT and to cause the ion(s) to oscillate back and forth between the ion mirrors and through the charge detection cylinder to measure and record multiple charge detection events.

[0015] FIG. 5A is a plot of charge detection cylinder charge vs. time illustrating an example charge detection threshold level in comparison to a large amplitude charge detection signal riding on noisy charge reference on the charge detection cylinder.

[0016] FIG. 5B is a plot of charge detection cylinder charge vs. time illustrating a modified charge detection threshold, as compared with FIG. 3A, selected to provide for

triggering on a combination of low-amplitude charge detection signals and noise on the charge detection cylinder during trigger trapping operation of the ELIT.

[0017] FIG. 6A is a plot of detection frequency vs. comparator threshold for one example ion inlet frequency illustrating example detection frequency and comparator threshold profile pairs associated with various different charge signal amplitudes.

[0018] FIG. 6B is a plot of detection probability vs. charge signal amplitude illustrating example detection probability and charge signal amplitude profile pairs associated with different comparator threshold values.

[0019] FIG. 6C is a plot of detection frequency vs ion inlet frequency illustrating an example detection frequency and ion inlet frequency profile for a given comparator threshold and charge signal amplitude pair.

[0020] FIG. 6D is a plot of correction factor vs. ion inlet frequency illustrating an example correction factor and ion inlet frequency for a given comparator threshold and ion charge level pair.

[0021] FIG. 7 is a flowchart illustrating an embodiment of a process for selecting and modifying the comparator threshold illustrated in FIG. 3 for trigger trapping control of the ELIT based on detection of low-charge ions.

[0022] FIG. 8A is a simplified block diagram of an embodiment of an ion separation instrument including the ELIT illustrated in FIGS. 1 - 3 and operating as described herein, showing example ion processing instruments which may form part of the ion source upstream of the ELIT and/or which may be disposed downstream of the ELIT to further process ion(s) exiting the ELIT.

[0023] FIG. 8B is a simplified block diagram of another embodiment of an ion separation instrument including the ELIT illustrated in FIGS. 1 - 3 and operating as described herein, showing an example implementation which combines conventional ion processing instruments with any of the embodiments of the ion mass detection system illustrated and described herein.

DESCRIPTION OF THE ILLUSTRATIVE EMBODIMENTS

[0024] For the purposes of promoting an understanding of the principles of this disclosure, reference will now be made to a number of illustrative embodiments shown in the attached drawings and specific language will be used to describe the same.

[0025] This disclosure relates to an electrostatic linear ion trap (ELIT) and an apparatus and method for selecting and modifying a charge detection threshold during trigger trapping operation thereof to facilitate trapping in the ELIT of weakly-charge ions, i.e., ions with

low charge magnitudes. For purposes of this disclosure, the phrase "charge detection event" is defined as detection of a charge associated with an ion passing a single time through a charge detector of the ELIT, and the phrase "ion measurement event" is defined as a collection of charge detection events resulting from oscillation of an ion back and forth through the charge detector a selected number of times or for a selected time period.

[0026] Referring to FIG. 1, charge detection mass spectrometer (CDMS) 10 is shown including an embodiment of an electrostatic linear ion trap (ELIT) 14 with control and measurement components coupled thereto. In the illustrated embodiment, the CDMS 10 includes an ion source 12 operatively coupled to an inlet of the ELIT 14. As will be described further with respect to FIG. 7A, the ion source 12 illustratively includes any conventional device or apparatus for generating ions from a sample and may further include one or more devices and/or instruments for separating, collecting, filtering, fragmenting and/or normalizing or shifting charge states of ions according to one or more molecular characteristics. As one illustrative example, which should not be considered to be limiting in any way, the ion source 12 may include a conventional electrospray ionization source, a matrix-assisted laser desorption ionization (MALDI) source or the like, coupled to an inlet of a conventional mass spectrometer. The mass spectrometer may be of any conventional design including, for example, but not limited to a time-of-flight (TOF) mass spectrometer, a reflectron mass spectrometer, a Fourier transform ion cyclotron resonance (FTICR) mass spectrometer, a quadrupole mass spectrometer, a triple quadrupole mass spectrometer, a magnetic sector mass spectrometer, or the like. In any case, the ion outlet of the mass spectrometer is operatively coupled to an ion inlet of the ELIT 14. The sample from which the ions are generated may be any biological or other material.

[0027] In the illustrated embodiment, the ELIT 14 illustratively includes a charge detector CD surrounded by a ground chamber or cylinder GC and operatively coupled to opposing ion mirrors M1, M2 respectively positioned at opposite ends thereof. The ion mirror M1 is operatively positioned between the ion source 12 and one end of the charge detector CD, and ion mirror M2 is operatively positioned at the opposite end of the charge detector CD. Each ion mirror M1, M2 defines a respective ion mirror region R1, R2 therein. The regions R1, R2 of the ion mirrors M1, M2, the charge detector CD, and the spaces between the charge detector CD and the ion mirrors M1, M2 together define a longitudinal axis 22 centrally therethrough which illustratively represents an ideal ion travel path through the ELIT 14 and between the ion mirrors M1, M2 as will be described in greater detail below.

[0028] In the illustrated embodiment, voltage sources V1, V2 are electrically connected to the ion mirrors M1, M2 respectively. Each voltage source V1, V2 illustratively includes one

or more switchable DC voltage sources which may be controlled or programmed to selectively produce a number, N, programmable or controllable voltages, wherein N may be any positive integer. Illustrative examples of such voltages will be described below with respect to FIGS. 2A and 2B to establish one of two different operating modes of each of the ion mirrors M1, M2 as will be described in detail below. In any case, ions move within the ELIT 14 along the longitudinal axis 22 extending centrally through the charge detector CD and the ion mirrors M1, M2 under the influence of electric fields selectively established by the voltage sources V1, V2.

[0029] The voltage sources V1, V2 are illustratively shown electrically connected by a number, P, of signal paths to a conventional processor 16 including a memory 18 having instructions stored therein which, when executed by the processor 16, cause the processor 16 to control the voltage sources V1, V2 to produce desired DC output voltages for selectively establishing ion transmission and ion reflection electric fields, TEF, REF respectively, within the regions R1, R2 of the respective ion mirrors M1, M2. P may be any positive integer. In some alternate embodiments, either or both of the voltage sources V1, V2 may be programmable to selectively produce one or more constant output voltages. In other alternative embodiments, either or both of the voltage sources V1, V2 may be configured to produce one or more time-varying output voltages of any desired shape. It will be understood that more or fewer voltage sources may be electrically connected to the mirrors M1, M2 in alternate embodiments.

[0030] The charge detector CD is illustratively provided in the form of an electrically conductive cylinder which is electrically connected to a signal input of a charge sensitive preamplifier CP, and the signal output of the charge preamplifier CP is electrically connected to the processor 16. With an ion trapped within the ELIT 14 and oscillating back and forth between the ion mirrors M1, M2 as will be described in further detail below, the charge preamplifier CP is illustratively operable in a conventional manner to detect a charge (CH) induced on the charge detection cylinder CD as the ion passes therethrough between the ion mirrors M1, M2, to produce a charge detection signal (CHD) corresponding thereto and to supply the charge detection signal CHD to the processor 16. The processor 16 is, in turn, illustratively operable to receive and digitize the charge detection signal CHD produced by the charge preamplifier CP, and to store the digitized charge detection signal CHD in the memory 18.

[0031] The processor 16 is further illustratively coupled to one or more peripheral devices 20 (PD) for providing peripheral device signal input(s) (PDS) to the processor 16 and/or to which the processor 16 provides signal peripheral device signal output(s) (PDS). In some embodiments, the peripheral devices 20 include at least one of a conventional display

monitor, a printer and/or other output device, and in such embodiments the memory 18 has instructions stored therein which, when executed by the processor 16, cause the processor 16 to control one or more such output peripheral devices 20 to display and/or record analyses of stored, digitized charge detection signals. In some embodiments, a conventional ion detector 24, e.g., in the form of one or more microchannel plate detectors, is positioned adjacent to the ion exit aperture of the ion mirror M2, and at least one output of the ion detector 24 is electrically connected to the processor 16. The ion detector 24 is operable in a conventional manner to detect ions exiting the ion mirror M2 of the ELIT 14 and to provide corresponding ion detection signal MCP to the processor 16. As will be described in greater detail below, ion detection information provided by the detector 24 to the processor 16 may be used to facilitate adjustment one or more of the components and/or operating conditions of the ELIT 14 to ensure adequate detection of ions passing through the charge detection cylinder CD.

[0032] The voltage sources V1, V2 are illustratively controlled in a manner, as described in detail below, which selectively traps an ion entering the ELIT 14 and causes the trapped ion to oscillate back and forth between the ion mirrors M1, M2 such that it repeatedly passes through the charge detection cylinder CD. A plurality of charge and oscillation period values are measured at the charge detector CD, and the recorded results are processed to determine mass-to-charge ratio, charge and mass values of the ion trapped in the ELIT 14.

[0033] Referring now to FIGS. 2A and 2B, embodiments are shown of the ion mirrors M1, M2 respectively of the ELIT 14 depicted in FIG. 1. Illustratively, the ion mirrors M1, M2 are identical to one another in that each includes a cascaded arrangement of 4 spaced-apart, electrically conductive mirror electrodes. For each of the ion mirrors M1, M2, a first mirror electrode 30_1 has a thickness W1 and defines a passageway centrally therethrough of diameter P1. An endcap 32 is affixed or otherwise coupled to an outer surface of the first mirror electrode 30_1 and defines an aperture A1 centrally therethrough which serves as an ion entrance and/or exit to and/or from the corresponding ion mirror M1, M2 respectively. In the case of the ion mirror M1, the endcap 32 is coupled to, or is part of, an ion exit of the ion source 12 illustrated in FIG. 1. The aperture A1 for each endcap 32 illustratively has a diameter P2.

[0034] A second mirror electrode 30_2 of each ion mirror M1, M2 is spaced apart from the first mirror electrode 30_1 by a space having width W2. The second mirror electrode 30_2, like the mirror electrode 30_1, has thickness W1 and defines a passageway centrally therethrough of diameter P2. A third mirror electrode 30_3 of each ion mirror M1, M2 is likewise spaced apart from the second mirror electrode 30_2 by a space of width W2. The third mirror electrode 30_2 has thickness W1 and defines a passageway centrally therethrough of width P1.

[0035] A fourth mirror electrode 30_4 is spaced apart from the third mirror electrode 30_3 by a space of width W2. The fourth mirror electrode 30_4 illustratively has a thickness of W1 and is formed by a respective end of the ground cylinder, GC disposed about the charge detector CD. The fourth mirror electrode 30_4 defines an aperture A2 centrally therethrough which is illustratively conical in shape and increases linearly between the internal and external faces of the ground cylinder GC from a diameter P3 defined at the internal face of the ground cylinder GC to the diameter P1 at the external face of the ground cylinder GC (which is also the internal face of the respective ion mirror M1, M2).

[0036] The spaces defined between the mirror electrodes $30_1 – 30_4$ may be voids in some embodiments, i.e., vacuum gaps, and in other embodiments such spaces may be filled with one or more electrically non-conductive, e.g., dielectric, materials. The mirror electrodes $30_1 – 30_4$ and the endcaps 32 are axially aligned, i.e., collinear, such that a longitudinal axis 22 passes centrally through each aligned passageway and also centrally through the apertures A1, A2. In embodiments in which the spaces between the mirror electrodes 30_1 - 30_4 include one or more electrically non-conductive materials, such materials will likewise define respective passageways therethrough which are axially aligned, i.e., collinear, with the passageways defined through the mirror electrodes $30_1 – 30_4$ and which illustratively have diameters of P2 or greater. Illustratively, P1 > P3 > P2, although in other embodiments other relative diameter arrangements are possible.

[0037] A region R1 is defined between the apertures A1, A2 of the ion mirror M1, and another region R2 is likewise defined between the apertures A1, A2 of the ion mirror M2. The regions R1, R2 are illustratively identical to one another in shape and in volume.

[0038] As described above, the charge detector CD is illustratively provided in the form of an elongated, electrically conductive cylinder positioned and spaced apart between corresponding ones of the ion mirrors M1, M2 by a space of width W3. In one embodiment, W1 > W3 > W2, and P1 > P3 > P2, although in alternate embodiments other relative width arrangements are possible. In any case, the longitudinal axis 22 illustratively extends centrally through the passageway defined through the charge detection cylinder CD, such that the longitudinal axis 22 extends centrally through the combination of the passageways defined by the regions R1, R2 of the ion mirrors M1, M2 and the passageway defined through the charge detection cylinder CD. In operation, the ground cylinder GC is illustratively controlled to ground potential such that the fourth mirror electrode 30_4 of each ion mirror M1, M2 is at ground potential at all times. In some alternate embodiments, the fourth mirror electrode 30_4 of either or both of the ion mirrors M1, M2 may be set to any desired DC reference potential, or to a switchable DC or other time-varying voltage source.

[0039] In the embodiment illustrated in FIGS. 2A and 2B, the voltage sources V1, V2 are each configured to each produce four DC voltages D1 – D4, and to supply the voltages D1 – D4 to a respective one of the mirror electrodes 30_1 – 30_4 of the respective ion mirror M1, M2. In some embodiments in which one or more of the mirror electrodes 30_1 – 30_4 is to be held at ground potential at all times, the one or more such mirror electrodes 30_1 – 30_4 may alternatively be electrically connected to the ground reference of the respective voltage supply V1, V2 and the corresponding one or more voltage outputs D1 – D4 may be omitted. Alternatively or additionally, in embodiments in which any two or more of the mirror electrodes 30_1 – 30_4 are to be controlled to the same non-zero DC values, any such two or more mirror electrodes 30_1 – 30_4 may be electrically connected to a single one of the voltage outputs D1 – D4 and superfluous ones of the output voltages D1 – D4 may be omitted.

[0040] Each ion mirror M1, M2 is illustratively controllable and switchable, by selective application of the voltages D1 – D4, between an ion transmission mode (FIG. 2A) in which the voltages D1 – D4 produced by the respective voltage source V1, V2 establishes an ion transmission electric field (TEF) in the respective region R1, R2 thereof, and an ion reflection mode (FIG. 2B) in which the voltages D1 – D4 produced by the respect voltage source V1, V2 establishes an ion reflection electric field (REF) in the respective region R1, R2 thereof. As illustrated by example in FIG. 2A, once an ion from the ion source 12 flies into the region R1 of the ion mirror M1 through the inlet aperture A1 of the ion mirror M1, the ion is focused toward the longitudinal axis 22 of the ELIT 14 by an ion transmission electric field TEF established in the region R1 of the ion mirror M1 via selective control of the voltages D1 – D4 of V1. As a result of the focusing effect of the transmission electric field TEF in the region R1 of the ion mirror M1, the ion exiting the region R1 of the ion mirror M1 through the aperture A2 of the ground chamber GC attains a narrow trajectory 36 into and through the charge detection cylinder CD that is close to the longitudinal axis 22. An identical ion transmission electric field TEF may be selectively established within the region R2 of the ion mirror M2 via like control of the voltages D1 – D4 of the voltage source V2. In the ion transmission mode, an ion entering the region R2 from the charge detection cylinder CD via the aperture A2 of M2 is focused toward the longitudinal axis 22 by the ion transmission electric field TEF within the region R2 so that the ion exits the ion mirror M2 through the aperture A1 thereof.

[0041] As illustrated by example in FIG. 2B, an ion reflection electric field REF established in the region R2 of the ion mirror M2 via selective control of the voltages D1 – D4 of V2 acts to decelerate and stop an ion entering the ion region R2 from the charge detection cylinder CD via the ion inlet aperture A2 of M2, to accelerate the ion in the opposite direction back through the aperture A2 of M2 and into the end of the charge detection cylinder CD

adjacent to M2 as depicted by the ion trajectory 38, and to focus the ion toward the central, longitudinal axis 22 within the region R2 of the ion mirror M2 so as to maintain a narrow trajectory of the ion back through the charge detector CD toward the ion mirror M1. An identical ion reflection electric field REF may be selectively established within the region R1 of the ion mirror M1 via like control of the voltages D1 – D4 of the voltage source V1. In the ion reflection mode, an ion entering the region R1 from the charge detection cylinder CD via the aperture A2 of M1 is decelerated and stopped by the ion reflection electric field REF established within the region R1, then accelerated in the opposite direction back through the aperture A2 of M1 and into the end of the charge detection cylinder CD adjacent to M1, and focused toward the central, longitudinal axis 22 within the region R1 of the ion mirror M1 so as to maintain a narrow trajectory of the ion back through the charge detector CD and toward the ion mirror M2. An ion that traverses the length of the ELIT 14 and is reflected by the ion reflection electric field REF in the ion regions R1, R2 in a manner that enables the ion to continue traveling back and forth through the charge detection cylinder CD between the ion mirrors M1, M2 as just described is considered to be trapped within the ELIT 14.

[0042] Example sets of output voltages D1 – D4 produced by the voltage sources V1, V2 respectively to control a respective one of the ion mirrors M1, M2 to the ion transmission and reflection modes described above are shown in TABLE I below. It will be understood that the following values of D1 – D4 are provided only by way of example, and that other values of one or more of D1 – D4 may alternatively be used.

TABLE I

Ion Mirror Operating Mode	Output Voltages (volts DC)
Transmission	V1: D1 = 0, D2 = 95, D3 = 135, D4 = 0 V2: D1 = 0, D2 = 95, D3 = 135, D4 = 0
Reflection	V1: D1 = 190, D2 = 125, D3 = 135, D4 = 0 V2: D1 = 190, D2 = 125, D3 = 135, D4 = 0

[0043] While the ion mirrors M1, M2 and the charge detection cylinder CD are illustrated in FIGS. 1 – 2B as defining cylindrical passageways therethrough, it will be understood that in alternate embodiments either or both of the ion mirrors M1, M2 and/or the charge detection cylinder CD may define non-cylindrical passageways therethrough such that one or more of the passageway(s) through which the longitudinal axis 22 centrally passes represents a cross-sectional area and profile that is not circular. In still other embodiments, regardless of the shape of the cross-sectional profiles, the cross-sectional areas of the

passageway defined through the ion mirror M1 may be different from the passageway defined through the ion mirror M2.

[0044] Referring now to FIG. 3, an embodiment is shown of the processor 16 illustrated in FIG. 1. In the illustrated embodiment, the processor 16 includes a conventional amplifier circuit 40 having an input receiving the charge detection signal CHD produced by the charge preamplifier CP and an output electrically connected to an input of a conventional Analog-to-Digital (A/D) converter 42. An output of the A/D converter 42 is electrically connected to a first processor 50 (P1). The amplifier 40 is operable in a conventional manner to amplify the charge detection signal CHD produced by the charge preamplifier CP, and the A/D converter is, in turn, operable in a conventional manner to convert the amplified charge detection signal to a digital charge detection signal CDS. The processor 50 is, in the illustrated embodiment, operable to store the charge detection signals CDS for each charge detection event in an ion measurement event such that an ion measurement event record stored in the processing circuit 50 includes multiple charge detection event measurements.

[0045] The processor 16 illustrated in FIG. 3 further includes a conventional comparator 44 having a first input receiving the charge detection signal CHD produced by the charge preamplifier CP, a second input receiving a threshold voltage CTH produced by a threshold voltage generator (TG) 46 and an output electrically connected to the processor 50. In some embodiments, the processor 16 further includes a signal conditioning circuit 45 having an input receiving the charge detection signal CHD and an output electrically connected to the comparator 44 as shown by example in FIG. 3. In embodiments which do not include the signal conditioning circuit 45, the comparator 44 is operable in a conventional manner to produce a trigger signal TR at the output thereof which is dependent upon the magnitude of the charge detection signal CDH relative to the magnitude of the threshold voltage CTH. In one embodiment, for example, the comparator 44 is operable to produce an “inactive” trigger signal TR at or near a reference voltage, e.g., ground potential, as long as CHD is less than CTH, and is operable to produce an “active” TR signal at or near a supply voltage of the circuitry 40, 42, 44, 45, 46, 50 when CHD is at or exceeds CTH. In alternate embodiments, the comparator 44 may be operable to produce an “inactive” trigger signal TR at or near the supply voltage as long as CHD is less than CTH, and is operable to produce an “active” trigger signal TR at or near the reference potential when CHD is at or exceeds CTH. Those skilled in the art will recognize other differing trigger signal magnitudes and/or differing trigger signal polarities that may be used to establish the “inactive” and “active” states of the trigger signal TR so long as such differing trigger signal magnitudes and/or different trigger signal polarities are distinguishable by the processor 50, and it will be understood that any such other different

trigger signal magnitudes and/or differing trigger signal polarities are intended to fall within the scope of this disclosure. In any case, the comparator 44 may additionally be designed in a conventional manner to include a desired amount of hysteresis to prevent rapid switching of the output between the reference and supply voltages.

[0046] In some embodiments which include the signal conditioning circuit 45 briefly described above, such a signal conditioning circuit 45 may illustratively be provided in the form of a conventional band-pass filter circuit configured to pass signals within a suitable frequency range so as to pass legitimate charge detection event signals to the comparator 44 but to block higher frequency noise pulses from reaching the comparator 44, thereby reducing the likelihood of noise-triggered detection events. In other embodiments which include the signal conditioning circuit 45, such a signal conditioning circuit 45 may be provided in the form of a signal shaping amplifier configured to produce an edge-detected Gaussian-shaped output signal, i.e., an output signal shaped like a Gaussian function. Such a signal shaping amplifier will illustratively convert the rising edge of a charge detection signal CHD to a short Gaussian-shaped pulse and the falling edge of the charge detection signal CHD to a similar Gaussian-shaped pulse of opposite polarity. In this embodiment, the comparator 44 will produce an "active" trigger signal TR when either of the Gaussian-shaped signals exceeds a switching threshold voltage of the comparator 44.

[0047] In the illustrated embodiment, the processor 50 is operable, i.e., programmed, to control the threshold voltage generator 46 to produce the threshold voltage CTH. In one embodiment, the threshold voltage generator 46 is implemented in the form of a conventional controllable DC voltage source configured to be responsive to a digital threshold control signal THC, e.g., in the form of a single serial digital signal or multiple parallel digital signals, to produce an analog threshold voltage CTH having a polarity and a magnitude defined by the digital threshold control signal THC. In alternate embodiments, the threshold voltage generator 46 may be provided in the form of a conventional digital-to-analog (D/A) converter responsive to a serial or parallel digital threshold voltage TCH to produce an analog threshold voltage CTH having a magnitude, and in some embodiments a polarity, defined by the digital threshold control signals THC. In some such embodiments, the D/A converter may form part of the processor 50. Those skilled in the art will recognize other conventional circuits and techniques for selectively producing the threshold voltage CTH of desired magnitude and/or polarity, and it will be understood that any such other conventional circuits and/or techniques are intended to fall within the scope of this disclosure.

[0048] In addition to the foregoing functions performed by the processor 50, the processor 50 is further operable to receive and process the output signals MCP produced by

the ion detector 24, in embodiments which include the ion detector 24, and to control the voltage sources V1, V2 as described above with respect to FIGS. 2A, 2B to selectively establish ion transmission and reflection fields within the regions R1, R2 of the ion mirrors M1, M2 respectively. In one embodiment, the processor 50 is illustratively provided in the form of a field programmable gate array (FPGA) programmed as just described to collect and store charge detection signals CDS for charge detection events and for ion measurement events, to produce the threshold control signal(s) TCH from which the magnitude and/or polarity of the threshold voltage CTH is determined or derived, and to control the voltage sources V1, V2 based on the ion detection signals MCP and based on the charge detection signals CHD relative to the threshold voltage CTH as determined by monitoring the output signal TR produced by the comparator 44. In this embodiment, the memory 18 described with respect to FIG. 1 is integrated into, and forms part of, the programming of the FPGA. In alternate embodiments, the processor 50 may be provided in the form of one or more conventional microprocessors or controllers and one or more accompanying memory units having instructions stored therein which, when executed by the one or more microprocessors or controllers, cause the one or more microprocessors or controllers to operate as just described. In other alternate embodiments, the processing circuit 50 may be implemented purely in the form of one or more conventional hardware circuits designed to operate as described above, or as a combination of one or more such hardware circuits and at least one microprocessor or controller operable to execute instructions stored in memory to operate as described above.

[0049] In any case, the embodiment of the processor 16 depicted in FIG. 3 further illustratively includes a second processor 52 coupled to the first processor 50 and also to the one or more peripheral devices 20. In some embodiments, the processor 52 may include the one or more peripheral devices 20. In any case, the processor 52 is illustratively operable to process the ion measurement event information stored in and/or by the first processor 50 to determine ion charge, mass-to-charge and mass information. The processor 52 may be provided in the form of any conventional computer or computing device capable of processing the ion measurement event information, i.e., having sufficient computing power, to determine, display, store and conduct at least some amount of analysis of ion mass information. In one embodiment, the processor 52 may be provided in the form of a conventional personal computer (PC), although in other embodiments the processor 52 may be or include one or more computers or computing devices with greater or lesser computing power.

[0050] As briefly described above with respect to FIGS. 2A and 2B, the voltage sources V1, V2 are illustratively controlled by the processor 50 in a manner which selectively establishes ion transmission and ion reflection electric fields in the region R1 of the ion mirror

M1 and in the region R2 of the ion mirror M2 to guide ions introduced into the ELIT 14 from the ion source 12 through the ELIT 14, and to then cause a single ion to be selectively trapped within the ELIT 14 such that the trapped ion repeatedly passes through the charge detector CD as it oscillates back and forth between M1 and M2. Referring to FIGS. 4A – 4C, simplified diagrams of the ELIT 14 of FIG. 1 are shown depicting an example of such sequential control and operation of the ion mirrors M1, M2 of the ELIT 14. In the following example, the processor 50 will be described as controlling the operation of the voltage sources V1, V2 in accordance with its programming, although it will be understood that in alternate embodiments the operation of the voltage source V1 and/or the operation of the voltage source V1 may be controlled, at least in part, by the processor 52 in accordance with its programming.

[0051] As illustrated in FIG. 4A, the ELIT control sequence begins with the processor 50 controlling the voltage source V1 to control the ion mirror M1 to the ion transmission mode of operation (T) by establishing an ion transmission field within the region R1 of the ion mirror M1, and also controlling the voltage source V2 to control the ion mirror M2 to the ion transmission mode of operation (T) by likewise establishing an ion transmission field within the region R2 of the ion mirror M2. As a result, ions generated by the ion source 12 pass into the ion mirror M1 and are focused by the ion transmission electric field TEF established in the region R1 toward the longitudinal axis 22 as they pass into the charge detection cylinder CD. The ions then pass through the charge detection cylinder CD and into the ion mirror M2 where the ion transmission field established within the region R2 of M2 focusses the ions toward the longitudinal axis 22 such that the ions pass through the exit aperture A1 of M2 as illustrated by the ion trajectory 60 illustrated in FIG. 4A. In the state illustrated in FIG. 4A, M1 and M2 are open and the ELIT 14 is fully open. In some embodiments, ion detection information produced by the ion detector 24 is used to adjust/modify one or more operating parameters or conditions of the ELIT 14 to ensure that one or more ions generated by the ion source 12 successfully enter and pass through the ELIT 14 as just described.

[0052] Referring now to FIG. 4B, after both of the ion mirrors M1, M2 have been operating in ion transmission operating mode for a selected time period and/or until successful ion transmission therethrough has been achieved, e.g., by monitoring ion detection signals produced by the ion detector 24 and adjusting/modifying one or more operating parameters or conditions of the ELIT 14 as needed, the processor 50 is illustratively operable to control the voltage source V2 to control the ion mirror M2 to the ion reflection mode (R) of operation by establishing an ion reflection field within the region R2 of the ion mirror M2, while maintaining the ion mirror M1 in the ion transmission mode (T) of operation as shown. As a result, an ion generated by the ion source 12 entering the ion mirror M1 is focused by the ion transmission

field established in the region R1 of the ion mirror M1 toward the longitudinal axis 22 such that the ion passes through the ion mirror M1 and into the charge detection cylinder CD as just described with respect to FIG. 4A. The ion then passes through the charge detection cylinder CD and into the ion mirror M2 where the ion reflection field established within the region R2 of M2 reflects, i.e., accelerates, the ion to cause it to travel in the opposite direction and back into the charge detection cylinder CD, as illustrated by the ion trajectory 62 in FIG. 4B. In the state illustrated in FIG. 4B, M1 is open, M2 is closed and the ELIT 14 is thus open at one end (M1) and closed at the other (M2).

[0053] Referring now to FIG. 4C, after the ion reflection electric field has been established in the region R2 of the ion mirror M2, the processor 50 is operable to control the voltage source V1 to control the ion mirror M1 to the ion reflection mode (R) of operation by establishing an ion reflection field within the region R1 of the ion mirror M1, while maintaining the ion mirror M2 in the ion reflection mode (R) of operation in order to trap the ion within the ELIT 14. In the state illustrated in FIG. 4C, M1 and M2 are closed, and the ELIT 14 is likewise closed. In some embodiments, the processor 50 is illustratively operable, i.e., programmed, to control the ELIT 14 in a "random trapping mode" in which the processor 50 is operable to control the ion mirror M1 to the reflection mode (R) of operation after the ELIT has been operating in the state illustrated in FIG. 4B, i.e., with M1 in ion transmission mode and M2 in ion reflection mode, for a selected time period. Until the selected time period has elapsed, the ELIT 14 is controlled to operate in the state illustrated in FIG. 4B.

[0054] The probability of trapping at least one ion in the ELIT 14 is relatively low using the random trapping mode of operation due to the timed control of M1 to ion reflection mode of operation without any confirmation that at least one ion is trapped within the ELIT 14. The number of trapped ions within the ELIT 14 during the random trapping mode of operation follows a Poisson distribution, and it is generally understood that random or "continuous" trapping is relatively inefficient as less than 0.1% of the ions are trapped.

[0055] In other embodiments particularly relevant to this disclosure, the processor 50 is operable, i.e., programmed, to control the ELIT 14 in a "trigger trapping mode" which illustratively carries a substantially greater probability of trapping a single ion therein. In a first version of the trigger trapping mode, the processor 50 is operable to monitor the trigger signal TR produced by the comparator 44 and to control the voltage source V1 to control the ion mirror M1 to the reflection mode (R) of operation to trap an ion within the ELIT 14 if/when the trigger signal TR changes the "inactive" to the "active" state thereof. In some embodiments, the processor 50 may be operable to control the voltage source V1 to control the ion mirror M1 to the reflection mode (R) immediately upon detection of the change of state of the trigger

signal TR, and in other embodiments the processor 50 may be operable to control the voltage source V1 to control the ion mirror M1 to the reflection mode (R) upon expiration of a predefined delay period following detection of the change of state of the trigger signal TR. In any case, the change of state of the trigger signal TR from the "inactive" state to the "active" state thereof results from the charge detection signal CHD produced by the charge preamplifier CP reaching or exceeding the threshold voltage CTH, and therefore corresponds to detection of a charge induced on the charge detection cylinder CD by an ion moving therein. With an ion thus moving within the charge detection cylinder CD, control by the processor 50 of the voltage source V1 to control the ion mirror M1 to the reflection mode (R) of operation results in a substantially improved probability, relative to the random trapping mode, of trapping the ion within the ELIT 14. Thus, when an ion has entered the ELIT 14 via the ion mirror M1 and is detected as either passing the first time through the charge detection cylinder CD toward the ion mirror M2 or as passing back through the charge detection cylinder CD after having been reflected by the ion reflection field established within the region R2 of the ion mirror M2 as illustrated in FIG. 4B, the ion mirror M1 is controlled to the reflection mode (R) as illustrated in FIG. 4C to trap the ion within the ELIT 14.

[0056] In a second version of the trigger trapping mode, the process or step illustrated in FIG. 4B is omitted or bypassed, and with the ELIT 14 operating as illustrated in FIG. 4A the processor 50 is operable to monitor the trigger signal TR produced by the comparator 44 and to control both voltage sources V1, V2 to control the respective ion mirrors M1, M2 to the reflection mode (R) of operation to trap an ion within the ELIT 14 if/when the trigger signal TR changes the "inactive" to the "active" state thereof. Thus, when an ion has entered the ELIT 14 via the ion mirror M1 and is detected as passing the first time through the charge detection cylinder CD toward the ion mirror M2 as illustrated in FIG. 4A, the ion mirrors M1 and M2 are both controlled to the reflection mode (R) as illustrated in FIG. 4C to trap the ion within the ELIT 14. In conventional trigger trapping mode with optimized ion inlet signal intensity, e.g., as depicted in FIG. 5A and described below, it has been shown that trapping efficiency, defined here as a ratio of single-ion trapping events and all acquired trapping events, can approach 90% as compared to 37% with random trapping.

[0057] In any case, with both of the ion mirrors M1, M2 controlled to the ion reflection operating mode (R) to trap an ion within the ELIT 14, the ion is caused by the opposing ion reflection fields established in the regions R1 and R2 of the ion mirrors M1 and M2 respectively to oscillate back and forth between the ion mirrors M1 and M2, each time passing through the charge detection cylinder CD as illustrated by the ion trajectory 64 depicted in FIG. 4C. In one embodiment, the processor 50 is operable to maintain the operating state illustrated in FIG. 4C

until the ion passes through the charge detection cylinder CD a selected number of times. In an alternate embodiment, the processor 50 is operable to maintain the operating state illustrated in FIG. 4C for a selected time period after controlling M1 (and M2 in some embodiments) to the ion reflection mode (R) of operation. When the ion has passed through the charge detection cylinder CD a selected number of times or has oscillated back-and-forth between the ion mirrors M1, M2 for a selected period of time, the sequence illustrated in FIGS. 4A – 4C returns to that illustrated in FIG. 4A where the processor 50 is operable, i.e., programmed, to control the voltage sources V1, V2 to control the ion mirrors M1, M2 respectively to the ion transmission mode (T) of operation by establishing an ion transmission fields within the regions R1, R2 of the ion mirrors M1, M2 respectively. The process then repeats for as many times as desired.

[0058] With an ion oscillating back and forth between the ion mirrors M1, M2 as illustrated in FIG. 4C, a charge is induced on the charge detector CD of the ELIT 14 each time the ion passes therethrough. Each such induced charge is detected by the charge preamplifier CP, and the corresponding charge detection signal (CHD) produced by the charge preamplifier CP is amplified by the amplifier circuit 40 and digitized by the A/D converter 42, and the magnitude and timing of the digitized charge detection signal CDS is recorded, i.e., stored, by the processor 50 as a charge detection event. Each recorded charge detection event record thus illustratively includes an ion charge value, corresponding to a magnitude of the detected charge, and an oscillation period value, corresponding to the elapsed time between charge detection events. The collection of charge detection events resulting from oscillation of an ion back and forth through the charge detector CD a selected number of times or for a selected time period make up an ion measurement event as this term is defined herein (also referred to as a trapping event).

[0059] Ion measurement event data, i.e., charge detection events making up an ion measurement event, is illustratively processed by the processor 52 to determine charge, mass-to-charge ratio and mass values of the ion. In one embodiment, the ion measurement event data is processed by computing, with the processor 16, a Fourier Transform of the recorded collection of charge detection events. The processor 16 is illustratively operable to compute such a Fourier Transform using any conventional digital Fourier Transform (DFT) technique such as for example, but not limited to, a conventional Fast Fourier Transform (FFT) algorithm. In any case, the processor 16 is then illustratively operable to compute an ion mass-to-charge ratio value (m/z), an ion charge value (z) and ion mass values (m), each as a function of the computed Fourier Transform. The processor 16 is illustratively operable to store the computed

results in the memory 18 and/or to control one or more of the peripheral devices 20 to display the results for observation and/or further analysis.

[0060] It is generally understood that the mass-to-charge ratio (m/z) of an ion oscillating back and forth through the charge detector CD of an ELIT between opposing ion mirrors M1, M2 thereof is inversely proportional to the square of the fundamental frequency ff of the oscillating ion according to the equation:

[0061] $m/z = C/ff^2$,

[0062] where C is a constant that is a function of the ion energy and also a function of the dimensions of the respective ELIT, and the fundamental frequency ff is determined directly from the computed Fourier Transform. The value of the ion charge, z, is proportional to the magnitude FTMAG of the fundamental frequency ff, taking into account the number of ion oscillation cycles. Ion mass, m, is then calculated as a product of m/z and z. In some cases, the magnitude(s) of one or more of the harmonic frequencies of the FFT may be added to the magnitude of the fundamental frequency for purposes of determining the ion charge, z. The processor 16 is thus operable to compute $m/z = C/ff^2$, $z = F(FTMAG)$ and $m = (m/z)(z)$. Multiple, e.g., hundreds or thousands or more, ion trapping events are typically carried out for any particular sample from which the ions are generated by the ion source 12, and ion mass-to-charge, ion charge and ion mass values are determined/computed for each such ion trapping event. The ion mass-to-charge, ion charge and ion mass values for such multiple ion trapping events are, in turn, combined to form spectral information relating to the sample. Such spectral information may illustratively take different forms, examples of which include, but are not limited to, ion count vs. mass-to-charge ratio, ion charge vs. ion mass (e.g., in the form of an ion charge/mass scatter plot), ion count vs. ion mass, ion count vs. ion charge, or the like.

[0063] With no charge induced on the charge detector CD by a charged particle passing therethrough, the charge detection cylinder CD illustratively operates at or around a reference charge level CH_{REF}. As the charge detection cylinder CD is not powered or grounded, the reference charge level CH_{REF} is typically tens of charges (i.e., elementary charges “e”) or less, although in some applications the reference charge level CH_{REF} may be more than tens of charges. The reference charge level CH_{REF} on the charge detection cylinder CD is subject to one or more potentially significant sources of charge noise which may introduce uncertainty in charge detection events as a result of uncertainty in the reference charge level at any point in time. For example, such noise, e.g., in the form of root-mean-square deviation (RMSD) noise, may add at least a factor of 10 or so to the average CH_{REF} level, and even with conventional noise reduction efforts employed it is difficult to reduce the

RMSD noise to less than 100 or so charges. Because of this, the threshold voltage CTH for purposes of trigger trapping, as described above with respect to FIGS. 4B and 4C, is typically set sufficiently above the reference charge level CH_{REF} to avoid false triggering of the comparator 44 by charge noise. Referring to FIG. 5A, for example, a plot is shown of the charge detection signal CHD produced by the charge preamplifier CP vs. time in which an example charge noise waveform 70 is shown superimposed on the reference charge level CH_{REF}. One source of such charge noise 70 is the input of the charge sensitive preamplifier CP. Capacitance of the charge detector CD also contributes, as does spurious noise caused by external events and extraneous charges induced on the charge detection cylinder resulting from switching of either or both of the ion mirrors M1, M2 between ion transmission and ion reflection modes of operation.

[0064] An example trigger trapping event 72 is also illustrated in FIG. 5A which occurs between times t_1 and t_2. In the illustrated example, at least one ion having a relatively strong charge is detected as passing through the charge detection cylinder such that the charge detection signal CHD produced by the charge preamplifier is substantially greater than the combination of the charge noise 70 and the reference charge level CH_{REF} as shown. In this example, the threshold voltage CTH applied by the threshold voltage generator 46 to the comparator 44 is well-above the combination of the charge noise 70 and the reference charge level CH_{REF} so as not to incur false activations of the trigger signal TR ("false trigger events") by charge noise peaks riding on the reference charge level CH_{REF}, and is also well below the magnitude of the charge detection signal CHD during the trigger trapping event 72. In one embodiment, the threshold voltage CTH is illustratively set at a post-preamplifier level that is equivalent to a charge level CH on the charge detection cylinder CD of approximately five times the average combination of the charge noise 70 and the reference charge level CH_{REF} e.g., at least 500 charges or so, although in other embodiments the threshold voltage CTH may be greater or less than this example value.

[0065] In the description that follows, the gain of the preamplifier CP illustrated in FIG. 1 and described above will be assumed to be 1.0 to simplify the description of the threshold voltage CTH relative to the charge level CH on the charge detection cylinder CD. If the gain of the preamplifier CP is 1.0, then the charge detection signal CHD = CH and the threshold voltage CTH will thus be compared by the comparator 44 directly with the charge level CH existing on the charge detection cylinder CD at any point in time. It will be understood, however, that a preamplifier gain of 1.0 is assumed only to simplify the following discussion, and that in practice the gain of the preamplifier may be greater than 1.0. Control of the actual

threshold voltage CTH implemented in any particular application of the CDMS system 10 will therefore generally take into account the gain of the charge preamplifier CP.

[0066] Such charge noise 70, from any source, is undesirable as it necessitates setting a comparator threshold voltage CTH artificially high to avoid false trigger events as just described. However, doing so leaves an undesirably large range of magnitudes of the charge detection signal CHD below CTH which will not cause the comparator 44 to activate the trigger signal TR, but which could have been detectable if not for the high level of charge noise 70. As a result, neither conventional version of trigger trapping described above will can be effectively performed with weakly-charged ions, i.e., ions having charge magnitudes resulting in CHD < CTH.

[0067] However, many weakly-charged ions can be detected with specific control of the threshold voltage CTH. For example, as will be shown below, a probabilistic relationship exists between the magnitude of the threshold voltage CTH and corresponding detectable combinations of the charge detection signal CHD resulting from weakly-charged, i.e., low-charge, ions and the charge noise. Thus, as illustrated by example in FIG. 5B, although the charge noise 74 generally remains below the illustrated threshold voltage CTH the combination of the charge noise 74 and a low-charge ion detection event 76 on top of the charge noise 74 between times t_5 and t_6 rises above CTH, thereby resulting in an active trigger signal TR. The combination of charge noise 74 on the charge detection cylinder CD and a low charge induced on the charge detection cylinder CD by a weakly-charged ion passing therethrough is thus detectable through controlled selection of the threshold voltage CTH. It is possible, however, that peaks in the charge noise 74 alone may exceed CTH and thereby result in an active trigger signal TR which triggers a trapping event by the ELIT 14, as illustrated by the noise peak 78 between times t_3 and t_4 in FIG. 5B. Any such noise-based trigger will correspondingly result in an empty trapping event, i.e., one in which no ion is trapped in the ELIT 14. Optimization of the magnitude of the threshold voltage CTH, as will be described below, accordingly requires balancing the conflicting goals of lowering the magnitude of the threshold voltage CTH sufficiently to allow weakly-charged ions to trigger a trapping event while also maintaining the magnitude of the threshold voltage CTH sufficiently high to minimize empty trapping events.

[0068] The following analysis illustratively assumes a Gaussian noise spectrum with root-mean-square (RMS) noise charges on the charge detection cylinder CD, and assuming a 50% duty cycle of the ELIT 14, corresponding to a ratio of time spent by an ion in the charge detection cylinder CD of the ELIT 14 and total time spent traversing the first and second ion mirrors M1, M2 and the charge detection cylinder CD during one complete oscillation cycle of a

trapping event. It will be understood that the while the numerical values of the results of the following analysis may vary with different duty cycles, the remainder of the analysis will continue to hold true.

[0069] In trigger trapping operation of the ELIT 14 as described above with respect to FIGS. 4A – 4C, it can be shown that the detection frequency, defined here as the number of ions per second detectable by the charge detection cylinder CD of the ELIT 14, is a function of both the comparator threshold CTH and the magnitude of the charge of such ions passing through the charge detection cylinder CD ("charge signal amplitude"), i.e., as induced by the charge on the charge detection cylinder CD and detectable by charge preamplifier with a gain of 1.0, which is assigned here for convenience such that the magnitude of the charge detection signal CHD produced by the charge preamplifier CP and compared by the comparator 44 directly with the threshold voltage CTH will be equal to that of the charge, as briefly described above. Referring to FIG. 6A, for example, a plot of detection frequency vs. comparator threshold CTH (in units of charges) is shown illustrating example detection frequency and comparator threshold profile pairs associated with different respective ion charge levels, i.e., charge signal amplitudes.

[0070] The profile 80 depicted in FIG. 6A illustratively represents the detection frequency for ions randomly trapped by noise. As illustrated in FIG. 6A, the detection frequency of noise 80 decreases below approximately CTH = 170 e because the time interval between noise trigger events below CTH = 170 e becomes too small for ions to be able to enter the ELIT 14. Above CTH = 170 e, the detection frequency of noise 80 flattens because the trapping time is fixed with a maximum of t^{-1} trapping events per second. Above approximately CTH = 270 e, the detection frequency of noise 80 decreases because, in this range, the occurrences of noise exceeding CTH will naturally decrease with increasing CTH magnitude. As FIG. 6A also illustrates, the maximum detection efficiency achieved with noise trigger trapping is slightly less than 0.001, which is the same maximum detection efficiency achievable with random or continuous trigger trapping as described above.

[0071] The remaining profiles 82 – 92 depicted in FIG. 6A illustrate detection frequency profiles for noise plus charge signal trigger trapping with different charge signal amplitudes ranging from 50 to 300 e. For example, the profile 82 corresponds to an ion charge level or charge signal amplitude of 50 e, the profile 84 corresponds to an ion charge level or charge signal amplitude of 100 e, the profile 86 corresponds to an ion charge level or charge signal amplitude of 150 e, the profile 88 corresponds to an ion charge level or charge signal amplitude of 200 e, the profile 90 corresponds to an ion charge level or charge signal amplitude of 250 e and the profile 92 corresponds to an ion charge level or charge signal

amplitude of 300 e. In each case, the profiles 82 – 92 exhibit a single maximum or peak. This maximum or peak illustratively results from the two competing goals describe above. As just described with respect to noise trigger trapping, for example, increasing comparator threshold values CTH above that at which the respective detection frequency peak occurs results in a corresponding decrease in the number of occurrences of the noise + charge signal amplitude exceeding CTH. On the other hand, as CTH decreases below that at which the respective detection frequency peak occurs, more trapping events are triggered by noise alone and the time available for triggered trapping likewise decreases. The optimum comparator threshold magnitude CTH for each such charge signal amplitude thus occurs at the respective detection frequency peak, thereby maximizing the detection efficiency for ions having the corresponding charge signal amplitude.

[0072] As further illustrated in FIG. 6A, the optimum comparator threshold magnitude CTH decreases with decreasing charge signal amplitude. In the illustrated example, the optimum comparator threshold magnitude T1 for a charge signal amplitude of 50 e is approximately 260 e, the optimum comparator threshold magnitude T2 for a charge signal amplitude of 100 e is approximately 280 e, the optimum comparator threshold magnitude T3 for a charge signal amplitude of 150 e is approximately 300 e, the optimum comparator threshold magnitude T4 for a charge signal amplitude of 200 e is approximately 320 e, etc. Although not shown in FIG. 6A, the example detection frequency profiles 80 – 92 are defined for only one particular ion inlet frequency, in this case 1 Hz. It should be noted that even with a charge amplitude as low as 50 e, selection of the corresponding optimum comparator threshold CTH of approximately 270 e results in a 10-fold increase in detection probability as compared with random or continuous trapping.

[0073] For purposes of this description, ion inlet frequency is defined as the number of ions in the flow or beam of ions supplied by the ion source 12 to the ELIT 14 (via the ion inlet aperture A1 of the ion mirror M1 as illustrated by example in FIG. 4A) which pass by a fixed point per second. In any case, different ion inlet frequencies will produce different sets of detection frequency profiles albeit of the same general shape and following the same relationships illustrated in FIG. 6A. Generally, increasing ion inlet frequencies will result in corresponding increases in each of the respective optimum comparator threshold magnitudes. As such, an optimum comparator threshold magnitude value, i.e., at which the respective peak detection frequency occurs, is a function of the charge signal amplitude and a function of the ion inlet frequency.

[0074] As further still illustrated in FIG. 6A, the maximum achievable detection frequency also decreases with decreasing charge signal amplitude. This feature is also

illustrated in FIG. 6B which depicts a plot of detection probability vs. charge signal amplitude for a fixed ion inlet frequency, here again 1 Hz, illustrating example detection probability and charge signal amplitude profiles associated with different comparator threshold values. In the illustrated plot, for example, the profile 100 represents the detection probability vs. charge signal amplitude for a comparator threshold value of 260 e, the profile 102 represents the detection probability vs. charge signal amplitude for a comparator threshold value of 280 e, the profile 104 represents the detection probability vs. charge signal amplitude for a comparator threshold value of 300 e and the profile 106 represents the detection probability vs. charge signal amplitude for a comparator threshold value of 320 e. As with the plot illustrated in FIG. 6A, different ion inlet frequencies will produce different sets of detection probability vs charge signal amplitude profiles of the same general shape and following the same relationships illustrated in FIG. 6B. As such, the detection probability is a function of the charge signal amplitude, of the comparator threshold magnitude and of the ion inlet frequency.

[0075] As also illustrated in FIG. 6A and described above, the plot of FIG. 6B demonstrates in a different context that the choice of comparator threshold CTH depends on the charge signal amplitude. Thus, as the charge signal amplitude decreases, the magnitude of the comparator threshold CTH should likewise be controlled to decrease to an optimum value for the charge signal amplitude as illustrated in both FIGS. 6A and 6B. As illustrated most clearly in FIG. 6B, however, doing so will also reduce the detection probability for higher amplitude charge signals since the detection efficiency is reduced by a higher noise triggering rate. FIG. 6B further illustrates that below a certain charge signal amplitude (different for each comparator threshold magnitude) each detection probability decreases, and above the respective certain charge signal amplitudes the magnitudes of the detection probabilities are proportional to the magnitudes of the comparator thresholds. Based on FIG. 6B, it is apparent that when controlling the magnitude of the comparator threshold CTH as illustrated in FIG. 6A to trigger on low-charge signal amplitudes, the intensities of the measured ion spectrum should be corrected using the illustrated decreasing detection probabilities with decreasing comparator threshold magnitudes in order to reflect the relative abundances of the ions supplied by the ion source 12 to the ELIT 14. In this regard, a correction factor arrangement will be described below with respect to FIGS. 6C and 6D.

[0076] Referring now to FIG. 6C, a plot is shown of detection frequency vs. ion inlet frequency illustrating an example detection frequency and ion inlet frequency profile 108 associated with an example pair of charge signal amplitude and optimum comparator threshold magnitude, here, 150 e and 300 e respectively (e.g., corresponding to the intersection of the profile 86 and T3 illustrated in FIG. 6A). It will be understood that different pairs of charge

signal amplitude and optimum comparator threshold magnitude will produce different detection frequency vs ion inlet frequency profiles, albeit generally of the same shape. In any case, the profile 108 illustrates that as the ion frequency increases so too does the detection frequency. Illustratively, the profile 108 is non-linear because only a certain number of ions can be detected in the available time.

[0077] Rearrangement of the above-described relationships in the form of detection probability vs. ion inlet frequency illustratively produces a profile similar to that illustrated in FIG. 6C but mirrored about a horizontal axis extending approximately through the midpoint of the profile 108, thereby demonstrating a corresponding non-linear decrease in the detection probability with increasing ion inlet frequency further evidencing the need to account for the attendant decrease in detection efficiency so that the distribution of ion masses in the spectrum reflects the distribution in the flow of ions supplied to the ELIT 14 by the ion source 12. In this regard, FIG. 6D depicts a plot of a correction factor (1/detection probability) vs. detection frequency illustrating an example correction factor and detection frequency profile 110 associated with an example pair of charge signal amplitude and optimum comparator threshold magnitude, again, 150 e and 300 e respectively.

[0078] It will be understood that different pairs of charge signal amplitude and optimum comparator threshold magnitude will produce different correction factor vs ion detection frequency profiles, albeit generally of the same shape. In any case, the intensities of the measured ion spectrum will be multiplied by appropriate correction factors so that the intensities in the measured data reflect the relative abundances of the ions in the flow of ions supplied to the ELIT 14 by the ion source 12. Moreover, it is desirable to limit the detection frequency so that the applicable correction factor does not lie on the rapidly rising portion of the profile 110, e.g., greater than about 4.5 Hz). Correction factors in this range are large and strongly dependent upon detection frequency such that small errors in the detection frequency will lead to large errors in the correction factor.

[0079] Referring now to FIG. 7, a flowchart is shown illustrating an embodiment of a process 150 for selecting and modifying the comparator threshold CTH for trigger trapping control of the ELIT 14 triggered by low-charge ions. The process 150 illustratively embodies one example implementation of the concepts illustrated in FIGS. 5B – 6D, and is illustratively provided, at least in part, in the form of instructions stored in the memory 18 of the processor 16 which, when executed by the processor 50 and/or 52, cause the processor 50 and/or 52 to execute the operations described below with respect to FIG. 7. In this regard, the process 150 will be described below as being executed by the processor 50, although it will be understood that the process 150 may alternatively be executed, in whole or in part, by the processor 52 or

by one or more external processors in communication with the processor 50 and/or the processor 52.

[0080] In some embodiments of the process 150, the value(s) of the charge signal amplitude for triggering the ELIT 14 to trap the corresponding ion therein may be manually selected by a user of the CDMS system 10. In some such embodiments, the processor 50 and/or the processor 52 may be programmed to execute a control graphic user interface (GUI) process in which the processor 50 and/or 52 is/are operable to control at least one display monitor included in the peripheral devices 20 to display a corresponding control GUI including one or more selectable GUI elements for entering one or more charge signal amplitude values. In alternate embodiments, the processor 16/50 may be programmed to select the value(s) of the charge signal amplitude, e.g., singly and/or by executing a step-wise sweep of a range of charge signal amplitudes and executing the process 150 at each incremental charge signal amplitude value. Other conventional apparatuses, devices and/or techniques for selecting one or more charge signal amplitude values will occur to those skilled in the art, and it will be understood that any such other conventional apparatuses, devices and/or techniques are intended to fall within the scope of this disclosure.

[0081] The process 150 begins at step 152 where, prior to controlling the ELIT in a trigger trapping mode as just, described, the processor 50 is operable to store a number of maps in the memory 18 corresponding to relationships illustrated in some of the FIGS. 6A – 6D. In some embodiments, the processor 50 is operable to create one or more such maps and to store the one or more created maps in the memory 18. Alternatively or additionally, one or all of the maps may be created using a different processor and/or system, and transferred to the memory 18 of the processor 50 and/or the processor 52 in a conventional manner. In any case, the processor 50 is illustratively operable at step 152 to create and/or store a set of comparator threshold maps ("CTH maps") in the memory 18 each including multiple pairs of optimum comparator threshold values and corresponding charge signal amplitudes for a different ion inlet frequency to capture at least some of the relationships described above with respect to FIG. 6A. Using FIG. 6A as a non-limiting example, if the charge signal amplitudes for the profiles 82, 84, 86 and 88 are CHA1, CHA2, CHA3 and CHA4 respectively, one example set of CTH maps may include the pairs T1/CHA1, T2/CHA2, T3/CHA3 and T4/CHA4 for each of three different ion inlet frequencies F1 = 1 Hz, F2 = 2 Hz and F3 = 3 Hz. It will be understood that more or fewer such CTH maps may alternatively be created and/or stored for more or fewer ion inlet frequency values, and/or that any such number of CTH maps may include more or fewer optimum comparator threshold value and charge signal amplitude pairs. In any case, the set of CTH maps may illustratively be stored in the memory 18 in any

convenient form, examples of which may include, but are not limited to, one or more arrays, one or more lists (linked or otherwise), one or more tables (lookup tables or otherwise), one or more spreadsheets, one or more charts, one or more plots, one or more graphs, one or more relational databases or data structures, or the like.

[0082] The processor 50 is further illustratively operable at step 152 to create and/or store a set of detection frequency maps ("DF maps") in the memory 18 each including multiple detection frequency values mapped to corresponding ion inlet frequency values for a different pair of optimized comparator threshold and charge signal amplitude values to capture multiple optimized comparator threshold/charge signal amplitude value instances of the relationship described above with respect to FIG. 6C. Using FIG. 6C as a non-limiting example, one example set of DF maps may include a plurality of pairs of ion frequency values and corresponding detection frequency values for each of the four pairs T1/CHA1, T2/CHA2, T3/CHA3 and T4/CHA4 of optimized comparator threshold/charge signal amplitude values. It will be understood that more or fewer such DF maps may alternatively be created and/or stored for more or fewer pairs of optimized comparator threshold/charge signal amplitude values, and/or that any such number of DF maps may include more or fewer pairs of ion frequency values and corresponding detection frequency values. In any case, the set of DF maps may illustratively be stored in the memory 18 in any convenient form as just described with respect to the set of CTH maps.

[0083] The processor 50 is further illustratively operable at step 152 to create and/or store a set of correction factor maps ("CF maps") in the memory 18 each including multiple detection frequency values mapped to corresponding correction factor values for a different pair of optimized comparator threshold and charge signal amplitude values to capture multiple optimized comparator threshold/charge signal amplitude value instances of the relationship described above with respect to FIG. 6D. Using FIG. 6D as a non-limiting example, one example set of CF maps may include a plurality of pairs of correction factor values and corresponding detection frequency values for each of the four pairs T1/CHA1, T2/CHA2, T3/CHA3 and T4/CHA4 of optimized comparator threshold/charge signal amplitude values. It will be understood that more or fewer such CF maps may alternatively be created and/or stored for more or fewer pairs of optimized comparator threshold/charge signal amplitude values, and/or that any such number of CF maps may include more or fewer pairs of correction factor values and corresponding detection frequency values. In any case, the set of CF maps may illustratively be stored in the memory 18 in any convenient form as just described with respect to the set of CTH maps.

[0084] Those skilled in the art will appreciate that in some applications the information in the set of DF maps may be combined with the set of CF maps to form a single set of maps including multiple ion inlet frequency values mapped to corresponding correction factor values for a different pair of optimized comparator threshold and charge signal amplitude values to capture in one set of maps multiple optimized comparator threshold/charge signal amplitude value instances of the relationships described above with respect to FIGS. 6B – 6D. It will also be understood that in alternate embodiments, the one or more of the variables CTH, DF and CF may be computed based directly on other measured and/or selected parameters. In such embodiments, one or more corresponding sets of maps for CTH, DF and CF need not be created at step 152. In the extreme case where CTH, DF and CF are all computed based directly on other measured and/or selected parameters, step 152 may be omitted.

[0085] Following step 152, the process 150 advances to step 154 where the processor 50 is operable to control V1 and V2 to open M1 and M2 (and thus open the ELIT 14) so that ions generated by the ion source 12 pass into and through the ELIT 14 as illustrated by example in FIG. 4A. Thereafter at step 156, the processor 50 is operable to measure the ion inlet frequency IF. As the ion beam or trajectory or flow is, at the time of execution of step 156, passing from the ion source 12 directly through the charge detection cylinder CD, the processor 50 is illustratively operable in one embodiment to measure the ion inlet frequency IF by processing the charge detection signal CDS (see, e.g., FIG. 3) to determine timing information relating to times between occurrences of charges CH induced on the charge detector CD by ions passing therethrough. In other embodiments, the ion inlet frequency may be alternatively or additionally measured by one or more conventional sensors suitably positioned within the ion source 12 and/or between the ion source 12 and the ELIT 14. In still other embodiments, the ion inlet frequency may be alternatively or additionally measured or otherwise determined by an ion separation instrument, e.g., a mass analyzer or mass spectrometer, positioned in the ion source 12 between an ion generating apparatus or device and the ion inlet of the ELIT 14.

[0086] Following step 156 (or during step 154 and/or step 156), the process 150 advances to step 158 where a charge signal amplitude value CHA is selected, e.g., by a user of the CDMS 10 and/or automatically by the processor 50 as described above. In any case, CHA selected at step 158 is a charge magnitude value which is desired to be used as a trigger to cause the processor 50 to close the ELIT 14 to trap a corresponding ion therein. Illustratively, CHA has a magnitude less than or equal to the conventional threshold level normally used for strongly charged ions as illustrated in FIG. 5A and described above. Typically, CHA will have a value of between just above the noise floor on the charge detection

cylinder CD and noise + 500 e or so, although other values of CHA outside this example range may be selected in other embodiments.

[0087] Following step 158, the process 150 advances to step 160 where the processor 50 is illustratively operable to select one or more of the CTH maps stored in the memory based on the measured ion inlet frequency IF and on the selected charge signal amplitude value CHA. In some instances, the measured IF value may correspond to a single CTH map, and in other embodiments the measured IF vale may be between IF values of two different CTH maps. In the former case, the processor 50 is operable to retrieve the single CTH map stored in the memory 18 and in the latter case the processor 50 is operable to retrieve the two different CTH maps stored in the memory 18. Once retrieved, the processor 50 is operable to map the selected CHA value to a corresponding optimized comparator threshold value TH using the map(s). In instances in which a single map is retrieved, the processor 50 is operable to select as TH the optimized comparator threshold value paired with the selected CHA value stored in the single selected map. In other instances in which a single map is retrieved, the selected CHA value may be between two CHA values stored in the single map. In such instances, the processor 50 is illustratively operable to estimate a suitable optimized comparator threshold value TH using one or more conventional interpolation techniques or other estimation techniques. Likewise in instances in which two CTH maps are retrieved from memory, conventional interpolation or other estimation techniques may be used to estimate a suitable optimized comparator threshold value TH from the data contained in the two selected tables. In embodiments of the process 150 which do not have a set of CTH maps stored in the memory 18, the processor 50 is alternatively operable at step 160 to compute CTH based on CHA and IF using one or more equations based on the relationships between CTH, CHA and IF illustrated in FIGS. 6A and 6B and described hereinabove.

[0088] Following step 160, the processor 50 is illustratively operable at step 162 to control the voltage source V2 to close the ion mirror M2 so that ions generated by the ion source 12 pass into and through the open ion mirror M1 of the ELIT 14 and are reflected by the ion reflection field established in M2 to trap ions entering M2 from the charge detection cylinder CD and then accelerating the trapped ions in the opposite direction back into and through the charge detection cylinder CD as illustrated by example in FIG. 4B. Thereafter at step 164, the processor 50 is operable to control the voltage source 46 (see FIG. 3) to produce the optimized comparator threshold value TH determined from the one or more stored CTH maps at step 160. Thereafter at step 166, the processor 50 is illustratively operable to monitor the trigger signal TR produced by the comparator 44 to determine if/when the trigger signal TR changes from “inactive” to “active,” thereby informing the processor 50 that the magnitude of

the charge detection signal CHD produced by the charge preamplifier CP has exceeded the magnitude of the optimized comparator threshold TH produced by the voltage source 46 as a result of execution of step 164.

[0089] While the trigger signal TR remains "inactive," the process 150 illustratively advances to step 168 where the processor 150 is illustratively operable to determine whether a time T has expired since execution of step 164 or if the user (or processor 50) has overridden the expiry period. If so, the process 150 loops back to step 154 to re-execute the process 150 for selection of another charge signal amplitude value CHA, and otherwise the process 150 loops back to step 166 to continue to monitor TR. Step 168 is illustratively included in some embodiments in which it may be desirable to allow only a predefined time period for the charge detection signal CHD to trigger the comparator 44 and/or to allow the user or processor 150 to cancel and restart the process 150. In any case, if/when the processor 150 determines at step 166 that the trigger signal TR has changed state from "inactive" to "active," the process 150 illustratively advances from the YES branch of step 166 to step 170 where the processor 150 is illustratively operable to control V1 to close M1, thereby closing the ELIT 14 and trapping the ion therein as illustrated in FIG. 4C and described above.

[0090] Execution of steps 162 – 170 illustratively represent control of the ELIT 14 by the processor 50 according to the first version of trigger trapping described above with respect to FIGS. 4A – 4C. In alternate embodiments of the process 150, the processor 50 may be operable to control the ELIT 14 according to the second version of trigger trapping as also described above with respect to FIGS. 4A – 4C. In such embodiments, step 162 may be omitted and step 170 may be modified to include control of V1 and V2 to close M1 and M2 together or one after the other to close the ELIT 14 to trap the ion therein. In any case, following step 170 the process 150 illustratively advances to step 172 where the processor 50 is operable to determine whether the trapping event begun at step 170 is complete, e.g., by the passage of a predefined or selectable time period or by oscillation of the ion back and forth between the ion mirrors M1, M2 a predefined or selectable number of times. Until the trapping event has concluded, the process 150 loops from the NO branch of step 172 to the beginning of step 172.

[0091] When the processor 50 determines at step 172 that the trapping event has concluded, the process 150 advances to step 174 where the processor 50 is illustratively operable to process the charge detection event (CDE) measurement values collected during the trapping event to determine, in a conventional manner, a mass-to-charge value (m/z), a charge (z) and a mass (m) of the ion trapped in the ELIT 14 during the trapping event.

[0092] Following step 174, the process 150 advances to step 176 where the processor 50 is illustratively operable to select one or more of the detection frequency (DF) maps stored in the memory based on the measured ion charge z determined at step 174, the optimized comparator threshold value TH determined at step 160 and used at step 164 to conduct the comparison, and the ion inlet frequency IF measured at step 156. In some instances, the measured ion charge z, the optimized comparator threshold value TH and the measured IF value may together identify a single DF map, and in other embodiments the measured ion charge z and/or the optimized comparator threshold value TH and/or the measured IF value may identify two or more different DF maps. As described above with respect to step 160, the processor 50 is operable at step 176 to map the measured IF and z values to a corresponding detection frequency DF using the one or more DF map(s), e.g., directly and/or using one or more conventional interpolation techniques or other estimation techniques. In embodiments of the process 150 which do not have a set of DF maps stored in the memory 18, the processor 50 is alternatively operable at step 176 to compute DF based on the optimized threshold value CTH and the measured values of IF and z using one or more equations based on the relationships between CTH, ion charge amplitude and IF illustrated in FIG. 6C and described hereinabove.

[0093] Following step 176, the process 150 advances to step 178 where the processor 50 is illustratively operable to select one or more of the correction factor (CF) maps stored in the memory based on the measured ion charge z determined at step 174, the optimized comparator threshold value TH determined at step 160 and used at step 164 to conduct the comparison and the detection frequency DF just determined at step 174. In some instances, the charge signal amplitude value CHA, the optimized comparator threshold value TH and the DF value determined at step 176 may together identify a single CF map, and in other embodiments the measured ion charge z and/or the optimized comparator threshold value TH and/or the determined DF value may identify two or more different CF maps. As described above with respect to step 160, the processor 50 is operable at step 178 to map the determined DF value to a corresponding correction factor CF using the one or more CF map(s), e.g., directly and/or using one or more conventional interpolation techniques or other estimation techniques. In alternate embodiments in which the DF and CF maps are combined into a single set of maps as described above, steps 176 and 178 may likewise be replaced with a single step in which the CF value is determined from such single set of maps. In other alternate embodiments, steps 176 and 178, or the single step just described, may be executed during execution of any one or more of steps 162 – 174.

[0094] In embodiments of the process 150 which do not have a set of CF maps stored in the memory 18, the processor 50 is alternatively operable to compute CF based on the optimized threshold value CTH selected at step 160 and used at step 164 to conduct the comparison, the measured ion charge z determined at step 174 and the DF value determined at step 176 using one or more equations based on the relationships between CTH, ion charge amplitude and DF illustrated in FIG. 6D and described hereinabove. In other alternate embodiments, steps 176 and 178 may be combined such that the processor 50 is operable to compute CF based on the optimized threshold value CTH selected at step 160 and used at step 164 to conduct the comparison and the measured values of ion charge z determined at step 174 and IF determined at step 156 using one or more equations based on the relationships between CTH, ion charge amplitude and IF illustrated in FIGS. 6C and 6D and described hereinabove.

[0095] Following step 178, the process 150 advances to step 180 where the processor 50 is illustratively operable to multiply the intensity of the ion measurements determined at step 174 by the correction factor CF so that the ion intensities in the measured spectrum are corrected to reflect the relative abundances of the ions supplied by the ion source 12 to the ELIT 14. As one example, the correction factor CF determined for each ion measurement illustratively operates as a weighting factor multiplier against a default count value of 1.0 for each detected ion such that, when the correction factor CF is included, the default count (1.0) of the measured ion is multiplied by the correction factor CF. If the detection probability of the ion is 0.5, for example, the correction factor is therefore 2.0 and the weighted count value of the measured ion is therefore likewise 2.0. Thus, because the detection efficiency of this example ion is only 0.5, the measured count value will only be half of that in the ion supplied by the ion source 12 to the ELIT 14, and the measured count value of this ion must therefore be corrected by the correction factor so as to be correctly counted as 2 ions in order to reflect the corresponding abundance of this ion in the ions being supplied by the ion source 12 to the ELIT 14.

[0096] In embodiments of the process 150 in which a user manually or otherwise selects the charge signal amplitude value CHA at step 158, the process 150 illustratively advances from step 180 to step 188 where the process 150 concludes. In alternate embodiments in which the processor 150 is operable to sweep CHA over a selected range of CHA values, the process 180 illustratively includes an additional step 182 following step 180 as shown by dashed-line representation in FIG. 7. In such embodiments, step 182 illustratively includes a step 184 in which the processor 150 is operable to determine whether the process 150 has been executed with each of the CHA values in the selected range. If so, the process

concludes at step 188. Otherwise, the process 150 follows the NO branch of step 184 to step 186 where the processor 50 is operable to increment the charge signal amplitude value CHA by a programmed or selected incremental step value, after which the process 150 loops back to step 154 to re-execute the process 150 using the new CHA value. It will be understood that in such embodiments, step 158 will be skipped as the new CHA value has already been selected at step 186.

[0097] Referring now to FIG. 8A, a simplified block diagram is shown of an embodiment of an ion separation instrument 200 which may include the ELIT 14 configured and operable as described herein, which may include the charge detection mass spectrometer (CDMS) 10 configured and operable as described herein, and which may include any number of ion processing instruments forming part of the ion source 12 upstream of the ELIT 14 and/or which may include any number of ion processing instruments disposed downstream of the ELIT 14 to further process ion(s) exiting the ELIT 14. In this regard, the ion source 12 is illustrated in FIG. 8A as including a number, Q, of ion source stages $IS_1 - IS_Q$ which may be or form part of the ion source 12, where Q may be any positive integer. Alternatively or additionally, an ion processing instrument 210 is illustrated in FIG. 8A as being coupled to the ion outlet of the ELIT 14, wherein the ion processing instrument 210 may include any number of ion processing stages $OS_1 - OS_R$, where R may be any positive integer.

[0098] Focusing on the ion source 12, it will be understood that the source 12 of ions entering the ELIT 14 may be or include, in the form of one or more of the ion source stages $IS_1 - IS_Q$, one or more conventional sources of ions as described above, and may further include one or more conventional instruments for separating ions according to one or more molecular characteristics (e.g., according to ion mass, ion mass-to-charge, ion mobility, ion retention time, or the like) and/or one or more conventional ion processing instruments for collecting and/or storing ions (e.g., one or more quadrupole, hexapole and/or other ion traps), for filtering ions (e.g., according to one or more molecular characteristics such as ion mass, ion mass-to-charge, ion mobility, ion retention time and the like), for fragmenting or otherwise dissociating ions, for normalizing or shifting ion charge states, and the like. It will be understood that the ion source 12 may include one or any combination, in any order, of any such conventional ion sources, ion separation instruments and/or ion processing instruments, and that some embodiments may include multiple adjacent or spaced-apart ones of any such conventional ion sources, ion separation instruments and/or ion processing instruments.

[0099] Turning now to the ion processing instrument 210, it will be understood that the instrument 210 may be or include, in the form of one or more of the ion processing stages $OS_1 - OS_R$, one or more conventional instruments for separating ions according to one or more

molecular characteristics (e.g., according to ion mass, ion mass-to-charge, ion mobility, ion retention time, or the like) and/or one or more conventional ion processing instruments for collecting and/or storing ions (e.g., one or more quadrupole, hexapole and/or other ion traps or guides), for filtering ions (e.g., according to one or more molecular characteristics such as ion mass, ion mass-to-charge, ion mobility, ion retention time and the like), for fragmenting or otherwise dissociating ions, for normalizing or shifting ion charge states, and the like. It will be understood that the ion processing instrument 210 may include one or any combination, in any order, of any such conventional ion separation instruments and/or ion processing instruments, and that some embodiments may include multiple adjacent or spaced-apart ones of any such conventional ion separation instruments and/or ion processing instruments. In any implementation which includes one or more mass spectrometers, any one or more such mass spectrometers may be implemented in any of the forms described above with respect to FIG. 1.

[00100] As one specific implementation of the ion separation instrument 200 illustrated in FIG. 8A, which should not be considered to be limiting in any way, the ion source 12 illustratively includes 3 stages, and the ion processing instrument 210 is omitted. In this example implementation, the ion source stage IS_1 is a conventional source of ions, e.g., electrospray, MALDI or the like, the ion source stage IS_2 is a conventional ion filter, e.g., a quadrupole or hexapole ion guide, and the ion source stage IS_3 is a mass spectrometer of any of the types described above. In this embodiment, the ion source stage IS_2 is controlled in a conventional manner to preselect ions having desired molecular characteristics for analysis by the downstream mass spectrometer, and to pass only such preselected ions to the mass spectrometer, wherein the ions analyzed by the ELIT 14 will be the preselected ions separated by the mass spectrometer according to mass-to-charge ratio. The preselected ions exiting the ion filter may, for example, be ions having a specified ion mass or mass-to-charge ratio, ions having ion masses or ion mass-to-charge ratios above and/or below a specified ion mass or ion mass-to-charge ratio, ions having ion masses or ion mass-to-charge ratios within a specified range of ion mass or ion mass-to-charge ratio, or the like. In some alternate implementations of this example, the ion source stage IS_2 may be the mass spectrometer and the ion source stage IS_3 may be the ion filter, and the ion filter may be otherwise operable as just described to preselect ions exiting the mass spectrometer which have desired molecular characteristics for analysis by the downstream ELIT 14. In other alternate implementations of this example, the ion source stage IS_2 may be the ion filter, and the ion source stage IS_3 may include a mass spectrometer followed by another ion filter, wherein the ion filters each operate as just described.

[00101] As another specific implementation of the ion separation instrument 200 illustrated in FIG. 8A, which should not be considered to be limiting in any way, the ion source 12 illustratively includes 2 stages, and the ion processing instrument 210 is again omitted. In this example implementation, the ion source stage IS_1 is a conventional source of ions, e.g., electrospray, MALDI or the like, the ion source stage IS_2 is a conventional mass spectrometer of any of the types described above. This is the implementation of the CDMS 10 described above with respect to FIG. 1 in which the ELIT 14 is operable to analyze ions exiting the mass spectrometer.

[00102] As yet another specific implementation of the ion separation instrument 200 illustrated in FIG. 8A, which should not be considered to be limiting in any way, the ion source 12 illustratively includes 2 stages, and the ion processing instrument 210 is omitted. In this example implementation, the ion source stage IS_1 is a conventional source of ions, e.g., electrospray, MALDI or the like, and the ion processing stage OS_2 is a conventional single or multiple-state ion mobility spectrometer. In this implementation, the ion mobility spectrometer is operable to separate ions, generated by the ion source stage IS_1, over time according to one or more functions of ion mobility, and the ELIT 14 is operable to analyze ions exiting the ion mobility spectrometer. In an alternate implementation of this example, the ion source 12 may include only a single stage IS_1 in the form of a conventional source of ions, and the ion processing instrument 210 may include a conventional single or multiple-stage ion mobility spectrometer as a sole stage OS_1 (or as stage OS_1 of a multiple-stage instrument 210). In this alternate implementation, the ELIT 14 is operable to analyze ions generated by the ion source stage IS_1, and the ion mobility spectrometer OS_1 is operable to separate ions exiting the ELIT 14 over time according to one or more functions of ion mobility. As another alternate implementation of this example, single or multiple-stage ion mobility spectrometers may follow both the ion source stage IS_1 and the ELIT 14. In this alternate implementation, the ion mobility spectrometer following the ion source stage IS_1 is operable to separate ions, generated by the ion source stage IS_1, over time according to one or more functions of ion mobility, the ELIT 14 is operable to analyze ions exiting the ion source stage ion mobility spectrometer, and the ion mobility spectrometer of the ion processing stage OS_1 following the ELIT 14 is operable to separate ions exiting the ELIT 14 over time according to one or more functions of ion mobility.

[00103] As still another specific implementation of the ion separation instrument 200 illustrated in FIG. 8A, which should not be considered to be limiting in any way, the ion source 12 illustratively includes 2 stages, and the ion processing instrument 210 is omitted. In this example implementation, the ion source stage IS_1 is a conventional liquid chromatograph, e.g.,

HPLC or the like configured to separate molecules in solution according to molecule retention time, and the ion source stage IS_2 is a conventional source of ions, e.g., electrospray or the like. In this implementation, the liquid chromatograph is operable to separate molecular components in solution, the ion source stage IS_2 is operable to generate ions from the solution flow exiting the liquid chromatograph, and the ELIT 14 is operable to analyze ions generated by the ion source stage IS_2. In an alternate implementation of this example, the ion source stage IS_1 may instead be a conventional size-exclusion chromatograph (SEC) operable to separate molecules in solution by size. In another alternate implementation, the ion source stage IS_1 may include a conventional liquid chromatograph followed by a conventional SEC or vice versa. In this implementation, ions are generated by the ion source stage IS_2 from a twice separated solution; once according to molecule retention time followed by a second according to molecule size, or vice versa.

[00104] Referring now to FIG. 8B, a simplified block diagram is shown of another embodiment of an ion separation instrument 220 which illustratively includes a multi-stage mass spectrometer instrument 230 and which also includes the ion mass detection system 10, i.e., CDMS, illustrated and described herein implemented as a high-mass ion analysis component. In the illustrated embodiment, the multi-stage mass spectrometer instrument 230 includes an ion source (IS) 12, as illustrated and described herein, followed by and coupled to a first conventional mass spectrometer (MS1) 232, followed by and coupled to a conventional ion dissociation stage (ID) 234 operable to dissociate ions exiting the mass spectrometer 232, e.g., by one or more of collision-induced dissociation (CID), surface-induced dissociation (SID), electron capture dissociation (ECD) and/or photo-induced dissociation (PID) or the like, followed by and coupled to a second conventional mass spectrometer (MS2) 236, followed by a conventional ion detector (D) 238, e.g., such as a microchannel plate detector or other conventional ion detector. The ion mass detection system 10, i.e., CDMS, is coupled in parallel with and to the ion dissociation stage 234 such that the ion mass detection system 10, i.e., CDMS, may selectively receive ions from the mass spectrometer 236 and/or from the ion dissociation stage 232.

[00105] MS/MS, e.g., using only the ion separation instrument 230, is a well-established approach where precursor ions of a particular molecular weight are selected by the first mass spectrometer 232 (MS1) based on their m/z value. The mass selected precursor ions are fragmented, e.g., by collision-induced dissociation, surface-induced dissociation, electron capture dissociation, or photo-induced dissociation, in the ion dissociation stage 234. The fragment ions are then analyzed by the second mass spectrometer 236 (MS2). Only the m/z values of the precursor and fragment ions are measured in both MS1 and MS2. For high mass

ions, the charge states are not resolved and so it is not possible to select precursor ions with a specific molecular weight based on the m/z value alone. However, by coupling the instrument 230 to the CDMS 10 illustrated and described herein, it is possible to select a narrow range of m/z values and then use the CDMS 10 to determine the masses of the m/z selected precursor ions. The mass spectrometers 232, 236 may be, for example, one or any combination of a magnetic sector mass spectrometer, time-of-flight mass spectrometer or quadrupole mass spectrometer, although in alternate embodiments other mass spectrometer types may be used. In any case, the m/z selected precursor ions with known masses exiting MS1 can be fragmented in the ion dissociation stage 234, and the resulting fragment ions can then be analyzed by MS2 (where only the m/z ratio is measured) and/or by the CDMS instrument 10 (where the m/z ratio and charge are measured simultaneously). Low mass fragments, i.e., dissociated ions of precursor ions having mass values below a threshold mass value, e.g., 10,000 Da (or other mass value), can thus be analyzed by conventional MS, using MS2, while high mass fragments (where the charge states are not resolved), i.e., dissociated ions of precursor ions having mass values at or above the threshold mass value, can be analyzed by CDMS 10.

[00106] It will be understood that the dimensions of the various components of the ELIT 14 and the magnitudes of the electric fields established therein, as implemented in any of the systems 10, 200, 220 illustrated in the attached figures and described above, may illustratively be selected so as to establish a desired duty cycle of ion oscillation within the ELIT 14, corresponding to a ratio of time spent by an ion in the charge detection cylinder CD and a total time spent by the ion traversing the combination of the ion mirrors M1, M2 and the charge detection cylinder CD during one complete oscillation cycle. For example, a duty cycle of approximately 50% may be desirable for the purpose of reducing noise in fundamental frequency magnitude determinations resulting from harmonic frequency components of the measured signals. Details relating to such dimensional and operational considerations for achieving a desired duty cycle, e.g., such as 50%, are illustrated and described in co-pending U.S. Patent Application Ser. No. 62/616,860, filed January 12, 2018, co-pending U.S. Patent Application Ser. No. 62/680,343, filed June 4, 2018 and co-pending International Patent Application No. PCT/US2019/_____, filed January 11, 2019, all entitled ELECTROSTATIC LINEAR ION TRAP DESIGN FOR CHARGE DETECTION MASS SPECTROMETRY, the disclosures of which are all expressly incorporated herein by reference in their entireties.

[00107] It will be further understood that one or more charge calibration or resetting apparatuses may be used with the ELIT 14 alone and/or in any of the systems 10, 200, 220 illustrated in the attached figures and described herein. An example of one such charge

calibration or resetting apparatus is illustrated and described in co-pending U.S. Patent Application Ser. No. 62/680,272, filed June 4, 2018 and in co-pending International Patent Application No. PCT/US2019/_____, filed January 11, 2019, both entitled APPARATUS AND METHOD FOR CALIBRATING OR RESETTING A CHARGE DETECTOR, the disclosures of which are both expressly incorporated herein by reference in their entireties.

[00108] It will be still further understood that the trigger trapping techniques illustrated in the attached figures and described herein may be implemented in each of two or more ELITs and/or in each of two or more ELIT regions in systems and/or applications which include at least one ELIT array having two or more ELITs or having two or more ELIT regions. Examples of some such ELITs and/or ELIT arrays are illustrated and described in co-pending U.S. Patent Application Ser. No. 62/680,315, filed June 4, 2018 and in co-pending International Patent Application No. PCT/US2019/_____, filed January 11. 2019, both entitled ION TRAP ARRAY FOR HIGH THROUGHPUT CHARGE DETECTION MASS SPECTROMETRY, the disclosures of which are both expressly incorporated herein by reference in their entireties.

[00109] It will be further understood that one or more ion source optimization apparatuses and/or techniques may be used with one or more embodiments of the ion source 12 as part of or in combination with any of the systems 10, 200, 220 illustrated in the attached figures and described herein, some examples of which are illustrated and described in co-pending U.S. Patent Application Ser. No. 62/680,223, filed June 4, 2018 and entitled HYBRID ION FUNNEL-ION CARPET (FUNPET) ATMOSPHERIC PRESSURE INTERFACE FOR CHARGE DETECTION MASS SPECTROMETRY, and in co-pending International Patent Application No. PCT/US2019/_____, filed January 11, 2019 and entitled INTERFACE FOR TRANSPORTING IONS FROM AN ATMOSPHERIC PRESSURE ENVIRONMENT TO A LOW PRESSURE ENVIRONMENT, the disclosures of which are both expressly incorporated herein by reference in their entireties.

[00110] It will be still further understood that the trigger trapping techniques illustrated in the attached figures and described herein may be implemented in or as part of systems configured to operate in accordance with real-time analysis and/or real-time control techniques, some examples of which are illustrated and described in co-pending U.S. Patent Application Ser. No. 62/680,245, filed June 4, 2018 and co-pending International Patent Application No. PCT/US2019/_____, filed January 11, 2019, both entitled CHARGE DETECTION MASS SPECTROMETRY WITH REAL TIME ANALYSIS AND SIGNAL OPTIMIZATION, the disclosures of which are both expressly incorporated herein by reference in their entireties. As one non-limiting example, one or more real-time control apparatus and/or techniques described in the patent application identified in this paragraph may be used to select one or

more values of the charge signal amplitude values CHA, to control the voltage source 44 illustrated in FIG. 3 to selectively control the magnitude of the comparator threshold voltage CTH, and/or to modify or regulate the signal intensity of ions entering the ELIT and/or the detection frequency as described above with respect to FIG. 6D.

[00111] It will be still further understood that in any of the systems 10, 200, 220 illustrated in the attached figures and described herein, the ELIT 14 may be replaced with an orbitrap, and that the trigger trapping techniques illustrated in the attached figures and described herein may be used with such an orbitrap. An example of one such orbitrap is illustrated and described in co-pending U.S. Patent Application Ser. No. 62/769,952, filed November 20, 2018 and in co-pending International Patent Application No. PCT/US2019/_____, filed January 11, 2019, both entitled ORBITRAP FOR SINGLE PARTICLE MASS SPECTROMETRY, the disclosures of which are both expressly incorporated herein by reference in their entireties.

[00112] It will be yet further understood that the trigger trapping techniques illustrated and described herein may be used in systems and/or applications in which one or more ion inlet trajectory control apparatuses and/or techniques is/are used to provide for simultaneous measurements of multiple individual ions within the ELIT 14. Examples of some such ion inlet trajectory control apparatuses and/or techniques are illustrated and described in co-pending U.S. Patent Application Ser. No. 62/774,703, filed December 3, 2018 and in co-pending International Patent Application No. PCT/US2019/_____, filed January 11, 2019, both entitled APPARATUS AND METHOD FOR SIMULTANEOUSLY ANALYZING MULTIPLE IONS WITH AN ELECTROSTATIC LINEAR ION TRAP, the disclosures of which are both expressly incorporated herein by reference in their entireties.

[00113] While this disclosure has been illustrated and described in detail in the foregoing drawings and description, the same is to be considered as illustrative and not restrictive in character, it being understood that only illustrative embodiments thereof have been shown and described and that all changes and modifications that come within the spirit of this disclosure are desired to be protected. For example, it will be understood that the ELIT 14 illustrated in the attached figures and described herein is provided only by way of example, and that the concepts, structures and techniques described above may be implemented directly in ELITs of various alternate designs. Any such alternate ELIT design may, for example, include any one or combination of two or more ELIT regions, more, fewer and/or differently-shaped ion mirror electrodes, more or fewer voltage sources, more or fewer DC or time-varying signals produced by one or more of the voltage sources, one or more ion mirrors defining additional electric field regions, or the like.

What is claimed is:

1. A system for trapping ions for measurement thereof, comprising:

an electrostatic linear ion trap (ELIT),

a source of ions configured to supply ions to the ELIT,

a processor operatively coupled to the ELIT, and

a memory having instructions stored therein which, when executed by the at least one processor, cause the at least one processor to (i) produce at least one control signal to open the ELIT to allow ions supplied by the source of ions to enter the ELIT, (ii) determine an ion inlet frequency corresponding to a frequency of ions flowing from the source of ions into the open ELIT, (iii) generate or receive a target ion charge value, (iv) determine an optimum threshold value as a function of the target ion charge value and the determined ion inlet frequency, and (v) produce at least one control signal to close the ELIT when a charge of an ion within the ELIT exceeds the optimum threshold value to thereby trap the ion in the ELIT.

2. The system of claim 1, wherein the ELIT includes a first ion mirror defining a first passageway, a second ion mirror defining a second ion passageway and a charge detection cylinder defining a third passageway therethrough, wherein the first, second and third passageways are coaxially aligned with the charge detection cylinder disposed between the first and second ion mirrors such that a longitudinal axis of the ELIT passes centrally through each of the first, second and third passageways, the first ion mirror defining an ion inlet aperture via which ions supplied by the source of ions flow into the ELIT.

3. The system of claim 2, further comprising at least one voltage source operatively coupled to the processor and to the first and second ion mirrors and configured to produce voltages for selectively establishing an ion transmission electric field or an ion reflection electric field therein, the ion transmission electric field configured to focus an ion passing through a respective one of the first and second ion mirrors toward the longitudinal axis, the ion reflection electric field configured to cause an ion entering a respective one of the first and second ion mirrors from the charge detection cylinder to stop and accelerate in an opposite direction back through the charge detection cylinder and toward the other of the first and second ion mirrors while also focusing the ion toward the longitudinal axis.

4. The system of claim 3, wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to produce at least one control signal to open the ELIT by controlling the at least one voltage source to establish the ion transmission electric field in the first and second ion mirrors such that ions supplied by the source of ions flow into the first ion mirror and then through the charge

detection cylinder and the second ion mirror, each ion flowing through the charge detection cylinder inducing a respective charge thereon.

5. The system of claim 3 or claim 4, wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to produce at least one control signal to close the ELIT by controlling the at least one voltage source to simultaneously establish the ion reflection electric field in the first and second ion mirrors when the charge of the ion within the ELIT exceeds the optimum threshold value to thereby trap the ion in the ELIT and cause the trapped ion to oscillate back and forth between the first and second ion mirrors each time passing through the charge detection cylinder and inducing a corresponding charge thereon.

6. The system of claim 3 or claim 4, wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to produce at least one control signal to close the ELIT by controlling the at least one voltage source to establish the ion reflection electric field in the second ion mirror after determining the optimum threshold value, and, after the ion reflection electric field is established in the second ion mirror, controlling the at least one voltage source to establish the ion reflection electric field in the first ion mirror when the charge of the ion within the ELIT exceeds the optimum threshold value to thereby trap the ion in the ELIT, wherein the ion reflection electric fields established in the first and second ion mirrors together cause the trapped ion to oscillate back and forth between the first and second ion mirrors each time passing through the charge detection cylinder and inducing a corresponding charge thereon.

7. The system of any of claims 4 through 6, further comprising means for determining the ion inlet frequency and providing the determined ion inlet frequency to the processor.

8. The system of any of claims 2 through 6, further comprising a charge preamplifier having an input operatively coupled to the charge detection cylinder and an output operatively coupled to the processor, the charge preamplifier configured to produce a charge detection signal at the output thereof each time a charge is induced on the charge detection cylinder by an ion passing therethrough,

wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to determine the ion inlet frequency by monitoring the charge detection signals produced by the charge preamplifier as the ions entering the ELIT from the ion source pass through the charge detection cylinder and determining a frequency of the monitored charge detection signals.

9. The system of any of claims 1 through 8, further comprising means responsive to user input of the target ion charge value to supply the target ion charge value to the processor.

10. The system of any of claims 1 through 8, further comprising a display monitor,

wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to control the display monitor to display a control graphic user interface (GUI) including one or more selectable GUI elements, and to receive the target ion charge value via user interaction with the one or more selectable GUI elements.

11. The system of any of claims 1 through 8, wherein the processor is a first processor and further comprising:

a display monitor, and

a second processor programmed to control the display monitor to display a control graphic user interface (GUI) including one or more selectable GUI elements, to receive the target ion charge value via user interaction with the one or more selectable GUI elements and to provide the received target ion charge value to the first processor,

and wherein the instructions stored in the memory further include instructions which, when executed by the first processor, cause the first processor to receive the target ion charge value from the second processor.

12. The system of any of claims 1 through 8, wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to generate the target ion charge value.

13. The system of claim 12, wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to (vi) produce at least one control signal to open the ELIT after the ELIT has been closed for a trapping event time duration in which the ion is trapped within the ELIT, (vii) to modify the generated target ion charge value by an incremental charge value, and (viii) to repeat (i), (ii), (iv) and (v) using the modified target ion charge value.

14. The system of claim 13, wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to repeat (vi) through (viii) over a range of target ion charge values.

15. The system of any of claims 2 through 6 and 9 through 14, further comprising:

a charge preamplifier having an input operatively coupled to the charge detection cylinder and an output operatively coupled to the processor, the charge preamplifier configured to produce a charge detection signal at the output thereof each time a charge is induced on the charge detection cylinder by an ion passing therethrough,

a threshold generator circuit having an input coupled to the processor and an output, and

a comparator circuit having a first input coupled to an output of the charge preamplifier, a second input coupled to the output of the threshold generator circuit, and an output coupled to the processor,

wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to control the threshold generator to produce a signal at the output thereof equal to the optimum threshold value, to monitor the output of the comparator and to produce the at least one control signal to close the ELIT in response to a change of state of the output of the comparator resulting from a magnitude of the charge detection signal produced by the charge preamplifier exceeding the optimum threshold value.

16. The system of any of claims 8 through 14, further comprising:

a threshold generator circuit having an input coupled to the processor and an output, and

a comparator circuit having a first input coupled to an output of the charge preamplifier, a second input coupled to the output of the threshold generator circuit, and an output coupled to the processor,

wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to control the threshold generator to produce a signal at the output thereof equal to the optimum threshold value, to monitor the output of the comparator and to produce the at least one control signal to close the ELIT in response to a change of state of the output of the comparator resulting from a magnitude of the charge detection signal produced by the charge preamplifier exceeding the optimum threshold value.

17. The system of claim 15 or claim 16, further comprising a band-pass filter coupled between the output of the charge preamplifier and the first input of the comparator, the band-pass filter restricting the charge detection signal produced by the charge preamplifier to a predefined band of frequencies less than a frequency range of noise on the charge detection cylinder.

18. The system of claim 15 or claim 16, further comprising a signal shaping amplifier coupled between the output of the charge preamplifier and the first input of the comparator, the signal shaping amplifier producing a Gaussian-shaped pulse on each of rising and falling edges of the charge detection signal produced by the charge preamplifier.

19. The system of any of claims 1 through 18, wherein the memory has stored therein a plurality of optimum threshold value maps each including a plurality of optimum threshold values mapped to corresponding charge values for a different ion inlet frequency,

and wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to determine the optimum threshold value by selecting one or more of the plurality of optimum threshold maps stored in the memory based on the target ion charge value and on the determined ion inlet frequency, and to determine the optimum threshold value from the selected one or more of the plurality of optimum threshold maps based on the target ion charge value and the determined ion inlet frequency.

20. The system of any of claims 2 through 6 and 9 through 14, further comprising a charge preamplifier having an input operatively coupled to the charge detection cylinder and an output operatively coupled to the processor, the charge preamplifier configured to produce a charge detection signal at the output thereof each time a charge is induced on the charge detection cylinder by an ion passing therethrough,

and wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to record the charge detection signals produced by the charge preamplifier resulting from repeated detection of a charge of the ion over a duration of a trapping event in which the ion is trapped within the ELIT.

21. The system of any of claims 8 and 15 through 19, wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to record the charge detection signals produced by the charge preamplifier resulting from repeated detection of a charge of the ion over a duration of a trapping event in which the ion is trapped within the ELIT.

22. The system of claim 20 or claim 21, wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to process the recorded charge detection signals to determine a charge of the trapped ion and at least one of a mass-to-charge ratio and a mass of the trapped ion.

23. The system of claim 22, wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to determine

a correction factor as a function of the determined optimum threshold value, the determined ion inlet frequency and the determined charge of the trapped ion, and to correct an intensity of the measured ion by the correction factor to reflect a relative abundance of the ion in the ions supplied by the ion source to the ELIT.

24. The system of claim 23 wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to determine a detection frequency of the trapped ion as a function of the determined ion inlet frequency and the determined charge of the trapped ion, and to determine the correction factor as a function of the determined detection frequency, the determined optimum threshold value and the determined charge of the trapped ion.

25. The system of claim 24, wherein the memory has stored therein a plurality of detection frequency maps each including multiple detection frequency values mapped to corresponding ion inlet frequency values for a different pair of optimum threshold and ion charge amplitude values,

and wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to determine the detection frequency by selecting one or more of the plurality of detection frequency maps stored in the memory based on the determined charge of the trapped ion, the determined optimum threshold value and the determined ion inlet frequency, and to determine the detection frequency from the selected one or more of the plurality of detection frequency maps based on the determined charge of the trapped ion, the determined optimum threshold value and the determined ion inlet frequency.

26. The system of claim 25, wherein the memory has stored therein a plurality of correction factor maps each including multiple correction factor values mapped to corresponding detection frequency values for a different pair of optimum threshold and ion charge amplitude values,

and wherein the instructions stored in the memory further include instructions which, when executed by the processor, cause the processor to determine the correction factor by selecting one or more of the plurality of correction factor maps stored in the memory based on the determined charge of the trapped ion, the determined optimum threshold value and the determined detection frequency, and to determine the correction factor from the selected one or more of the plurality of correction factor maps based on the determined charge of the trapped ion, the determined optimum threshold value and the determined detection frequency.

27. A system for separating ions, comprising:

the ion trapping system of any of claims 1 through 26, wherein the source of ions is configured to generate ions from a sample, and

at least one ion separation instrument configured to separate the generated ions as a function of at least one molecular characteristic,

wherein ions exiting the at least one ion separation instrument are supplied to the ELIT.

28. The system of claim 27, wherein the ELIT comprises a charge detection cylinder disposed between first and second ion mirrors, and wherein the ELIT is configured and controlled such that an ion trapped therein oscillates back and forth through the charge detection cylinder between the first and second ion mirrors with a duty cycle, corresponding to a ratio of time spent by the ion moving through the charge detection cylinder and a total time spent by the ion traversing a combination of the first and second ion mirrors and the charge detection cylinder during one complete oscillation cycle, of approximately 50%.

29. The system of claim 27 or claim 28, wherein the ELIT is operatively coupled to the source of ions and to the processor, and wherein the ELIT comprises a plurality of axially aligned charge detection cylinders each disposed between respective ion mirrors to form one of a corresponding plurality of cascaded ELIT regions, and wherein the instructions stored in the memory include instructions which, when executed by the processor, cause the processor to control the ELIT to consecutively trap a single ion in each of the plurality of ELIT regions.

30. The system of claim 27 or claim 28, wherein the ELIT comprises a plurality of ELITs each operatively coupled to the processor,

and further comprising means for guiding ions from the at least one ion separation instrument to each of the plurality of ELITs,

and wherein the instructions stored in the memory include instructions which, when executed by the processor, cause the processor to control the ELITs and the means for guiding ions from the at least one ion separation instrument to each of the plurality of ELITs to consecutively trap a single ion in each of the plurality of ELITs.

31. The system of any of claims 27 through 30, wherein the at least one ion separation instrument comprises one or any combination of at least one instrument for separating ions as a function of mass-to-charge ratio, at least one instrument for separating ions in time as a function of ion mobility, at least one instrument for separating ions as a function of ion retention time and at least one instrument for separating ions as a function of molecule size.

32. The system of claim 31, wherein the at least one ion separation instrument comprises one or a combination of a mass spectrometer and an ion mobility spectrometer.

33. The system of any of claims 27 through 32, further comprising at least one ion processing instrument positioned between the ion source and the at least one ion separation instrument, the at least one ion processing instrument positioned between the ion source and the at least one ion separation instrument comprising one or any combination of at least one instrument for collecting or storing ions, at least one instrument for filtering ions according to a molecular characteristic, at least one instrument for dissociating ions and at least one instrument for normalizing or shifting ion charge states.

34. The system of any of claims 27 through 33, further comprising at least one ion processing instrument positioned between the at least one ion separation instrument and the ELIT, the at least one ion processing instrument positioned between the at least one ion separation instrument and the ELIT comprising one or any combination of at least one instrument for collecting or storing ions, at least one instrument for filtering ions according to a molecular characteristic, at least one instrument for dissociating ions and at least one instrument for normalizing or shifting ion charge states.

35. The system of any of claims 27 through 34, wherein the ELIT is configured to allow ion exit therefrom,

and wherein the system further comprises at least one ion separation instrument positioned to receive ions exiting the ELIT and to separate the receive ions as a function of at least one molecular characteristic.

36. The system of claim 35, further comprising at least one ion processing instrument positioned between the ELIT and the at least one ion separation instrument, the at least one ion processing instrument positioned between the ELIT and the at least one ion separation instrument comprising one or any combination of at least one instrument for collecting or storing ions, at least one instrument for filtering ions according to a molecular characteristic, at least one instrument for dissociating ions and at least one instrument for normalizing or shifting ion charge states.

37. The system of claim 35, further comprising at least one ion processing instrument positioned to receive ions exiting the at least one ion separation instrument that is itself positioned to receive ions exiting the ELIT, the at least one ion processing instrument positioned to receive ions exiting the at least one ion separation instrument that is positioned to receive ions exiting the ELIT comprising one or any combination of at least one instrument for collecting or storing ions, at least one instrument for filtering ions according to a molecular

characteristic, at least one instrument for dissociating ions and at least one instrument for normalizing or shifting ion charge states.

38. The system of any of claims 27 through 34, wherein the ELIT is configured to allow ion exit therefrom,

and wherein the system further comprises at least one ion processing instrument positioned to receive ions exiting the ELIT, the at least one ion processing instrument positioned to receive ions exiting the ELIT comprising one or any combination of at least one instrument for collecting or storing ions, at least one instrument for filtering ions according to a molecular characteristic, at least one instrument for dissociating ions and at least one instrument for normalizing or shifting ion charge states.

39. A system for separating ions, comprising:

an ion source configured to generate ions from a sample,

a first mass spectrometer configured to separate the generated ions as a function of mass-to-charge ratio,

an ion dissociation stage positioned to receive ions exiting the first mass spectrometer and configured to dissociate ions exiting the first mass spectrometer,

a second mass spectrometer configured to separate dissociated ions exiting the ion dissociation stage as a function of mass-to-charge ratio, and

the system of claim 27 coupled in parallel with and to the ion dissociation stage such that the system of claim 27 can receive ions exiting either of the first mass spectrometer and the ion dissociation stage, wherein the system of claim 27 is a charge detection mass spectrometer (CDMS),

wherein masses of precursor ions exiting the first mass spectrometer are measured using the CDMS, mass-to-charge ratios of dissociated ions of precursor ions having mass values below a threshold mass are measured using the second mass spectrometer, and mass-to-charge ratios and charge values of dissociated ions of precursor ions having mass values at or above the threshold mass are measured using the CDMS.

40. A method of trapping in an electrostatic linear ion trap (ELIT) ions supplied by a source of ions for measurement thereof, the method comprising:

(i) producing, with a processor, at least one control signal to open the ELIT to allow ions supplied by the source of ions to enter the ELIT,

(ii) determining, with the processor, an ion inlet frequency corresponding to a frequency of ions flowing from the source of ions into the open ELIT,

(iii) generating or receiving, with the processor, a target ion charge value,

(iv) determining, with the processor, an optimum threshold value as a function of the target ion charge value and the determined ion inlet frequency, and

(v) producing, with the processor, at least one control signal to close the ELIT when a charge of an ion within the ELIT exceeds the optimum threshold value to thereby trap the ion in the ELIT.

41. The method of claim 40, wherein the ELIT includes a first ion mirror defining a first passageway, a second ion mirror defining a second ion passageway and a charge detection cylinder defining a third passageway therethrough, wherein the first, second and third passageways are coaxially aligned with the charge detection cylinder disposed between the first and second ion mirrors such that a longitudinal axis of the ELIT passes centrally through each of the first, second and third passageways, the first ion mirror defining an ion inlet aperture via which ions supplied by the source of ions flow into the ELIT,

and wherein at least one voltage source is operatively coupled to the processor and to the first and second ion mirrors and configured to produce voltages for selectively establishing an ion transmission electric field or an ion reflection electric field therein, the ion transmission electric field configured to focus an ion passing through a respective one of the first and second ion mirrors toward the longitudinal axis, the ion reflection electric field configured to cause an ion entering a respective one of the first and second ion mirrors from the charge detection cylinder to stop and accelerate in an opposite direction back through the charge detection cylinder and toward the other of the first and second ion mirrors while also focusing the ion toward the longitudinal axis,

and wherein producing the at least one control signal to open the ELIT comprises controlling, with the processor, the at least one voltage source to establish the ion transmission electric field in the first and second ion mirrors such that ions supplied by the source of ions flow into the first ion mirror and then through the charge detection cylinder and the second ion mirror, each ion flowing through the charge detection cylinder inducing a respective charge thereon.

42. The method of claim 41, wherein producing the at least one control signal to close the ELIT comprises controlling, with the processor, the at least one voltage source to simultaneously establish the ion reflection electric field in the first and second ion mirrors when the charge of the ion within the ELIT exceeds the optimum threshold value to thereby trap the ion in the ELIT and cause the trapped ion to oscillate back and forth between the first and second ion mirrors each time passing through the charge detection cylinder and inducing a corresponding charge thereon.

43. The method of claim 41, wherein producing the at least one control signal to close the ELIT comprises controlling, with the processor, the at least one voltage source to establish the ion reflection electric field in the second ion mirror after determining the optimum threshold value, and, after the ion reflection electric field is established in the second ion mirror, controlling the at least one voltage source to establish the ion reflection electric field in the first ion mirror when the charge of the ion within the ELIT exceeds the optimum threshold value to thereby trap the ion in the ELIT, wherein the ion reflection electric fields established in the first and second ion mirrors together cause the trapped ion to oscillate back and forth between the first and second ion mirrors each time passing through the charge detection cylinder and inducing a corresponding charge thereon.

44. The method of any of claims 40 through 43, further comprising a charge preamplifier having an input operatively coupled to the charge detection cylinder and an output operatively coupled to the processor, the charge preamplifier configured to produce a charge detection signal at the output thereof each time a charge is induced on the charge detection cylinder by an ion passing therethrough,

wherein determining the ion inlet frequency comprises monitoring, by the processor, the charge detection signals produced by the charge preamplifier as the ions entering the ELIT from the ion source pass through the charge detection cylinder and determining a frequency of the monitored charge detection signals.

45. The method of any of claims 40 through 44, wherein the target ion charge value is received by the processor from a user via control of an electronic apparatus or device coupled to the processor.

46. The method of any of claims 40 through 44, further comprising a display monitor controlled by the processor to display a control graphic user interface (GUI) including one or more selectable GUI elements,

wherein the target ion charge value is received via user interaction with the one or more selectable GUI elements.

47. The method of any of claims 40 through 44, wherein the target ion charge value is generated by the processor.

48. The method of claim 47, further comprising:

(vi) producing at least one control signal to open the ELIT after the ELIT has been closed for a trapping event time duration in which the ion is trapped within the ELIT,

(vii) modifying the generated target ion charge value by an incremental charge value, and

(viii) repeating (i), (ii), (iv) and (v) using the modified target ion charge value.

49. The method of claim 48, further comprising repeating (vi) through (viii) over a range of target ion charge values.

50. The method of any of claims 44 through 49, further comprising a threshold generator circuit having an input coupled to the processor and an output, and a comparator circuit having a first input coupled to an output of the charge preamplifier, a second input coupled to the output of the threshold generator circuit, and an output coupled to the processor,

wherein the method further comprises controlling, with the processor, the threshold generator to produce a signal at the output thereof equal to the optimum threshold value, monitoring, with the processor, the output of the comparator and producing, with the processor, the at least one control signal to close the ELIT in response to a change of state of the output of the comparator resulting from a magnitude of the charge detection signal produced by the charge preamplifier exceeding the optimum threshold value.

51. The method of claim 50, further comprising restricting the charge detection signal produced by the charge preamplifier to a predefined band of frequencies less than a frequency range of noise on the charge detection cylinder.

52. The method of claim 50 or 51, shaping the charge detection signal produced by the charge preamplifier to produce a Gaussian-shaped pulse on each of rising and falling edges thereof.

53. The method of any of claims 40 through 52, further comprising storing, with the processor in a memory, a plurality of optimum threshold value maps each including a plurality of optimum threshold values mapped to corresponding charge values for a different ion inlet frequency,

wherein determining the optimum threshold value comprises selecting, by the processor, one or more of the plurality of optimum threshold maps stored in the memory based on the target ion charge value and on the determined ion inlet frequency, and determining, with the processor, the optimum threshold value from the selected one or more of the plurality of optimum threshold maps based on the target ion charge value and the determined ion inlet frequency.

54. The method of any of claims 44 through 53, further comprising recording, with the processor, the charge detection signals produced by the charge preamplifier resulting from repeated detection of a charge of the ion over a duration of a trapping event in which the ion is trapped within the ELIT.

55. The method of claim 54, further comprising processing, with the processor, the recorded charge detection signals to determine a charge of the trapped ion and at least one of a mass-to-charge ratio and a mass of the trapped ion.

56. The method of claim 55, further comprising determining, with the processor, a correction factor as a function of the determined optimum threshold value, the determined ion inlet frequency and the determined charge of the trapped ion, and correcting, with the processor, an intensity of the measured ion by the correction factor to reflect a relative abundance of the ion in the ions supplied by the ion source to the ELIT.

57. The method of claim 56, further comprising determining, with the processor, a detection frequency of the trapped ion as a function of the determined ion inlet frequency and the determined charge of the trapped ion, and determining, with the processor, the correction factor as a function of the determined detection frequency, the determined optimum threshold value and the determined charge of the trapped ion.

58. The method of claim 57, further comprising storing, with the processor in a memory, a plurality of detection frequency maps each including multiple detection frequency values mapped to corresponding ion inlet frequency values for a different pair of optimum threshold and ion charge amplitude values,

and wherein determining the detection frequency comprises selecting, by the processor, one or more of the plurality of detection frequency maps stored in the memory based on the determined charge of the trapped ion, the determined optimum threshold value and the determined ion inlet frequency, and determining, with the processor, the detection frequency from the selected one or more of the plurality of detection frequency maps based on the determined charge of the trapped ion, the determined optimum threshold value and the determined ion inlet frequency.

59. The method of claim 58, further comprising storing, with the processor in the memory, a plurality of correction factor maps each including multiple correction factor values mapped to corresponding detection frequency values for a different pair of optimum threshold and ion charge amplitude values,

and wherein determining the correction factor comprises selecting, with the processor, one or more of the plurality of correction factor maps stored in the memory based on the

determined charge of the trapped ion, the determined optimum threshold value and the determined detection frequency, and determining, with the processor, the correction factor from the selected one or more of the plurality of correction factor maps based on the determined charge of the trapped ion, the determined optimum threshold value and the determined detection frequency.

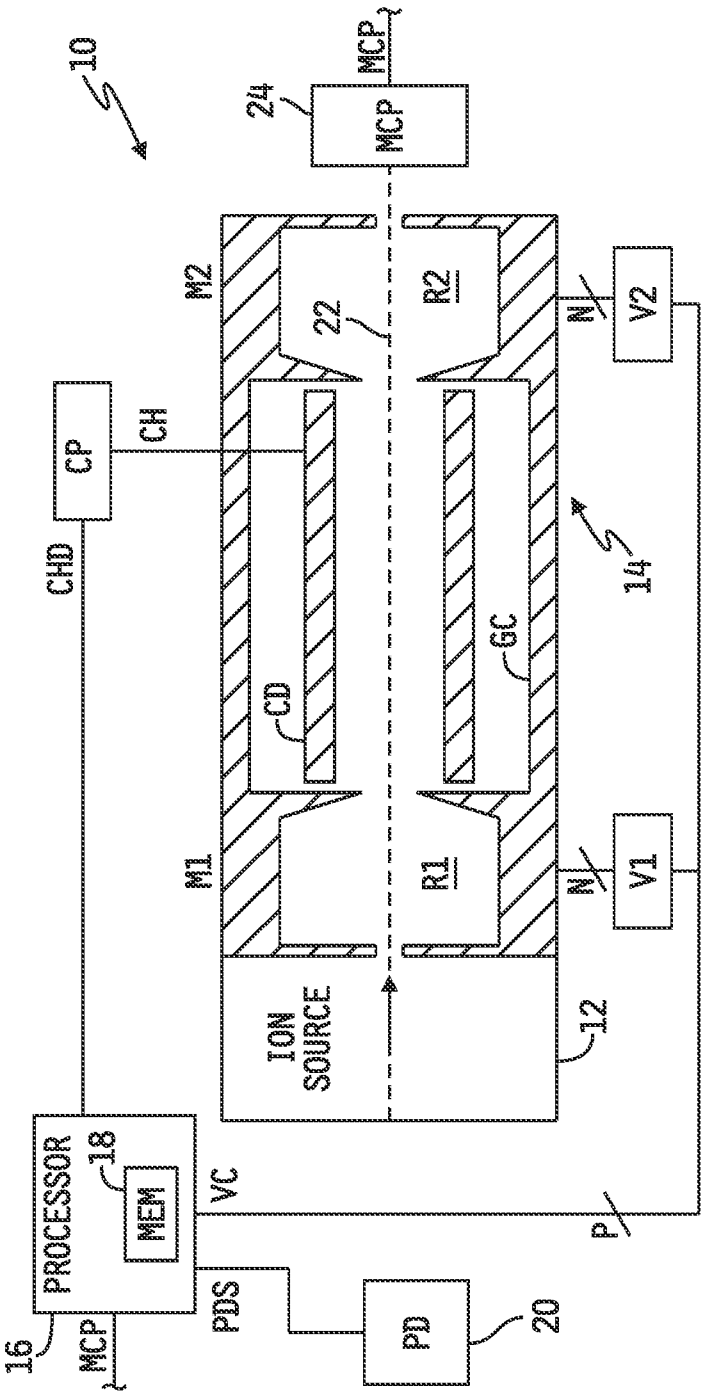

10
24
MCP
MCP
M2
22
R2
N
V2
CP
CH
CHD
CD
GC
14
M1
R1
N
V1
ION SOURCE
12
PROCESSOR
18
MEM
VC
P
16
MCP
PDS
PD
20

FIG. 1

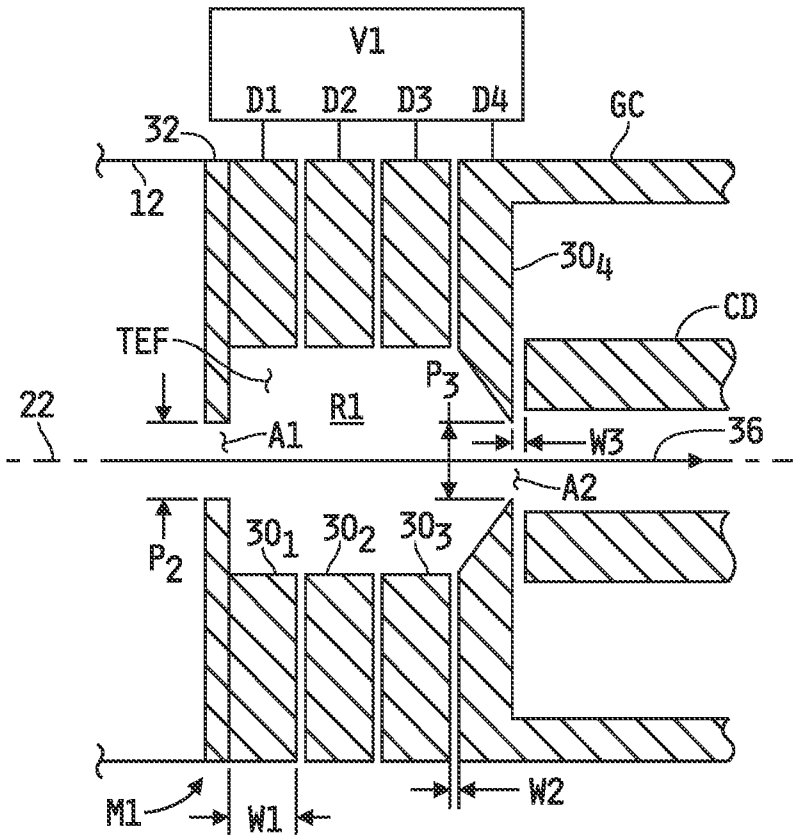

V1
D1
D2
D3
D4
GC
32
12
30_4
CD
TEF
P_3
22
R1
A1
W3
36
A2
P_2
30_1
30_2
30_3
M1
W1
W2

FIG. 2A

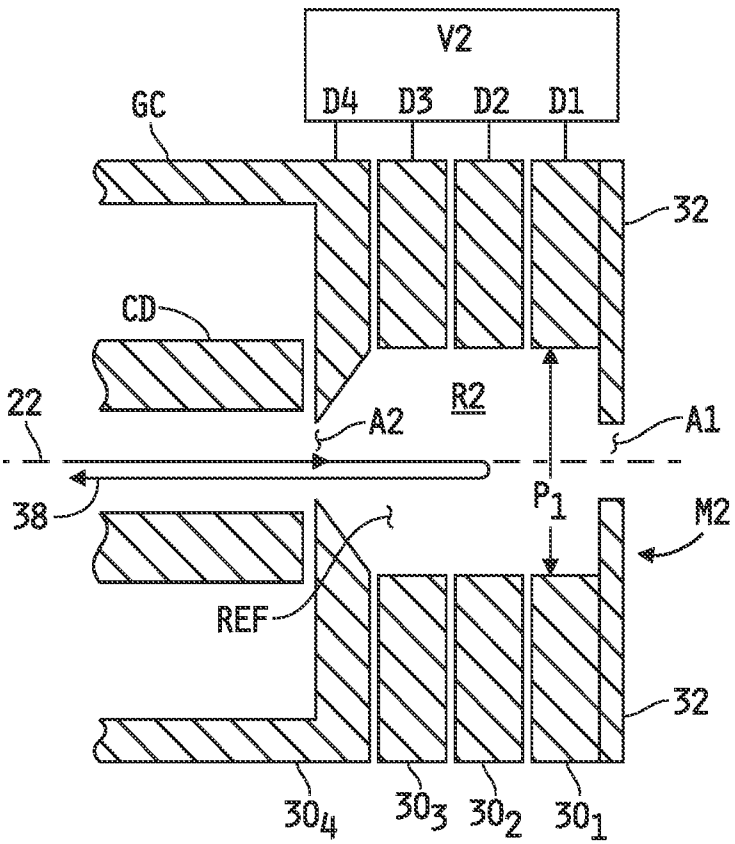

V2
D4
D3
D2
D1
GC
32
CD
22
R2
A2
A1
38
P_1
M2
REF
32
30_4
30_3
30_2
30_1

FIG. 2B

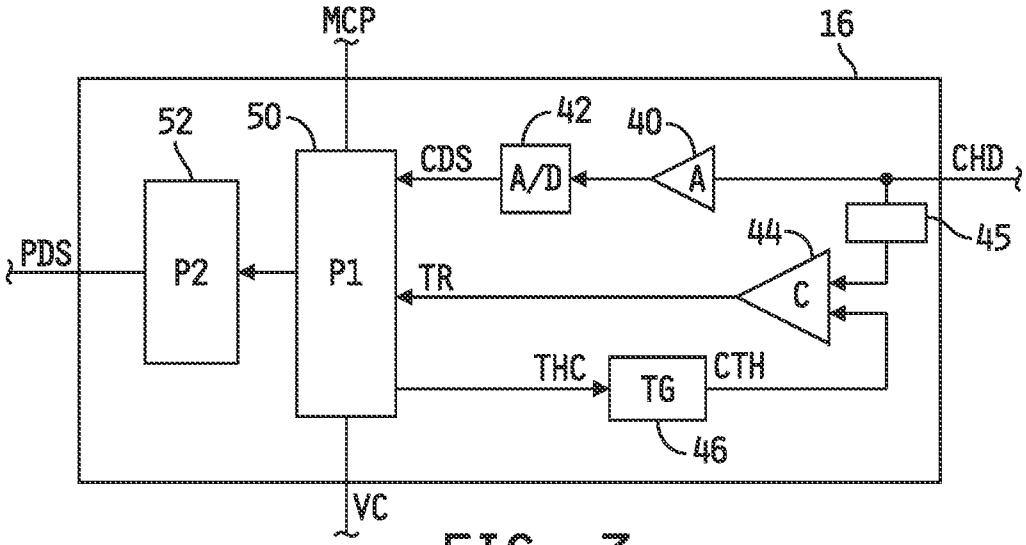


FIG. 3

FIG. 4A

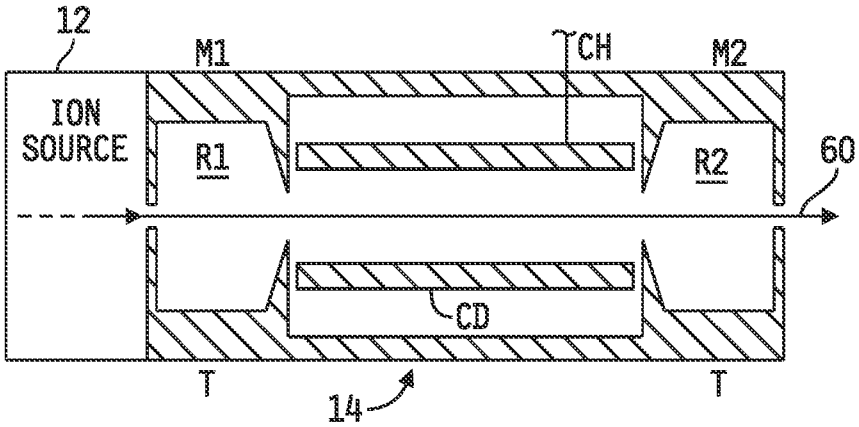


FIG. 4B

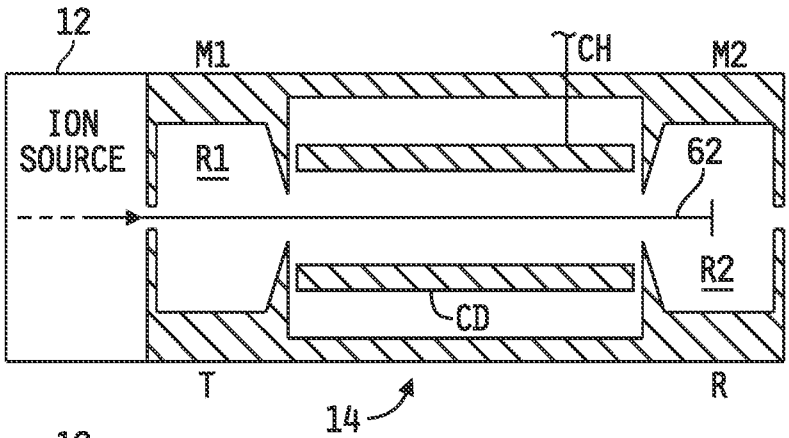
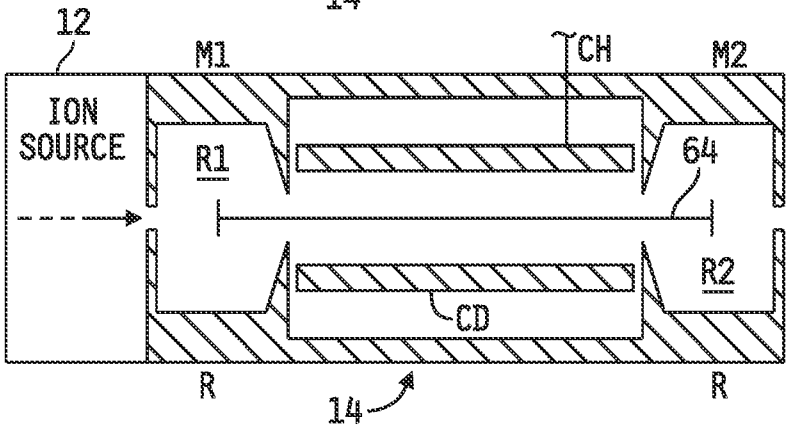


FIG. 4C



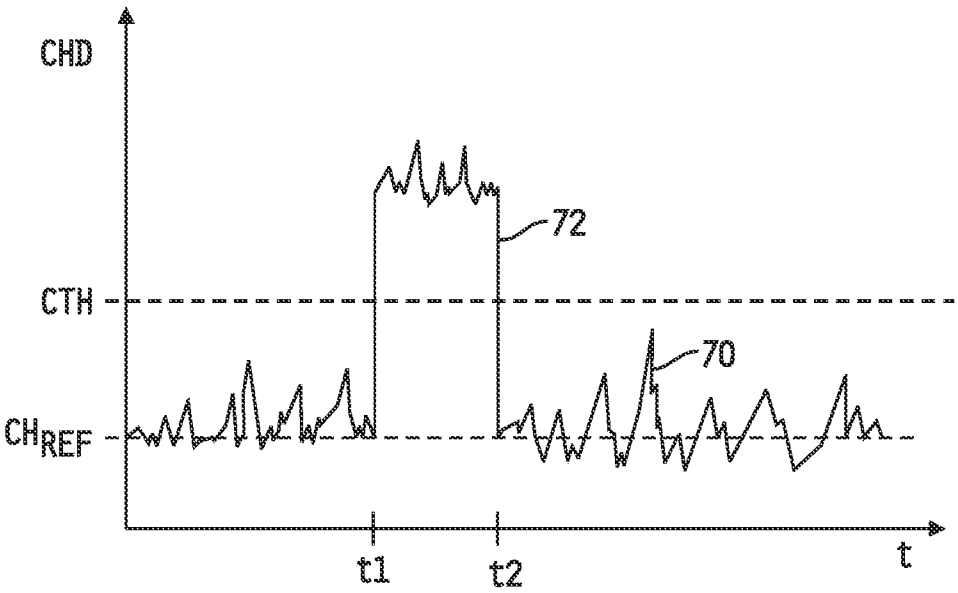


FIG. 5A

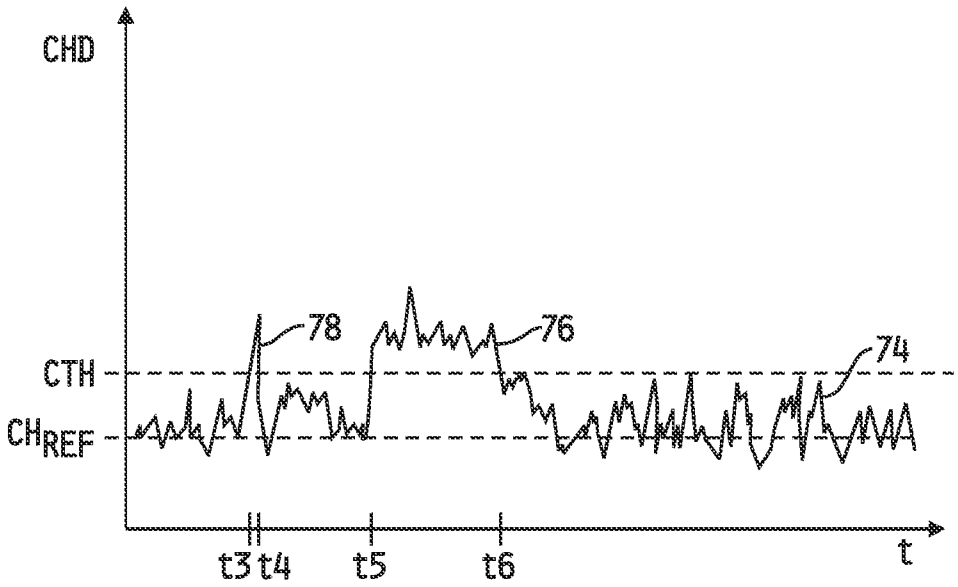


FIG. 5B

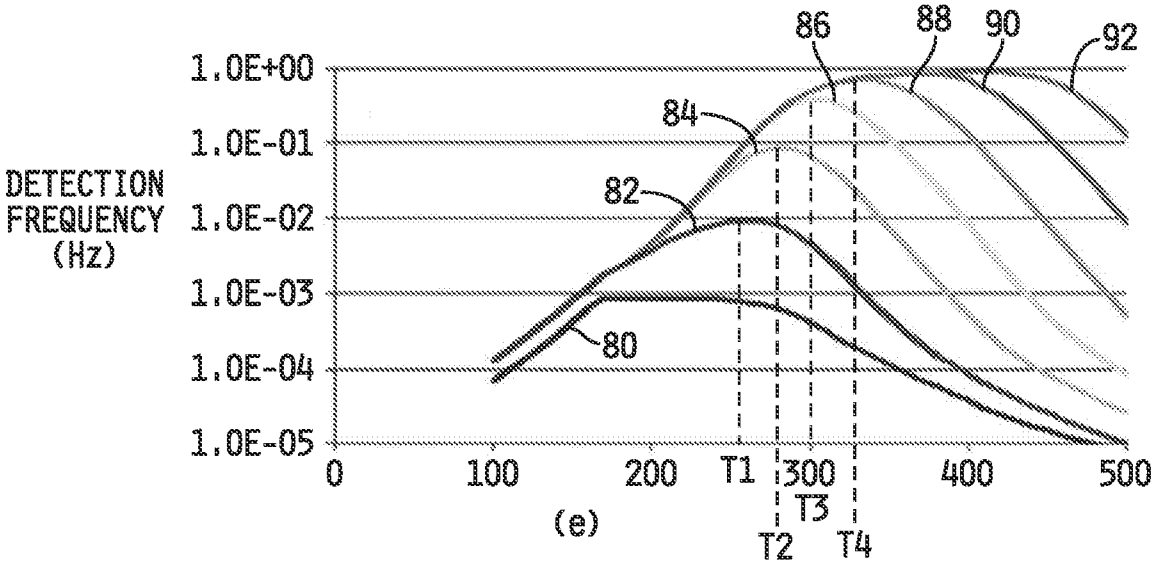

DETECTION FREQUENCY (Hz)
1.0E+00
1.0E-01
1.0E-02
1.0E-03
1.0E-04
1.0E-05
0
100
200
300
400
500
(e)
T1
T2
T3
T4
80
82
84
86
88
90
92

FIG. 6A

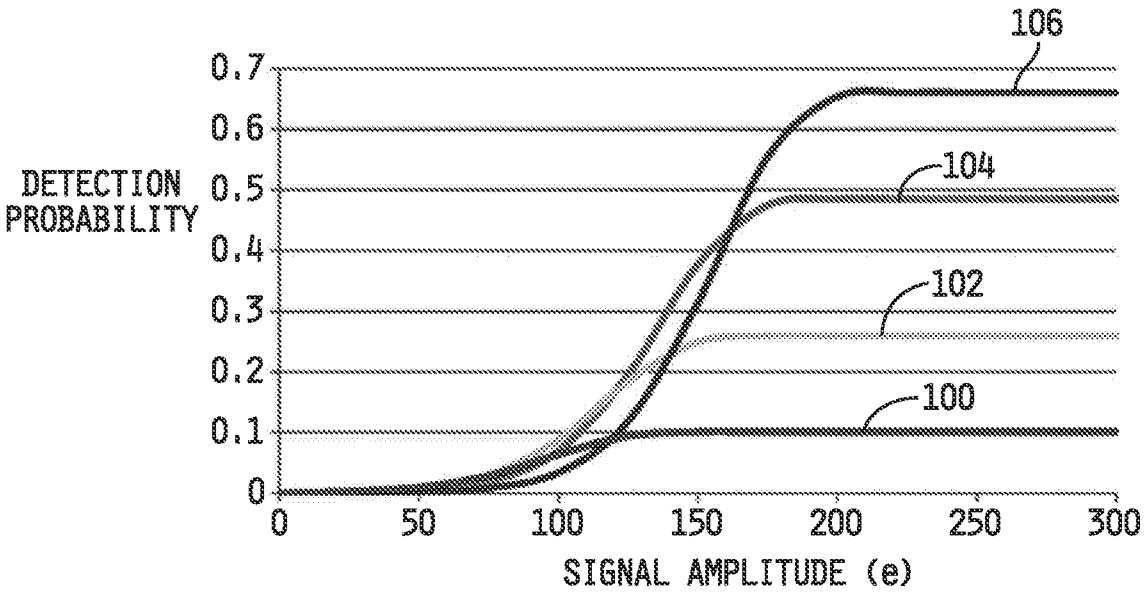

DETECTION PROBABILITY
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
0
50
100
150
200
250
300
SIGNAL AMPLITUDE (e)
106
104
102
100

FIG. 6B

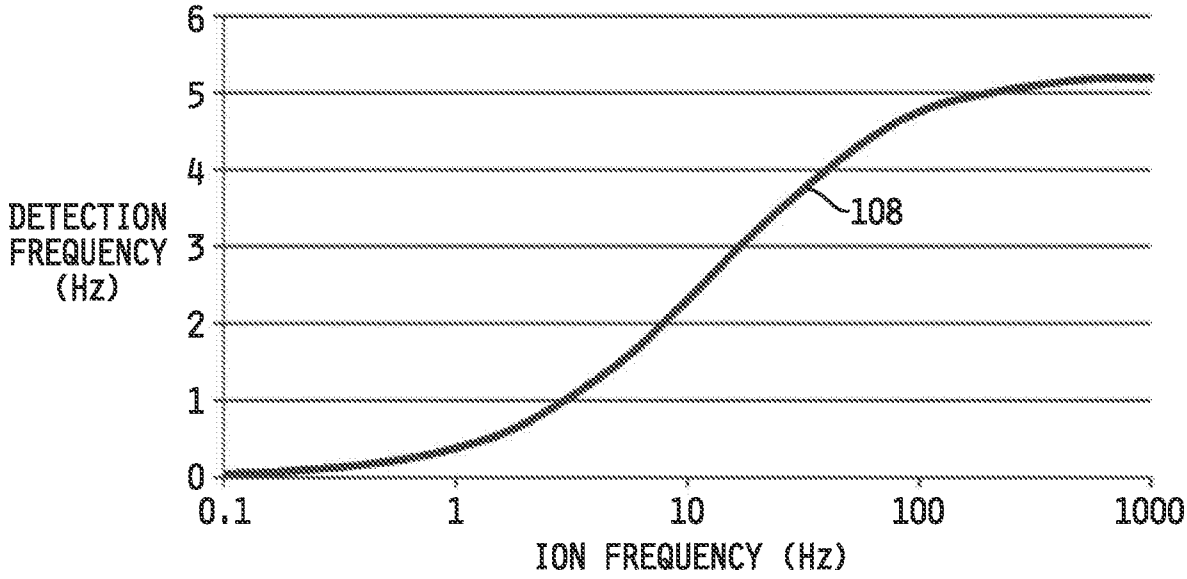

DETECTION FREQUENCY (Hz)
6
5
4
3
2
1
0
0.1
1
10
100
1000
ION FREQUENCY (Hz)
108

FIG. 6C

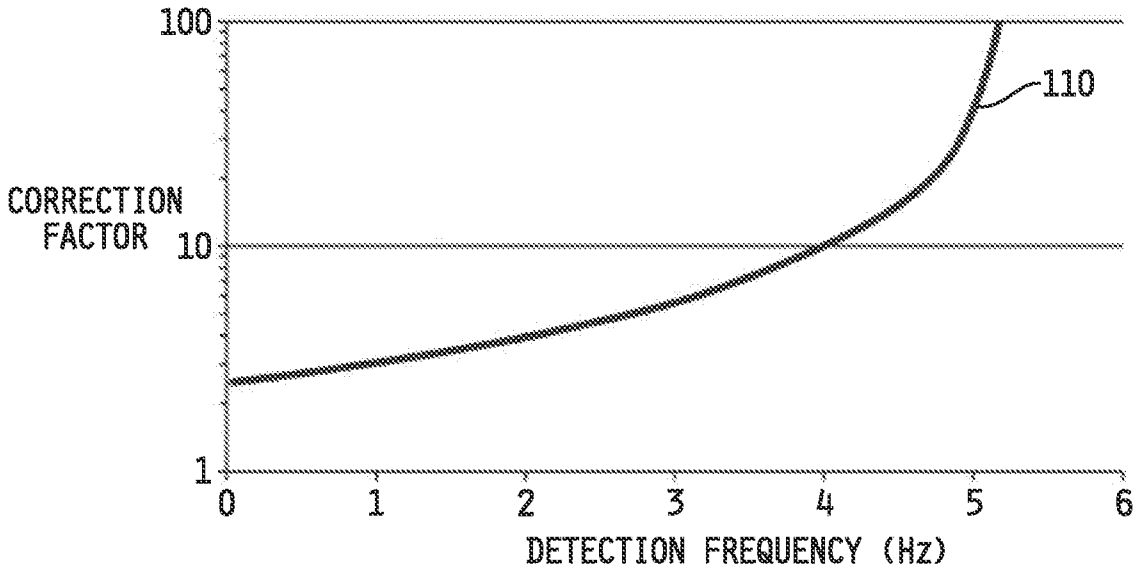

CORRECTION FACTOR
100
10
1
0
1
2
3
4
5
6
DETECTION FREQUENCY (Hz)
110

FIG. 6D

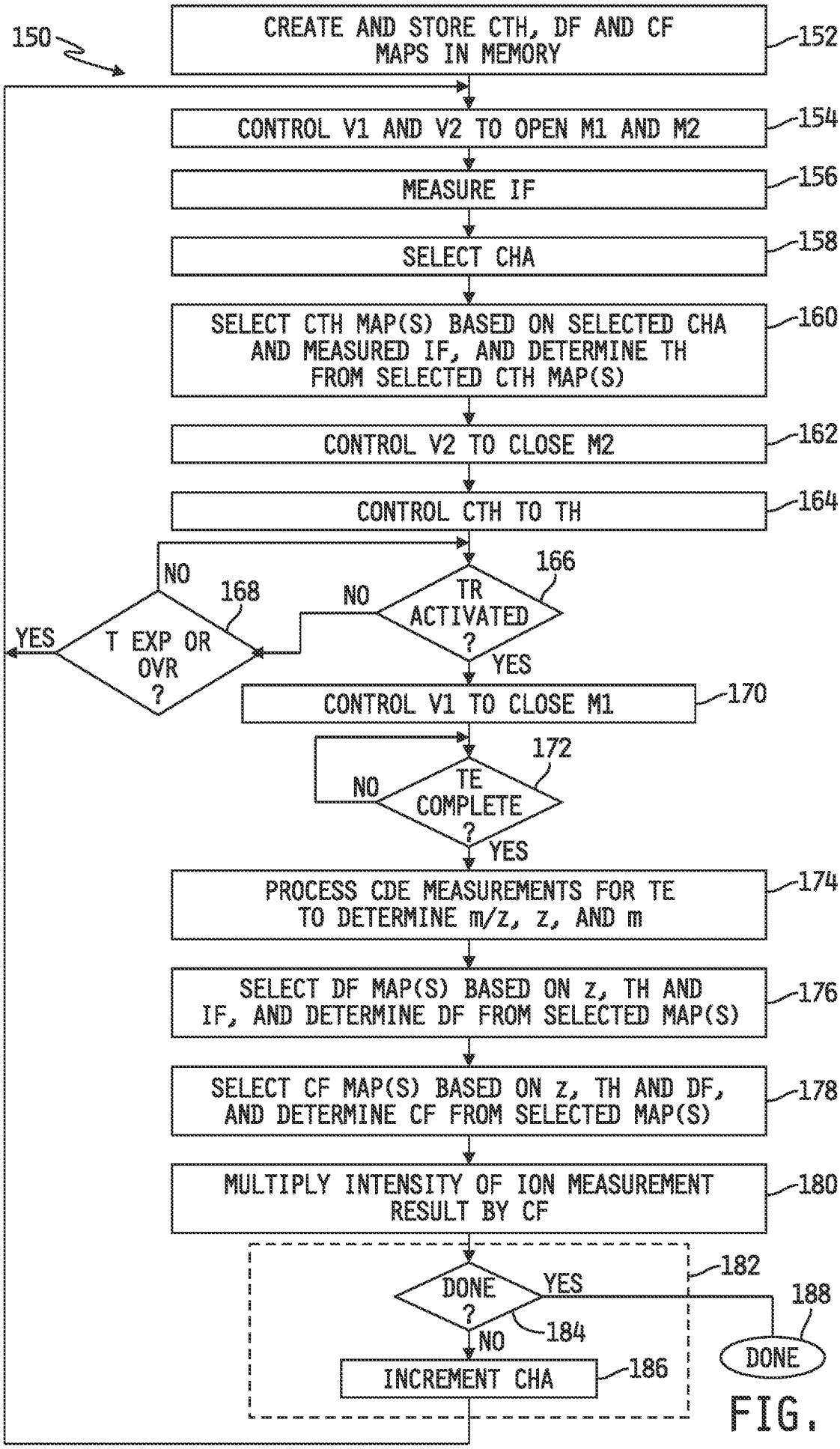

150
CREATE AND STORE CTH, DF AND CF MAPS IN MEMORY
152
CONTROL V1 AND V2 TO OPEN M1 AND M2
154
MEASURE IF
156
SELECT CHA
158
SELECT CTH MAP(S) BASED ON SELECTED CHA AND MEASURED IF, AND DETERMINE TH FROM SELECTED CTH MAP(S)
160
CONTROL V2 TO CLOSE M2
162
CONTROL CTH TO TH
164
TR ACTIVATED ?
166
NO
YES
T EXP OR OVR ?
168
NO
YES
CONTROL V1 TO CLOSE M1
170
TE COMPLETE ?
172
NO
YES
PROCESS CDE MEASUREMENTS FOR TE TO DETERMINE m/z, z, AND m
174
SELECT DF MAP(S) BASED ON z, TH AND IF, AND DETERMINE DF FROM SELECTED MAP(S)
176
SELECT CF MAP(S) BASED ON z, TH AND DF, AND DETERMINE CF FROM SELECTED MAP(S)
178
MULTIPLY INTENSITY OF ION MEASUREMENT RESULT BY CF
180
DONE ?
182
YES
NO
184
INCREMENT CHA
186
DONE
188

FIG. 7

FIG. 8A

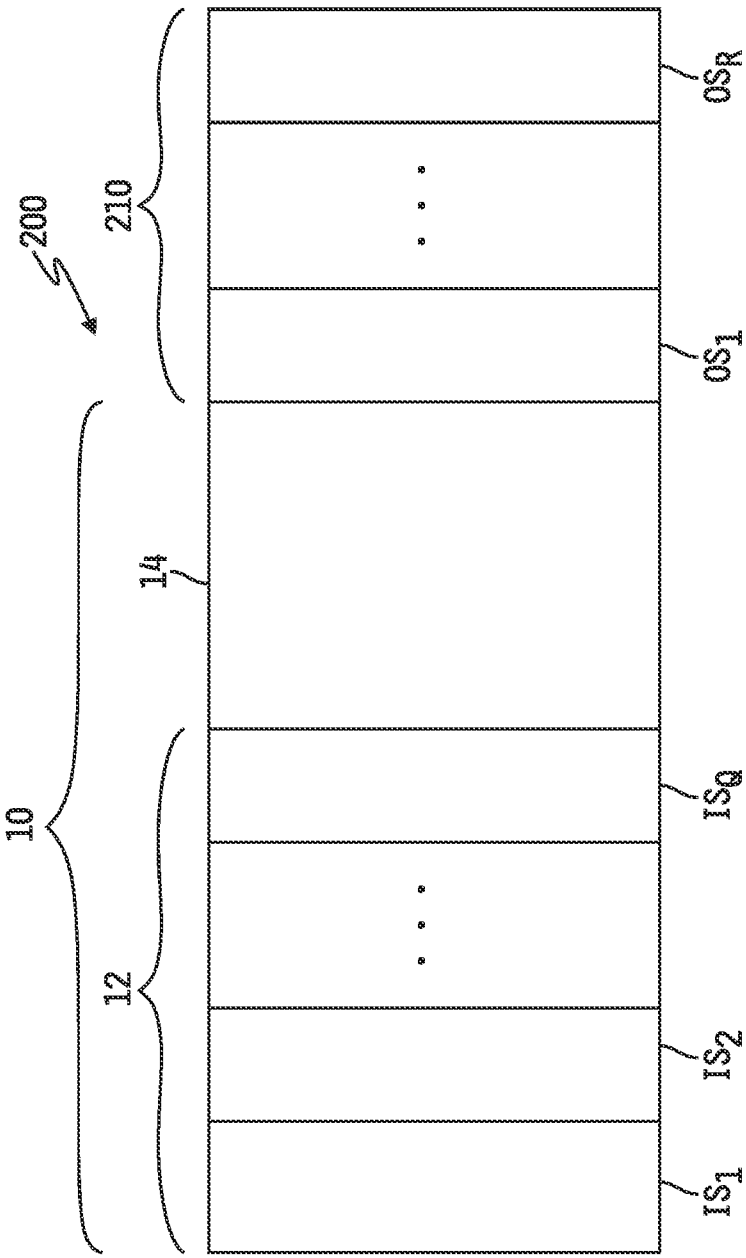
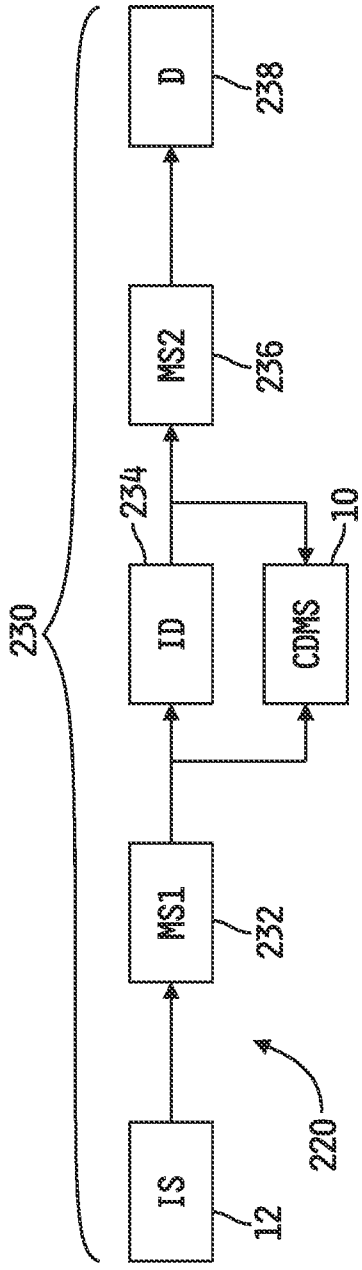

200
210
10
14
12
OS_R
OS_1
IS_Q
IS_2
IS_1

FIG. 8B


230
IS
12
MS1
232
ID
234
MS2
236
D
238
CDMS
10
220

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2019/013280

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01J49/42
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DAVID Z. KEIFER ET AL: "Charge detection mass spectrometry: weighing heavier things", THE ANALYST, vol. 142, no. 10, 1 January 2017 (2017-01-01), pages 1654-1671, XP055546909, UK ISSN: 0003-2654, DOI: 10.1039/C7AN00277G page 1657 - page 1661; figures 2a, 2b	1-59

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 March 2019	05/04/2019

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Peters, Volker

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