(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
11 October 2001 (11.10.2001)

PCT

(10) International Publication Number
WO 01/76071 A3

(51) International Patent Classification[7]: H03K 19/003, 19/00

(21) International Application Number: PCT/US01/07395

(22) International Filing Date: 8 March 2001 (08.03.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/539,289 30 March 2000 (30.03.2000) US

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(81) Designated States *(national)*: CN, JP, KR.

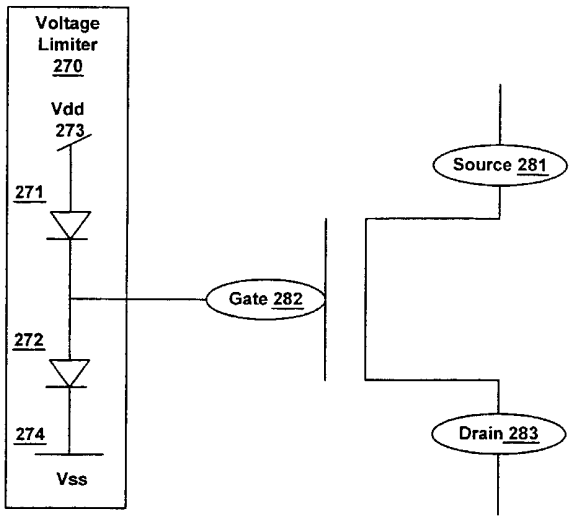
(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *with international search report*

(88) Date of publication of the international search report:
31 January 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: HIGH VOLTAGE CMOS SIGNAL DRIVER SYSTEM AND METHOD



(57) Abstract: The system and method facilitates the transmission of relatively high voltage signals via a thin oxide gate CMOS device without an excessivelydetrimental electric field build up across the thin oxide layers forming a gatein a CMOS device. The high voltage CMOS thin oxide gate system andmethod provides a degradation repression bias voltage signal to the thin oxide gate of the CMOS device. The degradation repression bias voltage signal establishes a differential voltage potential between the source and draincomponents of the thin oxide gate output CMOS device and the gate component of the thin oxide gate output CMOS device. The degradation repression bias voltage signal is maintained at a level that prevents that excessively detrimental electric field stresses are not induced in oxide layersthat form the thin oxide gate in the output CMOS device. The System and method does not require additional power supplies or reference voltages and does not cause the thin gate oxide device to dissipate additional power in a static (non-switching) state.

WO 01/76071 A3

INTERNATIONAL SEARCH REPORT

Inte. ional Application No
PCT/US 01/07395

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03K19/003 H03K19/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 465 054 A (ERHART RICHARD A) 7 November 1995 (1995-11-07) column 8, line 27 -column 11, line 8; figure 4 ---	1-5,11, 15,17-19
A	US 5 528 190 A (HONNIGFORD EDWARD H) 18 June 1996 (1996-06-18) column 1, line 46 - line 61 column 2, line 63 -column 6, line 38; figures 1-3 ---	1,11,15
A	US 5 815 354 A (BRACERAS GEORGE MARIA ET AL) 29 September 1998 (1998-09-29) column 2, line 50 -column 4, line 8; figures 1,2 ---	1,11,15

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
3 October 2001	12/10/2001

Name and mailing address of the ISA	Authorized officer
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2

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

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PCT/US 01/07395

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 986 472 A (HINEDI FAHD ET AL) 16 November 1999 (1999-11-16) column 4, line 65 -column 5, line 11; figures 1,2	1,11,15

INTERNATIONAL SEARCH REPORT

Information on patent family members

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PCT/US 01/07395

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