Multi-cell display of the type in which each cell includes electrodes on either side of a layer of display material for applying actuating potential thereacross, for instance a liquid crystal display, which includes a source of chopped DC actuating potential connected to one of the electrodes of each of the cells, and capacitive means in series with each of the cells. Also included are a transistor for each of the cells having its collector emitter terminal connected in a series circuit with the cell and the source of chopped DC potential. The cells are divided into M groups of N cells each and a set of M selectively actuable driving circuits are connected to the transistors of the cells of the corresponding M groups for applying a base-emitter junction saturating potential to the transistors of the cells. A set of N sequentially actuable driving circuits are connected to the transistors of the corresponding cells of each of the M groups for sequentially applying an enabling voltage to the sets of transistors connected thereto for enabling the actuation of the set of M driving circuits to selectively saturate the base-emitter junctions of the successive sets of transistors and for preventing the saturation of the base-emitter junctions of the others of the transistors.

16 Claims, 8 Drawing Figures
DRIVE CIRCUIT FOR A LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

This invention relates generally to multiplexed displays and more particularly to multiplexed liquid crystal and other types of displays which can incorporate large numbers of display elements.

The scanning or multiplexing of large size liquid crystal displays present very difficult problems. These problems are present to some extent in every kind of large scale display, but are made particularly acute by some intrinsic electrical properties of liquid crystal materials.

In large-scale multiplex displays it is usually possible to distinguish three main parts: row drivers, column drivers and the display panel. The row and column drivers are the sources of whatever wave forms are needed to operate the elements of the display panel.

In order to be driven in a multiplex mode the elements of the display panel should possess a threshold voltage so they may be selectively addressed by coincident pulses from the row and column drivers and, in order to maximize the brightness and contrast, each element should store the information displayed by it during the time taken to address all the other elements of the display. This time, called the frame time in TV applications, will be indicated as T while the small time during which each element is addressed will be indicated as t. The ratio t/T is called the duty cycle of the multiplex display. When t is very small compared with T the duty cycle is very small and the storage property of the element becomes very important.

In addition to these properties, if the display is to be of commercial interest, the fabrication of the drivers must be amenable to integrated circuit technology, power consumption must be low and there must not be any observable flicker.

A liquid crystal display cell by itself satisfied neither the requirement for a threshold voltage nor that of a storage capability. Therefore in the various schemes so far proposed each element of the liquid crystal display is combined with a variety of other circuit components to achieve the desired performance. For example, each element of a liquid crystal display could be combined with a flip-flop and a driving switch in order to provide the desired storage capability. This scheme, however, is clearly too expensive and therefore impractical. Also, to obtain a long life from the liquid crystal material it is necessary that the display be driven with an AC voltage which further complicates the driving circuitry.

Another of the schemes proposed to date for a multiplex liquid crystal display uses a field effect transistor and a capacitor for each element of the display to provide the desired characteristics. This scheme, however, has several disadvantages in that the capacitor cannot be integrated, the requirements for the electrical characteristics of the field effect transistors are very strict, in that they must have extremely high isolation and minimum parasitic capacitances and the row and column drivers required are very expensive since they must provide voltages which invert their polarity at each frame. Also these voltages are too high for many low power applications.

OBJECTS AND SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an expensive multiplex liquid crystal display.

It is a further object of the invention to provide a multiplexed liquid crystal display capable of operating with a very small duty cycle.

It is a further object of the invention to provide an improved multiplex liquid crystal in which the liquid crystal is driven with an alternating current while the applied voltages are DC.

In accordance with these and other objects of the invention, applicant provides a multiplex driving circuit for a multicell display which includes a source of chopped DC actuating potential connected to one of the electrodes of each of the cells, capacitive means in series with each of the cells, and a transistor for each of the cells, each cell, corresponding capacitive means and collector-emitter terminals of the corresponding transistor being connected in a series circuit with the source of chopped DC actuating potential. Also provided are a set of M selectively actuable driving circuits connected to the transistors of the cells of the corresponding M group for applying base-emitter junctions saturating pulses to the transistors of the cells of the corresponding groups and a set of N sequentially actuable driving circuits connected to the transistors of the corresponding cells of each of the M groups for sequentially applying a base-emitter junction enabling voltage to the successive sets of transistors connected thereto in order to enable the actuation of said M driving circuits to selectively saturate the base-emitter junctions of the successive sets of transistors and for preventing the saturation of the base-emitter junctions of the other of the transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic diagram of a simplified equivalent circuit of an elemental display cell driving circuit according to the invention.

FIG. 2 is a schematic diagram of the circuit of FIG. 1 when the transistor is on.

FIG. 3 is a schematic diagram of the circuit of FIG. 1 when the voltage across the collector-emitter junction of the transistor is reversed.

FIG. 4 is an edge view of a display cell according to the invention.

FIG. 5 is a schematic diagram of a multiplexed display according to the invention.

FIG. 6 is a front view of a multicharacter F segment display which can be driven in accordance with the invention.

FIG. 7 is an edge view of a multiplexed display according to the invention.

FIG. 8 is a schematic diagram of one cell of those shown in FIG. 5.

DETAILED DESCRIPTION

Referring to FIG. 1 of the drawings, there is illustrated the elemental circuit of the type connected to each cell of the multicell display according to the invention which allows the multiplex driving or scanning of the display.

For the purposes of the discussion of the electrical properties of the circuit of FIG. 1, the elemental display cell, which is the illustrated embodiment of the invention is made up of a layer of liquid material having electrodes disposed opposite one another on either side thereof, may be shown as an equivalent resistor 11. The resistor 11 is connected in a series circuit with a source 12 of chopped DC voltage, a capacitor 13 and the col-
lector-emitter terminals of bipolar transistor 15. The base of the transistor 15 is connected through a resistor 17 to a selectively actuable source 19 of a relatively high frequency base-emitter junction saturating pulses and the emitter is connected to a point of reference potential, such as ground. The magnitude V of the output of the voltage source 12 should be large enough to activate the display cell represented by the resistor 11, and, for liquid crystal cells should be on the order of 4 to 30 volts depending on the liquid crystal material and type of operation.

When the source 19 is off, both the emitter and base of transistor 15 are at ground so that the transistor 15 is biased off and acts essentially like a diode which, when the collector is positive with respect to the emitter, prevents the flow of current in the series circuit. When the voltage at the collector is negative with respect to that at the emitter, however, the transistor 15 acts as a forward biased diode so that a current flow exists from the emitter to the collector in the series circuit. Since the chopped DC driving voltage of the voltage source 14 varies between 0 and +V, the collector of the transistor never becomes negative with respect to the emitter while the source 19 is off so that the transistor 15 does not conduct and the display cell represented by the resistor 11 is not actuated.

When the source 19 is actuated, it supplies a series of narrow, low magnitude pulses to the base of the transistor 15 in order to saturate the base-emitter junction. Specifically, these pulses may have an amplitude of about 3 volts and a duration of as little as a microsecond or less. A pulse from the source 19 which is applied to the base of the transistor 15 while the chopped DC driving voltage is at +V acts to saturate the base-emitter junction of the transistor 15 so that the transistor 15 becomes impulsively conductive. Since the resistance 11 of the display cell is very high, on the order of megohms for a liquid crystal cell, the collector current of the transistor 15 is very low.

Once the base-emitter junction of the transistor 15 is saturated by a pulse from source 19, the transistor 15 stays on for a much longer time than the length of the driving pulse because of the slow turnover of the transistor 15 under saturation with extremely low collector current. This property of the transistor 15 is very important and coupled with the capacitor 13 allows the multiplexing of the display according to the invention.

In FIG. 2 there is shown a simplified equivalent circuit of the circuit of FIG. 1 during the period when the emitter-base junction of transistor 15 is saturated by a pulse from source 19 and the voltage from source 14 is at +V. During this time a current flows in the circuit in the direction indicated by the arrow 21 which current charges the capacitor 13 in the polarity shown. If the base-emitter junction saturating pulses from the source 19 are spaced close enough to one another, the transistor 15 remains conducting through the entire half cycle of the source 14 during which the driving voltage +V is present and the capacitor 13 charges to a voltage +V, which, depending on the value of the capacitor 13, can be very close to +V.

When the output voltage of the source 14 drops to 0 during the second half cycle of the chopped DC, the simplified equivalent circuit of the circuit of FIG. 1 becomes that illustrated in FIG. 3 of the drawings. In this case the change on capacitor 13, built up during the first half cycle of the source 14, causes the collector of the bipolar transistor 15 to become negative with respect to the emitter, thereby causing the transistor to act essentially as a forward biased diode or a short circuit. The capacitor 13 therefore discharges through the display cell, illustrated as the equivalent resistor 11, and a current flows in the resistor 11 in the direction indicated by the arrow 23 which is opposite to the direction of the current in FIG. 2. Thus the display cell is held on by the voltage on the capacitor 13 during the second half cycle of the driving voltage source 14 and AC current exists in the display cell. The existence of the AC current in the cell is extremely important since liquid crystal cells operating with AC driving inherently have much longer lives than those which are driven by DC currents.

For nematic liquid crystal displays operating in the dynamic scanning mode, it has been found desirable, in order to charge the capacitor 13 completely, to drive the base of the transistor 15 with at least five pulses during the charging half period of the source 14. Thus if the frequency of the voltage source 14 is 40 Hz, the minimum frequency to drive the base should be on the order of 200 Hz. By using a slower frequency for the voltage source 14, the minimum desirable frequency for the base drive can be as low as 100 Hz.

For liquid crystal displays operating in the twisted nematic or field effect, mode, it is possible to drive the base of the transistor 15 with a smaller number of pulses during the charging half cycle of the source 14. Satisfactory displays of this type have been fabricated in which only one or two pulses are applied to the base of the transistor 14 during the charging half cycle of the source 14. This is thought to be because of the much lower current levels experienced in a liquid crystal display operating in the twisted nematic mode relative to one operating in the dynamic scanning mode.

As stated above, the base-emitter junction saturation current from the source 19 can be as narrow as 1 microsecond or less. Thus, if the frequency of the source 14 is 40 Hz, and if the base of the transistor 15 is actuated by 1 microsecond pulses spaced by distances of 1 milisecond, it would be equivalent to a multiplex circuit having a duty cycle of 1/1000 with 12 base-emitter junction saturation pulses being present during each charging half period of the chopped DC display driving voltage. Under these conditions the display cell is fully on when actuated by the pulses to the base of the transistor 15.

A particular advantage of the multiplex circuit according to the invention is that, at least for liquid crystal displays, the capacitor connected in series with the display element may be included within the display itself in the manner illustrated in FIG. 4 of the drawings. FIG. 4 shows an edge view of a cell of a display, in this case a liquid crystal display, according to the invention. A layer of liquid crystal material 25 is confined between a pair of substrates 27 and 29. Opposite one another on the internal faces of the substrates 27 and 29 are deposited electrodes 31 and 33 which are used for applying an actuating voltage across the liquid crystal material therebetween. In order to incorporate the series capacitor within the cell, applicant deposits a layer of dielectric material 35 over the electrode 31. In this way a capacitive element is generated having its plates formed by the electrode 31 and the portion of the liquid crystal material 25 in contact with the dielectric layer 35. The resistivity of the dielectric material 35 is
preferable at least in order of magnitude higher than that of liquid crystal material 25.

The value of the capacitor generated by the dielectric layer 35 depends on the dielectric constant and the thickness of the dielectric layer 35 and is preferably on the order of 500 picofarads for the multiplexing of nematic liquid crystal displays operating in the dynamic scattering mode. The dielectric layer 35 may be made of any good dielectric material which does not react with the liquid crystal material. SiO, SiO2, Al2O, barium titanate, tantalum oxide, mylar, teflon and polyvinylidene fluoride are all suitable. The layer can be deposited by various methods including chemical or chemical processes, spray, evaporation, sputtering, or any other technique of preparing thin films. In addition, the layer may be formed by a thin layer of glass, plastic, or ceramic. The thickness of the layer is not critical. For silicon monoxide, thicknesses on the order of one half a micron to 1/4 microns are preferred. The capacitive layer cannot be too thin since the resulting capacitance becomes too high and the capacitor does not become fully charged during the first half cycle of the driving voltage.

The ability to include the series capacitor within the display element itself is a significant advantage of the multiplex driving circuit according the invention since this capacitor could not otherwise be integrated with present day integrated circuit techniques.

In a matrix display there are generally two types of system organization, one incorporating element-at-a-time addressing and the other incorporating line-at-a-time addressing. With the first system the elements of a display are updated with new information, one-at-a-time in an orderly sequence, once every frame. With line-at-a-time addressing the rows of the display elements are enabled sequentially to receive the successive lines of information from the column drivers which are synchronized with the row drivers. This system requires more complicated column drivers since they must be able to store a full line of information. Line-at-a-time addressing, however, results in the considerably higher duty cycle for a display since the duty cycle is 1/n where n is the number of rows, while element-at-a-time addressing results in a duty cycle of 1/N where N is the number of elements in the display. The multiplexing circuit according to the invention is suitable for either element-at-a-time or line-at-a-time addressing.

Referring to FIGS. 5 and 7 of the drawings there is illustrated a multiplex display according to the invention which will be discussed in terms of a liquid crystal display 36 having a uniform back electrode 37 and a segmented front electrode 39 disposed on either side of a layer of liquid crystal material 41. Each cell of the display 36 is defined by an electrode segment 39 and the portion of a back electrode 37 opposite thereto. A source 43 of chopped DC driving voltage is connected to the back electrode. A capacitive dielectric layer 45 is disposed over each of the electrode segments 39.

For a display 36 operating in the dynamic scattering mode, the frequency of the source 43 should be on the order of from 20 to 200 Hz and the amplitude of the driving voltage +V is on the order of from 15 to 50 volts. For a display 36 operating in the two-nematic mode the frequency of the source 43 should be on the order of 50 to 10 KHz and +V should be on the order of 3 to 15 volts depending on the material and other display parameters.

Each of the segment 39 is connected to the collector of one of the transistors 47 of the transistor matrix 49 shown in FIG. 5. The transistor matrix 49 is illustrated as being a 4 x 4 matrix but, as indicated by the broken row and column bus lines, the matrix can be expanded in either direction to whatever size is desired. Since an edge view of the display 36 is illustrated in FIG. 7, only four electrode segments 39 are shown. It should be understood, however, that the number of electrode segments 39 corresponds in a 1 for 1 relationship to the number of transistors 47 in the matrix 49. The electrode segments 39 may be arranged over the area of the liquid crystal display 36 in whatever arrangement is desired.

The base of each of the transistors 47 is connected to one of the row driving busses 51 and the emitter of each of the transistors is connected to one of the column driving busses 53 as shown in FIG. 8 which illustrates the connections to an individual transistor. Each of the row driving busses 51 is connected through a corresponding resistor 55 to a selectively actuable row driving circuit 57. Each of the column driving busses 53 is connected to one of the column driving circuits 59.

The column driving circuits 59 normally apply a voltage of about +3 volts to the emitters of the transistors 47 connected thereto, thereby biasing them off. The column driving circuits 59 operate sequentially to apply a negative going 3 volt pulse to the emitters of the transistors 47 of the successive columns of the matrix 49 to 0 volts.

The output of the row driving circuits 57 on the other hand are normally at 0 volts and are selectively actuable to apply a positive going 3 volt base-emitter junction saturating pulse to the bases of the transistors 47 connected thereto. When a row driving circuit 57 applies a pulse to a transistor 47 whose emitter is being held at +3 volts by a corresponding column driving circuit 59, the transistor 47 remains off and the corresponding cell of the display is not actuated. If, however, a row driving circuit 57 applies positive going 3 volt pulse to a transistor 47 whose emitter is connected to a column circuit 59 whose output is at 0 volts, the base-emitter junction of the transistor 47 becomes saturated and, if the chopped DC driving voltage source 43 is applying a voltage +V to the back electrode 37 of the display 36, the transistor 47 becomes impulsively conductive.

As explained in relation to FIGS. 1 through 3, a transistor 47 whose base-emitter junction is saturated by the coincidence of pulses from the corresponding row and column drivers 57 and 59, remains conductive for a much longer time than the width of the pulse applied to the base. As stated above, for a dynamic scattering display, if five or more coincident row and column pulses are applied to the transistor 47 during each half cycle of the driving voltage source 43, the corresponding display cell is fully actuated in the manner described in relation to FIGS. 1 through 3. Only one or two coincident row and column pulses are needed for each half cycle of a twisted nematic liquid crystal display.

For element-at-a-time operation, the column driving circuits 59 can be actuated in sequence to enable the transistors 47 in the successive columns of the matrix 49 to be turned on selectively by pulses from the row driving circuits 57. The row driving circuits 57 are op-
erated in a selective sequential manner synchronized with the column driving circuits 59. Thus the row driving circuit 57 for the first row of the matrix 49 selectively applies a series of energizing pulses to the row bus 51 of the first row for selectively energizing the successive transistors 47 of the first row in synchronism with the application by the column driving circuits 59 of enabling signals to the successive column buses 53. Subsequently the row driving circuits 57 of the second row of the matrix 49 selectively applies a series of pulses to the row bus 51 of the second row in synchronism with the next sequence of column enabling pulses generated by the column driving circuits 59.

This process is repeated for each row of the matrix 49 until each element of the display has been selectively energized, after which the cycle is repeated, started with the transistor 47 connected to the first row and column of the matrix 49. The duty cycle for a display operating in this mode is 1/N where N is equal to the number of elements in the display. As stated above, duty cycles lower than 1/1000 are easily obtainable with the driving circuit according to the invention.

For row-at-a-time operation (in this case column-at-a-time operation) the column driving circuits 59 are operated sequentially while the row driving circuits 57 are operated in parallel in synchronism with the column driving circuits 59 to selectively energize the transistors 47 of the successive columns of the matrix 49. In this case the duty cycle is 1/n where n is equal to the number of columns in the matrix 49.

It should be apparent that it is equally possible to energize the matrix 49 with sequentially operable row driving circuits 57 and selectively actuable column driving circuits 59.

In FIG. 6 of the drawings there is illustrated a multi-character numeric display which can be driven in a multiplex manner according to the invention. Each character of the display includes a seven segment electrode 61 on one substrate and a back electrode 63 on the other substrate. A capacitive layer of dielectric material (not shown) may be deposited over either the segmented electrodes 61 or the back electrodes 63. In order to drive this display according to the invention the back electrodes 63 are connected to a source of chopped DC actuating potential while the segmented electrodes 61 are individually connected to the collectors of transistors connected in a matrix such as that discussed above in relation to FIG. 5. Such a matrix could conveniently have seven rows which are connected to seven selectively actuable row driving circuits and a number of columns equal to the number of digits in the display. Each of the columns is connected to a separate sequentially operable column driving circuit.

Although the multiplex displays of the invention have been described largely in relation to liquid crystal displays, the driving system according to the invention can also be used for other types of displays, such as suspended crystal displays, for which its characteristics are suited. Furthermore, the term transistor as used in this specification should be interpreted to refer to any electronic component in which a flow of current between two terminals may be controlled by a current or voltage at a third terminal and in which, for the current level needed to drive the display element, the current continues to flow between the two terminals for a period of time after the excitation is removed from the third termi

and which component is operable at the voltage and current levels appropriate for the particular type of display.

By a bipolar transistor is meant one which acts as a switch controlled by the base when the collector-emitter current is in the forward direction (e.g. from collector to emitter for a NPN transistor) and as a forward biased diode when the collector-emitter current is in the reverse direction. Other types of transistors, such as MOS transistors, which do not act as a forward biased diode in the reverse direction, may also be made to act like a bipolar transistor if, for instance, a diode is connected in parallel with it to allow current flow in the reverse direction.

I claim:

1. In a display including a plurality of display cells, each of the type actuable by a potential applied across display material between a pair of electrodes and wherein said cells are arranged in M groups of N cells, a driving circuit for multiplexing the cells comprising:
a source of chopped DC actuating potential; capacitive means for each of said cells; a transistor for each of said cells, each of said transistors having a base terminal, an emitter terminal and a collector terminal, said collector terminal connected in series with said capacitive means and said source of chopped DC potential, wherein the collector terminal of each transistor is connected to its associated capacitive means and wherein each transistor enables current flow in one direction between the emitter and collector thereof in response to simultaneous pulses applied to said base and emitter thereof;
as a set of M selectively actuable driving circuits each connected to the base of the transistor of each cell of the corresponding group for applying base-emitter junction saturating pulses to the transistors of the cell of at least one of the M groups; and a set of N sequentially actuable driving circuits each connected to the emitter of one transistor in each of the M groups for sequentially applying base-emitter junction enabling pulses to the successive sets of transistors connected thereto for enabling the selective actuation of said set of M driving circuits to saturate said base emitter junction of said successive groups of transistors and for preventing the saturation by said M driving circuits of the base-emitter junction of the transistors of the others of said groups.

2. A display according to claim 1 wherein said capacitive means for each of said cells includes a layer of dielectric material deposited over one of said electrodes.

3. A display, according to claim 1 wherein said transistor for each of said cells comprises a bipolar transistor, said cell and corresponding capacitive means being connected in the collector of said bipolar transistor.

4. The display of claim 1 wherein said display material includes a dynamic scattering type of liquid crystal material and wherein the multiplex driving circuit operates in an element-at-a-time mode, the frequency of the base-emitter junction saturating pulses selectively applied to the transistors by each of said M selectively actuable driving circuits being equal to at least 10 times the frequency of said chopped DC actuating potential divided by the duty cycle of the display.
5. The display of claim 3 wherein each of said M selectively actuable driving circuits applies a set of N pulses to the transistors connected thereto in synchronism with the sequential application of a set of N enabling pulses to the successive of transistors connected to each of said M selectively actuable driving circuits by said set of N sequentially actuable driving circuits, said set of M driving circuits operating sequentially to selectively apply sets of N pulses to the transistors connected to the successive groups of N cells.

6. The display of claim 5 wherein said display material includes dynamic scattering type liquid crystal material and wherein said set of pulses generated by each of said M selectively actuable driving circuits have a frequency of at least 10 times the frequency of said chopped DC actuating potential divided by the duty cycle of the display.

7. The display of claim 3 wherein said set of M selectively actuable driving circuits are synchronized with one another and with said set of N sequentially actuable driving circuits for selectively actuating in parallel the successive sets of corresponding cells of each of the M groups of cells.

8. The display of claim 7 wherein said display material includes dynamic scattering type liquid crystal material and wherein the frequency of the pulses applied by said set of M selectively actuable driving circuits and said sets of N sequentially actuable driving circuits is equal to at least 10 times the frequency of said chopped DC actuating potential divided by N times the duty cycle of the display.

9. The display of claim 1 wherein said electrodes are disposed opposite one another on either side of said portion of a layer of display material and wherein said capacitive means includes a layer of dielectric material deposited over one of said electrodes.

10. In a display including a plurality of display cells, each of the type actuable by a potential applied across display material between a pair of electrodes and wherein said cells are arranged in M groups of N cells, a driving circuit for multiplexing the cells comprising:

a. a source of chopped DC actuating potential;

b. a capacitive means for each of said cells;

c. transistor means for each of said cells, each of said transistor means having a pair of current carrying terminals, one terminal of said pair of terminals connected in series with its associated capacitive means and said source of chopped DC potential with said one terminal connected to the capacitive means, a third terminal for controlling the current at said pair of terminals, and wherein the application of a voltage in a predetermined range to said third terminal prevents current flow in one direction through said pair of terminals;

d. a set of M selectively actuable driving circuits connected to the transistor means of the cells of the corresponding M groups for selectively applying actuating pulses to said third terminal of the transistor means of the cells of the corresponding groups; and

e. a set of N sequentially actuable driving circuits connected to the transistor means of the corresponding cells of each of the M groups for sequentially applying enabling pulses to the successive sets of transistor means connected thereto for enabling the selective actuation of said set of M driving circuits to selectively apply a voltage outside of said predetermined range to said third terminals of said successive groups of transistor means for rendering said transistors impulsive conductive and for holding the voltage at the third terminal of the others of said transistor means within said predetermined range.

11. The display of claim 10 wherein said transistor means comprises a bipolar transistor.

12. A circuit for driving a display cell of the type having display material between a pair of electrodes and actuable by a potential thereacross during use, the circuit comprising:

a. first means for developing a first chopped DC actuating potential signal;

b. capacitive means associated with the display cell and connected in series with said first means;

c. transistor means having a pair of current carrying terminals, one of said pair of terminals connected in series with said first means and said capacitive means with said one terminal connected to said capacitive means, a third terminal and said transistor means responsive to the simultaneous application of switching signals at the other of said pair of terminals and the third terminal for enabling current flow in one direction through said pair of current carrying terminals;

d. second means for applying a second switching signal to said third terminal; and

e. third means for selectively applying a third switching signal to said other terminal simultaneously with the application of said second signal to said third terminal.

13. A circuit according to claim 12, wherein said transistor means comprises a bipolar transistor.

14. A circuit for driving a plurality display cells disposed in M groups of N cells, each cell of the type having display material between a pair of electrodes and actuable by a potential thereacross during use, the circuit comprising:

a. first means for developing a first chopped DC actuating potential signal;

b. a plurality of capacitive means, each associated with one of the cells;

c. a plurality of transistor means, each associated with one cell and each having a pair of current carrying terminal, one terminal of said pair of terminals connected in series with said first means and the corresponding one of said capacitive means with said one terminal connected to said corresponding capacitive means, a third terminal and each transistor means responsive to the simultaneous application of switching signals at the other of said pair of terminals and the third terminal for enabling current flow in one direction through said pair of current carrying terminals;

d. a set of M second means each for selectively applying a second switching signal to the third terminal of one group of N transistor means; and

e. a set of N third means for sequentially applying third switching signals to successive groups of M other terminals simultaneously with the application of at least one second signal to the third terminal of one group of N transistor means, whereby successive groups of at least one transistor means are enabled to permit current flow in one direction
through the current carrying terminals to drive a corresponding display cell.

15. A circuit according to claim 14, wherein each of said transistor means comprises a bipolar transistor.

16. A circuit according to claim 15, wherein each of said capacitive means includes a layer of dielectric material deposited over one of the electrodes of one cell.