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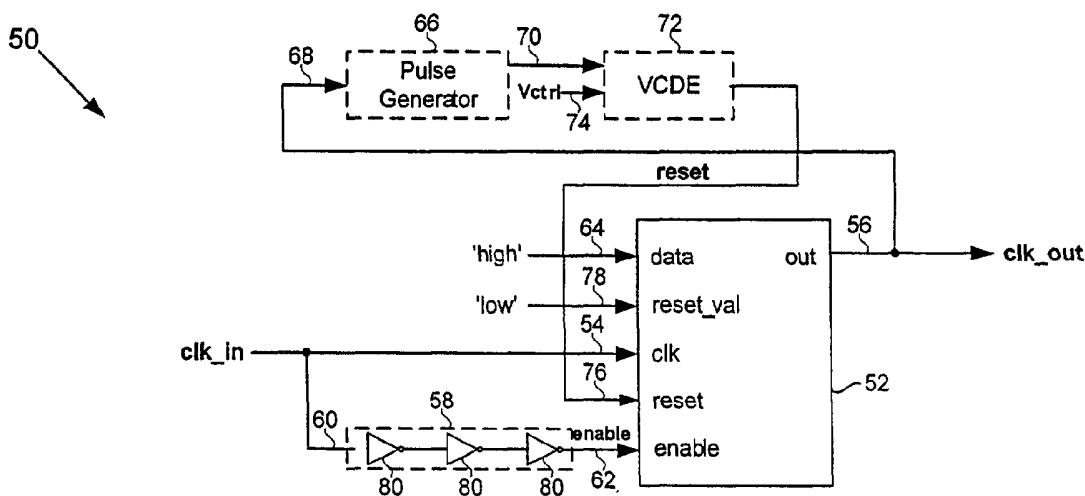
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(54) Title: FREQUENCY MULTIPLIER



(57) Abstract: A frequency multiplier design that uses a flip-flop to output (1) a first edge on an output clock signal upon receipt of a first transition of an input clock signal and (2) a second edge on the output clock signal before receipt of a second transition of the input clock signal is provided. The frequency multiplier design uses circuitry dependent on the output clock signal to reset the flip-flop after some delay but before the second transition of the input clock signal, wherein the resetting of the flip-flop causes the flip-flop to output the second edge on the output clock signal.

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FREQUENCY MULTIPLIER

Background of Invention

[0001] As shown in Figure 1, a typical computer system **10** has, among other components, a microprocessor **12**, one or more forms of memory **14**, integrated circuits **16** having specific functionalities, and peripheral computer resources (not shown), e.g., monitor, keyboard, software programs, etc. These components communicate with one another via communication paths **19**, e.g., wires, buses, etc., to accomplish the various tasks of the computer system **10**.

[0002] In order to properly accomplish such tasks, the computer system **10** relies on the basis of time to coordinate its various operations. To this end, a crystal oscillator **18** generates a system clock signal **sys_clk** (also referred to in the art as “reference clock”) to various parts of the computer system **10**. However, modern microprocessors and other integrated circuits typically operate at frequencies significantly higher than that of the signals most crystal oscillators can provide, and accordingly, designers often implement various techniques to increase or multiply the frequency of the system clock signal to particular computer system components.

[0003] For example, as shown in Figure 1, because the microprocessor **12** is able to operate at frequencies higher than that of the system clock signal **sys_clk**, a phase locked loop **22** is often used to output a chip clock signal **chip_clk** to the microprocessor **12**, in which case, the chip clock signal **chip_clk** has a frequency that is significantly higher than that of the system clock signal **sys_clk**. However, in some circumstances, although frequency multiplication may be needed, implementation of a complex clock generator, such as the phase locked loop **22** shown in Figure 1, may prove to be difficult or too costly in terms of space and design time.

[0004] To this end, integrated circuit designers have implemented various simpler

frequency multiplier designs, one of which is shown in Figure 2. In Figure 2, an exclusive-OR gate 30 has a first input 32 operatively connected to a first clock signal **clk_in** and an output 34 operatively connected to a second clock signal **clk_out**. A delay chain 38 formed by a series inverters 40 has an input 42 operatively connected to the first clock signal **clk_in** and an output operatively connected to a second input 44 of the exclusive-OR gate 30.

[0005] Figure 3 shows a timing diagram in accordance with the typical frequency multiplier design shown in Figure 2. The timing diagram shows clock waveforms for the first clock signal **clk_in** (at the first input 32 of the exclusive-OR gate 30 shown in Figure 2), the second input 44 of the exclusive-OR gate 30 shown in Figure 2, and the second clock signal **clk_out** (at the output 34 of the exclusive-OR gate 30 shown in Figure 2).

[0006] As shown in Figure 3, the clock waveform at the second input 44 is delayed with respect to the clock waveform of the first input 32 (due to the delay of the delay chain 38 shown in Figure 2). Because the exclusive-OR gate 30 outputs 'high' when its inputs are different, and because the clock waveforms at the first input 32 and the second input 44 are different after each rising and falling edge for a period of time less than half a clock waveform cycle at the first input 32 (and at the second input 44), the clock waveform for the output 34 of the exclusive-OR gate 30, i.e., the second clock signal **clk_out**, has a frequency twice that of the first clock signal **clk_in**.

Summary of Invention

[0007] According to one aspect of the present invention, an integrated circuit comprises a flip-flop with a clock input operatively connected to a first clock signal and an output operatively connected to a second clock signal, a pulse generator with an input operatively connected to the second clock signal, and a voltage controlled delay element with an input operatively connected to an output

of the pulse generator and an output operatively connected to a reset input of the flip-flop.

[0008] According to another aspect, an integrated circuit comprises flip-flop means for inputting a first transition of a first clock signal and outputting a first type of edge on a second clock signal upon receipt of the first transition, and means for resetting the flip-flop means before the flip-flop means inputs a second transition of the first clock signal, where the flip-flop means outputs a second type of edge on the second clock signal dependent on the means for resetting the flip-flop means.

[0009] According to another aspect, a method for multiplying a frequency of a first clock signal comprises generating a first type of edge on a second clock signal upon receipt of a first transition of the first clock signal, generating a pulse dependent on the first type of edge, delaying the pulse, and generating a second type of edge on the second clock signal upon receipt of the pulse.

[0010] Other aspects and advantages of the invention will be apparent from the following description and the appended claims.

Brief Description of Drawings

[0011] Figure 1 shows a typical computer system.

[0012] Figure 2 shows a typical frequency multiplier design.

[0013] Figure 3 shows a timing diagram in accordance with the typical frequency multiplier design shown in Figure 2.

[0014] Figure 4 shows a frequency multiplier design in accordance with an embodiment of the present invention.

[0015] Figure 5 shows a pulse generator in accordance with the embodiment shown in Figure 4.

[0016] Figure 6 shows a voltage controlled delay element in accordance with the embodiment shown in Figure 4.

[0017] Figure 7 shows a timing diagram in accordance with the embodiment shown in Figure 4.

Detailed Description

[0018] Embodiments of the present invention relate to a frequency multiplier design that uses a flip-flop to output (1) a first edge on an output clock signal upon receipt of a first transition of an input clock signal and (2) a second edge on the output clock signal before receipt of a second transition of the input clock signal. The frequency multiplier design uses circuitry dependent on the output clock signal to reset the flip-flop after some delay but before the second transition of the input clock signal, wherein the resetting of the flip-flop causes the flip-flop to output the second edge on the output clock signal.

[0019] Figure 4 shows a frequency multiplier **50** in accordance with an embodiment of the present invention. The frequency multiplier **50** uses a flip-flop **52** that has a clock input **54** operatively connected to a first clock signal **clk_in** and an output **56** operatively connected to a second clock signal **clk_out**. Moreover, the frequency multiplier **50** uses a delay chain **58** that has an input **60** operatively connected to the first clock signal **clk_in** and an output operatively connected to an edge enable signal **enable** that is operatively connected to an edge enable input **62** of the flip-flop **52**. Depending on the edge enable input **62**, the flip-flop **52** is triggered by either a rising (positive) edge or a falling (negative) edge at the clock input **54**.

[0020] When the clock input **54** is triggered by a first transition on the input clock signal **clk_in**, the flip-flop **52** outputs a rising (positive) edge on the second clock signal **clk_out** due to the flip-flop's **52** data input **64** being operatively connected

to 'high.' Those skilled in the art will note that, in one or more other embodiments, the flip-flop 52 may be arranged to output a falling (negative) edge on the second clock signal **clk_out** by operatively connecting the flip-flop's 52 data input 64 to 'low.'

[0021] Still referring to Figure 4, the frequency multiplier 50 uses a pulse generator 66 that has an input 68 operatively connected to the second clock signal **clk_out**. The pulse generator 66 is used to produce a pulse dependent on the second clock signal **clk_out**. A more detailed description of the pulse generator 66 is given below with respect to Figure 5.

[0022] The pulse generator 66 has an output 70 operatively connected to a voltage controlled delay element (VCDE) 72 that delays the passage of the pulse produced by the pulse generator 66. In the embodiment shown in Figure 4, the amount of delay is dependent on a voltage control input, **Vctrl** 74, to the voltage controlled delay element 72. However, those skilled in the art will understand that the voltage controlled delay element 72 may be arranged to have a delay not dependent on such a voltage control input. A more detailed description of the voltage controlled delay element 72 is given below with respect to Figure 6.

[0023] The voltage controlled delay element 72 outputs the delayed pulse on a reset signal **reset** that is operatively connected to an output of the voltage controlled delay element 72. The reset signal **reset** is operatively connected to a reset input 76 of the flip-flop 52, and thus, when the voltage controlled delay element 72 outputs the delayed pulse on the reset signal **reset**, the flip-flop 52 is reset, which, in turn, causes the flip-flop 52 to output a falling (negative) edge on the second clock signal **clk_out** due to the flip-flop's 52 reset value input 78 being operatively connected to 'low.' Those skilled in the art will note that, in one or more other embodiments, the flip-flop 52 may be arranged to output a rising (positive) edge on the second clock signal **clk_out** by operatively connecting the

flip-flop's 52 reset value input 78 to 'high.'

[0024] Before receipt of a second transition of the first clock signal **clk_in**, the delay chain 58, formed by a series of delay elements 80, is arranged to, after some delay, toggle the edge enable input 62 in order to change the type of edge that triggers the flip-flop 52 at the clock input 54. Thus, the flip-flop 52 outputs a 'high' edge on the second clock signal **clk_out** upon receipt of the second transition of the first clock signal **clk_in**. Accordingly, by triggering the flip-flop 52 and outputting a first edge on the second clock signal **clk_out** for every transition of the first clock signal **clk_in**, and by resetting the flip-flop 52 and outputting a second edge on the second clock signal **clk_out** between transitions of the first clock signal **clk_in**, the second output clock signal **clk_out** is controlled to have a frequency twice than that of the first clock signal **clk_in**. An exemplary timing diagram of the frequency multiplier's 50 behavior is shown in Figure 7.

[0025] Those skilled in the art will understand that due to the dual edge triggered and resettable behavior of the flip-flop 52, the flip-flop 52 may be referred to as a "dual edge triggered resettable flip-flop."

[0026] Figure 5 shows an exemplary pulse generator 66 in accordance with the embodiment shown in Figure 4. The pulse generator 66 uses a logic gate 100 that has a first input 102 operatively connected to an input **in** of the pulse generator 66 and an output 104 operatively connected to an output **out** of the pulse generator 66. The pulse generator 66 also uses a delay chain 106, formed by a series of delay elements 108, that has an input 110 operatively connected to the input **in** of the pulse generator 66 and an output operatively connected to a second input 112 of the logic gate 100. Accordingly, for every rising (positive) edge on the input **in**, the pulse generator 66 produces a 'high-going' pulse on the output **out**. The width of the pulse is determined by the delay of the delay chain 106. Those skilled in the

art will understand that, in one or more other embodiments, a different logic gate may be used to produce another type of pulse, e.g., a 'low-going' pulse.

[0027] Figure 6 shows an exemplary voltage controlled delay element 72 in accordance with the embodiment shown in Figure 4. The voltage controlled delay element 72 uses a series of delay elements 114 to delay a signal passing from an input **in** of the voltage controlled delay element 72 to an output **out** of the voltage controlled delay element 72. The voltage controlled delay element 72 also uses a transistor 116 dependent on a control voltage **Vctrl** to slow down or speed up the delay between the input **in** and the output **out**. In addition to being operatively connected to the series of delay elements 114, the transistor 116 is operatively connected to a capacitor 118 that is used to store/dissipate charge. Those skilled in the art will understand that, in one or more other embodiments, other means for regulating the delay between the input **in** and the output **out** may be implemented.

[0028] To exemplify the behavior of the frequency multiplier 50 shown in Figure 4, Figure 7 shows an exemplary timing diagram in accordance with the frequency multiplier 50 shown in Figure 4. The timing diagram shows waveforms for the first clock signal **clk_in** (at the clock input 54 of the flip-flop 52 shown in Figure 4), the second clock signal **clk_out** (at the output 56 of the flip-flop 52 shown in Figure 4), the reset signal **reset** (at the reset input 76 of the flip-flop 52 shown in Figure 4), and the edge enable signal **enable** (at the edge enable input 62 of the flip-flop 52 shown in Figure 4).

[0029] Referring to Figure 7 and assuming that the flip-flop (52 in Figure 4) is initially in a rising (positive) edge triggered state, when a rising (positive) edge 82 occurs on the first clock signal **clk_in**, the flip-flop (52 in Figure 4) outputs a rising (positive) edge 84 on the second clock signal **clk_out**. Based on this rising (positive) edge 84 on the second clock signal **clk_out**, the pulse generator (66 in Figure 4) and the voltage controlled delay element (72 in Figure 4) produce a

pulse **86** on the reset signal **reset**. This pulse **86** on the reset signal **reset**, which is operatively connected to the reset input (**76** in Figure 4), resets the flip-flop (**52** in Figure 4), which, in turn, causes the flip-flop (**52** in Figure 4) to output a falling (negative) edge **88** on the second clock signal **clk_out**.

[0030] Before a falling (negative) edge **90** occurs on the first clock signal **clk_in**, the delay chain (**58** in Figure 4) toggles **91** the edge enable signal **enable**, which, in turn, causes the flip-flop (**52** in Figure 4) to go to a falling (negative) edge triggered state. Accordingly, upon receipt of a falling (negative) **90**, the flip-flop (**52** in Figure 4) outputs a rising (positive) edge **92** on the second clock signal **clk_out**. Based on this rising (positive) edge **92** on the second clock signal **clk_out**, the pulse generator (**66** in Figure 4) and the voltage controlled delay element (**72** in Figure 4) produce a pulse **94** on the reset signal **reset**. This pulse **94** on the reset signal **reset**, which is operatively connected to the reset input (**76** in Figure 4), resets the flip-flop (**52** in Figure 4), which, in turn, causes the flip-flop (**52** in Figure 4) to output a falling (negative) edge **96** on the second clock signal **clk_out** before receipt of the next rising (positive) edge **82** on the first clock signal **clk_in**. Before the next rising (positive) edge **82** occurs on the first clock signal **clk_in**, the delay chain (**58** in Figure 4) toggles **98** the edge enable signal **enable**, which, in turn, causes the flip-flop (**52** in Figure 4) to go back to a rising (positive) edge triggered state. Accordingly, as evident from Figure 5, the frequency of the second clock signal **clk_out** has a frequency twice than that of the first clock signal **clk_in**.

[0031] Advantages of the present invention may include one or more of the following. In one or more embodiments, because a simple frequency multiplier may be used instead of a complicated clock generator, e.g., a phase locked loop, valuable integrated circuit space and design time may be saved.

[0032] While the invention has been described with respect to a limited number of

embodiments, those skilled in the art, having benefit of this disclosure, will appreciate that other embodiments can be devised which do not depart from the scope of the invention as disclosed herein. Accordingly, the scope of the invention should be limited only by the attached claims.

Claims

- [c1] An integrated circuit, comprising:
- a flip-flop with a clock input operatively connected to a first clock signal and an output operatively connected to a second clock signal;
 - a pulse generator with an input operatively connected to the second clock signal; and
 - a voltage controlled delay element with an input operatively connected to an output of the pulse generator and an output operatively connected to a reset input of the flip-flop.
- [c2] The integrated circuit of claim 1, wherein the flip-flop is arranged to cause the second clock signal to have a frequency greater than that of the first clock signal.
- [c3] The integrated circuit of claim 1, further comprising:
- a delay chain with an input operatively connected to the first clock signal and an output operatively connected to an edge enable input of the flip-flop.
- [c4] The integrated circuit of claim 3, wherein the delay chain comprises a series of delay elements.
- [c5] The integrated circuit of claim 3, wherein the delay chain is arranged to toggle the edge enable input between a first transition of the first clock signal and a second transition of the first clock signal.
- [c6] The integrated circuit of claim 1, wherein the flip-flop is a dual edge triggered resettable flip-flop.

- [c7] The integrated circuit of claim 1, wherein the flip-flop is arranged to output a first type of edge on the second clock signal upon receipt of a first transition of the first clock signal, and wherein the flip-flop is arranged to output a second type of edge on the second clock signal before receipt of a second transition of the first clock signal.
- [c8] The integrated circuit of claim 7, wherein generation of the second type of edge is dependent on the reset input.
- [c9] The integrated circuit of claim 7, wherein the flip-flop is arranged to output the first type of edge on the second clock signal upon receipt of the second transition of the first clock signal.
- [c10] The integrated circuit of claim 1, wherein the pulse generator comprises:
a logic gate with a first input operatively connected to the second clock signal; and
a delay chain with an input operatively connected to the second clock signal and an output operatively connected to a second input of the logic gate.
- [c11] The integrated circuit of claim 1, wherein the voltage controlled delay element comprises a delay chain.
- [c12] An integrated circuit, comprising:
flip-flop means for inputting a first transition of a first clock signal and outputting a first type of edge on a second clock signal upon receipt of the first transition; and
means for resetting the flip-flop means before the flip-flop means inputs a second transition of the first clock signal, wherein the flip-flop means outputs a second type of edge on the second clock signal

dependent on the means for resetting the flip-flop means.

- [c13] The integrated circuit of claim 12, wherein the flip-flop means outputs the first type of edge on the second clock signal upon receipt of the second transition.
- [c14] The integrated circuit of claim 12, wherein the means for resetting comprises:
means for generating a pulse dependent on the second clock signal; and
means for delaying the second type of edge on the second clock signal dependent on the pulse.
- [c15] A method for multiplying a frequency of a first clock signal, comprising:
generating a first type of edge on a second clock signal dependent on a first transition of the first clock signal;
generating a pulse dependent on the first type of edge;
delaying the pulse; and
generating a second type of edge on the second clock signal dependent of the pulse.
- [c16] The method of claim 15, further comprising:
generating the first type of edge on the second clock signal dependent on a second transition of the first clock signal.
- [c17] The method of claim 16, wherein generating the second type of edge occurs before receipt of the second transition of the first clock signal.

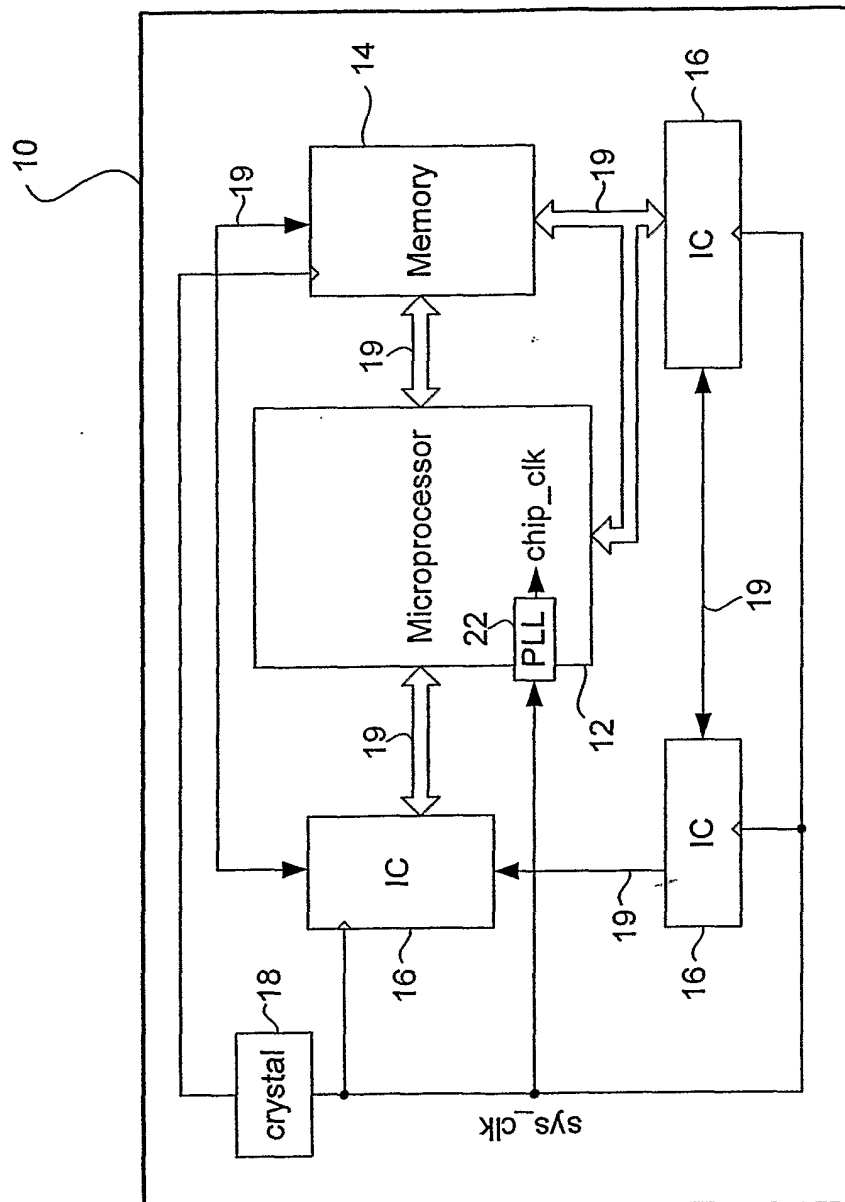


FIGURE 1
(Prior Art)

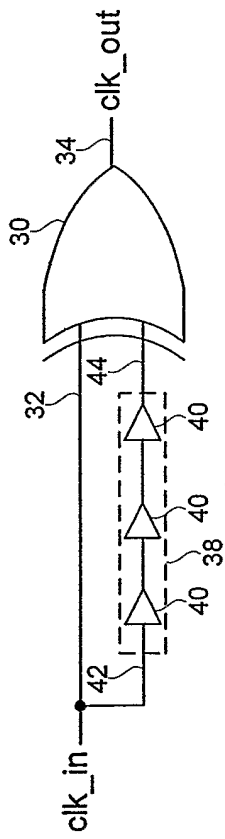


FIGURE 2
(Prior Art)

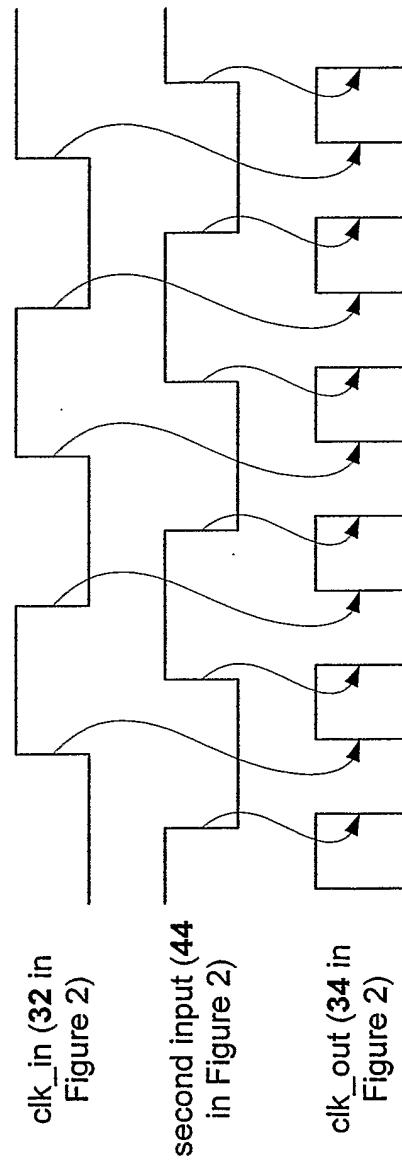


FIGURE 3
(Prior Art)

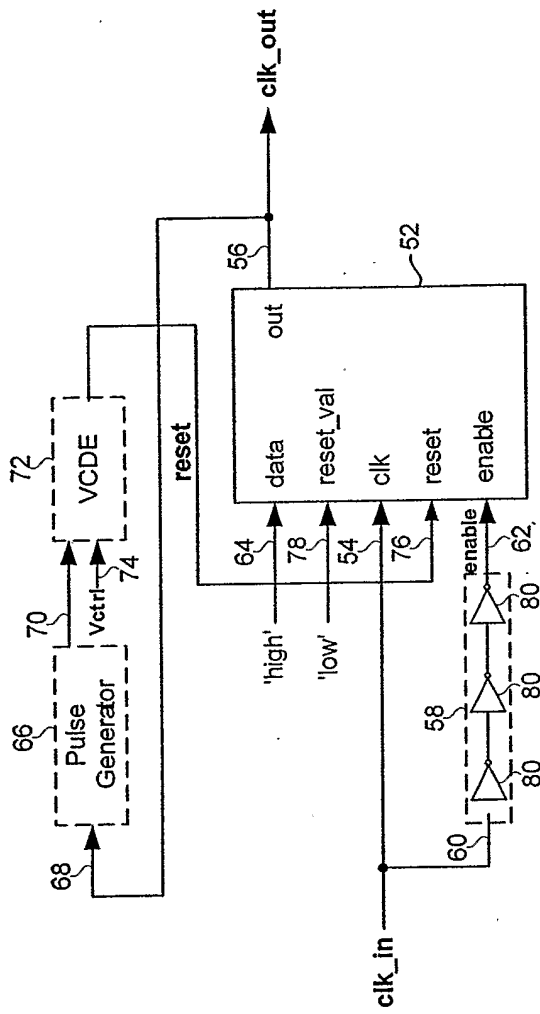


FIGURE 4

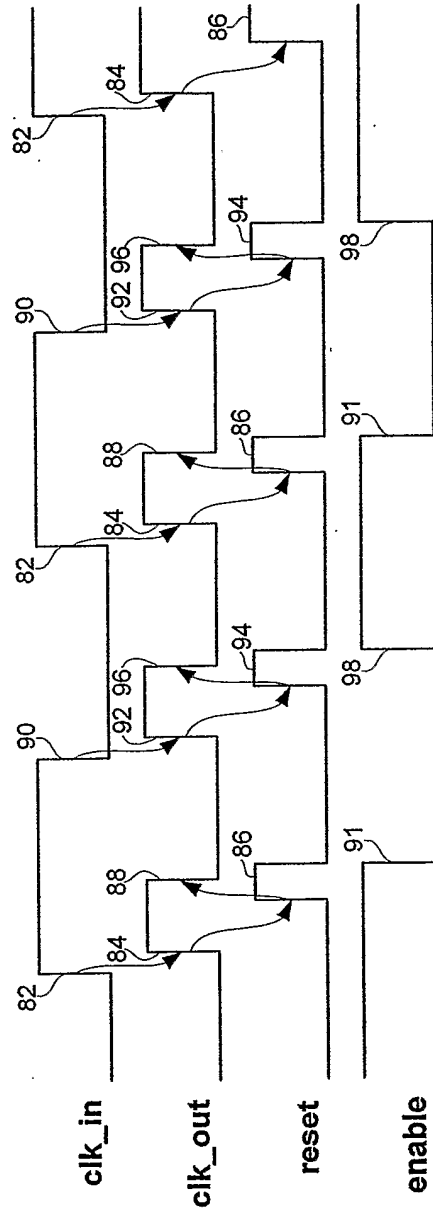


FIGURE 7

50

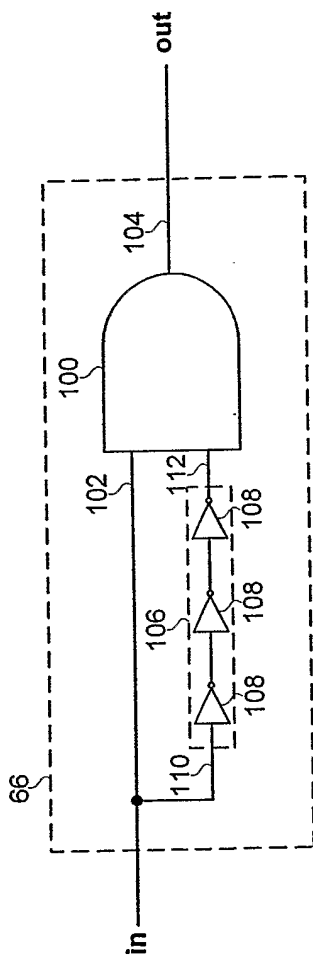


FIGURE 5

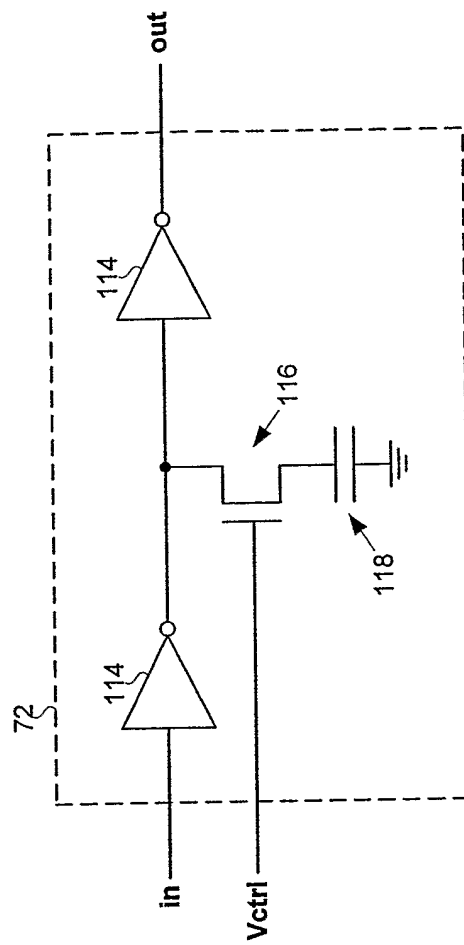


FIGURE 6

INTERNATIONAL SEARCH REPORT

Internati application No
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A. CLASSIFICATION OF SUBJECT MATTER
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According to International Patent Classification (IPC) or to both national classification and IPC

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

WPI Data, EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 121 015 A (NGO DUC) 9 June 1992 (1992-06-09) figure 5 -----	1-4, 12, 15
X	US 6 208 183 B1 (ALI AKBAR ET AL) 27 March 2001 (2001-03-27) figure 3 -----	1, 2, 6, 12, 15
X	EP 0 800 276 A (TOKYO SHIBAURA ELECTRIC CO) 8 October 1997 (1997-10-08) figures 6,6 -----	1, 2, 6, 12, 15
X	EP 0 800 275 A (TOKYO SHIBAURA ELECTRIC CO) 8 October 1997 (1997-10-08) figure 1 -----	1, 2, 6, 12, 15

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Patent family members are listed in annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5121015	A	09-06-1992	NONE
US 6208183	B1	27-03-2001	NONE
EP 0800276	A	08-10-1997	JP 3323054 B2 09-09-2002 JP 9270702 A 14-10-1997 DE 69700270 D1 22-07-1999 DE 69700270 T2 11-11-1999 EP 0800276 A1 08-10-1997 KR 251263 B1 15-04-2000 US 6005420 A 21-12-1999
EP 0800275	A	08-10-1997	JP 3442924 B2 02-09-2003 JP 9270680 A 14-10-1997 EP 0800275 A1 08-10-1997 KR 215625 B1 16-08-1999 US 5955902 A 21-09-1999