

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
25 November 2010 (25.11.2010)

(10) International Publication Number
WO 2010/134026 A4

(51) International Patent Classification:

H01J 37/317 (2006.01)

(21) International Application Number:

PCT/IB2010/052217

(22) International Filing Date:

19 May 2010 (19.05.2010)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

61/179,762 20 May 2009 (20.05.2009) US

(71) Applicant (for all designated States except US): MAP-PER LITHOGRAPHY IP B.V. [NL/NL]; Computerlaan 15, NL-2628XK Delft (NL).

(72) Inventors; and

(75) Inventors/Applicants (for US only): VAN DE PEUT, Teunis [NL/NL]; Galicie 14, NL-3831JD Leusden (NL). WIELAND, Marco Jan-Jaco [NL/NL]; Boeroestraat 23, NL-2612GD Delft (NL).

(74) Agents: MOOIJ, Maarten et al.; Hoyng Monegier LLP, Rembrandt Tower 31st Floor, Amstelplein 1, NL-1096 HA Amsterdam (NL).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,

HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))

Published:

— with international search report (Art. 21(3))
— with amended claims and statement (Art. 19(1))

(88) Date of publication of the international search report: 13 January 2011

Date of publication of the amended claims and statement: 21 April 2011

(54) Title: DUAL PASS SCANNING

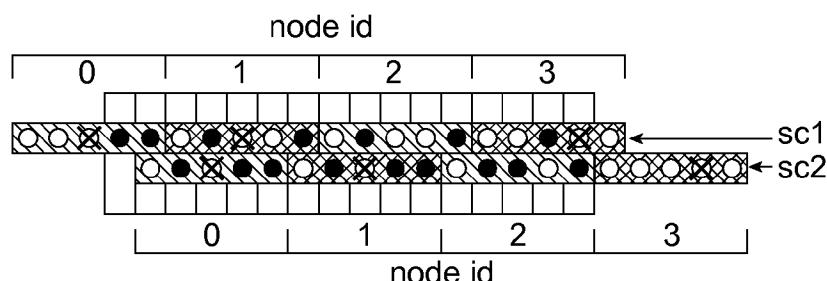


Fig. 15

(57) Abstract: A method for exposing a wafer using a plurality of charged particle beamlets. The method comprises identifying non-functional beamlets among the beamlets, allocating a first subset of the beamlets for exposing a first portion of the wafer, the first subset excluding the identified non-functional beamlets, performing a first scan for exposing the first portion of the wafer using the first subset of the beamlets, allocating a second subset of the beamlets for exposing a second portion of the wafer, the second subset also excluding the identified non-functional beamlets, and performing a second scan for exposing the second portion of the wafer using the second subset of the beamlets, wherein the first and second portions of the wafer do not overlap and together comprise the complete area of the wafer to be exposed.

AMENDED CLAIMS
received by the International Bureau on 05 January 2011 (05.01.11)

1. A method for exposing a wafer using a plurality of charged particle beamlets comprising:
 - identifying non-functional beamlets among the beamlets;
 - allocating a first subset of the beamlets for exposing a first portion of the wafer, the first subset excluding the identified non-functional beamlets;
 - executing an algorithm to determine a first wafer position in conjunction with the allocation of the first subset of beamlets to the first portion of the wafer;
 - moving the wafer to the first position;
 - performing a first scan for exposing the first portion of the wafer using the first subset of the beamlets;
 - allocating a second subset of the beamlets for exposing a second portion of the wafer, the second subset also excluding the identified non-functional beamlets;
 - executing an algorithm to determine a second wafer position in conjunction with the allocation of the second subset of beamlets to the second portion of the wafer;
 - moving the wafer to the second position;
 - performing a second scan for exposing the second portion of the wafer using the second subset of the beamlets;
 - wherein the first and second portions of the wafer do not overlap and together comprise the complete area of the wafer to be exposed, and the first and second subsets of beamlets are substantially equal in size.
2. The method of claim 1, wherein the first and second portions are substantially equal in size.

3. The method of any of the preceding claims, wherein the first and second portions each comprise selected stripes from a plurality of fields of the wafer.
4. The method of any of the preceding claims, wherein identifying the non-functional beamlets comprises measuring the beamlets to identify failed or out-of-specification beamlets.
5. The method of claim 4, wherein measuring the beamlets comprises directing the plurality of beamlets onto a sensor and detecting presence of the beamlets.
6. The method of any of the preceding claims, wherein measuring the beamlets comprises directing the plurality of beamlets onto a sensor and measuring beamlet position.
7. The method of any of the preceding claims, wherein measuring the beamlets comprises scanning the plurality of beamlets onto a sensor and measuring beamlet deflection.
8. The method of any of the preceding claims, wherein measuring the beamlets comprises scanning the plurality of beamlets onto a sensor and measuring beamlet current.
9. The method of any of the preceding claims, wherein the plurality of beamlets are divided into groups, each group of beamlets for exposing a corresponding stripe within each field of the wafer.
10. The method of any of the preceding claims, wherein a position of the wafer with respect to the plurality of beamlets is different at the beginning of the second scan than at the beginning of the first scan.

11. The method of any of the preceding claims, further comprising:
 - calculating a first wafer position of the wafer with respect to the plurality of beamlets;
 - moving the wafer to the first position before beginning the first scan;
 - calculating a second wafer position of the wafer with respect to the plurality of beamlets;
 - moving the wafer to the second position before beginning the second scan;
 - wherein the first position in conjunction with the allocation of the first subset of beamlets to the first portion of the wafer, and the second position in conjunction with the allocation of the second subset of beamlets to the second portion of the wafer, results in the first and second portions being exposed by beamlets of only one of the subsets of beamlets.
12. The method of any of the preceding claims, further comprising executing an algorithm to determine a first position in conjunction with the allocation of the first subset of beamlets to the first portion of the wafer, and a second position in conjunction with the allocation of the second subset of beamlets to the second portion of the wafer, that will result in the first and second portions being exposed by beamlets of only one of the subsets of beamlets.
13. The method of any of the preceding claims, wherein the beamlets are switched on and off by a beamlet blanker array during each scan according to beamlet control data.
14. The method of claim 13, wherein the beamlet control data comprise first beamlet control data for switching the first subset of beamlets during the first scan, and second beamlet control data for switching the second subset of beamlets during the second scan, and wherein the method further comprises transmitting the first beamlet control data to the beamlet blanker array during the first scan and transmitting the second beamlet control data to the beamlet blanker array during the second scan.

15. The method of claim 14, further comprising processing pattern data to generate the beamlet control data, and wherein the second beamlet control data is generated during the first scan.
16. The method of claim 15, wherein processing the pattern data comprises rasterizing the pattern data to generate the beamlet control data, and wherein the rasterizing for the second beamlet control data is performed during the first scan.
17. The method of claim 15, wherein processing the pattern data comprises preparing the beamlet control data for streaming to the beamlet blanker array, and wherein the second beamlet control data is prepared for streaming to the blanker array during the first scan.
18. The method of claim 14, further comprising processing pattern data to generate the beamlet control data, and wherein the first beamlet control data of the next wafer to be exposed is generated during the second scan of the wafer currently being exposed.
19. The method of claim 18, wherein processing the pattern data comprises rasterizing the pattern data to generate the beamlet control data, and wherein the rasterizing for the first beamlet control data of the next wafer to be exposed is performed during the second scan of the wafer currently being exposed.
20. The method of claim 18, wherein processing the pattern data comprises preparing the beamlet control data for streaming to the beamlet blanker array, and wherein the first beamlet control data of the next wafer to be exposed is prepared for streaming to the blanker array during the second scan of the wafer currently being exposed.
21. The method of claim 14, further comprising:

providing a first number of processing units sufficient for processing the pattern data to generate the first beamlet control data;

providing a second number of channels for transmitting the beamlet control data to the beamlet blanker array, each channel transmitting data for a corresponding group of beamlets;

connecting the processing units to the channels corresponding to the first subset of beamlets for exposing the first portion of the wafer;

processing the pattern data in the processing units to generate the first beamlet control data; and

transmitting the first beamlet control data to the beamlet blanker array.

22. The method of claim 14, further comprising:

providing a third number of processing units sufficient for processing the pattern data to generate the second beamlet control data;

providing a fourth number of channels for transmitting the beamlet control data to the beamlet blanker array, each channel transmitting data for a corresponding group of beamlets;

connecting the processing units to the channels corresponding to the second subset of beamlets for exposing the second portion of the wafer;

processing the pattern data in the processing units to generate the second beamlet control data; and

transmitting the second beamlet control data to the beamlet blanker array.

23. The method of claim 18, wherein the first number of processing units is sufficient for processing the pattern data to generate the first beamlet control data and processing the pattern data to generate the second beamlet control data, but not sufficient for processing the pattern data to generate both the first and second beamlet control data at the same time.

24. The method of claim 18, wherein seven processing units are provided for every twelve channels.

25. Lithography system comprising a charged particle optics column including a blanker for generating charged particle beamlets for projection of a pattern onto a target, a target support, said column and target support being moveable relative to one another in the system, the system further comprising a data path for processing and transferring pattern data to a blanker of said column, said blanker arranged capable of switching each of said beamlets on and off in respect of projection on said target, said datapath comprising processing units for processing pattern data into projection data related to a stripe on said target forming a projection area of a beamlet at relative movement of target support and column, said data path thereto comprising channels connected to the blanker for individually controlling a beamlet by said projection data, the system further being provided with a switch for switching connection a processing unit between different channels.

BRIEF STATEMENT UNDER ARTICLE 19 PCT

The claims have been amended to incorporate the subject matter of claim 2 into claim 1, requiring that the first and second subsets of beamlets are substantially equal in size.

D1 (EP 1 523 027) describes a lithography system in which defective beams are blocked during a first scan of a wafer. An additional scan is performed by shifting pattern data to use beams with good properties. In one embodiment the number of beams that reach the wafer simultaneously during each scan is made as even as possible.

D2 (WO 2007/013802 A1) describes a lithography system in which out-of-specification beamlets are switched off during a first scan of a wafer, and an additional scan is performed using properly functioning beamlets in place of the out-of-specification beamlets. Where a small number of beamlets are out-of-specification, this results in a first scan by a large number of beamlets and a second scan by only a small number of beamlets.

The invention uses a second scan to augment the first scan for functioning beamlets as well as defective beamlets. A beam measurement identifies failed and out-of-specification beamlets. Using this information, a first and second scan can be calculated that will result in every pixel of the wafer being assigned for scanning by functioning beamlets. An algorithm calculates the channels to be used for the first and second scans and the corresponding wafer offset required for each scan, to result in all stripes being written by functioning channels. For a two-pass scan, the algorithm looks for a 50/50 split of channels between each scan that does not use any channels. This divides the total exposure current between two (or more) scans, so that the total beamlet current for each scan is reduced, and the heating imparted to the wafer by each scan is also reduced resulting in less localized or instantaneous heat load, and the required capacity in the data path is also reduced.