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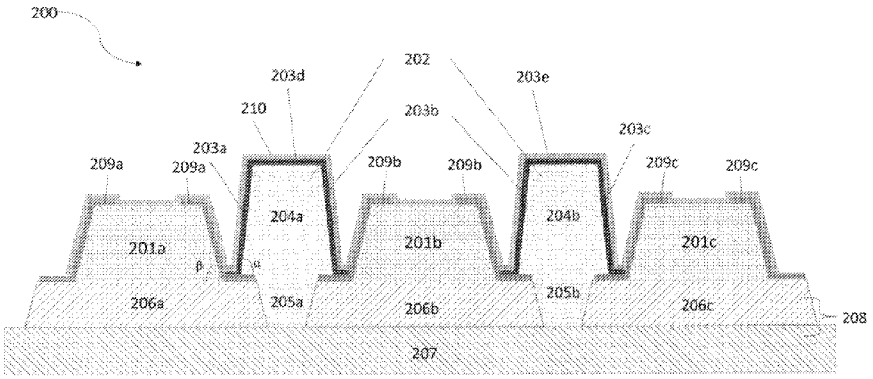


Figure 2

(57) Abstract: A light-emitting diode (LED) chip structure with a cup-like reflective element is provided. The LED chip structure comprises a substrate, an isolation element and a mesa including an LED surrounded by the isolation element. The isolation element comprises an upper isolation part and a lower isolation part. The lower isolation part is positioned in the substrate and the upper isolation part protrudes from a surface of the substrate. A reflective layer is disposed on a sidewall of the upper isolation part, and a bottom of the reflective layer does not contact the mesa. The cup-like reflective element at least includes the isolation element with the reflective layer.

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LIGHT-EMITTING DIODE CHIP STRUCTURES WITH REFLECTIVE ELEMENTS

RELATED APPLICATION

[0001] This application claims priority to United States Provisional Patent Application No. 63/013,358, filed April 21, 2020, entitled "LIGHT-EMITTING DIODE CHIP STRUCTURES WITH REFLECTIVE ELEMENTS," which is hereby incorporated by reference.

TECHNICAL FIELD

[0002] The present disclosure relates generally to light-emitting diode (LED) display devices, and more particularly, to LED chip structures with one or more reflective elements.

BACKGROUND

[0003] With the development of mini LED and micro LED technologies in recent years, consumer devices and applications such as augmented reality (AR), projection, heads-up display (HUD), mobile device displays, wearable device displays, and automotive displays, require LED panels with improved resolution and brightness. LEDs can be miniaturized and act as pixel light emitters in a display system, for example in a micro-display system. When trying to achieve better resolution and brightness on a small display, it may be challenging to meet both the resolution and brightness requirements. That is, pixel resolution and brightness may be difficult to balance at the same time as they can have an opposite relationship. For example, getting a high brightness for each pixel may result in a low resolution. On the other hand, obtaining a high resolution may bring the brightness down.

[0004] Also, light emitted by the micro-LED may be generated from spontaneous emissions and thus may not be directional, resulting in a large divergence angle. A large divergence angle may cause various problems in a micro-LED display. On one hand, due to the large divergence angle, only a small portion of the light emitted by the micro-LEDs can be utilized. This may significantly reduce the efficiency and brightness of a micro-LED display system. On the other hand, due to the large divergence angle, the light emitted by one

micro-LED pixel may illuminate its adjacent pixels, resulting in light crosstalk between pixels, loss of sharpness, and loss of contrast. Conventional solutions reducing the large divergence angle may not effectively handle the light emitted from the micro-LED as a whole, and may utilize only the central portion of the light emitted from the micro-LED, leaving the rest of the light emitted at more oblique angles to be unutilized.

[0005] As a result, it would be desirable to provide an LED structure for display devices that addresses the above-mentioned drawbacks, amongst others.

SUMMARY

[0006] Exemplary embodiments of the present disclosure are directed to LED chip structures with one or more reflective elements. In some embodiments, the reflective elements are cup-like structures that surround an LED pixel unit.

[0007] Exemplary embodiments of LED chip structures in the present disclosure include an isolation element comprising an upper isolation part and a lower isolation part. Exemplary embodiments also include a reflective layer disposed directly or indirectly on the upper isolation part. The isolation element can reduce the divergence of light emitted from a mesa including an LED pixel unit, and reduce the light crosstalk between adjacent pixels. For example, the isolation element and the reflective layer can utilize the light from oblique angles. In this way, higher efficiency can be achieved in collecting and converging this light for high-brightness and power-efficient display than conventional solutions. In addition, the isolation element can block the light emitting from LEDs in adjacent pixels, which can effectively suppress the inter-pixel crosstalk and enhance color contrast and sharpness. Exemplary embodiments of the present disclosures can improve projection brightness and contrast, and therefore reduce power consumption in projection applications. Exemplary embodiments of the present disclosures can also improve the light-emission directionality of the display, and therefore provide user with better image quality and protect user's privacy in direct-view applications.

[0008] Exemplary embodiments of the present disclosure can provide multiple advantages. One advantage is that exemplary embodiments of the present disclosure can suppress inter-pixel light crosstalk and enhance brightness. For example, pitch refers to the distance between the centers of adjacent pixels on a display panel. Pitch may vary from

about 40 microns, to about 20 microns, to about 10 microns, and/or to about 5 microns or below. A single pixel area is fixed when the pitch specification is determined. Exemplary embodiments of the present disclosure can suppress the inter-pixel light crosstalk at a smaller pitch while enhancing brightness within a single pixel in a power-efficient manner. Another advantage is that in exemplary embodiments of the present disclosure, a light-emitting diode can be directly bonded on the substrate with pixel drivers without introducing an intermediate substrate, which can improve heat dissipation and thus enhance the reliability and performance of the LED chip.

[0009] The present disclosure thus includes, without limitation, the following exemplary embodiments.

[0010] Some exemplary embodiments provide a first LED chip structure. The first LED chip structure comprises a substrate and an isolation element. The isolation element comprises an upper isolation part and a lower isolation part. The lower isolation part is positioned in the substrate, and the upper isolation part protrudes from a surface of the substrate. The first LED chip structure also comprises a reflective layer disposed on a sidewall of the upper isolation part. The first LED chip structure further comprises a mesa including an LED component surrounded by the isolation element, and a bottom portion of the reflective layer does not contact the mesa.

[0011] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the substrate includes a semiconductor wafer and a bonding metal layer on top of the semiconductor wafer.

[0012] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the reflective layer is disposed on the sidewall and a top surface of the upper isolation part, and the bottom portion of the reflective layer extends in a direction from the isolation element to the mesa.

[0013] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the first LED chip structure further comprises a dielectric layer which is disposed at a bottom of a sidewall of the mesa, and the dielectric layer is covered by the bottom portion of the reflective layer.

[0014] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, a height of the upper isolation part is higher than a height of the lower isolation part.

[0015] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, a bottom width of the upper isolation part is equal to or wider than a top width of the lower isolation part.

[0016] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the bottom width of the upper isolation part is longer than the top width of the lower isolation part and shorter than twice the top width of the lower isolation part, two protrusions are formed at each bottom end of the upper isolation part, and a width of each of the two protrusions is less than half of the top width of the lower isolation part.

[0017] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, in a side view, a cross section of the upper isolation part is a trapezoid and a cross section of the lower isolation part is an inverted trapezoid, the bottom of the upper isolation part covering a top of the lower isolation part. In some embodiments, an area of the bottom of the upper isolation part is greater than an area of the top of the lower isolation part.

[0018] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the upper isolation part and the lower isolation part are axisymmetric and co-axial.

[0019] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, a height of the upper isolation part is higher than a height of the mesa, relative to a surface of the substrate, and a tilt angle of the sidewall of the upper isolation part is greater than a tilt angle of the sidewall of the mesa, relative to an axis normal to the surface of the substrate.

[0020] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the tilt angle of the sidewall of the mesa is

smaller than 45°, and the tilt angle of the sidewall of the upper isolation part is greater than 45°.

[0021] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the dielectric layer covers a top surface and the sidewall of the mesa, the top surface of the mesa including an area not covered by the dielectric layer or free of the dielectric layer.

[0022] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the dielectric layer is transparent to the light emitted from the first LED chip structure.

[0023] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the dielectric layer comprises one or more of silicon-containing dielectric layer, aluminum-containing dielectric layer or titanium-containing dielectric layer.

[0024] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the silicon-containing dielectric layer comprises an oxide or nitride of silicon, the aluminum-containing dielectric layer comprises an oxide of aluminum, and the titanium-containing dielectric layer comprises an oxide of titanium.

[0025] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the oxide of titanium is Ti_3O_5.

[0026] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the reflective layer includes a multi-layered structure.

[0027] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the multi-layered structure comprises a stack of one or more reflective material layers and one or more dielectric material layers.

[0028] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the reflective layer comprises one or more metallic conductive materials with a high reflectance. In some embodiments, the high

reflectance is above 70%. In some embodiments, the high reflectance is above 80%. In some embodiments, the high reflectance is above 90%.

[0029] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the one or more metallic conductive materials comprise one or more of aluminum, gold or silver.

[0030] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the top surface and the sidewall of the mesa and the top surface and the sidewall of the upper isolation part are fully or partially covered by a conductive layer. In some embodiments, the conductive layer is continuous.

[0031] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the conductive layer is transparent to the light emitted from the first LED chip structure.

[0032] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the isolation element comprises photosensitive dielectric material.

[0033] In some exemplary embodiments or any combination of preceding exemplary embodiments of the first LED chip structure, the photosensitive dielectric material is SU-8 or photosensitive polyimide (PSPI).

[0034] Other exemplary embodiments provide a second LED chip structure. The second LED chip structure comprises a substrate, an isolation element, a mesa, a dielectric layer and a conductive layer. The isolation element comprises an upper isolation part and a lower isolation part. The lower isolation part is positioned in the substrate and the upper isolation part protrudes from a surface of the substrate. The mesa including an LED component is surrounded by the isolation element. The dielectric layer covers a top surface and a sidewall of the mesa, and the top surface of the mesa further includes an area not covered by the dielectric layer, e.g. free of the dielectric layer. The conductive layer covers the dielectric layer, the top surface of the mesa with the area free of the dielectric layer, and at least a sidewall of the upper isolation part. The reflective layer is at least disposed on the

conductive layer covering the sidewall of the upper isolation part, and a bottom portion of the reflective layer does not contact the mesa.

[0035] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the substrate includes a semiconductor wafer and a bonding metal layer on top of the semiconductor wafer.

[0036] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the conductive layer is disposed on a top surface and the sidewall of the upper isolation part, and the reflective layer is disposed on the conductive layer disposed on the top surface and the side wall of the upper isolation part, and wherein the bottom portion of the reflective layer extends from the isolation element to the mesa.

[0037] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, a height of the upper isolation part is higher than a height of the lower isolation part.

[0038] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, a bottom width of the upper isolation part is equal to or wider than a top width of the lower isolation part.

[0039] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the bottom width of the upper isolation part is longer than the top width of the lower isolation part and shorter than twice the top width of the lower isolation part, two protrusions are formed at each bottom end of the upper isolation part, and a width of each of the two protrusions is less than half of the top width of the lower isolation part.

[0040] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, in a side view, a cross section of the upper isolation part is a trapezoid and a cross section of the lower isolation part is an inverted trapezoid, the bottom of the upper isolation part covering a top of the lower isolation part. In some embodiments, an area of the bottom of the upper isolation part is greater than an area of the top of the lower isolation part.

[0041] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the upper isolation part and the lower isolation part are axisymmetric and co-axial.

[0042] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, a height of the upper isolation part is higher than a height of the mesa, relative to a surface of the substrate, and a tilt angle of the sidewall of the upper isolation part is greater than a tilt angle of the sidewall of the mesa, relative to an axis normal to the surface of the substrate.

[0043] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the tilt angle of the sidewall of the mesa is smaller than 45°, and the tilt angle of the sidewall of the upper isolation part is greater than 45°.

[0044] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the dielectric layer is transparent to the light emitted from the second LED chip structure.

[0045] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the dielectric layer comprises one or more of silicon-containing dielectric layer, aluminum-containing dielectric layer or titanium-containing dielectric layer.

[0046] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the silicon-containing dielectric layer comprises an oxide or nitride of silicon, the aluminum-containing dielectric layer comprises an oxide of aluminum, and the titanium-containing dielectric layer comprises an oxide of titanium.

[0047] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the oxide of titanium is Ti_3O_5.

[0048] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the reflective layer includes a multi-layered structure.

[0049] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the multi-layered structure comprises a stack of one or more reflective material layers and one or more dielectric material layers.

[0050] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the reflective layer comprises one or more metallic conductive materials with a high reflectance. In some embodiments, the high reflectance is above 70%. In some embodiments, the high reflectance is above 80%. In some embodiments, the high reflectance is above 90%.

[0051] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the one or more metallic conductive materials comprise one or more of aluminum, gold or silver.

[0052] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the conductive layer is transparent to the light emitted from the second LED chip structure.

[0053] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the isolation element comprises photosensitive dielectric material.

[0054] In some exemplary embodiments or any combination of preceding exemplary embodiments of the second LED chip structure, the photosensitive dielectric material is SU-8 or photosensitive polyimide (PSPI).

[0055] These and other features, aspects, and advantages of the present disclosure will be apparent from a reading of the following detailed description together with the accompanying figures, which are briefly described below. The present disclosure includes any combination of two or more features or elements set forth in this disclosure, regardless of whether such features or elements are expressly combined or otherwise recited in a specific example embodiment described herein. This disclosure is intended to be read holistically such that any separable features or elements of the disclosure, in any of its aspects and exemplary embodiments, should be viewed as combinable unless the context of the disclosure clearly dictates otherwise.

[0056] It will therefore be appreciated that this brief Summary is provided merely for purposes of summarizing some exemplary embodiments so as to provide a basic understanding of some aspects of the disclosure. Accordingly, it will be appreciated that the above described exemplary embodiments are merely examples and should not be construed to narrow the scope or spirit of the disclosure in any way. Other example embodiments, aspects and advantages will become apparent from the following detailed description taken in conjunction with the accompanying figures which illustrate, by way of example, the principles of some described exemplary embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

[0057] So that the present disclosure can be understood in greater details, a more particular description may be had by reference to the features of various embodiments, some of which are illustrated in the appended drawings. The appended drawings, however, merely illustrate pertinent features of the present disclosure and are therefore not to be considered limiting, for the description may admit to other effective features.

[0058] Figure 1 illustrates a top view of an LED chip structure, in accordance with some exemplary embodiments.

[0059] Figure 2 illustrates a cross-sectional view of an LED chip structure, in accordance with some exemplary embodiments.

[0060] Figure 3 illustrates a cross-sectional view of another LED chip structure, in accordance with some exemplary embodiments.

[0061] Figure 4 illustrates a cross-sectional view of a reflective layer with a multi-layered structure, in accordance with some exemplary embodiments.

[0062] In accordance with common practice, the various features illustrated in the drawings may not be drawn to scale. Accordingly, the dimensions of the various features may be arbitrarily expanded or reduced for clarity. In addition, some of the drawings may not depict all of the components of a given system, method or device. Finally, like reference numerals may be used to denote like features throughout the specification and figures.

DETAILED DESCRIPTION

[0063] Some embodiments of the present disclosure will now be described more fully hereinafter with reference to the accompanying figures, in which some, but not all embodiments of the disclosure are shown. Indeed, various embodiments of the disclosure may be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these exemplary embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the disclosure to those skilled in the art. For example, unless otherwise indicated, reference to something as being a first, second or the like should not be construed to imply a particular order. Also, something may be described as being above something else (unless otherwise indicated) may instead be below, and vice versa; and similarly, something described as being to the left of something else may instead be to the right, and vice versa. Like reference numerals refer to like elements throughout.

[0064] Exemplary embodiments of the present disclosure are generally directed to LED display devices, and in particular, to LED chip structures with a reflective layer.

[0065] Figure 1 illustrates a top view of an LED chip structure 100, in accordance with some exemplary embodiments. As shown, in some embodiments, the LED chip structure 100 includes one or more mesas 101 (e.g., mesas 101a, 101b and 101c). Each of the mesas 101 may include an LED or a micro-LED. Each of the mesas 101 has a top and a bottom. For example, the circle 120a may indicate a top of the mesa 101b and the circle 120b may indicate a bottom of the mesa 101b, and the surface connecting the top of the mesa 101b and the bottom of the mesa 101b. i.e., the sidewalls of the mesa, represented in the figure by the space between circle 120a and circle 120b. In some embodiments, the diameter of the top of each of the mesas 101 may be in the range of 1μm – 8μm, and the diameter of the bottom of each of the mesas may be in the range of 3μm – 10μm. In some embodiments, the diameter of the top of each of the mesas 101 may be in the range of 8μm – 25μm, and the diameter of the bottom of each of the mesas may be in the range of 10μm – 35μm. The distance between centers of the two adjacent mesas may be in the range of 1μm -10μm. In some embodiments, the distance between centers of the two adjacent mesas may vary from about 40 μm, to about 20 μm, to about 10 μm, and/or to about 5 μm or below. The sizes of

the mesas and distances between the mesas depends on the resolution of the display. For example, for a display panel with 5000 Pixels Per Inch (PPI), the diameter or width of the top of the mesa 101b may be 1.5μm and the diameter or width of the bottom of the mesa 101b may be 2.7μm. The height of the mesa is about 1.3μm. The distance between the closest bottom edges of the mesa 101a and the mesa 101b may be 2.3μm.

[0066] In some embodiments, the mesas 101 may be surrounded by at least one isolation element 102. The isolation element 102 can isolate light emitted from different mesas. For example, the isolation element 102 can isolate at least some of the light emitted from the mesa 101a and/or 101c from the light emitted from the mesa 101b when a height of the isolation element 102 is higher than a height of the mesa 101a and/or 101c. Therefore, the isolation element 102 can suppress the inter-pixel light crosstalk and improve the contrast of LED displays.

[0067] In some embodiments, the LED chip structure 100 also includes one or more reflective layers 103 (e.g., reflective layers 103a, 103b and 103c). Each of the reflective layers 103 may be disposed on a sidewall of the isolation element 102. For example, as shown in Figure 1, the reflective layer 103b may be disposed on a circular sidewall of the isolation element 102 surrounding the mesa 101b. The reflective layers 103 can reflect light emitted from the mesas 101 and therefore enhance the brightness and luminous efficacy of LED displays. For example, the light emitted from the mesa 101b may arrive at the reflective layer 103b and may be reflected upwardly by the reflective layer 103b.

[0068] The reflective layers 103, together with the isolation element 102, can utilize reflection direction and/or reflection intensity of the light emitted from the mesas 101. For instance, the sidewall of the isolation element 102 may be inclined at a certain angle, and therefore the reflective layer 103b disposed on the sidewall of the isolation element 102 is inclined at the same angle (within manufacturing tolerances). When the light emitted from the mesa 101b arrives at the reflective layer 103b, the light emitted from the mesa 101b would be reflected by the reflective layer 103b in accordance with the angle of the sidewall of the isolation element 102. The material of the reflective layers 103 may be highly reflective, and therefore most of (for example, above 60%) the light emitted from the mesas 101, e.g., the mesa 101b, can be reflected. Some elements of the LED chip structure 100 are omitted in

Figure 1 for simplicity of illustration. Some embodiments of LED chip structures with greater details will be described with reference to Figures 2-4 below.

[0069] Figure 2 illustrates a cross-sectional view of an LED chip structure 200, in accordance with some exemplary embodiments. In some embodiments, the cross section of the LED chip structure 200 is taken along the A-A line in Figure 1. As shown, in some embodiments, the LED chip structure 200 includes a substrate 208, which includes a wafer 207 and one or more bonding metal layers 206 on top of the wafer 207. The bonding metal layer 206 (e.g., bonding metal layers 206a, 206b and 206c) may be disposed on the wafer 207 and electrically bond the wafer 207. In some embodiments, the thickness of the bonding metal layer 206 is about 0.1 micron to about 3 microns. For example, for a display panel with 5000 PPI, the thickness of a bonding metal layer 206 is about 1.3 μm. In some instances, two metal layers are included in the bonding metal layer 206. One of the metal layers is deposited on the mesa 201. A counterpart bonding metal layer is also deposited on the wafer 207. In some embodiments, compositions for the bonding metal layer 206 include Au-Au bonding, Au-Sn bonding, Au-In bonding, Ti-Ti bonding, Cu-Cu bonding, or a mixture thereof. For example, if Au-Au bonding is selected, the two layers of Au respectively need a Cr coating as an adhesive layer, and Pt coating as an anti-diffusion layer. And the Pt coating is between the Au layer and the Cr layer. The Cr and Pt layers are positioned on the top and bottom of the two bonded Au layers. In some embodiments, when the thicknesses of the two Au layers are about the same, under a high pressure and a high temperature, the mutual diffusion of Au on both layers bond the two layers together. Eutectic bonding, thermal compression bonding, and transient liquid phase (TLP) bonding are example techniques that may be used.

[0070] In some embodiments, the LED chip structure 200 may include a pixel driver integrated circuitry (IC) integrated in the wafer 207. The wafer 207 may contain silicon as a carrier material with high thermal conductivity, which can facilitate heat dissipation and provide low thermal expansion.

[0071] In some embodiments, the LED chip structure 200 also includes at least one isolation element 202, similar as the isolation element 102 explained above with reference to Figure 1. As shown in Figure 2, in some embodiments, the isolation element 202 may

include one or more upper isolation parts 204 (e.g., upper isolation parts 204a and 204b) and one or more lower isolation parts 205 (e.g., lower isolation parts 205a and 205b). For example, as shown in Figure 2, the isolation element 202 includes the upper isolation part 204a and the lower isolation part 205a. In some embodiments, the upper isolation part 204a and the lower isolation part 205a are integrally formed as one part as shown in Figure 2. The lower isolation part 205a is positioned in the substrate 208, e.g., within the region of the bonding metal layer 206. The upper isolation part 204a protrudes from a surface of the substrate 208, e.g., from the top surface of the bonding metal layer 206, and is positioned on a top of the lower isolation part 205a.

[0072] In one embodiment, the upper isolation parts 204 (e.g., the upper isolation parts 204a and 204b) may be electrically connected to each other, e.g., by using a conductive material or expanding the upper isolation parts to contact or overlap with each other. In another embodiment, the upper isolation parts 204 (e.g., the upper isolation parts 204a and 204b) may be isolated from each other, e.g., by using a buffer space disposed between adjacent upper isolation parts.

[0073] In some embodiments, the LED chip structure 200 also includes one or more mesas 201 (e.g., mesas 201a, 201b and 201c) surrounded by the isolation element 202, similarly as explained above with reference to Figure 1. For example, as shown in Figure 2, the mesa 201b is surrounded by the isolation element 202, e.g., by the upper isolation parts 204a and 204b and by the lower isolation parts 205a and 205b. The mesas 201 may be positioned on top of the substrate 208, e.g., on top of the bonding metal layer 206, and may be driven by a pixel driver IC individually or collectively.

[0074] In some embodiments, the mesas 201 may be electrically connected to the wafer 207 via the bonding metal layer 206. For example, although not shown in Figure 2, p-electrodes of mesas 201 and outputs of driving transistors may be positioned underneath the mesas 201, and are electrically connected by the bonding metal layer 206. The mesa current driving signal connection (between p-electrode of mesa and output of the pixel driver), ground connection (between n-electrode and system ground), the Vdd connection (between source of the pixel driver and system Vdd), and the control signal connection to the gate of the pixel driver are made in accordance with various embodiments, for example as described

in U.S. patent application Ser. No. 15/135,217 (U.S. publication No. 2017/0179192) "Semiconductor Devices with Integrated Thin-Film Transistor Circuitry," which is incorporated by reference herein.

[0075] The mesas 201 may be LEDs or micro-LEDs, which produce widely diverging light. For example, the mesa 201b may be a LED or micro-LED, or may be a group of LEDs or micro-LEDs. In one embodiment, an amount of light emitted from the sidewalls of the mesas 201 is greater than the amount of light emitted from the top of the mesas 201. This may cause a wide divergence of the emitted light and a large angular extent of the far field profile, possibly up to 180 degrees, which creates inter-pixel light crosstalk. The isolation element 202 can suppress the inter-pixel light crosstalk. In some embodiments, as shown in Figure 2, the mesa 201b is surrounded by the upper isolation parts 204a and 204b and by the lower isolation parts 205a and 205b. The isolation element 202 may perform as optical isolations isolating at least some of the light emitted from the mesas 201. For example, some of the light emitted from the mesa 201b may be isolated by the upper isolation parts 204a and 204b, thus preventing the light emitted from the mesas 201a and/or 201c from illuminating the light emitted from the mesa 201b.

[0076] In some embodiments, the LED chip structure 200 further includes one or more reflective layers 203 (e.g., reflective layers 203a, 203b and 203c), similarly as explained above with reference to Figure 1. Each of the reflective layers 203 is disposed on one or more sidewalls of one or more upper isolation parts of the isolation element 202. For example, as shown in Figure 2, the reflective layer 203b is disposed on the sidewall of the upper isolation part 204a, and is also disposed on the sidewall of the upper isolation part 204b. In some embodiments, each of the reflective layers 203 including the bottom of each of the reflective layers does not directly contact the each of the mesas 201. For example, a bottom of the reflective layer 203b does not contact or directly touch the mesa 201b, or other mesas 201a and 201c. The reflective layers 203 can perform as passive optics that reflect some of the light emitted from mesas 201. For example, light emitted from the mesa 201b may arrive at and be reflected upwardly by the reflective layers 203b, thus reducing the divergence of light emitted by the mesa 201b.

[0077] In some embodiments, the reflective layers 203 are disposed on one or more sidewalls of one or more upper isolation parts 204 and/or disposed on a top surface of one or more upper isolation parts 204. For example, as shown in Figure 2, the reflective layer 203b may be disposed on the sidewalls of the upper isolation parts 204a and 204b, and reflective layers 203d and 203e may be disposed on tops of the upper isolation parts 204a and 204b respectively. The bottom of the reflective layers 203 extends from the isolation element 202 to a mesa. For example, a bottom of the reflective layer 203b extends from the upper isolation parts 204a and 204b to the mesa 201b. In one embodiment, the reflective layers 203a-203e may be the same reflective layer formed in using the same materials in the same process.

[0078] In some embodiments, the reflective layers 203 may comprise one or more metallic conductive materials with a high reflectance to the light emitted from the LED chip structure 200. In some embodiments, the high reflectance is above 70%. In some embodiments, the high reflectance is above 80%. In some embodiments, the high reflectance is above 90%. In these embodiments, the one or more metallic conductive materials may comprise one or more of aluminum, gold or silver. In some embodiments, the reflective layers 203 can be fabricated by one or more of electron beam deposition or sputtering process.

[0079] In some embodiments, the LED chip structure 200 further includes one or more dielectric layers 209 (e.g., dielectric layers 209a, 209b and 209c). Each of the dielectric layers 209 may be positioned above a top surface portion of the bonding metal layer 206 between the mesas 201 at the bottom of a sidewall of each of the mesas 201. For example, for a display panel with 5000 PPI, the width of the top surface portion of the bonding metal layer 206 is 0.55 μm at one bottom side end of the mesa 201. And a bottom portion of the dielectric layer 209 above the top surface portion of the bonding metal layer 206 is covered by the bottom portion of each of the reflective layers 203. For example, as shown in Figure 2, the dielectric layer 209b is disposed above a top surface portion of the bonding metal layer 206b between the mesas 201 at the bottom of a sidewall of the mesa 201b. And a bottom portion of the dielectric layer 209b above the top surface portion of the bonding metal layer 206b is covered by the bottom portion of each of the reflective layers 203b. In some

embodiments, the dielectric layers 209 can be fabricated by one or more of chemical vapor deposition (CVD), atomic layer deposition (ALD) or sputtering.

[0080] In some embodiments, each of the dielectric layers 209 may further cover a top surface and the sidewall of each of the mesas 201, while the top surface of each of the mesas 201 may include an area not covered by the corresponding dielectric layer, i.e., an area free of dielectric layer. For example, as shown in Figure 2, the dielectric layer 209b covers the sidewall of the mesa 201b as well as the top surface of the mesa 201b. The top surface of the mesa 201b includes an area or opening not covered by the dielectric layer 209b. Using the dielectric layers 209 can ensure that the bottom of each of the reflective layers 203 does not directly contact the mesas 201.

[0081] In some embodiments, the dielectric layer 209 may be transparent. In some embodiments, the dielectric layer 209 is transparent to the light emitted from the LED chip structure 200. In some embodiments, the dielectric layer 209 may comprise one or more of silicon-containing dielectric layer, aluminum-containing dielectric layer or titanium-containing dielectric layer. In these embodiments, for the dielectric layers 209, the silicon-containing dielectric layer may comprise an oxide or nitride of silicon, the aluminum-containing dielectric layer may comprise an oxide of aluminum, and the titanium-containing dielectric layer may comprise an oxide of titanium. In one embodiment, for the dielectric layer 209, the oxide of titanium is Ti_3O_5.

[0082] In some embodiments, the LED chip structure 200 further includes at least one conductive layer 210. The top surface and the sidewall of each of the mesas 201 and the top surface and the sidewall of each of the upper isolation parts 204 are covered by the conductive layer 210. For example, as shown in Figure 2, the conductive layer 210, directly or indirectly, covers the top surfaces and the sidewalls of the upper isolation parts 204a and 205a as well as the top surface and the sidewall of the mesa 201b. In some embodiments, the conductive layer 210 is transparent. In some embodiments, the conductive layer 210 is transparent to the light emitted from the LED chip structure 200. In some embodiments, the conductive layer 210 may include a transparent conductive oxide (TCO) layer containing one or more of indium tin oxide (ITO) or ZnO.

[0083] In some embodiments, the conductive layer 210 can be fabricated by one or more of thermal vaporization or sputtering process. The conductive layer 210 may be fabricated before or after the formation of the reflective layer 203, as long as current in the conductive layer 210, for example, current for an N-electrode, can be rapidly and uniformly distributed by the reflective layer 203. For example, the conductive layer 210 can be above the reflective layer 203 (as shown in Figure 2) or covered by reflective layer 203 (as shown in Figure 3). In some embodiments, the dielectric layers 209 may be fabricated before or after the formation of the isolation element 202, as long as the isolation element 202 and the conductive layer 210 are insulated from the bonding metal layer 206, for example, current for an N-electrode within the conductive layer 210 and the reflective layer 203 is insulated from the bonding metal layer 206 which is connected to a P-electrode. The conductive layer 210 can conduct electric current, e.g., between the mesa 201b and system Vdd.

[0084] As explained above, the isolation element 202 can isolate light emitted from one mesa (e.g., the mesa 201a) from light emitted from another mesa (e.g., the mesa 201b) when the isolation element 202 is higher than the mesas 201. In some embodiments, for the isolation element 202, the height of each of the upper isolation parts 204 is determined as the distance from the top surface of the upper isolation part 204 to the top surface of the bonding metal layer 206. In some embodiments, for the isolation element 202, the height of each of the lower isolation parts 205 is determined as the distance from the bottom surface of the lower isolation part 205 to the top surface of the bonding metal layer 206. In some embodiments, for the isolation element 202, heights of the upper isolation parts 204 may be higher than the heights of the lower isolation parts 205. For example, as shown in Figure 2, a height of the upper isolation part 204a is higher than a height of the lower isolation part 205a. In other embodiments, the heights of the upper isolation parts 204 can be the same as or lower than the heights of the lower isolation part 205. In addition, heights of the upper isolation parts may be different. For example, the height of the upper isolation part 204a may be different from the height of the upper isolation part 204b. Heights of the lower isolation parts 205 may be different as well. For example, the height of the lower isolation part 205a may be different from the height of the lower isolation part 205b.

[0085] In some embodiments, for the isolation element 202, a bottom width of each of the upper isolation parts 204 may be equal to or wider than a top width of each of the

lower isolation parts 205. For example, as shown in Figure 2, a bottom width of the upper isolation part 204a may be equal to or wider than a top width of the lower isolation part 205b. For example, for a display panel with 5000 PPI, the bottom width of the upper isolation part 204b is about 1.7 μm, the top width of the lower isolation part 205b is about 1.2μm and the bottom width of the lower isolation part 205b is about 0.3μm. In these embodiments, there is a difference between the bottom width of the upper isolation part 204a and the top width of the lower isolation part 205a, and therefore two protrusions are formed at a bottom of the upper isolation part 204a. The bottom width of the upper isolation part 204a may exceed the top width of the lower isolation part 205a by less than the top width of the lower isolation part 205a. The total bottom width of the upper isolation part 204a is longer than the top width of the lower isolation part 204a but is shorter than twice the top width of the lower isolation part 204a. In some embodiments, the width of each of the protrusions is less than half of the top width of the lower isolation part 204a. In other embodiments, widths of each of the two protrusions may be different. For example, a width of the left protrusion of the bottom of the upper isolation part 204a is different from the width of the right protrusion of the bottom of the upper isolation part 204a. For example, for a display panel with 5000 PPI, a width of the left protrusion of the bottom of the upper isolation part 204a is about 0.2 μm.

[0086] In some embodiments, for the isolation element 202, a cross section of each of the upper isolation parts 204 is a trapezoid and a cross section of each of the lower isolation parts 205 is an inverted trapezoid, and the bottom of each of the upper isolation parts 204 covers a top of each of the lower isolation parts 205. In some embodiments, an area of the bottom of the upper isolation part 204 is greater than an area of the top of the lower isolation part 205. For example, as shown in Figure 2, a cross section of the upper isolation part 204a is a trapezoid and a cross section of the lower isolation part 205a is an inverted trapezoid. The bottom of the upper isolation part 204a covers a top of the lower isolation part 205a. In addition, the trapezoid and the inverted trapezoid may be isosceles or right-angled. For example, the upper isolation part 204a is trapezoid and the lower isolation part 205a is inverted trapezoid, both of which can be isosceles. In other embodiments, an upper isolation part (e.g., the upper isolation part 204a) and a corresponding lower isolation part (e.g., the lower isolation part 205a) may be axisymmetric and/or co-axial.

[0087] In some embodiments, a height of each the upper isolation parts 204 may be higher than a height of each of the mesas 201, relative to a surface of the bonding metal layer 206. In some embodiments, a tilt angle of the sidewall of each of the upper isolation parts 204 may be greater than a tilt angle of the sidewall of each of the mesas 201, relative to an axis normal to the surface of the wafer 207.

[0088] For example, as shown in Figure 2, the height of the upper isolation part 204a may be higher than a height of the mesa 201b, relative to a surface of the bonding metal layer 206. The height of the upper isolation part 204a may also be higher than rest of the mesas 201 (i.e., the mesa 201a and 201c). Also, as shown in Figure 2, the tilt angle α relative to a top surface of the bonding metal layer 206 of the sidewall of an upper isolation part 204a may be smaller than 90°, and the tilt angle β relative to a top surface of the bonding metal layer 206 of the sidewall of the mesa 201a may be smaller than 90°. The tilt angle α of the sidewall of the upper isolation part 204a may be smaller than the tilt angle β of the sidewall of the mesa 201a. In some embodiments, the tilt angle β of the sidewall of the mesa 201a may be greater than 45°, and the tilt angle α of the sidewall of the upper isolation part 204a may be smaller than 45°.

[0089] In some embodiments, the isolation element 202 comprises dielectric material such as silicon oxide. In some embodiments, the isolation element 202 comprises photosensitive dielectric material. In some embodiments, the photosensitive dielectric material comprises SU-8 or photosensitive polyimide (PSPI). . In other embodiments, the isolation element 202 comprises photoresist. Yet in some embodiments, the isolation element 202 can be produced by photo-lithography process.

[0090] The LED chip structure 200 can increase an overall collimation of light produced by the mesas 201. Light beams that are already fairly collimated (such as light beam emitted from tops of mesas) do not hit the isolation element 202 and emerge from the LED chip structure 200 without being redirected by the isolation element 202. In contrast, light beams that are not well collimated (such as light beams emitted from sidewalls of the mesas 201) will hit the isolation element 202 and be re-directed to a more collimated direction, including the same direction as the light beams emitted from the top of the mesas 201. Therefore, the divergence angles are reduced while the overall collimation of the light

produced by the mesas 201, including in the forward direction (vertical direction of the LED chip surface), is increased. Luminous efficacy in a small angle and brightness of the LED chip structure 200 are also enhanced.

[0091] Figure 3 illustrates a cross-sectional view of an LED chip structure 300, in accordance with some exemplary embodiments. In some embodiments, the cross section of the LED chip structure 300 is taken along the A-A line in Figure 1. As shown, in some embodiments, the LED chip structure 300 includes a substrate 308, which includes a wafer 307 and one or more bonding metal layers 306 and on top of the wafer 307. Each bonding metal (e.g., bonding metal layer 306a, 306b and 306c) may be formed on the wafer 307. The materials and structures of the bonding metal layer 306 is similar to the bonding metal layer 206 described in Figure 2. In some embodiments, the LED chip structure 300 may include a pixel driver IC integrated in the wafer 307. The wafer 307 may contain silicon as a carrier material with high thermal conductivity, which facilitates heat dissipation and realize low thermal expansion.

[0092] In some embodiments, the LED chip structure 300 also includes at least one isolation element 302, similar as the isolation element 102 explained above with reference to Figure 1. As shown in Figure 3, in some embodiments, the isolation element 302 may include one or more upper isolation parts 304 (e.g., upper isolation parts 304a and 304b) and one or more lower isolation parts 305 (e.g., lower isolation parts 305a and 305b). For example, as shown in Figure 3, the isolation element 302 includes the upper isolation part 304a and the lower isolation part 305a. In some embodiments, the upper isolation part 304a and the lower isolation part 305a are integrally formed as one part as shown in Figure 3. The lower isolation part 305a is positioned in the substrate 308, e.g., within the region of the bonding metal layer 306. The upper isolation part 304a protrudes from a surface of the substrate 308, e.g., from the top surface of the bonding metal layer 306, and is positioned on a top of the lower isolation part 305a.

[0093] In some embodiments, the isolation element 302 may comprise photosensitive dielectric material. In other embodiments, the photosensitive dielectric material may be SU-8 or photosensitive polyimide (PSPI). Yet in some embodiments, the isolation element 302 can be produced by photo-lithography process. In one embodiment, the upper isolation parts 304

(e.g., upper isolation parts 304a and 304b) may be electrically connected to each other, e.g., by using a conductive material or expanding the upper isolation parts to contact or overlap with each other. In another embodiment, the upper isolation parts 304 (e.g., upper isolation parts 304a and 304b) may be isolated from each other, e.g., by using a buffer space disposed between adjacent upper isolation parts.

[0094] In some embodiments, the LED chip structure 300 also includes one or more mesas 301 (e.g., mesas 301a, 301b and 301c) surrounded by the isolation element 302, similarly as explained above with reference to Figure 1. For example, as shown in Figure 3, the mesa 301b is surrounded by the isolation element 302, e.g., by the upper isolation parts 304a and 304b and by the lower isolation parts 305a and 305b. The mesas 301 may be positioned on top of the substrate 308, e.g., on top of the bonding metal layer 306, and may be driven by the pixel driver IC individually or collectively.

[0095] In some embodiments, the mesas 301 may be electrically connected to the wafer 307 via the bonding metal layer 306. For example, although not shown in Figure 3, p-electrodes of mesas 301 and outputs of driving transistors may be positioned underneath the mesas 301, and are electrically connected by the bonding metal layer 306. The mesas 301 may be LEDs or micro-LEDs, which produce widely diverging light. For example, the mesa 301b may be a LED or micro-LED, or may be a group of LEDs or micro-LEDs. The isolation element 302 can suppress the inter-pixel crosstalk. In some embodiments, as shown in Figure 3, the mesa 301b is surrounded by the upper isolation parts 304a and 304b and by the lower isolation parts 305a and 305b. The isolation element 302 may perform as optical isolations isolating some of the light emitted from the mesas 301. For example, some of the light emitted from the mesa 301b may be isolated by the upper isolation parts 304a and 304b, thus suppressing the inter-pixel light crosstalk.

[0096] In some embodiments, the LED chip structure 300 further includes one or more dielectric layers 309 (e.g., dielectric layers 309a, 309b and 309c). Each of the dielectric layers 309 may be positioned above a top surface portion of the bonding metal layer 306 between the mesas 301 at the bottom of a sidewall of each of the mesas 301. For example, for a display panel with 5000 PPI, the width of the top surface portion of the bonding metal layer 306 is 0.55 μm at one bottom side end of the mesa 301. And a bottom portion of the

dielectric layer 309 above the top surface portion of the bonding metal layer 306 is covered by a bottom portion of each of the conductive layers 310 as described below.

[0097] In some embodiments, each of the dielectric layers 309 may cover a top surface and a sidewall of each of the mesas 301, while the top surface of each of the mesas 301 may include an area not covered by the corresponding dielectric layer. For example, as shown in Figure 3, the dielectric layer 309b covers the sidewall of the mesa 301b, as well as part of the top surface of the mesa 301b. In addition, the top surface of the mesa 301b includes an area or opening not covered by the dielectric layer 309b. Using the dielectric layers 309 can ensure that a conductive layer 310 or the bottom of each of the reflective layers 303 does not directly contact the mesas 301. In some embodiments, the dielectric layers 309 can be produced by one or more of CVD, ALD or sputtering process.

[0098] In some embodiments, the dielectric layers 309 may be transparent. In some embodiments, the dielectric layers 309 are transparent to the light emitted from the LED chip structure 300. In some embodiments, the dielectric layers 309 may comprise one or more of silicon-containing dielectric layer, aluminum-containing dielectric layer or titanium-containing dielectric layer. In these embodiments, for the dielectric layers 309, the silicon-containing dielectric layer may comprise an oxide or nitride of silicon, the aluminum-containing dielectric layer may comprise an oxide of aluminum, and the titanium-containing dielectric layer may comprise an oxide of titanium. In other embodiments, the oxide of titanium may be Ti_3O_5.

[0099] In some embodiments, the LED chip structure 300 further includes at least one conductive layer 310. As shown in Figure 3, the conductive layer 310 covers the dielectric layers 309, the top surface of each of the mesas 301 with the area not covered by the dielectric layers 309, and a sidewall of each of the upper isolation parts 304 (e.g., the upper isolation parts 304a and 304b). In some embodiments, as shown in Figure 3, the conductive layer 310 covers the top surfaces and the sidewalls of the upper isolation parts 304a and 304b as well as the top surface and the sidewall of the mesas such as the mesa 301b. In some embodiments, the conductive layer 310 is transparent. In some embodiments, the conductive layer 310 is transparent to the light emitted from the LED chip structure 300. In some

embodiments, the conductive layer 310 may include a transparent conductive oxide (TCO) layer containing one or more of indium tin oxide (ITO) or ZnO.

[00100] In some embodiments, the conductive layer 310 can be fabricated by one or more of thermal vaporization or sputtering process. The conductive layer 310 may be fabricated before or after the formation of the reflective layer 303, as long as current in the conductive layer 310, for example, current for an N-electrode, can be rapidly and uniformly distributed by the reflective layer 303. For example, the conductive layer 310 can be above the reflective layer 303 (as shown in Figure 2) or covered by reflective layer 303 (as shown in Figure 3). In some embodiments, the dielectric layers 309 may be fabricated before or after the formation of the isolation element 302, as long as the isolation element 302 and the conductive layer 310 are insulated from the bonding metal layer 206, for example, current for an N-electrode within the conductive layer 310 and the reflective layer 303 is insulated from the bonding metal layer 306 which is connected to a P-electrode. The conductive layer 310 can conduct electric current, e.g., between the mesa 301b and system Vdd.

[00101] In some embodiments, the LED chip structure 300 further includes one or more reflective layers 303 (e.g., reflective layers 303a, 303b and 303c), similarly as explained above with reference to Figure 1. Each of the reflective layers 303 is disposed on at least one or more sidewalls of one or more upper isolation parts 304 of the isolation element 302, and a bottom of each of the reflective layers 303 may not contact the mesas 301. For example, as shown in Figure 3, the reflective layer 303b is disposed on the sidewall of the upper isolation part 304a, as well as the sidewall of the upper isolation part 304b. In some embodiments, each of the reflective layers 303 including the bottom of each of the reflective layers 303 does not directly contact the each of the mesas 301. A bottom of the reflective layer 303b may not contact or directly touch the mesa 301b. The reflective layers 303 can perform as passive optics that reflect some of the light emitted from mesas 301. For example, light emitted from the mesa 301b may arrive at and be reflected upwardly by the reflective layer 303b, thus reducing the divergence of light emitted by the mesa 301b and enhancing the brightness and luminous efficacy.

[00102] In some embodiments, the reflective layers 303 may comprise one or more metallic conductive materials with a high reflectance to the light emitted from the LED chip

structure 300. In some embodiments, the high reflectance is above 70%. In some embodiments, the high reflectance is above 80%. In some embodiments, the high reflectance is above 90%. In these embodiments, the one or more metallic conductive materials may comprise one or more of aluminum, gold or silver. In some embodiments, the reflective layers 303 can be fabricated by one or more of electron beam deposition or sputtering process.

[00103] In some embodiments, the conductive layer 310 may be disposed on a top surface and the sidewall of each of the upper isolation parts 304 (e.g., the upper isolation parts 304a and 304b), and the reflective layer may be disposed on the conductive layer disposed on the top surface and the side wall of each of the upper isolation part. For example, as shown in Figure 3, the top surface and the sidewall of the upper isolation parts 304a and 304b are covered by the conductive layer 310, and the reflective layer further covers the conductive layer 310 covering the top surface and the sidewall of the upper isolation parts 304a and 304b. In some embodiments, the bottom of each of the reflective layers 303 may extend from the isolation element 302 to a corresponding mesa. For example, as shown in Figure 3, the bottom of the reflective layer 303b extends from the upper isolation parts 304a and 304b of the isolation element 302 to the mesa 301b.

[00104] As explained above, the isolation element 302 can isolate light emitted from the mesas 301a and/or 301c from light emitted from the mesa 301b because of the height. In some embodiments, for the isolation element 302, the height of each of the upper isolation parts 304 is determined as the distance from the top surface of the upper isolation part 304 to the top surface of the bonding metal layer 306. In some embodiments, for the isolation element 302, the height of each of the lower isolation parts 305 is determined as the distance from the bottom surface of the lower isolation part 305 to the top surface of the bonding metal layer 306. In some embodiments, for the isolation element 302, heights of the upper isolation parts 304 may be higher than the heights of the lower isolation parts 305. For example, as shown in Figure 3, a height of the upper isolation part 304a is higher than a height of the lower isolation part 305a. In other embodiments, the heights of the upper isolation parts 304 can be the same as or lower than the heights of the lower isolation part 305. In addition, the heights of the upper isolation parts may be different. For example, the height of the upper isolation part 304a may be different from the height of the upper isolation

part 304b. The heights of the lower isolation parts 305 may be different from each other as well. For example, the height of the lower isolation part 305a may be different from the height of the lower isolation part 305b.

[00105] In some embodiments, for the isolation element 302, a bottom width of each of the upper isolation parts 304 may be equal to or wider than a top width of each of the lower isolation parts 305. For example, as shown in Figure 3, a bottom width of the upper isolation part 304a may be equal to or wider than a top width of the lower isolation part 305b. For example, for a display panel with 5000 PPI, the bottom width of the upper isolation part 304b is about 1.7 μm, the top width of the lower isolation part 305b is about 1.2μm and the bottom width of the lower isolation part 305b is about 0.3μm. In these embodiments, there is a difference between the bottom width of the upper isolation part 304a and the top width of the lower isolation part 305a, and therefore two protrusions are formed at a bottom of the upper isolation part 304a. The bottom width of the upper isolation part 304a may exceed the top width of the lower isolation part 305a by less than the top width of the lower isolation part 305a. The total bottom width of the upper isolation part 304a is longer than the top width of the lower isolation part 304a but is shorter than twice the top width of the lower isolation part 304a. In some embodiments, the width of each of the protrusions is less than half of the top width of the lower isolation part 304a. In other embodiments, widths of each of the two protrusions may be different. For example, a width of the left protrusion of the bottom of the upper isolation part 304a is different from the width of the right protrusion of the bottom of the upper isolation part 304a. For example, for a display panel with 5000 PPI, a width of the left protrusion of the bottom of the upper isolation part 304a is about 0.2 μm.

[00106] In some embodiments, for the isolation element 302, a cross section of each of the upper isolation parts 304 is a trapezoid and a cross section of each of the lower isolation parts 305 is an inverted trapezoid, and the bottom of each of the upper isolation parts 304 covers a top of each of the lower isolation parts 305. In some embodiments, an area of the bottom of the upper isolation part 304 is greater than an area of the top of the lower isolation part 305. For example, as shown in Figure 3, a cross section of the upper isolation part 304a is a trapezoid and a cross section of the lower isolation part 305a is an inverted trapezoid. The bottom of the upper isolation part 304a covers a top of the lower isolation part 305a. In addition, the trapezoid and the inverted trapezoid may be isosceles or right-angled. For

example, the upper isolation part 304a is trapezoid and the lower isolation part 305a is inverted trapezoid, both of which can be isosceles. In other embodiments, an upper isolation part (e.g., the upper isolation part 304a) and a corresponding lower isolation part (e.g., the lower isolation part 305a) may be axisymmetric and/or co-axial.

[00107] In some embodiments, a height of each the upper isolation parts 304 may be higher than a height of each of the mesas 301 (e.g., mesa 301a, 301b and 301c), relative to a surface of the bonding metal layer 306, and a tilt angle of the sidewall of each of the upper isolation parts 304 may be greater than a tilt angle of the sidewall of each of the mesas 301 (e.g., mesa 301a, 301b and 301c), relative to an axis normal to the surface of the wafer 307.

[00108] For example, as shown in Figure 3, the height of the upper isolation part 304a may be higher than a height of the mesa 301b, relative to a surface of the bonding metal layer 306. The height of the upper isolation part 304a may also be higher than rest of the mesas 301 (i.e., the mesa 301a and 301c). Also, as shown in Figure 3, the tilt angle α relative to a top surface of the bonding metal layer 306 of the sidewall of an upper isolation part 304a may be smaller than 90°, and the tilt angle β relative to a top surface of the metal bonding layer 306 of the sidewall of the mesa 301a may be smaller than 90°. The tilt angle α of the sidewall of the upper isolation part 304a may be smaller than the tilt angle β of the sidewall of the mesa 301a. In some embodiments, the tilt angle β of the sidewall of the mesa 301a may be greater than 45°, and the tilt angle α of the sidewall of the upper isolation part 304a may be smaller than 45°.

[00109] Figures 1, 2 and 3 only illustrate the LED chip structures according to some embodiments. In other embodiments, the LED chip structures may include a different number of mesas 101 and/or a different number of reflective layers 103. In other embodiments, each of the mesas 101 may include multiple individual light elements, for example multiple LEDs or micro-LEDs connected in parallel or stacked one by one. In other embodiments, the mesas 101 may not be a circular shape from the top view. In other embodiments, the sidewall of the isolation element 102 surrounding each of the mesas 101 may not be a circular shape from the top view. That is, the sidewall of the isolation element 102 surrounding each of the mesas 101 may have other shapes from the top view, including but not limited to triangle, square, rectangular, pentagonal, hexagonal and octagonal. In other

embodiments, the isolation element 102 may include multiple separate or isolated sub-elements and each sub-element may surround one mesa. Buffer spaces may be provided between the multiple separate or isolated sub-elements.

[00110] Figure 4 illustrates a cross-sectional view of a reflective layer 400 with a multi-layered structure, in accordance with some exemplary embodiments. For the LED chip structures as described above, the reflective layer 400 may include a multi-layered structure. The multi-layered structure may comprise a stack of one or more reflective material layers and one or more dielectric material layers. In one exemplary embodiment, as illustrated in Figure 4, the reflective layer 400 includes a multi-layered structure comprising one reflective material layer 401 and one dielectric material layer 402. In other embodiments, the multi-layered structure may comprise two reflective material layers and one dielectric material layer positioned between the two reflective material layers. Yet in some other embodiments, the multi-layered structure may also comprise two dielectric material layers and one reflective material layer positioned between the two dielectric material layers. In some embodiments, the multi-layered structure may comprise two or more metal layers. For example, the metal layers may comprise one or more of TiAu, CrAl or TiWAg.

[00111] In some embodiments, the multi-layered structure may be multi-layered Omni-Directional Reflector (ODR), which comprises a metal layer and Transparent and Conductive Oxides (TCO). For example, the multilayered structure may comprise a dielectric material layer, a metal layer and TCO layer. In some embodiments, the multi-layered structure may comprise two or more dielectric material layers, which are disposed alternately to form a Distributed Bragg Reflector (DBR). For example, the multi-layered structure may comprises a dielectric material layer, a metal layer and a transparent dielectric layer. The transparent dielectric layer may comprise one or more of SiO_2, Si_3N_4 or Al_2O_3. The multi-layered structure may further comprise a dielectric material layer, a TCO and a DBR. In other embodiments, the reflective layer 400 may comprise one or more metallic conductive materials with a high reflectance. In some embodiments, the high reflectance is above 70%. In some embodiments, the high reflectance is above 80%. In some embodiments, the high reflectance is above 90%. In these embodiments, the one or more metallic conductive materials may comprise one or more of aluminum, gold or silver.

[00112] The preceding description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the embodiments described herein and variations thereof. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the subject matter disclosed herein. Thus, the present disclosure is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the following claims and the principles and novel features disclosed herein.

[00113] Different types of display panels can be fabricated according to one or more of embodiments in the present disclosure. For example, the resolution of a display panel can range from 8x8 to 3840x2160. Common display resolutions include QVGA with 320x240 resolution and an aspect ratio of 4:3, XGA with 1024x768 resolution and an aspect ratio of 4:3, D with 1280x720 resolution and an aspect ratio of 16:9, FHD with 1920x1080 resolution and an aspect ratio of 16:9, UHD with 3840x2160 resolution and an aspect ratio of 16:9, and 4K with 4096x2160 resolution. There can also be a wide variety of pixel sizes, ranging from sub-micron and below to 10 mm and above. The size of the overall display region can also vary widely, ranging from diagonals as small as tens of microns or less up to hundreds of inches or more.

[00114] Exemplary applications include display screens, light engines for home/office projectors and portable electronics such as smart phones, laptops, wearable electronics, AR and VR glasses, and retinal projections. The power consumption can vary from as low as a few milliwatts for retinal projectors to as high as kilowatts for large screen outdoor displays, projectors, and smart automobile headlights. In terms of frame rate, due to the fast response (nanoseconds) of inorganic LEDs, the frame rate can be as high as KHz, or even MHz for small resolutions.

[00115] Features of the present invention can be implemented in, using, or with the assistance of a computer program product, such as a storage medium (media) or computer readable storage medium (media) having instructions stored thereon/in which can be used to program a processing system to perform any of the features presented herein. The storage medium can include, but is not limited to, high-speed random access memory, such as

DRAM, SRAM, DDR RAM or other random access solid state memory devices, and may include non-volatile memory, such as one or more magnetic disk storage devices, optical disk storage devices, flash memory devices, or other non-volatile solid state storage devices. Memory optionally includes one or more storage devices remotely located from the CPU(s). Memory or alternatively the non-volatile memory device(s) within the memory, comprises a non-transitory computer readable storage medium.

[00116] Stored on any machine readable medium (media), features of the present invention can be incorporated in software and/or firmware for controlling the hardware of a processing system, and for enabling a processing system to interact with other mechanisms utilizing the results of the present invention. Such software or firmware may include, but is not limited to, application code, device drivers, operating systems, and execution environments/containers.

[00117] It will be understood that, although the terms "first," "second," etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another.

[00118] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the claims. As used in the description of the embodiments and the appended claims, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will also be understood that the term "and/or" as used herein refers to and encompasses any and all possible combinations of one or more of the associated listed items. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[00119] As used herein, the term "if" may be construed to mean "when" or "upon" or "in response to determining" or "in accordance with a determination" or "in response to detecting," that a stated condition precedent is true, depending on the context. Similarly, the phrase "if it is determined [that a stated condition precedent is true]" or "if [a stated condition precedent is true]" or "when [a stated condition precedent is true]" may be construed to mean

"upon determining" or "in response to determining" or "in accordance with a determination" or "upon detecting" or "in response to detecting" that the stated condition precedent is true, depending on the context.

[00120] The foregoing description, for purpose of explanation, has been described with reference to specific embodiments. However, the illustrative discussions above are not intended to be exhaustive or to limit the claims to the precise forms disclosed. Many modifications and variations are possible in view of the above teachings. The embodiments were chosen and described in order to best explain principles of operation and practical applications, to thereby enable others skilled in the art to best utilize the invention and the various embodiments.

What is claimed is:

1. A light-emitting diode (LED) chip structure, comprising:

a substrate;

an isolation element, comprising

an upper isolation part and a lower isolation part, wherein the lower isolation part is positioned in the substrate and the upper isolation part protrudes from a surface of the substrate;

a reflective layer disposed on a sidewall of the upper isolation part; and

a mesa including an LED component surrounded by the isolation element, wherein a bottom portion of the reflective layer does not contact the mesa.

2. The LED chip structure according to claim 1, wherein the reflective layer is disposed on the sidewall and a top surface of the upper isolation part, and the bottom of the reflective layer extends from the isolation element to the mesa.

3. The LED chip structure according to any one of claims 1-2, wherein a dielectric layer is disposed at a bottom of a sidewall of the mesa, and the dielectric layer is covered by the bottom portion of the reflective layer.

4. The LED chip structure according to any one of claims 1-3, wherein a height of the upper isolation part is higher that a height of the lower isolation part.

5. The LED chip structure according to any one of claims 1-4, wherein a bottom width of the upper isolation part is equal to or wider than a top width of the lower isolation part.

6. The LED chip structure according to claim 5, wherein the bottom width of the upper isolation part is longer than the top width of the lower isolation part and shorter than twice the top width of the lower isolation part, two protrusions are formed at each bottom end of the upper isolation part, and a width of each of the two protrusions is less than half of the top width of the lower isolation part.

7. The LED chip structure according to any one of claims 5-6, wherein, in a side view, a cross section of the upper isolation part is a trapezoid and a cross section of the lower isolation part is an inverted trapezoid, the bottom of the upper isolation part covering a top of the lower isolation part.

8. The LED chip structure according to any one of claims 5-7, wherein the upper isolation part and the lower isolation part are axisymmetrical and co-axial.

9. The LED chip structure according to any one of claims 1-8, wherein a height of the upper isolation part is higher than a height of the mesa, relative to a surface of the substrate, and a tilt angle of the sidewall of the upper isolation part is greater than a tilt angle of the sidewall of the mesa, relative to an axis normal to the surface of the substrate.

10. The LED chip structure according to claim 9, wherein the tilt angle of the sidewall of the mesa is smaller than 45°, and the tilt angle of the sidewall of the upper isolation part is greater than 45°.

11. The LED chip structure according to any one of claims 3-10, wherein the dielectric layer covers a top surface and the sidewall of the mesa, the top surface of the mesa including an area free of the dielectric layer.

12. The LED chip structure according to any one of claims 3-11, wherein the dielectric layer is transparent to light emitted from the LED chip structure.

13. The LED chip structure according to any one of claims 3-12, wherein the dielectric layer comprises one or more of silicon-containing dielectric layer, aluminum-containing dielectric layer or titanium-containing dielectric layer.

14. The LED chip structure according to claim 13, wherein the silicon-containing dielectric layer comprises an oxide or nitride of silicon, the aluminum-containing dielectric layer comprises an oxide of aluminum, and the titanium-containing dielectric layer comprises an oxide of titanium.

15. The LED chip structure according to claim 14, wherein the oxide of titanium is Ti_3O_5.

16. The LED chip structure according to any one of claims 1-15, wherein the reflective layer includes a multi-layered structure.

17. The LED chip structure according to claim 16, wherein the multi-layered structure comprises a stack of one or more reflective material layers and one or more dielectric material layers.

18. The LED chip structure according to any one of claims 1-17, wherein the reflective layer comprises one or more metallic conductive materials with a high reflectance above 80%.

19. The LED chip structure according to claim 18, wherein the one or more metallic conductive materials comprise one or more of aluminum, gold or silver.

20. The LED chip structure according to any one of claims 3-19, wherein a top surface and the sidewall of mesa and the top surface and the sidewall of the upper isolation part are covered by a conductive layer.

21. The LED chip structure according to claim 20, wherein the conductive layer is transparent to light emitted from the LED chip structure.

22. The LED chip structure according to any one of claims 1-21, wherein the isolation element comprises photosensitive dielectric material.

23. The LED chip structure according to claim 22, wherein the photosensitive dielectric material is SU-8 or photosensitive polyimide (PSPI).

24. The LED chip structure according to any one of claims 1-23, wherein the substrate comprises a semiconductor wafer and a bonding metal layer on top of the semiconductor wafer.

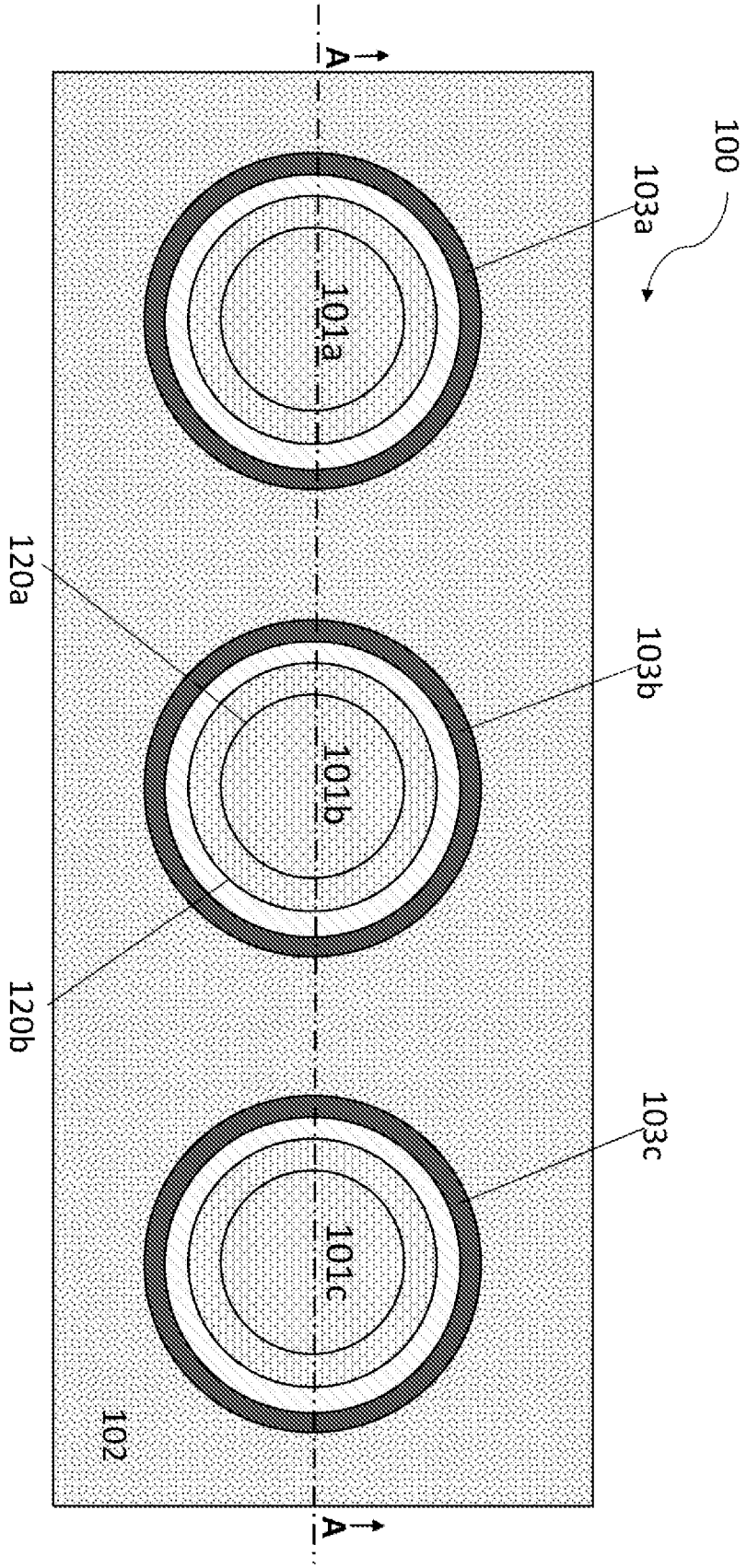


Figure 1

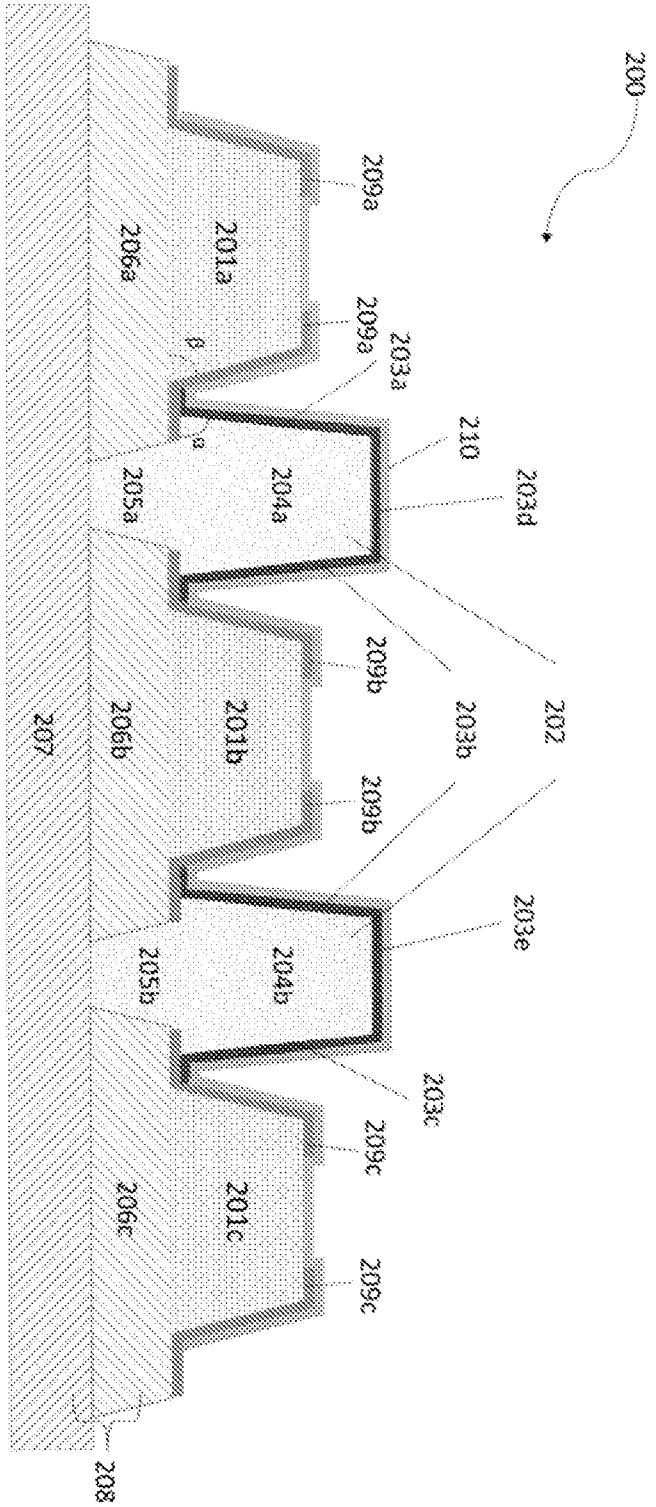

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Figure 2

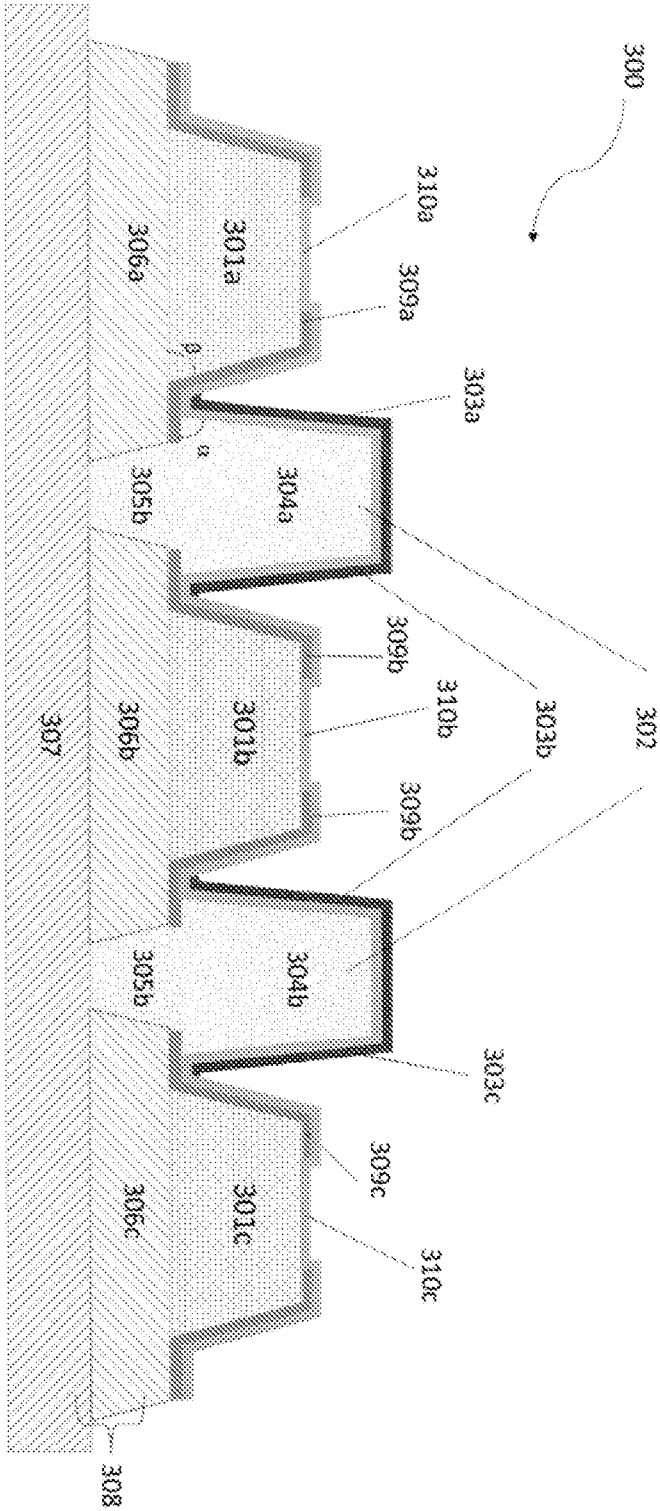

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Figure 3

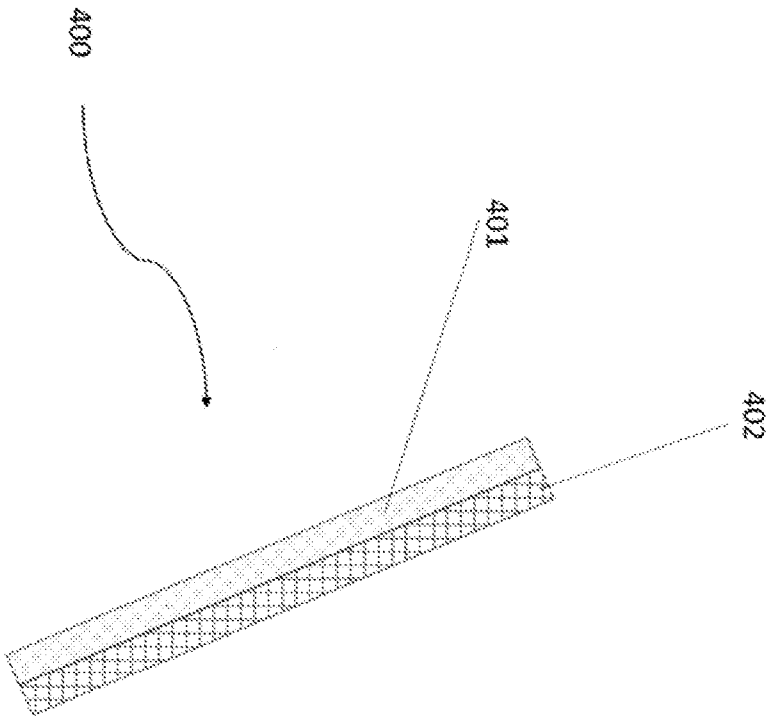


Figure 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 21/28364

A. CLASSIFICATION OF SUBJECT MATTER

IPC - H01L 23/00, G09G 3/32, H01L 25/075, H01L 33/60 (2021.01)

CPC - H01L 33/60, G09G 3/32, H01L 25/0753, G09G 3/2003, H01L 33/505, H01L 33/48, H01L 33/62, H01L 24/48, H01L 2224/48137, H01L 2924/12041, H01L 2933/0033, H01L 2933/005, H01L 2933/0058, G09G 2300/0426, G09G 2300/0452

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2018/0090058 A1 (HONG KONG BEIDA JADE BIRD DISPLAY LIMITED) 20 March 2018 (29.03.2018), Fig. 13A-13C, 14C; para [0054], [0055]	1-3
Y	US 2019/0074417 A1 (CREE, INC.) 07 March 2019 (07.03.2019), Fig 11B; para [0029], [0031], [0049], [0106], [0107]	1-3
A	US 2011/0284887 A1 (WU et al.) 24 November 2011 (24.11.2011), Fig. 1E; para [0021], [0022], [0027]	1-3
A	US 2008/0194054 A1 (LIN et al.) 14 August 2008 (14.08.2008), entire document	1-3

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 June 2021	AUG 05 2021
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Authorized officer Kari Rodriquez Telephone No. PCT Helpdesk: 571-272-4300

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 21/28364

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 4-24
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.