



- (51) International Patent Classification:  
H03F 3/38 (2006.01) H03F 3/217 (2006.01)  
H03K 7/00 (2006.01)
- (21) International Application Number:  
PCT/AU2013/000452
- (22) International Filing Date:  
30 April 2013 (30.04.2013)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:  
2012901689 30 April 2012 (30.04.2012) AU
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- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM,

AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:  
— with international search report (Art. 21(3))

- (54) Title: PULSE GENERATING CIRCUIT FOR AUDIO-FREQUENCY AMPLIFIERS AND REGULATED POWER SUPPLIES

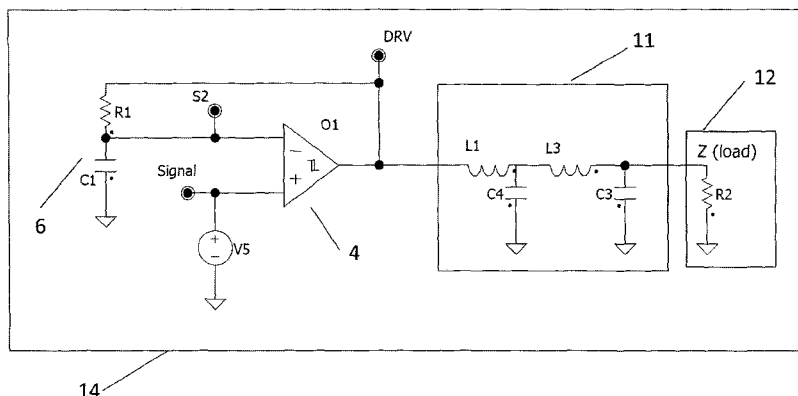


Figure 3

- (57) Abstract: A circuit for generating a series of pulses in response to a first signal, the circuit comprising: a lossy integrator which receives a second signal as its input; and a comparator which: receives the output of the lossy integrator at one of its inputs; and receives the first signal at the other of its inputs. This circuit can be incorporated into, for example, audio-frequency amplifiers and regulated power supplies.

WO 2013/163691 A1

## **PULSE GENERATING CIRCUIT FOR AUDIO-FREQUENCY AMPLIFIERS AND REGULATED POWER SUPPLIES**

### FIELD OF THE INVENTION

[0001] The present invention relates to electronic circuits. In particular, it relates to electronic circuits which can be incorporated into, for example, audio-frequency amplifiers and regulated power supplies.

### BACKGROUND TO THE INVENTION

[0002] Design criteria for an ideal audio-frequency amplifier include maximization of energy efficiency (and thus minimization of heat production), minimization of weight and minimization of bulk.

[0003] One type of highly efficient audio-frequency amplifier is known as a "class-D" amplifier. In a class-D amplifier, an input signal controls a pulse generator to produce a sequence of pulses of differing widths. These pulses are averaged over time (such as by using a low-pass filter) to produce an output signal. Because the pulses are of fixed amplitude, the switching elements (which are usually MOSFETs) are switched either completely on or completely off. A MOSFET operates with the lowest resistance when it is fully on and thus has the lowest power dissipation when in that condition, except when fully off where no power is consumed or drawn.

[0004] The invention described in US patent no. 8,289,097 assigned to Hypex Electronics B.V. (the "Hypex patent") discloses a pulse width modulation loop of a simple construction which disturbs the input signal to be processed as little as possible. The circuit can be incorporated into audio-frequency amplifiers such as a class-D amplifier.

[0005] Specifically, and referring to Figure 6 of the Hypex patent, the Hypex patent is concerned with a post filter fixed frequency converter with an external

sawtooth waveform. This sawtooth waveform is corrected by factors that represent the behaviour of the various parts of the circuit which include the filter, the feedback network, “the forward path” and the comparator. The invention disclosed in the Hypex patent is limited to “fixedly” determined or known clock circuits as described in paragraph [0023] of that document.

[0006] The Hypex patent also relies on predetermining the response of the amplifier by extensive internal measurement circuits so that the various factors can be determined. Of course these factors are very complex and are products of temperature, load, and frequency. To accurately determine these factors over these ranges requires significant computational effort.

[0007] Further, ‘Improved analogue class-D amplifier with carrier symmetry modulation’ B. H. Candy and S. M. Cox, *Audio Engineering Society 117<sup>th</sup> Convention, 28-31 October 2004 San Francisco, CA, USA* Convention Paper 6260, looks at reducing distortion in a class-D amplifier application. The analogue class-D amplifier disclosed follows the well known prior-art class-D structure with negative feedback, but includes modulation of the symmetry of the carrier oscillator waveform by a derivative of the input signal. The disclosed circuit compensates a nonlinear phase modulation effect that is intrinsic to the prior art structure.

[0008] Embodiments of the present invention provide circuits for generating pulse waveforms which are particularly suitable for, but not limited to, controlling the known class-D circuit. Furthermore, embodiments of the present invention aim to ameliorate some of the disadvantages of the prior art.

#### SUMMARY OF THE INVENTION

[0009] Accordingly, in one aspect, the present invention provides a circuit for generating a series of pulses in response to a first signal, the circuit comprising: a lossy integrator which receives a second signal as its input; and a comparator

which: receives the output of the lossy integrator at one of its inputs; and receives the first signal at the other of its inputs.

[0010] A lossy integrator refers to an integrator with a decay component. One embodiment of such a device is an RC network with a long time constant relative to the chosen switch frequencies. In mathematical terms, this may be an integrator, with or without error, with a decay term that may be either linear or non linear.

[0011] It is preferred that the lossy integrator comprises a resistor and a capacitor in series. Alternatively it is preferred that the lossy integrator comprises: a resistor and a capacitor in series; and a resistor in parallel with the capacitor, the input to the lossy integrator being applied across both resistors and the output from the lossy integrator being generated across the capacitor.

[0012] In an embodiment, the comparator receives the output of the lossy integrator at its summing input and receives the first signal at its negating input.

[0013] It is preferred that at least one of: the lossy integrator; and the comparator is implemented by using digital operations.

[0014] It is preferred that a signal which is determined by the output of the comparator controls the switching of at least one switching element.

[0015] It is preferred that the switching elements are in a half-bridge configuration. Alternatively, the switching elements are in a full-bridge configuration.

[0016] It is preferred that the switching elements switch power to a load.

[0017] It is preferred that a low-pass filter is interposed between the switching elements and the load. Alternatively, the load also operates as a low-pass filter.

[0018] It is preferred that the second signal depends at least partly on the output of at least one switching element.

[0019] It is preferred that the first signal depends at least in part on a bias signal.

[0020] It is preferred that first signal depends at least in part on a signal which is to be amplified.

[0021] It is preferred that each switching element is a transistor, for example, a FET.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0022] For a better understanding of the invention, and to show how it may be carried into effect, embodiments of it are shown, by way of non-limiting example only, in the accompanying drawings. In the drawings:

[0023] Figure 1 is a schematic of a circuit according to a first embodiment of the present invention.

[0024] Figure 2 is a set of graphs illustrating voltage waveforms at a number of points in Figure 1.

[0025] Figure 3 is a simplified schematic of Figure 1 and a second embodiment of the present invention.

[0026] Figure 3A is a mathematical model of the embodiment shown in Figure 3.

[0027] Figure 4 illustrates the voltage waveforms at a number of points in Figure 3.

[0028] Figure 4A is an alternative representation of the waveforms shown in Figure 4.

[0029] Figure 5 is a zoomed in view of the voltage waveforms shown in Figure 4.

[0030] Figure 6 is a schematic of a circuit according to a third embodiment of the present invention.

[0031] Figure 7 is a schematic of a circuit according to a fourth embodiment of the present invention.

[0032] Figure 8 illustrates the voltage waveforms at a number of points in Figure 7.

[0033] Figure 9 is a zoomed in view of the waveforms in the portion A-A' of Figure 8.

[0034] Figure 10 is a schematic of a circuit according to a fifth embodiment of the present invention.

[0035] Figure 10A is a mathematical model of the embodiment shown in Figure 10.

[0036] Figure 11 is a schematic of a circuit according to a sixth embodiment of the present invention.

[0037] Figure 12 is a schematic of a circuit according to a seventh embodiment of the present invention.

[0038] Figure 13 is a highly generalized functional diagram for a mathematical model of another embodiment of the invention.

[0039] Figure 14 is a highly generalized functional diagram for a mathematical model of yet another embodiment of the invention.

[0040] Figure 15 is a schematic of a circuit according to another embodiment of the present invention.

[0041] Figure 15A is a mathematical model of the embodiment shown in Figure 15.

[0042] Figure 16 illustrates the voltage waveforms of an input signal, a carrier signal according to a circuit of a previous embodiment, and a carrier signal according to the embodiment depicted in Figure 15.

#### DESCRIPTION OF PREFERRED EMBODIMENT

[0043] Structure of the embodiment of Figure 1

[0044] The circuit 1 of Figure 1 illustrates an embodiment of the invention which operates as a regulated power supply. The circuit 1 comprises a power supply unit 2, a bias generator 3, a comparator 4, a lossy integrator 6, a half-bridge switching circuit 7, a low-pass filter network 11 and a load 12.

[0045] The power supply unit 2 comprises two identical voltage sources  $V_2$ ,  $V_3$  which are grounded at the mid-point.

[0046] The bias generator 3 comprises two resistors  $R_4$  and  $R_5$  which are connected in series across the power supply rails  $V+$  or  $V-$ , generating a bias voltage  $V_{Bias}$  at their junction.  $V_{Bias}$  is determined by the voltages on each power supply rail and by the ratio  $R_5/(R_4+R_5)$ .

[0047] The lossy integrator 6 generates the signal  $S_2$ . The lossy integrator 6 comprises resistors  $R_1$  and  $R_3$  connected end-to-end between the output  $Out_1$  and ground, with capacitor  $C_1$  between the junction of resistors  $R_1$  and  $R_3$  and ground. The signal  $S_2$  is tapped off the junction of resistors  $R_1$  and  $R_2$ . The lossy integrator is thus a voltage divider, low pass filter. The break frequency of that filter is determined by the parallel equivalent resistance of  $R_1$  and  $R_3$  and by the capacitance of capacitor  $C_1$ . Ideally this  $RC$  value should be set above the maximum required signal frequency. Subtle but important is the fact that the signal distortion at the output  $Out_1$ , both the switched and steady state, is present in the integrator signal  $S_2$ .

[0048] The half-bridge switching circuit 7 comprises a first NFET circuit 8 and a second NFET circuit 9 which are connected in series between the positive and negative power supply rails  $V+$  or  $V-$ , to generate the output  $Out_1$  at their junction. The NFET circuit 8 receives the signal  $DRV$  at its input through an inverter  $Y_1$  111 and the NFET circuit 9 receives the signal  $DRV$  at its input. The signal  $Out_1$  represents the half bridge output voltage, and ideally is either  $V+$  or  $V-$  depending on which FET is on. In practical applications, this is not achievable in either steady state (not switching) or switching mode due to non-ideal behaviour of the FETs. This non-ideal behaviour results in distortion of the signal  $Out_1$  which in turn causes potential distortion at the load 12 if not compensated. This is a common major issue with traditional circuits.

[0049] The comparator 4 receives  $V_{Bias}$  at its inverting input and the signal S2 from the lossy integrator at its non-inverting input to generate a signal DRV. The comparator then compares the bias signal  $V_{Bias}$  with S2, and switches high or low depending on whichever is higher. The signal DRV switches one of the NFET circuits 8 and 9 on and the other of them off, depending on the polarity of the DRV signal. Theoretically the switching speed would be infinite, but delays are present throughout the system. These delays include the comparator hysteresis, the bridge switching delay and delays in the FET driver signals, and phase shift delays of the lossy integrator.

[0050] Operation of the embodiment of Figure 1

[0051] The operation of circuit 1 is illustrated by the signal traces shown in Figure 2. To simplify understanding of the circuit of Figure 1, each NFET circuit 8 and 9 can be considered to be a binary state machine with infinitely quick transition times. Referring to Figure 2, when the signal DRV 220 transitions from high to low, the top NFET 8 turns on, and simultaneously the bottom NFET 9 turns off. This means that Out1 is now equal to  $V+$ , having been equal to  $V-$  before DRV changed. The step response change in the input to the lossy integrator 6 causes a ramping voltage at S2, in this case up from where ever it was prior to the transition. This can be seen in Figure 2, where the waveform S2 210 is a triangle, or ramping function, as a result of the waveform DRV 220 transitioning.

[0052] When the ramp exceeds the Bias 230, DRV will change state again, which causes Out1 to go from  $V+$  back to  $V-$ , which in turn causes S2 to ramp down 211 again. When S2 falls back below the Bias 230, DRV will transition again 221.

[0053] The edge transition gradient at Out1 is of course not infinite, in fact, it is not even linear. Power rail fluctuations mean that there is always variation at Out1. The lossy integrator 6 detects these fluctuations, which are presented to

the comparator 4 along with the desired signal. The errors are compensated for by being compared to the original signal.

[0054] Assuming that the voltage rails, driver FETs and load are all stable then this example will resonate at the system's maximum speed with a fixed duty cycle. This will result in zero signal at the output at a low signal frequency, and a small signal at the switching frequency due to the filter. However if noise is injected into either FET or into the power supply rails, or if there are other noise sources, then the comparator 4 will automatically compensate to force the signal S2 to be neutral relative to the bias voltage. This results in a very small or zero difference across the load, and therefore very little or no noise.

[0055] The circuit 1 of Figure 1 therefore operates as a highly stable regulated power supply.

[0056] In the following description, where the components shown in any of the figures are the same as the components shown in the circuit of Figure 1, the same reference numbers are used to identify those components.

[0057] Simplified illustrative structure

[0058] The circuit illustrated in Figure 1 is shown in a simplified form (excluding the half-bridge switching circuit) in the schematic shown in Figure 3. This schematic will be used to illustrate aspects of the operation of the invention. Figure 3A is a mathematical model corresponding to the simplified circuit of Figure 3. This simplified circuit forms a second embodiment of the invention and could be used for various applications including an encoder, a low power amplifier, a low power supply unit or an isolating encoder.

[0059] Figures 4, 4A and 5 each illustrate the voltage waveforms at a number of points in Figure 3. The waveforms are placed on the same axis in Figures 4

and 5 to show their relative relationship. In Figure 4A the waveforms are placed on separate axis to more clearly show the individual shapes of the waveforms.

[0060] The circuit 14 includes a lossy integrator 6, a comparator 4, a filter network 11 and a load 12. The mathematical model shown in Figure 3A depicts a signal  $X(s)$  as an input to a comparator 4, the other input being a feedback signal from the output of the comparator 4 transformed by the function  $K1.F1(s)$  where  $K1$  is a constant and  $F1(s)$  represents the lossy integrator 6. The function  $H1(s)$  represents the filter network 11 in Figure 3.

[0061] The circuit 14 receives a signal from a signal source  $V5$  which is represented by the curve  $V_{\text{signal}}$  410 in Figures 4, 4A and 5. The lossy integrator 6 produces a triangle signal which is illustrated by the graph  $V_{S2}$  420 in Figures 4, 4A and 5. The comparator produces a pulse output which is represented by the graph  $V_{\text{DRV}}$  430 in Figures 4, 4A and 5. The filter 11 produces an output  $V_{R2}$  440 which is applied to the load 12. The circuit 14 may include a gain component by adding a resistor across  $C1$ . In addition,  $V5$  could be derived from the system voltage, thereby rejecting power rail ripple.

[0062] As can be seen from Figures 4, 4A and 5, so long as  $V_{S2}$  420 (the triangle output of the lossy integrator) is above the signal value  $V_{\text{signal}}$  410, the drive voltage  $V_{\text{DRV}}$  430 is low, and the output of the integrator  $V_{S2}$  420 decreases in value. If the output of the lossy integrator  $V_{S2}$  420 is below the signal  $V_{\text{signal}}$  410, then the drive voltage  $V_{\text{DRV}}$  430 is high, raising the output  $V_{S2}$  420 of the lossy integrator. This results in self oscillation because the triangle wave form  $V_{S2}$  420 of the lossy integrator will always be moving about the signal  $V_{\text{signal}}$  410 so long as  $V_{\text{signal}}$  410 stays within the  $V_{\text{DRV}}$  output boundaries defined by the high and low values.

[0063] The advantage of this embodiment is that hardware or software implementation of the circuit is simple compared to that of the prior art, such as

the Hypex patent referred to earlier. In addition, the distortion exhibited by the circuit is reduced compared to that of the prior art.

[0064] Other embodiments of the invention

[0065] The circuit 36 of Figure 6 is a simplified representation of third embodiment of the invention. The circuit 36 is a slightly more complex circuit than circuit 14 in Figure 3, in that it includes one additional component. The components shown in Figure 6 are a lossy integrator 6, a comparator 4, an inverter 37, a low-pass filter network 11 and a load 12. The output of the comparator 4 is an input to one side of the filter network 11 and the negated output of the comparator 4 is input to the other side of the filter network 11. This arrangement is advantageous over the circuit of Figure 3 because it results in a higher gain, a gain of 2, because there is an input to the filter network 11 in phase with, and in anti-phase with, the pulse output of the comparator 4. Furthermore it has four times the power of the circuit of Figure 3. In addition, there is no DC offset; this is preferable when using inductive loads such as speakers. As with circuit 14, further gain could be created by adding a resistor across C1.

[0066] The circuit 16 of Figure 7 illustrates a fourth embodiment of the invention. This embodiment can be used for audio applications where the frequency and amplitude range and control requirements are extreme, and therefore demonstrates one of the most difficult applications. This embodiment involves a half-bridge switching circuit and is advantageous over full-bridge circuits described below because it may provide a lower cost alternative in some applications. Figures 7, 8 and 9 relate to this embodiment.

[0067] The circuit 16 comprises a power supply unit 2, a comparator 4, a lossy integrator 6, a half-bridge circuit 7, a low-pass filter network 11 and a load 12. The circuit 16 differs from the circuit 1 in that it has a bias generator 17 that includes functionality which is not present in the bias generator 3 of circuit 1. The bias generator 17 now incorporates a signal V5 shifted by the Bias voltage.

[0068] As can be seen from the signal traces of Figures 8 and 9 the circuit 16 operates as a signal amplifier. Figure 8 illustrates a full cycle while Figure 9 illustrates a zoomed in section labelled A-A' of Figure 8. Referring to the waveforms in Figure 8, the voltage across the load  $V_{R2}$  950 is proportional to the signal  $V5$  920.  $S2$  930 can now be seen to also follow the signal 920. The zoomed-in traces of Figure 9 show that when the signal is at a minimum, i.e. simply the normal bias voltage, the switching looks very similar to the example of Figure 2, and the frequency is at a maximum. Consequently, when the signal is at a maximum the switching frequency reduces in response.

[0069] The circuit 19 of Figure 10 illustrates a fifth embodiment of the invention. Figure 10A is a simplified mathematical model corresponding to the circuit depicted in Figure 10. The circuit 19 comprises a power supply unit 2, a comparator 4, a lossy integrator 6, a half-bridge circuit 7, a low-pass filter network 11 and a load 12. The circuit 19 differs from the circuits 1 and 16 in the construction of the bias generator 21 and the addition of a signal and bias summing circuit 22. The bias generator 21 now incorporates a voltage following buffer O4 to provide an accurate voltage source representing the bias voltage, which also ensures that minimal signal is allowed to flow back into the bias source. This is then used to bias a differential amplifier in the signal and bias summing circuit 22 which mixes in the differential signal in  $V5$ . The result is a system which will reject voltage supply variation. This circuit provides power supply rejection and improves the practical noise performance of the combined amplifier and power supply performance.

[0070] The circuit 26 of Figure 11 illustrates a sixth embodiment of the invention. The circuit 26 comprises a power supply unit 2, a comparator 4, two lossy integrators 6, a "full-bridge" or "H-bridge" circuit 27, a low-pass filter network 11 and a load 12. The circuit 26, as with the circuit 19, differs from the circuits 1 and 16 in that it includes a bias generator 21 and a signal and bias summing circuit 22.

[0071] The H-bridge circuit 27 comprises a first, second, third and fourth NFET circuit 28, 29, 31 and 32 respectively. The NFET circuits 28 and 29 constitute one half-bridge circuit and the NFET circuits 31 and 31 constitute another half-bridge circuit. The low-pass filter 11 is now connected between the two half-bridge circuits and is terminated by the load 12.

[0072] As with the half-bridge circuits of figures 1, 7 and 10, a lossy integrator 6 connects to each bridge midpoint Out1. This is then buffered as before, with the bias now being generated by summing the two half bridge signals. If there is no error in the system, both signals will be identical but opposite about the bias. If the sides are not opposite, then the bias will move, representing error. This is then summed with the desired signal by the signal and bias summing circuit 22 and presented to the comparator 4. The comparator 4 compares the signal with the output of one of the lossy integrators 6. The comparator 4 will then switch to keep the two signals as close to each other as possible, as with the half bridge embodiment depicted in Figure 7.

[0073] By collecting and summing both halves of the bridge, the error across the output filter 11 is known with great accuracy. Any power rail fluctuation will appear on both halves equally, and will therefore move the bias point accordingly. This is then compensated by the comparator 4, ensuring that the voltage rail noise is rejected and not present on the output filter 11.

[0074] Any signal mixed with the bias can be considered to be further error, but as that signal should exist on both halves of the H-bridge 27 equally and in opposite polarity, it does not appear at the bias voltage. Therefore in compensating, the comparator actually adds the signal on both halves equally. Any imbalance as stated above, does appear in the bias signal, and is therefore rejected.

[0075] The circuit 34 of Figure 12 illustrates a sixth embodiment of the present invention. The circuit 34 comprises a power supply unit 2, a bias generator 3, a

comparator 4, a single lossy integrator 6, a full-bridge or H-bridge circuit 27, a low-pass filter network 11 and a load 12. The circuit 34 of Figure 12 has a reduced component count when compared with the circuit 26 of Figure 11, at the cost of reduced error detection.

[0076] Figure 13 shows a mathematical model 38 for another embodiment of the invention. The model 38 includes an input signal  $X(s)$  identified by reference number 39 as being summed with a bias voltage 41 at 40. The bias voltage 41 is generated in any suitable manner and preferable is generated in accordance with previously-described embodiments of the present invention. The resultant of that summation is one input to the comparator 42.

[0077] The other input to the comparator 42 is the summation 49 of a number of signals. One of those signals is the output of the comparator 42 transformed by the function  $K1.F1(s)$  46, where  $K1$  is a scaling ratio for gain and  $F1(s)$  is the lossy integrator. This creates the automatic oscillation. The functions  $H1(s)$  41 and  $H2(s)$  44 are various optional output filters. The second of the inputs to the summation 49 is the output of the comparator 42 transformed by the function  $H1(s).K2.F2(s)$ . The transformation  $K2.F2(s)$  47 is an optional additional feedback function. This embodiment allows any number of feedback paths ( $Kn.Fn(s)$ ), which are exemplified in Figure 13 only by the path  $H2(s).K3.F3(s)$ .

[0078] The model 51 of Figure 14 differs from the model 38 of Figure 13 only in respect of how the summation takes place. As with the model 38 of Figure 13, one of the inputs to the comparator 42 is the output of that comparator, scaled by the function  $K1.F1(s)$ . However, no other signals are summed at that point. Instead, the output of the comparator, further transformed by the transformations  $H1(s).K2.F2(s)$  and  $H2.K3.F3(S)$  are summed together with the bias and with the signal 39 at the summation 52.

[0079] Figure 15 is a schematic of a circuit 60 illustrating a further embodiment of the present invention. The circuit 60 comprises a power supply

unit 2, a bias generator 3, a comparator 4, two lossy integrators 6, a full bridge or H-bridge switching circuit 65, a low-pass filter network 11 and a load 12. In this embodiment Out1 is now connected via a derivative connection 66, comprising resistor R8 and capacitor C5, to Out2 of the lossy integrator 6, and Out2 is now connected via another derivative connection 66', comprising resistor R2 and capacitor C3, to Out1 of the other lossy integrator 6. The cross over provides the compensation (i.e. negation), while the resistance and capacitance values, of R8, R2 and C5, C3 respectively, in conjunction with the lossy integrators 6 determine the system frequency response. This enables a reduction in the total harmonic distortion (THD) of the system, cancelling part of the decaying waveform nature of a lossy integrator.

[0080] Figure 15A illustrates a mathematical model of Figure 15 wherein two independent transfer functions  $K1.F1(s)$ ,  $K1.F2(s)$  71, 72 receive input from the square wave output from the comparator 4.  $K1.F1(s)$  may be the lossy integrator responsible for the carrier generation and  $K2.F2(s)$  is a negative derivative. Summing these features neutralizes the THD effect of the lossy integrator because the carrier now contains more high frequency information which shifts the carrier gradients in the opposite direction to the parasitic THD of the lossy integrator 6.

[0081] Figure 16 shows an input signal 810 that is to be tracked and amplified. Waveforms 820 and 830 are carrier signals and waveform 820 is an original, non-compensated integrated signal from a prior art circuit and 830 is the waveform that results using the circuit of Figure 15 or model of Figure 15A which has a derivative connection.

[0082] The signal gain of a "lossy integrator" is not constant over the signal voltage range, tending to reduce as the input signal increases in magnitude.

[0083] In Figure 16, the waveforms 820 and 830 will change shape depending on the input signal 810.

[0084] The non-compensated integrated signal 820 has a long 'charge' period B-B' and a short 'discharge' period B'-B". This is a by-product of the digital time delay of the comparator, and the difference voltage gradients when the carrier is not about the mid-rail (where the carrier is symmetric). The result is an excessive overshoot tending towards the mid rail, an effect which becomes more pronounced as the signal moves further from mid rail and hence compression.

[0085] Waveform 830 is the result of using the circuit in Figure 15, that is, adding an approximate or ideal negative derivative. Note that the input signal is identical for the two carriers. However, the carrier waveform 830 differs from waveform 820 in a number of ways. The most obvious is the significantly smaller overshoot, which reduces the THD immediately. Another and more subtle difference is the change in the 'charging' (or rising) edge of the waveforms. In waveform 830 the decay initially is in fact reversed, causing acceleration away from mid rail. This acceleration is short, and begins to decay again. This is why the overshoot is reduced.

[0086] In addition, the carrier frequency is reduced, which has the advantage of reducing system noise, whilst also reducing switching power. The Hypex patent attempts to produce a similar effect but through much more complex means.

[0087] The invention differs from prior art circuits in many aspects. The circuit samples the output voltage of the switch unit, not the post filter output, and it is the switched stage that produces a triangle wave carrier via a lossy integrator. The inventor's assumption is that a correctly designed passive filter will add little distortion but attempts to use post filter network signals excessively may add intermodulation distortion due to the filter delay. While it is an option to add post filter feedback, it is desired to minimise this for the reasons already stated.

[0088] The lossy integrator creates a self-oscillating circuit where the frequency of operation is dependent on the propagation delay of the circuit which

is deliberately modified to suit the circuit task. Thus the filter design and operation is almost an independent function. The circuit frequency is not “fixedly” determined. This independent operation of the filter is required so that EMI issues can be addressed in many applications.

[0089] The circuit smears any intermodulation products to inaudible levels over a wide frequency range. Normally intermodulation products are caused by phase and frequency non-linearities that create sum and difference products between the fixed clock and modulation signal. Mathematically, the solution for intermodulation products between a variable carrier and a signal is not easily determined, but it can be envisaged that the level at any particular frequency has much less probability of staying in one spot (and thus audible) than a fixed frequency circuit.

[0090] It is acknowledged that a lossy integrator is somewhat non ideal, but the circuit function is simple and the non-linearity of the lossy integrator can be modified by adding a distorting function derived by a simple RC network. This network adds to the waveform at the compressed peaks and troughs and adds very little at the unaffected middle of the waveform. This, to the inventor’s knowledge is not reported in any known literature. This modification results in an amplifier that produces harmonic distortion that is orders of magnitude below most loudspeakers, and state of the art intermodulation distortion which is audible and annoying.

[0091] The circuits described in the above embodiments use analogue components. These circuits therefore operate in the continuous-time domain. However, the circuits can also operate in the discrete-time domain if the analogue components are substituted with digital components.

[0092] In software, the lossy integrator may be written in infinite impulse response (IIR) or finite impulse response (FIR) forms as appropriate. A digital

lossy integrator has either a fixed or non-fixed amount subtracted from it on every computational cycle or set of cycles, for example.

[0093] The present invention provides a new way to control the amplifier that mitigates or even removes many of the traditional issues inherent in class-D amplifier control approaches.

[0094] A significant difference of the present invention compared with the prior art is using an integrator combined with a single comparator. This results in a much simpler, yet superior system.

[0095] Furthermore, the present invention greatly reduces the impact rail imbalances can have on the resulting signal.

[0096] Another advantage of the present invention is realised when applied to brushless motors. The system's superior switching speed and transient response allow for enhanced, yet simple drive control.

[0097] While the present invention has been described with reference to a few specific embodiments, the description is illustrative of the invention and is not to be construed as limiting the invention. Various modifications may occur to those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.

[0098] A reference to any prior art in this specification is not, and should not be taken as, an acknowledgment or any form of suggestion that the referenced prior art forms part of the common general knowledge, whether in Australia or elsewhere.

[0099] Throughout this specification, the words "comprise", "comprised", "comprising" and "comprises" are to be taken to specify the presence of stated features, integers, steps or components but does not preclude the presence or

addition of one or more other features, integers, steps, components or groups thereof.

[00100] In the claims, each dependent claim is to be read as being within the scope of its parent claim or claims, in the sense that a dependent claim is not to be interpreted as infringed unless its parent claims are also infringed.

## CLAIMS:

1. A circuit for generating a series of pulses in response to a first signal, the circuit comprising:
  - a lossy integrator which receives a second signal as its input; and
  - a comparator which:
    - receives the output of the lossy integrator at one of its inputs; and
    - receives the first signal at the other of its inputs.
2. A circuit according to claim 1, in which the lossy integrator comprises a resistor and a capacitor in series.
3. A circuit according to claim 1, in which the lossy integrator comprises:
  - a resistor and a capacitor in series; and
  - a resistor in parallel with the capacitor,the input to the lossy integrator being applied across both resistors and the output from the lossy integrator being generated across the capacitor.
4. A circuit according to claim 1, in which at least one of:
  - the lossy integrator; and
  - the comparator,is implemented by using digital operations.
5. A circuit according to any one of the preceding claims, in which a signal which is determined by the output of the comparator controls the switching of at least one switching element.
6. A circuit according to claim 5, in which the switching elements are in a half-bridge configuration.
7. A circuit according to claim 5, in which the switching elements are in a full-bridge configuration.

8. A circuit according to any one of claims 5 to 7, in which the switching elements switch power to a load.
9. A circuit according to claim 8, in which a low-pass filter is interposed between the switching elements and the load.
10. A circuit according to claim 9, in which the load also operates as a low-pass filter.
11. A circuit according to any one of the preceding claims, in which the second signal depends at least partly on the output of at least one switching element.
12. A circuit according to any one of the preceding claims, in which the first signal depends at least in part on a bias signal.
13. A circuit according to any one of the preceding claims, in which the first signal depends at least in part on a signal which is to be amplified.
14. A circuit according to any one of the preceding claims, in which each switching element is a transistor.
15. A circuit according to claim 14, in which each transistor is a FET.
16. A regulated power supply comprising a circuit according to any one of claims 1 to 12.
17. An amplifier comprising a circuit according to any one of claims 1 to 12.

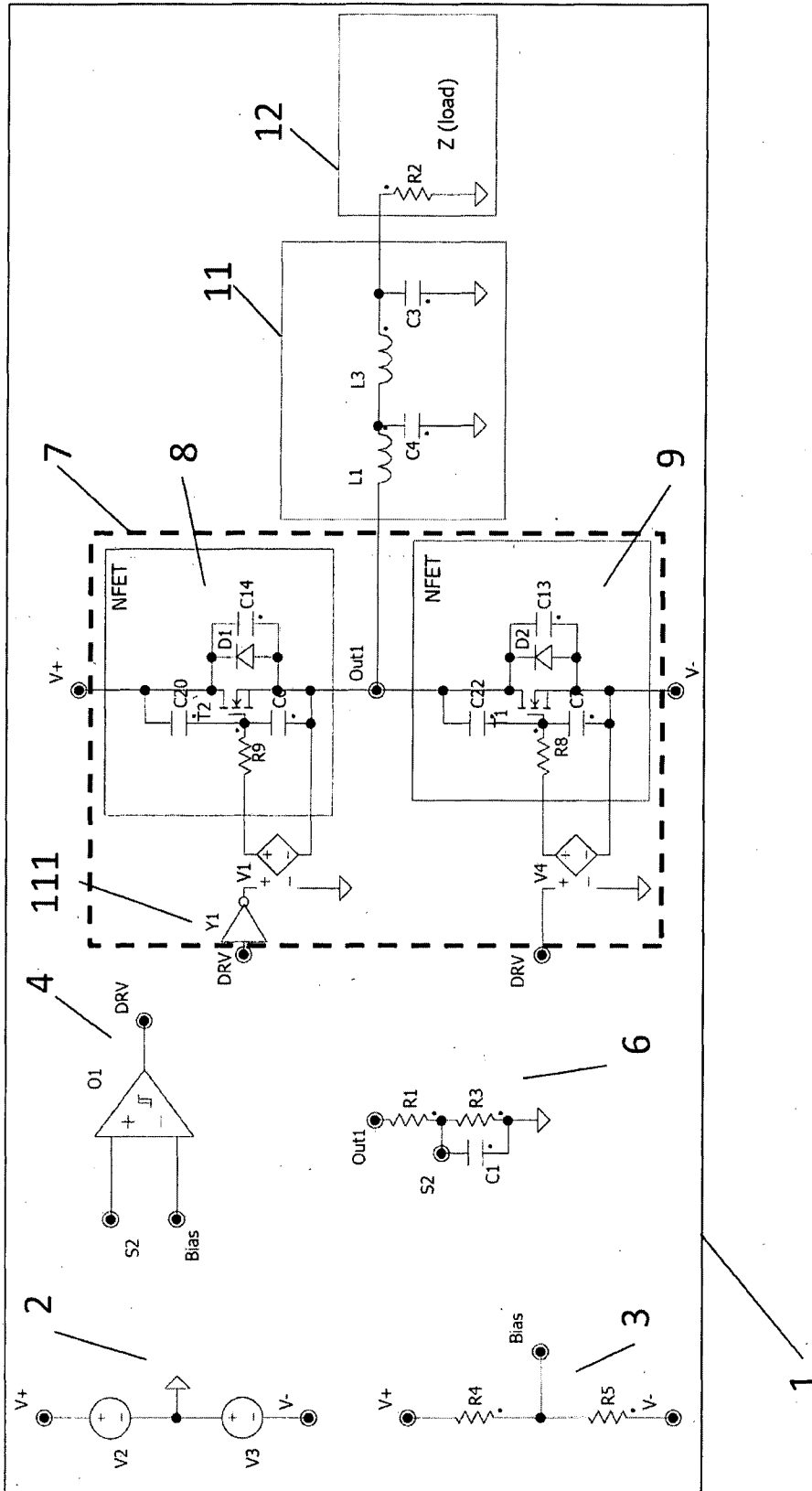


Figure 1

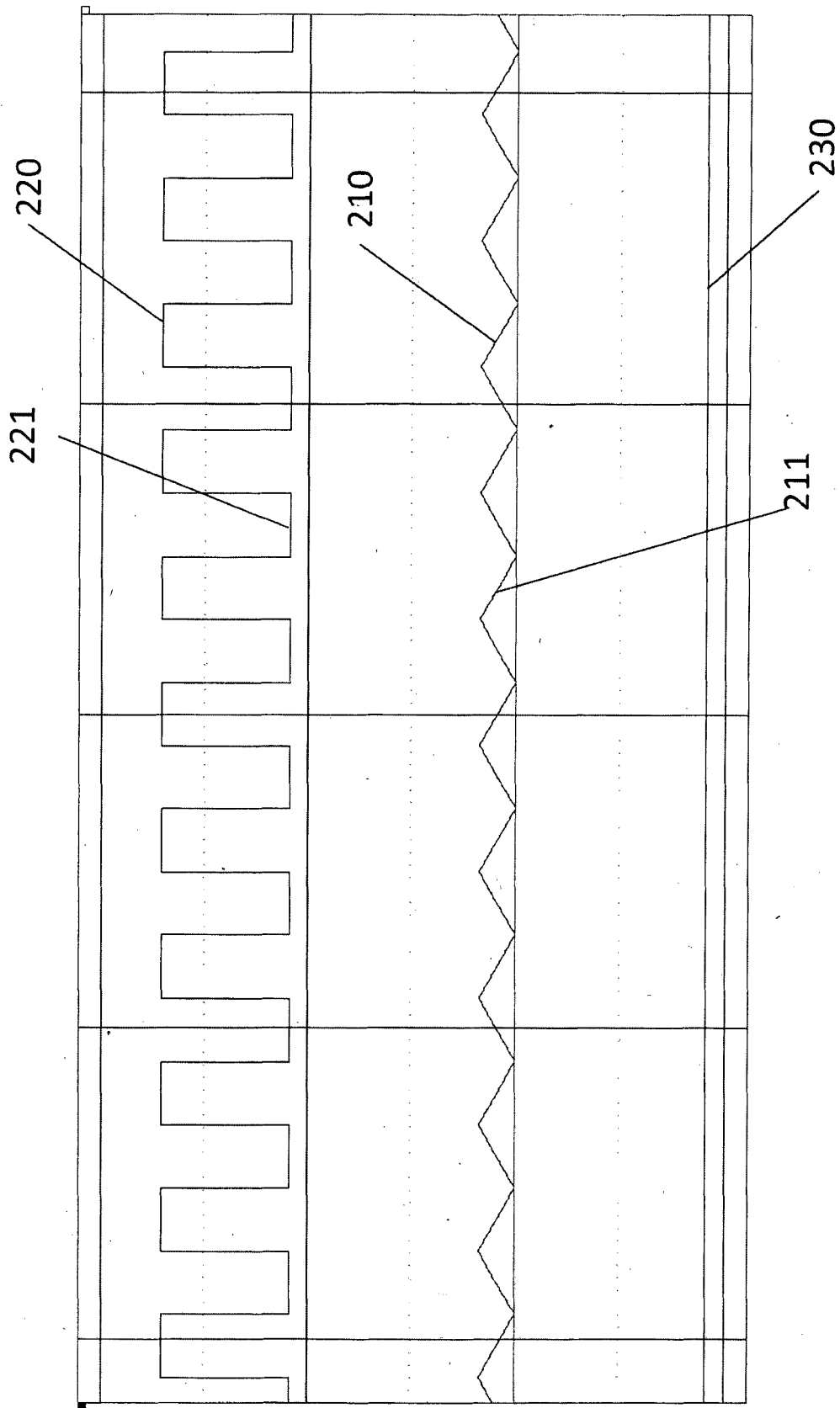


Figure 2

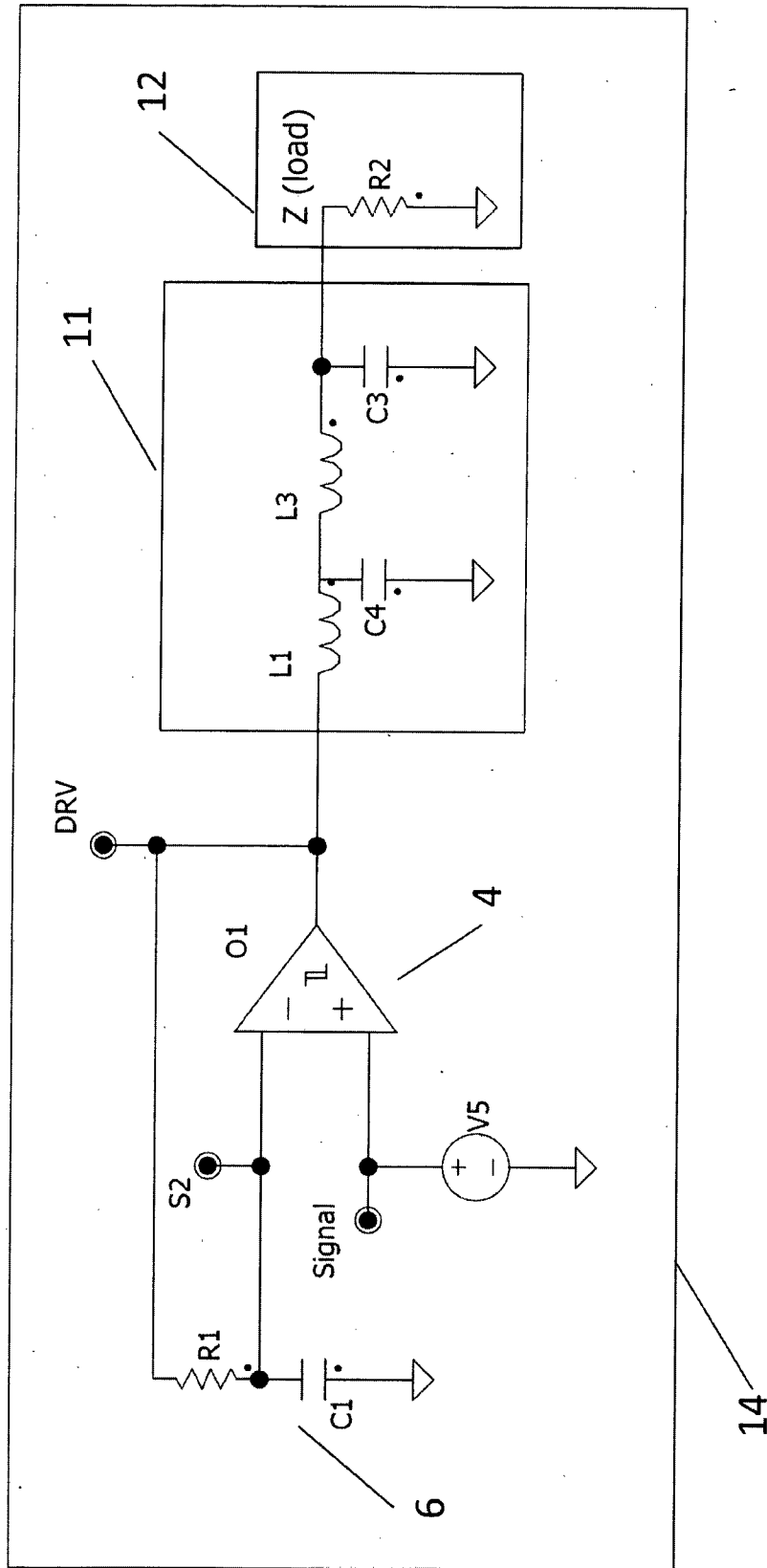


Figure 3

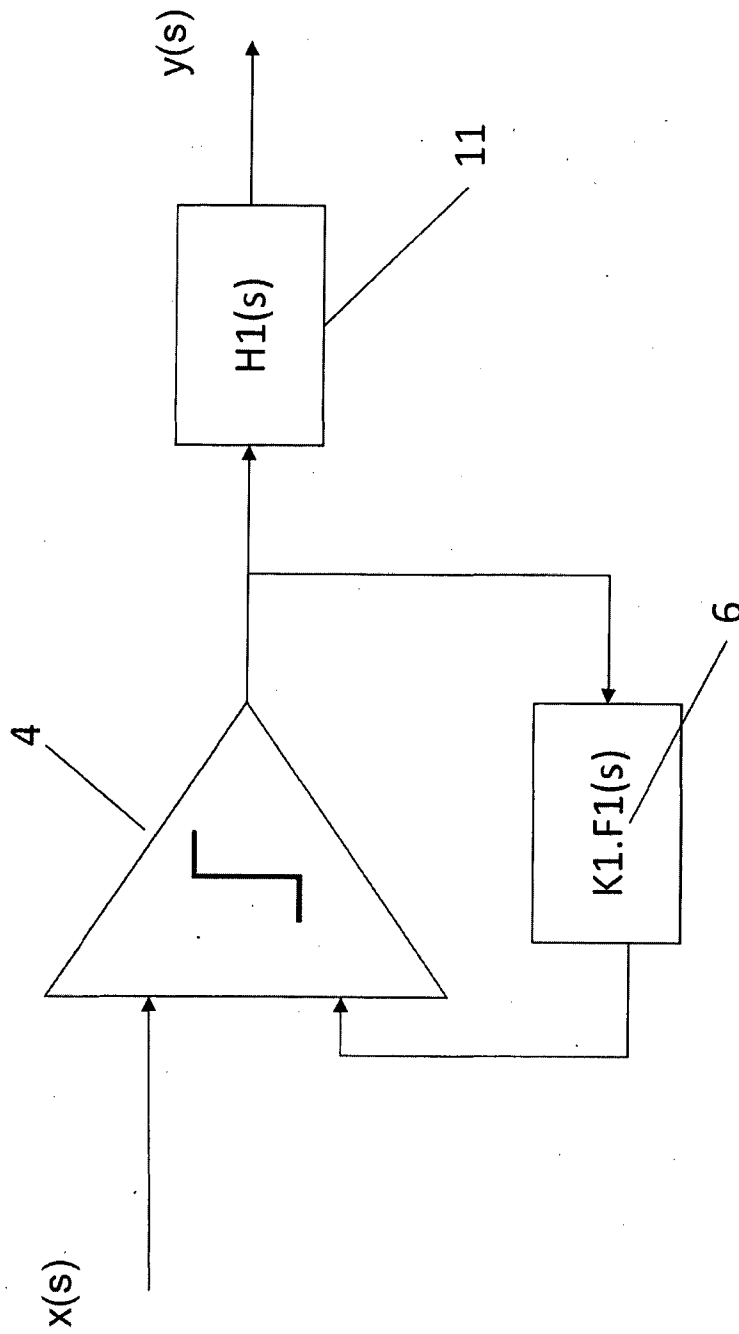


Figure 3A

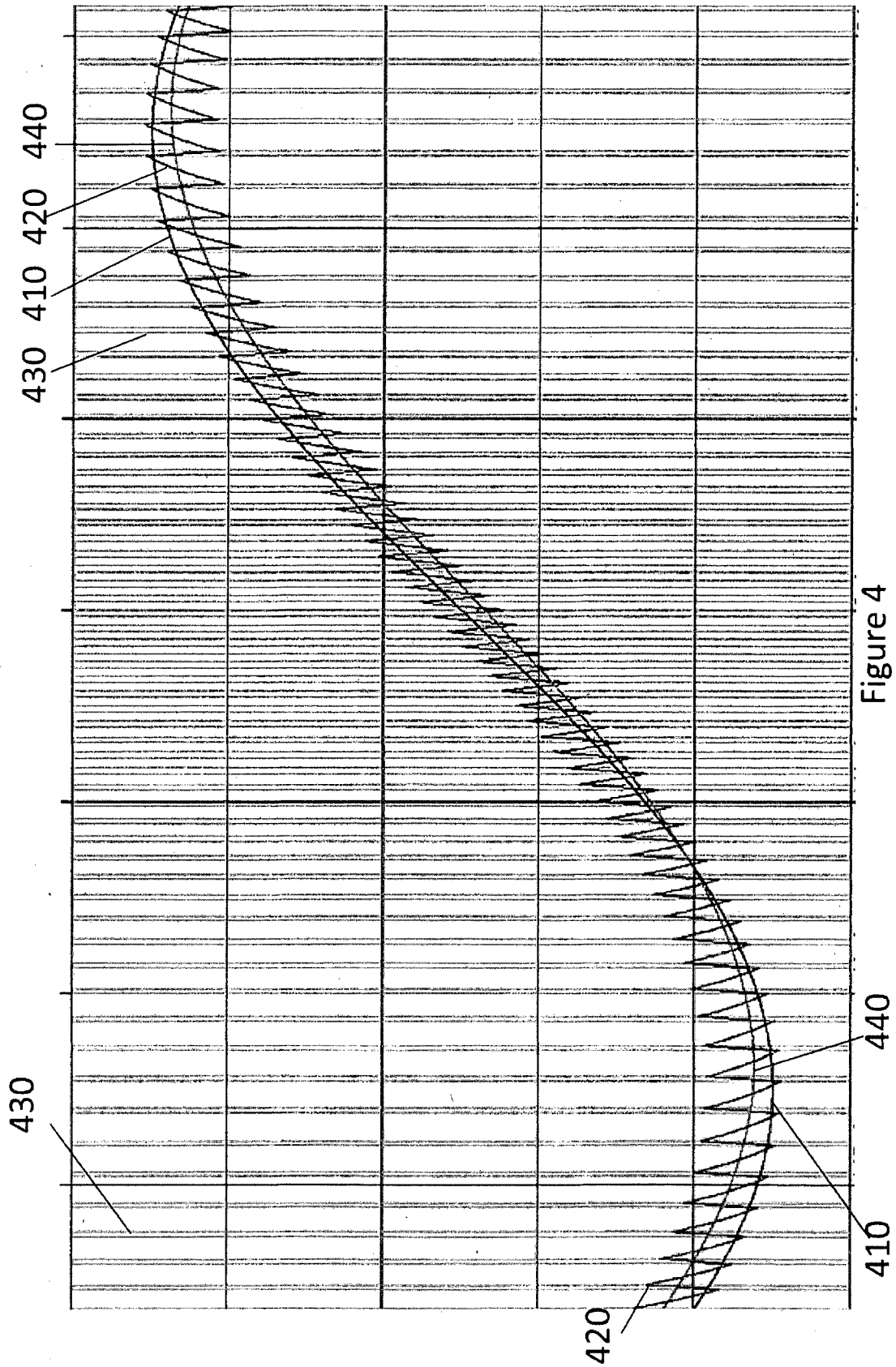


Figure 4

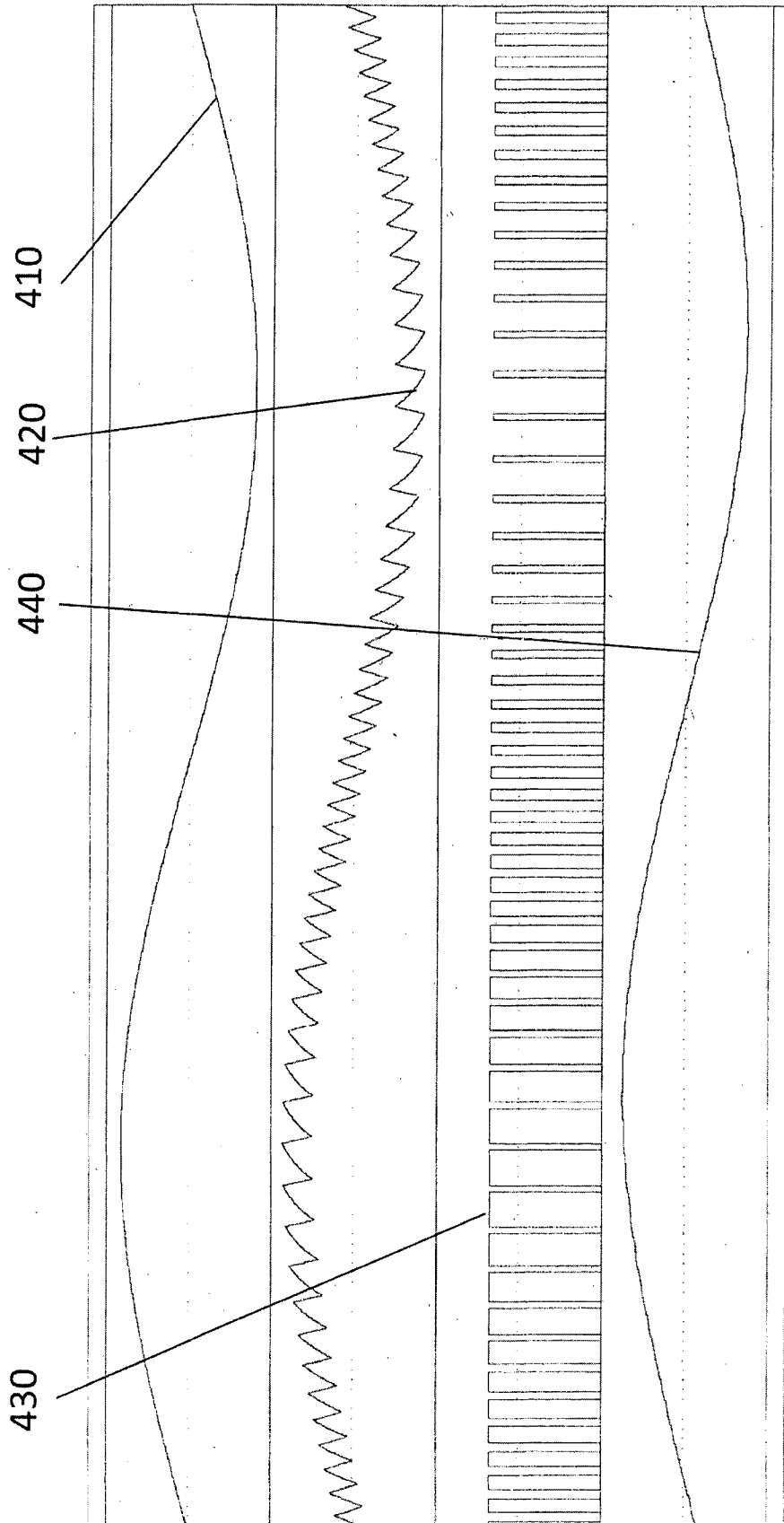


Figure 4A

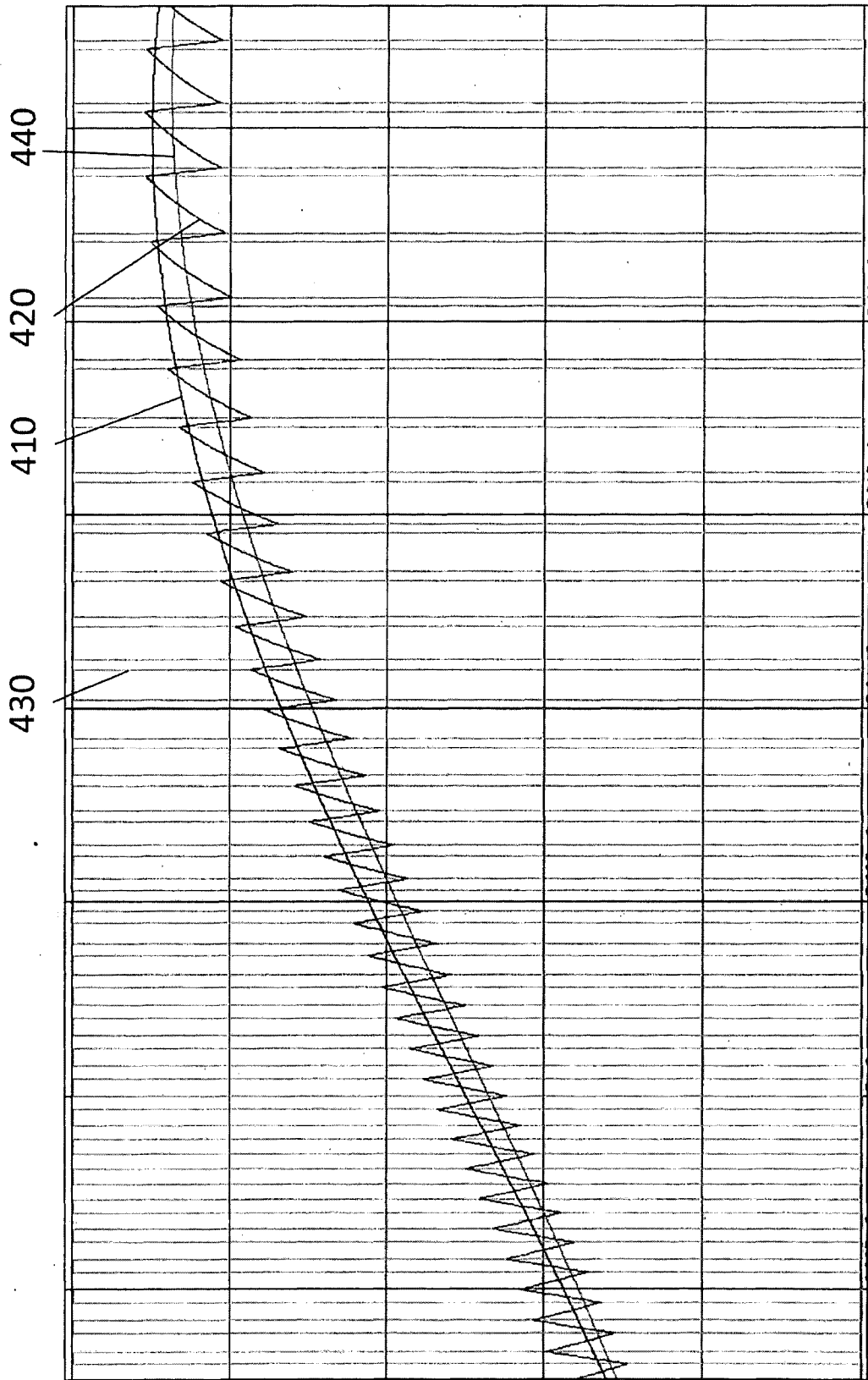


Figure 5



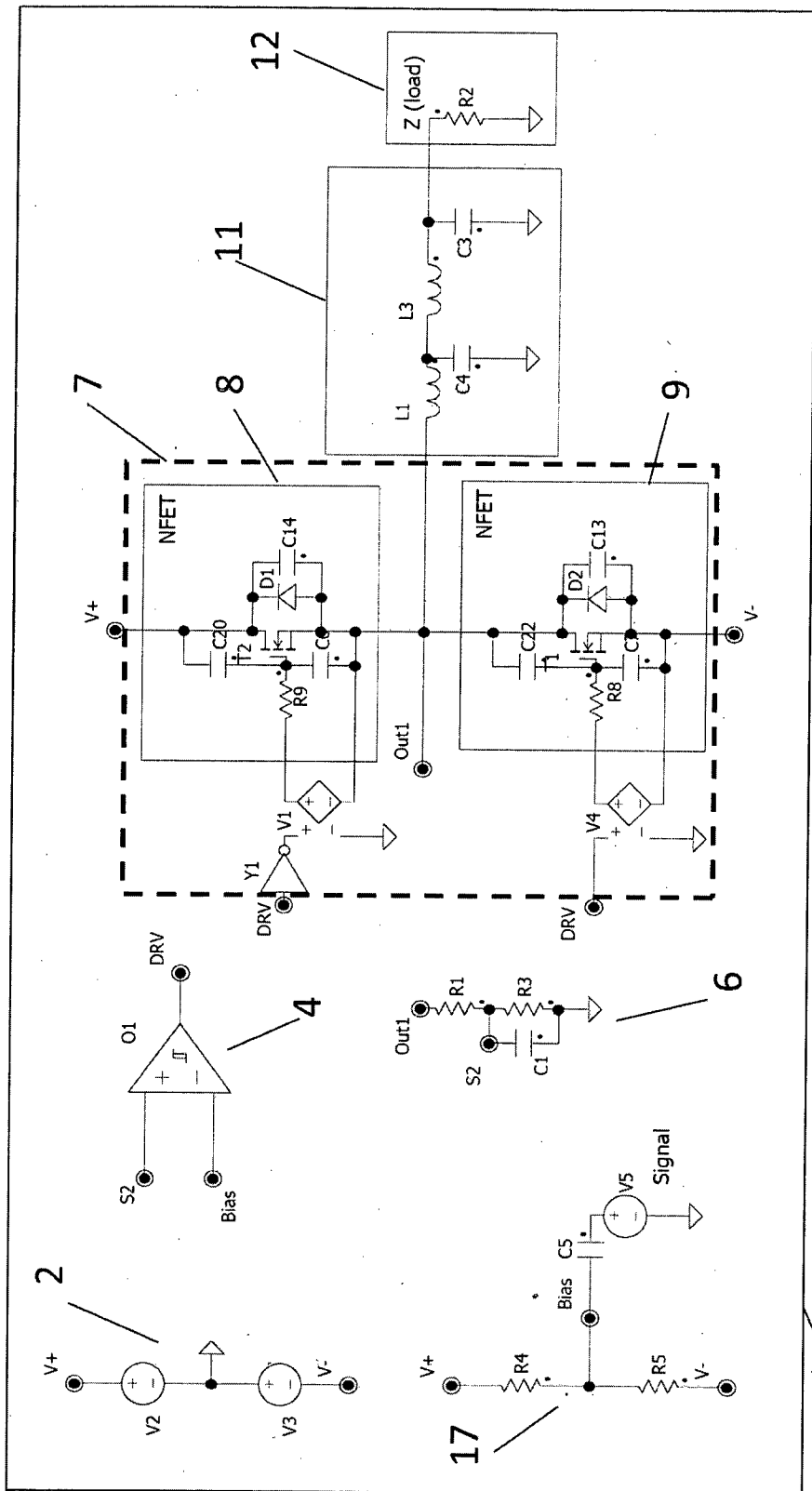


Figure 7

16

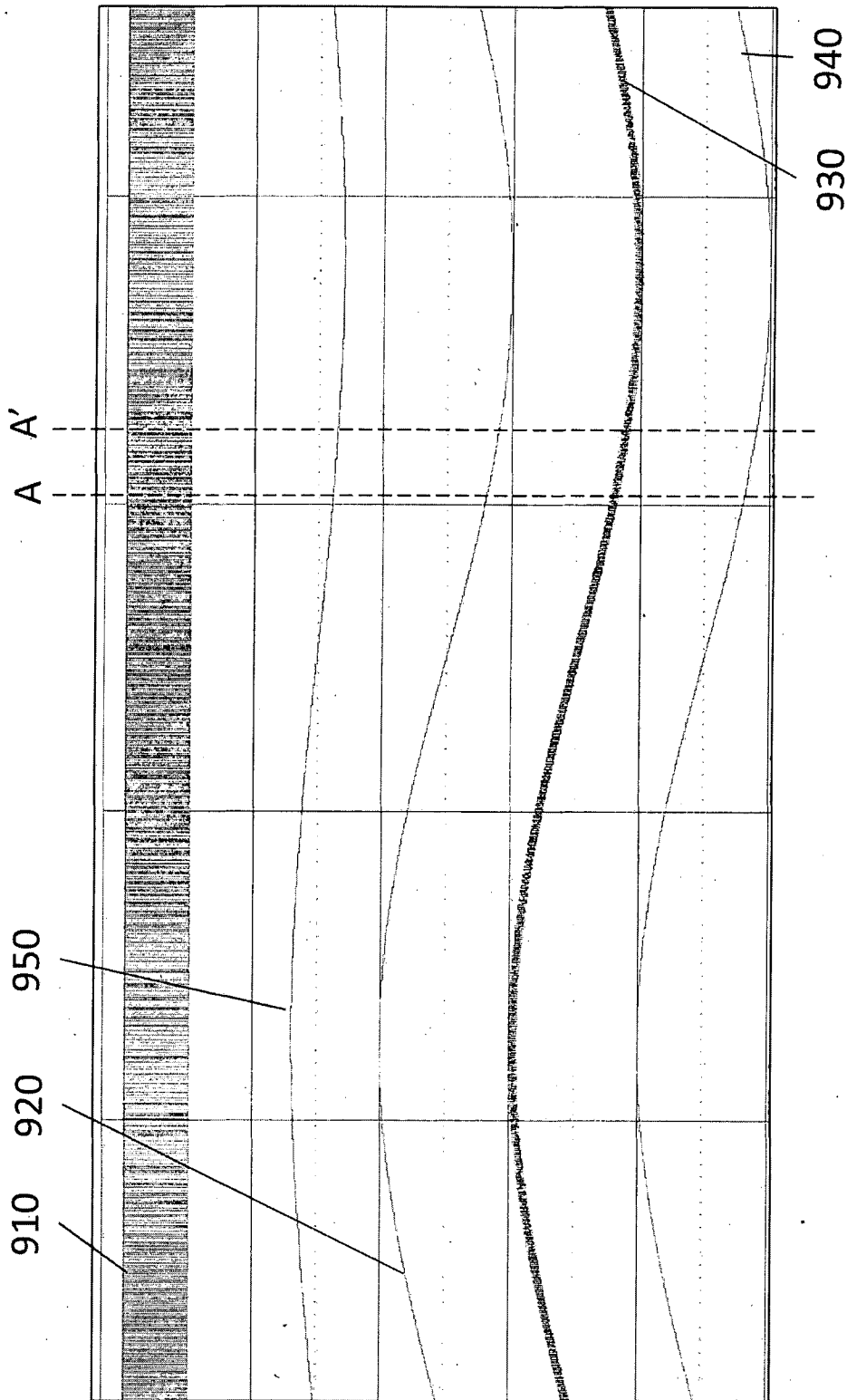


Figure 8

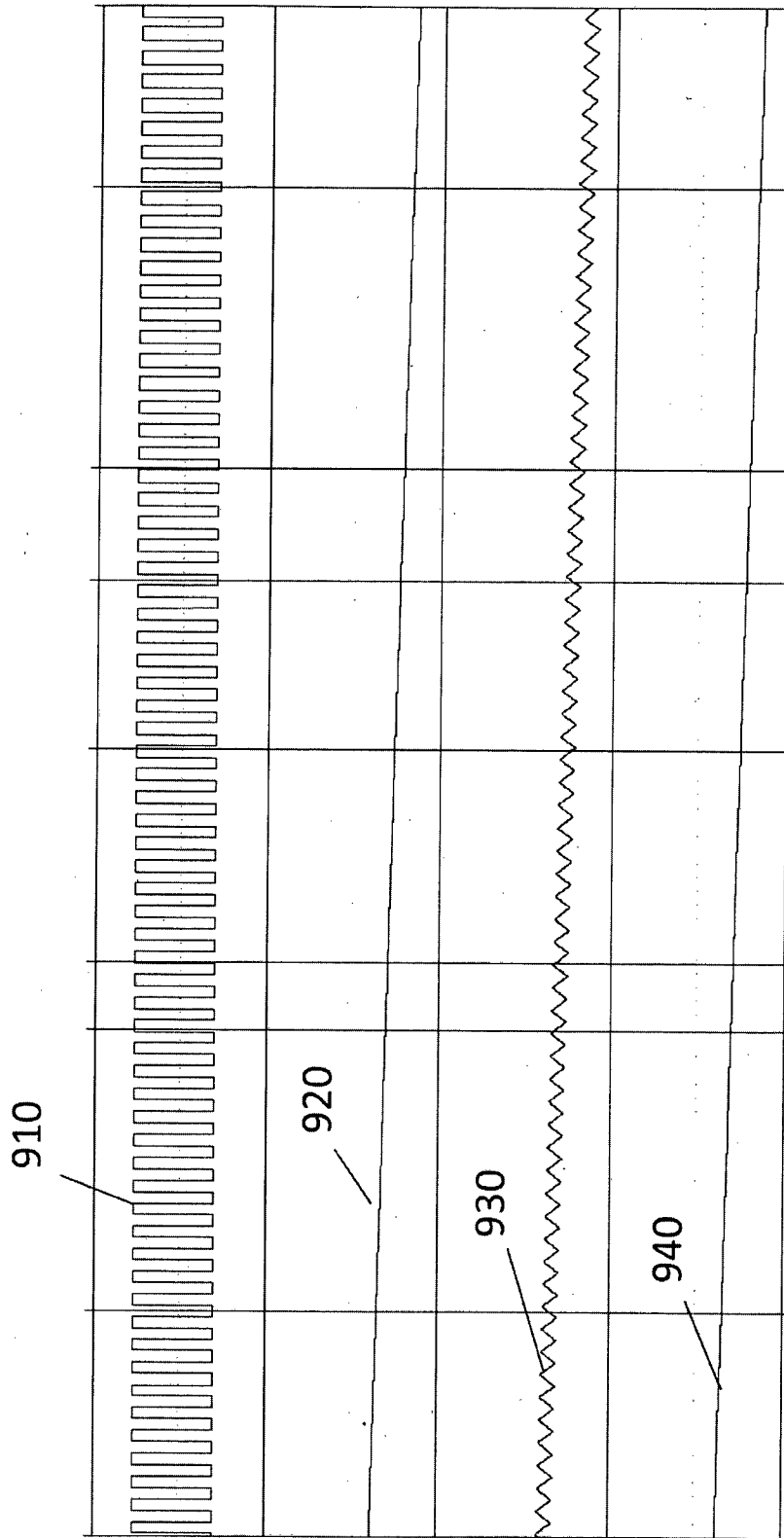


Figure 9

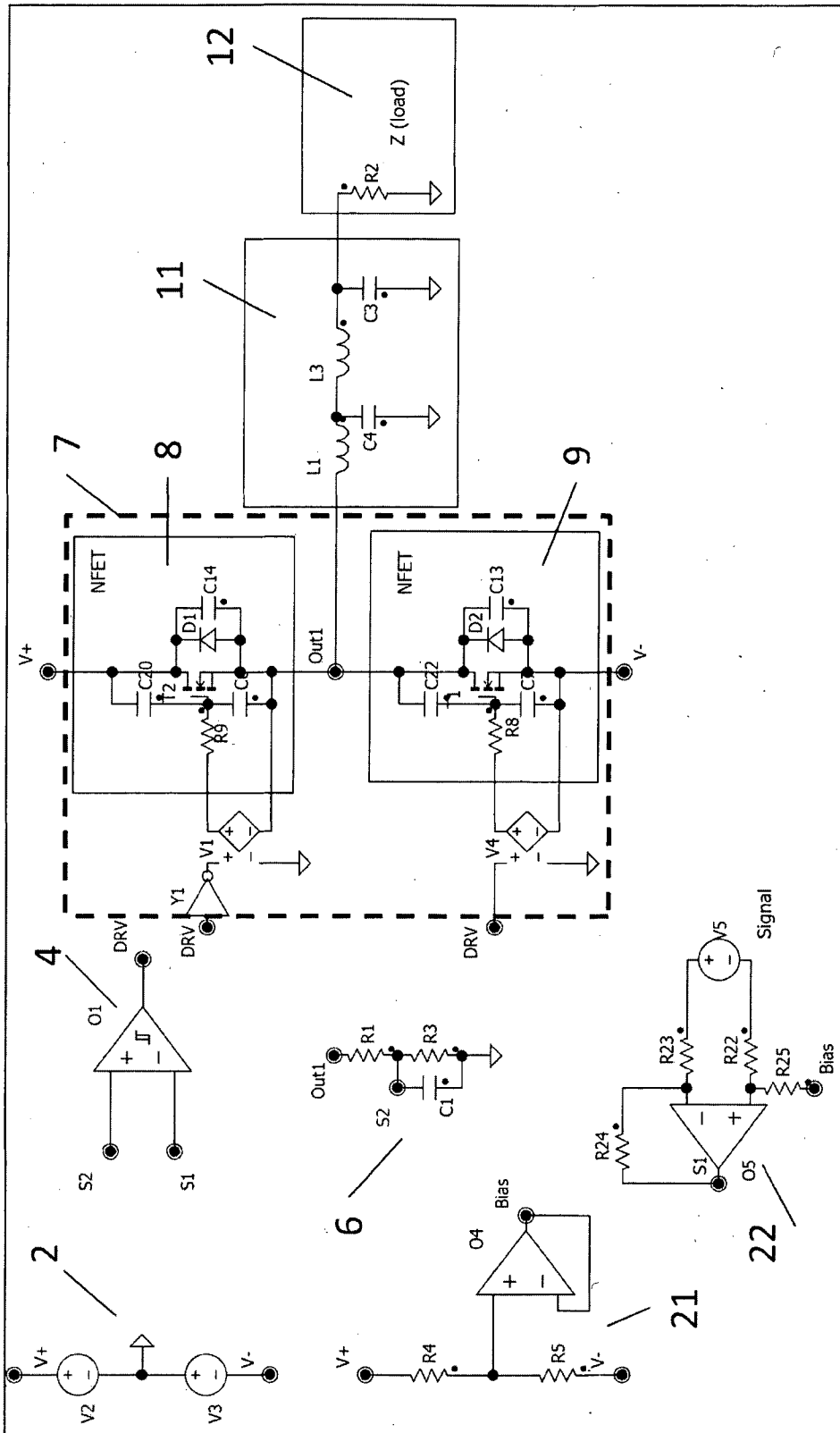


Figure 10

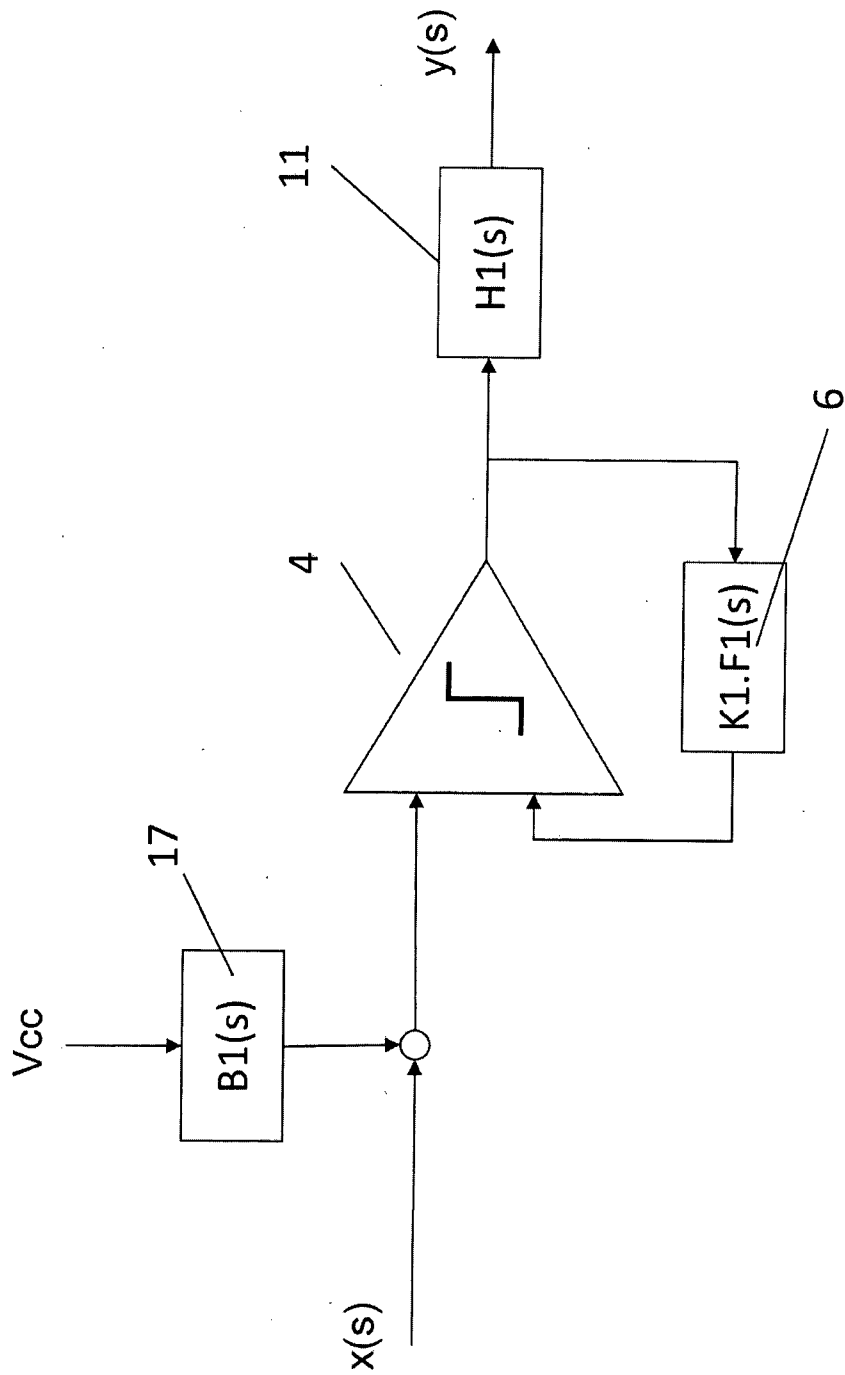


Figure 10A



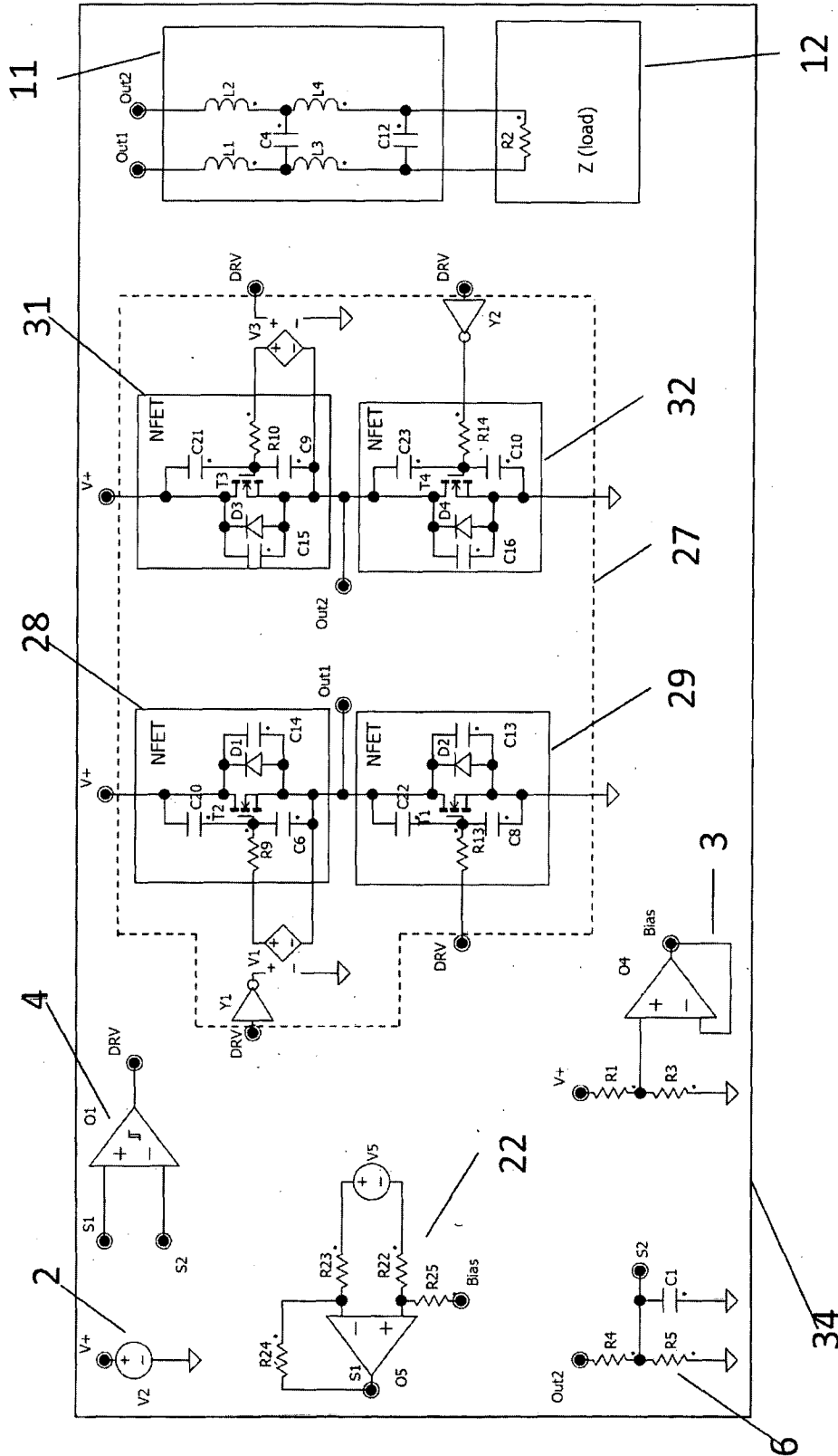


Figure 12

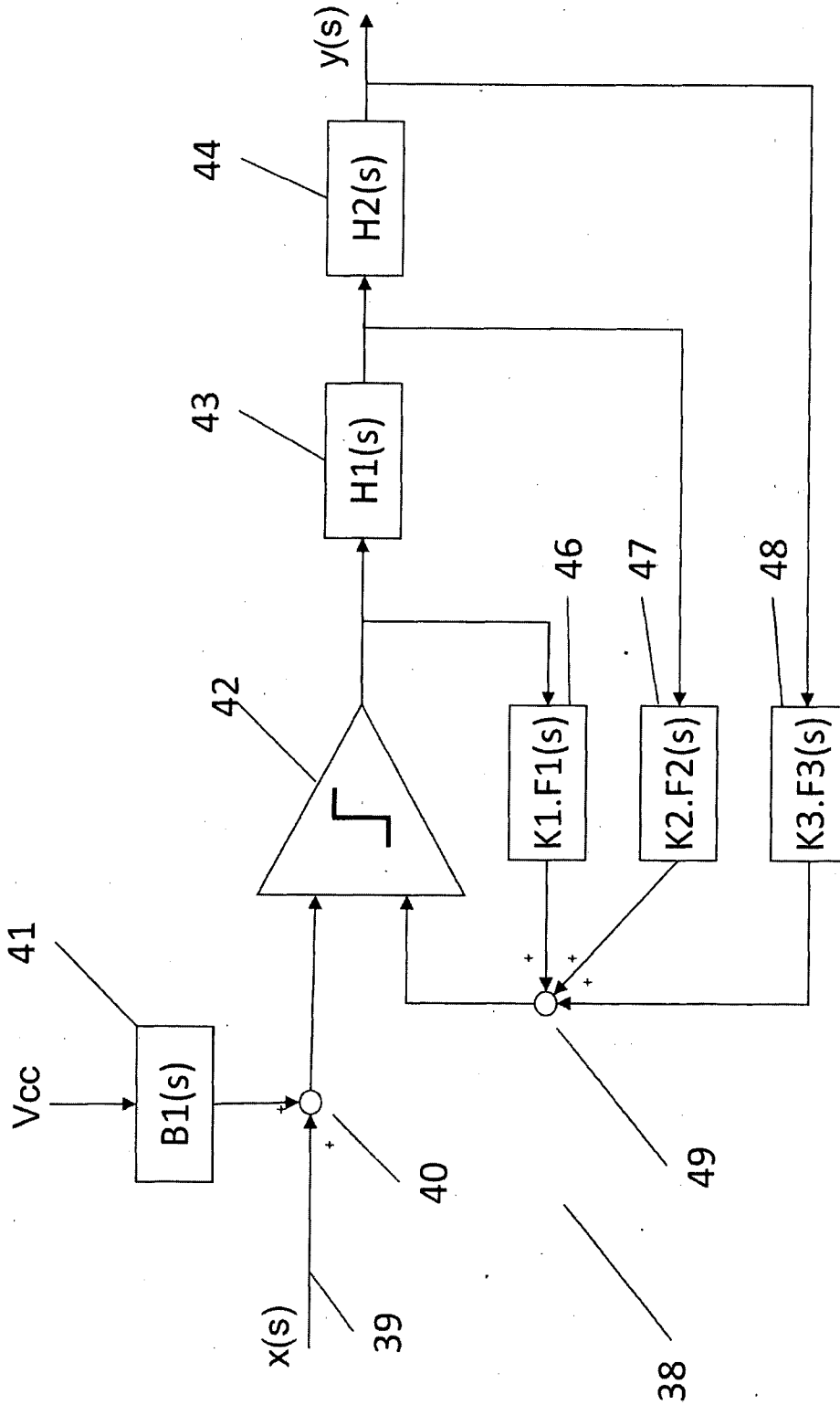


Figure 13



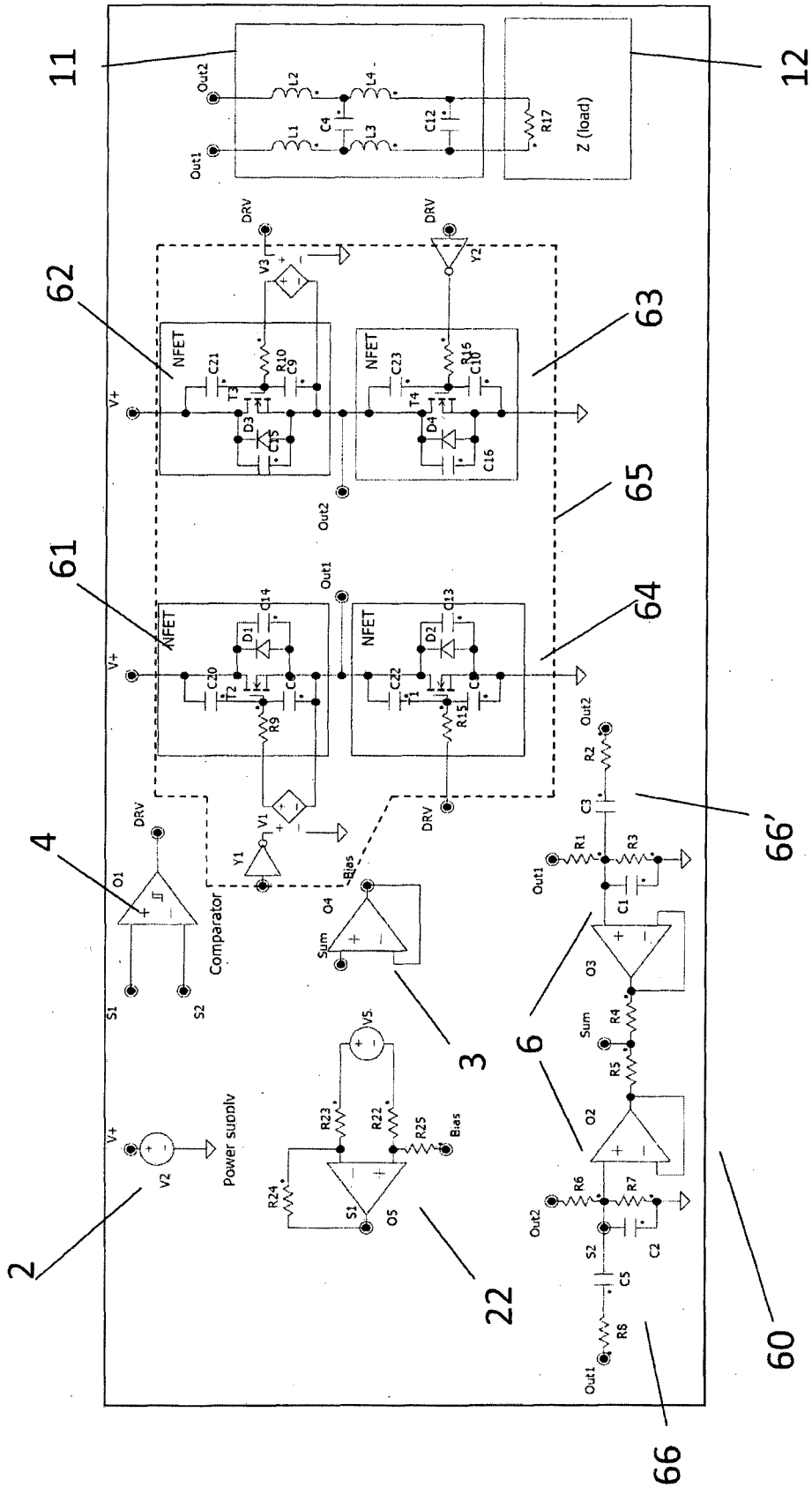


Figure 15

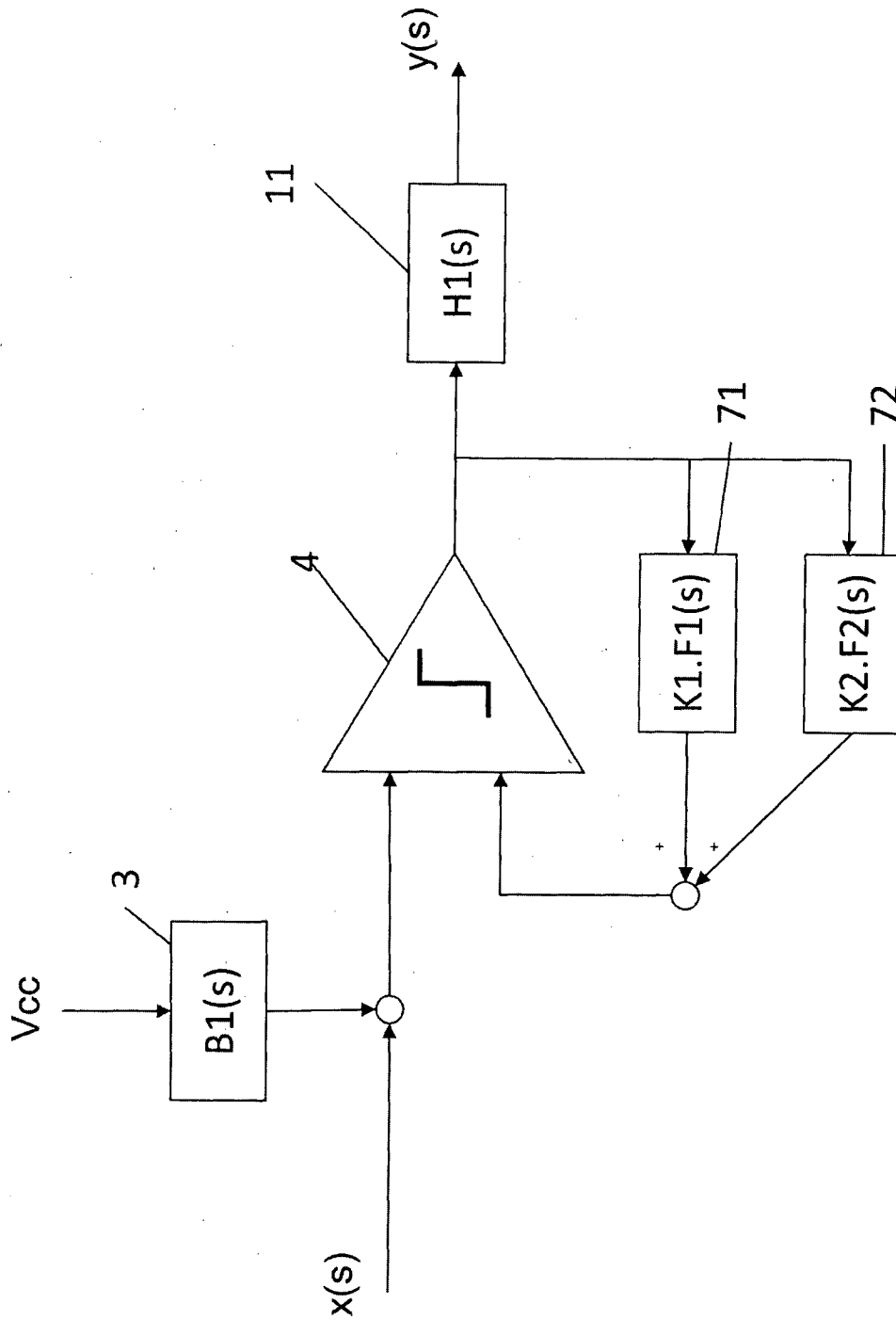


Figure 15A

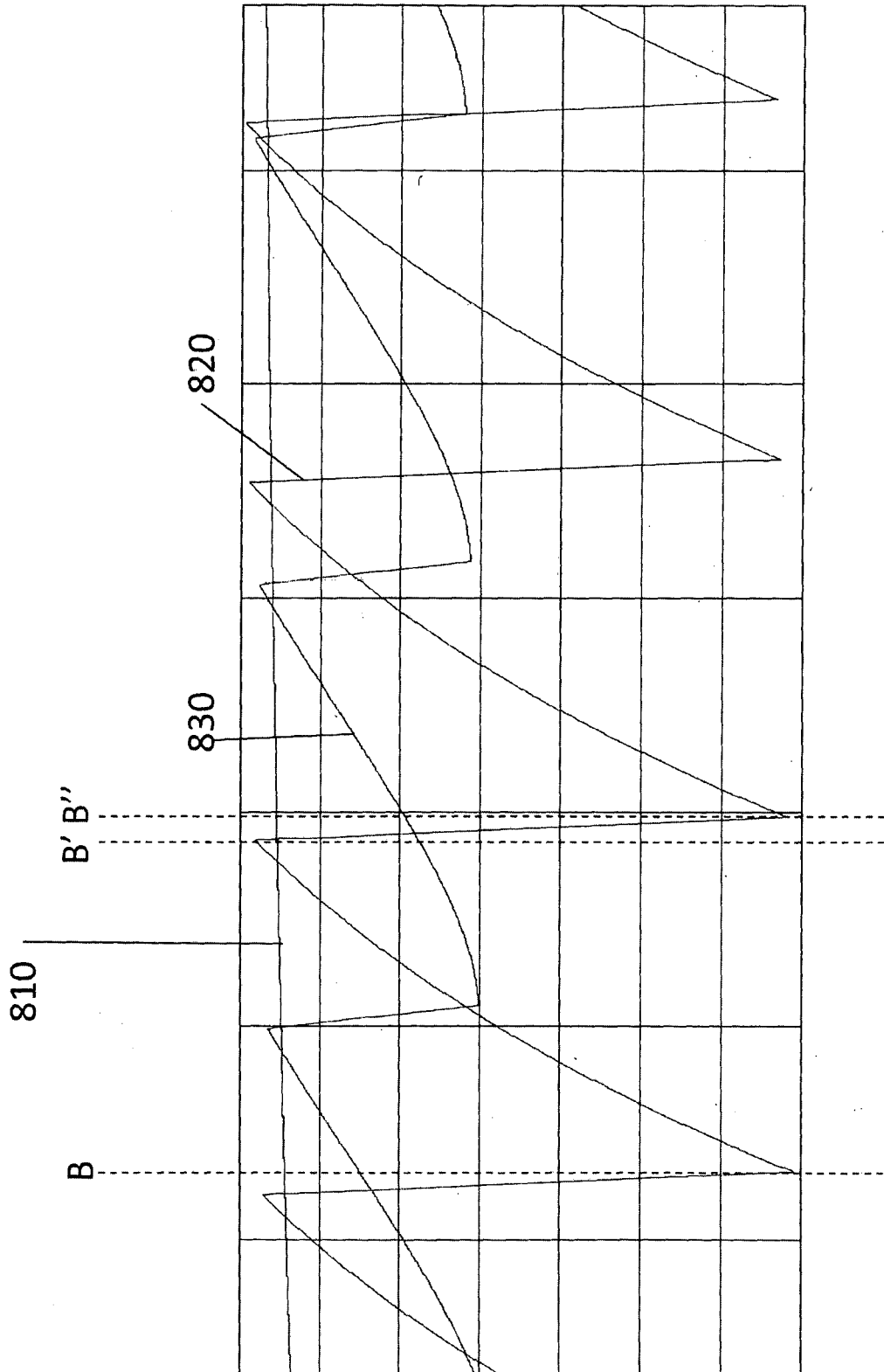


Figure 16

## INTERNATIONAL SEARCH REPORT

International application No.

**PCT/AU2013/000452**

## A. CLASSIFICATION OF SUBJECT MATTER

**H03F 3/38 (2006.01) H03K 7/00 (2006.01) H03F 3/217 (2006.01)**

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC, WPI: audio amplifier?, regulated power supply, pulse width modulator, lossy integrator, filter, comparator and similar terms.

GOOGLE PATENT: "pulse width modulator" "audio amplifier" integrator (also searched "lossy integrator") comparator

GOOGLE SCHOLAR: "pulse width modulator" "audio amplifier" integrator comparator

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
	Documents are listed in the continuation of Box C	



Further documents are listed in the continuation of Box C



See patent family annex

* Special categories of cited documents:		
"A" document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search  
28 June 2013Date of mailing of the international search report  
28 June 2013

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**INTERNATIONAL SEARCH REPORT**

International application No.

C (Continuation).

DOCUMENTS CONSIDERED TO BE RELEVANT

**PCT/AU2013/000452**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 7932778 B1 (CYRUSIAN) 26 April 2011 Col. 6 lines 10-47; Col. 7 lines 4-44; Col. 8 line 27- Col. 9 line 8; figs. 5, 8 and 9	1-17
X	US 2011/0095836 A1 (PUTZEYS) 28 April 2011 Paras [0004], [0045-0049], fig. 6	1-4

**INTERNATIONAL SEARCH REPORT**

Information on patent family members

International application No.

**PCT/AU2013/000452**

This Annex lists known patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

<b>Patent Document/s Cited in Search Report</b>		<b>Patent Family Member/s</b>	
<b>Publication Number</b>	<b>Publication Date</b>	<b>Publication Number</b>	<b>Publication Date</b>
US 7932778 B1	26 Apr 2011	US 7737776 B1	15 Jun 2010
		US 7932778 B1	26 Apr 2011
US 2011/0095836 A1	28 Apr 2011	EP 2269302 A1	05 Jan 2011
		JP 2011519224 A	30 Jun 2011
		US 2011095836 A1	28 Apr 2011
		US 8289097 B2	16 Oct 2012
		WO 2009131440 A1	29 Oct 2009

**End of Annex**