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(54) **Title**: TECHNIQUES FOR FORMING ELECTRICALLY CONDUCTIVE FEATURES WITH IMPROVED ALIGNMENT AND CAPACITANCE REDUCTION

Figure 11

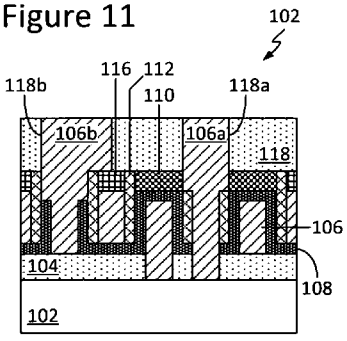
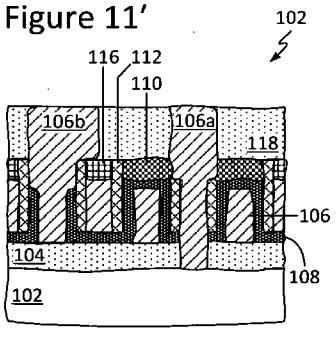


Figure 11'



(57) **Abstract**: Techniques are disclosed for forming electrically conductive features with improved alignment and capacitance reduction. In accordance with some embodiments, individual conductive features may be formed over a semiconductor substrate by a subtractive process (e.g., subtractive patterning). For a given feature, first and second barrier layers (conformal or otherwise) may be disposed along sidewalls thereof, and a helmet-like hardmask body may be disposed over a top surface thereof. Additional conductive features can be formed between existing features, using the barrier layers as alignment spacers, thereby halving (or otherwise reducing) feature pitch. A layer of another hardmask material may be disposed over the additionally formed features. That layer and the helmet-like hardmask bodies may be of different material composition, providing for etch selectivity with respect to one another. Additional layer(s) can be formed over the resultant topography, exploiting the hardmask etch selectivity in forming interconnects for adjacent integrated circuit layers.

WO 2017/111803 A1

TECHNIQUES FOR FORMING ELECTRICALLY CONDUCTIVE FEATURES WITH IMPROVED ALIGNMENT AND CAPACITANCE REDUCTION

BACKGROUND

In the manufacture of integrated circuits, interconnects may be formed over a semiconductor substrate using a copper-based damascene process. Such a process typically begins with a feature, such as a trench or through-hole, being etched into an insulator layer and filled with copper, resulting in a copper line or through-body via (TBV). Additional layers of insulator material and copper-filled features can be added, resulting in a multi-layer integrated circuit. With proper alignment, neighboring integrated circuit layers can be electrically connected by such interconnect features.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1–6 illustrate a process flow of fabricating an integrated circuit (IC) in accordance with an embodiment of the present disclosure.

Figure 7 illustrates a cross-sectional view of an IC configured in accordance with another embodiment of the present disclosure.

Figure 8 illustrates a cross-sectional view of an IC configured in accordance with another embodiment of the present disclosure.

Figure 9 illustrates a cross-sectional view of an IC after forming a hardmask layer, in accordance with an embodiment of the present disclosure.

Figure 10 illustrates a cross-sectional view of an IC configured in accordance with another embodiment of the present disclosure.

Figure 11 illustrates a cross-sectional view of an IC configured in accordance with another embodiment of the present disclosure.

Figure 11′ illustrates a cross-sectional view of an IC configured in accordance with another embodiment of the present disclosure.

Figures 12–17, in conjunction with Figures 1–2, illustrate a process flow of fabricating an IC in accordance with another embodiment of the present disclosure.

Figure 18 illustrates a cross-sectional view of an IC configured in accordance with another embodiment of the present disclosure.

Figure 19 illustrates a cross-sectional view of an IC configured in accordance with another embodiment of the present disclosure.

Figures 20–28 illustrate a process flow of fabricating an IC in accordance with another embodiment of the present disclosure.

Figure 29 illustrates a computing system implemented with integrated circuit structures or devices formed using the disclosed techniques in accordance with an example embodiment.

These and other features of the present embodiments will be understood better by reading the following detailed description, taken together with the figures herein described. In the drawings, each identical or nearly identical component that is illustrated in various figures may be represented by a like numeral. For purposes of clarity, not every component may be labeled in every drawing. Furthermore, as will be appreciated, the figures are not necessarily drawn to scale or intended to limit the described embodiments to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of the disclosed techniques may have less than perfect straight lines and right angles, and some features may have surface topography or otherwise be non-smooth, given real-world limitations of fabrication processes. In short, the figures are provided merely to show example structures.

DETAILED DESCRIPTION

Techniques are disclosed for forming electrically conductive features with improved alignment and capacitance reduction. The techniques may be implemented in a damascene process or a subtractive process. In more detail, and according to some embodiments, a plurality of conductive features may be formed over a semiconductor substrate by a damascene process, in which the individual features are formed directly within a dielectric layer that is then recessed. In other embodiments, a plurality of conductive features may be formed over a semiconductor substrate by a subtractive patterning process, in which a conductive material layer is patterned into the individual features. In either case, for a given feature, first and second barrier layers (which may be conformal or otherwise) may be disposed along sidewalls thereof, and a helmet-like (or otherwise cap-like) hardmask body may be disposed over a top surface thereof. In accordance with some embodiments, additional conductive features can be formed between existing features, using the barrier layers as alignment spacers. In this manner, the pitch of the features disposed over the substrate may be halved (or otherwise reduced). In some cases, a layer of another hardmask material may be disposed over the additionally formed features. In accordance with some embodiments, that second hardmask layer and the helmet-like hardmask bodies may be of different material composition, such that they exhibit etch selectivity with respect to one another. Additional layer(s) can be formed over the resultant topography, exploiting the etch selectivity of the hardmask materials in forming interconnects for adjacent

integrated circuit layers, as desired for a given target application or end-use. Numerous configurations and variations will be apparent in light of this disclosure.

General Overview

Existing approaches to addressing shorting margin and capacitance suffer from challenges related to reducing defects, preserving pattern fidelity, and minimizing damage to metal structures during etching. As device dimensions continue to scale down, interconnect features become narrower and formed closer together, exacerbating these and other non-trivial problems.

Thus, and in accordance with some embodiments of the present disclosure, techniques are disclosed for forming electrically conductive features with improved alignment and capacitance reduction. In accordance with some embodiments, a plurality of conductive features may be formed over a semiconductor substrate by either a damascene process, in which the individual features are formed directly within a dielectric layer that is then recessed, or a subtractive patterning process, in which a conductive material layer is patterned into the individual features. In either case, for a given feature, first and second barrier layers (which may be conformal or otherwise) may be disposed along sidewalls thereof, and a helmet-like or hat-like hardmask body may be disposed over a top surface thereof. In accordance with some embodiments, additional conductive features can be formed between existing features, using the barrier layers as alignment spacers. In this manner, the pitch of the features disposed over the substrate may be halved (or otherwise reduced). In some cases, a layer of another hardmask material may be disposed over the additionally formed features. In accordance with some embodiments, that second hardmask layer and the helmet-like hardmask bodies may be of different material composition, such that they exhibit etch selectivity with respect to one another. Additional layer(s) can be formed over the resultant topography, exploiting the etch selectivity of the hardmask materials in forming interconnects for adjacent integrated circuit layers, as desired for a given target application or end-use.

In accordance with some embodiments, the disclosed techniques can be used, for example, in forming a first plurality (e.g., a first half or other sub-set) of electrically conductive features all at once, and then forming a second plurality (e.g., a second half or other sub-set) of electrically conductive features all at once. Between patterning the individual pluralities, spacer and hardmask deposition processes described herein may be utilized to provide for architectures having features with high etch selectivity, preferential alignment, or both. As will be appreciated in light of this disclosure, the disclosed techniques can be employed with respect to any of a wide

range of conductive feature configurations, including, for example, interconnects, trenches, vias, and plug cuts, just to name a few.

In some cases, use of the disclosed techniques may provide for improved pattern fidelity, which may result in improved shorting margin by reducing the risk of shorting to the wrong conductive line. In some cases, patterning alternating conductive features, for example, at a pitch of $2x$ rather than a pitch of x, as described herein, may decrease the risk of shorting to the wrong conductive feature. Furthermore, in some instances, preservation of a hardmask layer configured as described herein over the top surfaces of conductive features may serve to increase the shorting margin with respect to conductive features of an overlying layer (e.g., vias or other interconnects in a superjacent layer). In some cases, the disclosed techniques can be utilized, for example, in patterning interconnects at tight pitch with improved etch placement error (EPE). In some cases, use of the disclosed techniques may serve to reduce the aspect ratio for metal (or other conductive material) deposition, because additional hardmasks may be patterned after the first set of conductive features. In some cases, use of the disclosed techniques may provide for staggering the heights of conductive features (e.g., alternating lines or trenches), which may serve to reduce capacitance for the host IC as compared to traditional architectures.

In accordance with some embodiments, use of the disclosed techniques may be detected, for example, by any one, or combination, of scanning electron microscopy (SEM), transmission electron microscopy (TEM), or other suitable inspection of a given integrated circuit or other semiconductor structure having any one, or combination, of: (1) the presence of multiple spacer materials, which spacers may be vertically and/or horizontally oriented, in the final interconnect stack; and (2) alternating conductive features (e.g., lines or trenches) of different heights.

Damascene Techniques and Structures

Figures 1–6 illustrate a process flow of fabricating an integrated circuit (IC) 100 in accordance with an embodiment of the present disclosure. The process may begin as in Figure 1, which illustrates a cross-sectional view of an IC 100 configured in accordance with an embodiment of the present disclosure. As can be seen, IC 100 includes a semiconductor substrate 102, which may have any of a wide range of configurations. For instance, semiconductor substrate 102 may be configured as any one, or combination, of a bulk semiconductor substrate, a semiconductor-on-insulator (XOI, where X represents a semiconductor material) structure such as silicon-on-insulator (SOI), a semiconductor wafer, and a multi-layered structure. In accordance with some embodiments, semiconductor substrate 102 may be formed from any one, or combination, of semiconductor materials, such as silicon (Si), germanium (Ge), and silicon germanium (SiGe), among others. In some cases, semiconductor

substrate 102 may include one or more conductive features (e.g., interconnects) disposed therein. It should be noted that substrate 102 need not be formed from a semiconductor at all, in some embodiments. Other suitable materials and configurations for semiconductor substrate 102 will depend on a given application and will be apparent in light of this disclosure.

IC 100 also includes a dielectric layer 104 disposed over semiconductor substrate 102. Dielectric layer 104 may be formed from any of a wide range of dielectric materials. For instance, in some embodiments, dielectric layer 104 may be formed from an oxide or carbon (C)-doped oxide, such as silicon oxide (SiO_2), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), zirconium oxide (ZrO_2), tantalum oxide (Ta_2O_5), titanium oxide (TiO_2), or lanthanum oxide (La_2O_3), among others. In some embodiments, dielectric layer 104 may be formed from a nitride, such as silicon nitride (Si_3N_4), or an oxynitride, such as silicon oxynitride (SiON), a carbide, such as silicon carbide (SiC), or an oxycarbonitride, such as silicon oxycarbonitride (SiOCN). In some embodiments, dielectric layer 104 may be formed from a combination of any of the aforementioned materials. In some embodiments, dielectric layer 104 may be a homogeneous dielectric structure (e.g., comprising only a single dielectric material), whereas in other embodiments, dielectric layer 102 may be a heterogeneous dielectric structure (e.g., comprising portions of different dielectric material composition). In some cases, dielectric layer 104 may be configured to serve, at least in part, as an inter-layer dielectric (ILD) for IC 100. In some instances, dielectric layer 104 may be configured to provide shallow trench isolation (STI) for IC 100.

Dielectric layer 104 can be formed over semiconductor substrate 102 via any suitable standard, custom, or proprietary technique(s), as will be apparent in light of this disclosure. In accordance with some embodiments, dielectric layer 104 may be formed via any one, or combination, of a physical vapor deposition (PVD) process, such as sputter deposition, a spin-on deposition (SOD) process, and a chemical vapor deposition (CVD) process, such as plasma-enhanced CVD (PECVD). The dimensions of dielectric layer 104 may be customized, as desired for a given target application or end-use. In some cases, dielectric layer 104 may have a thickness, for example, in the range of about 50–150 nm (e.g., about 50–100 nm, about 100–150 nm, or any other sub-range in the range of about 50–150 nm). Other suitable materials, formation techniques, and configurations for dielectric layer 104 will depend on a given application and will be apparent in light of this disclosure.

In accordance with some embodiments, dielectric layer 104 may be patterned with one or more features 104a, which may be of any of a wide range of configurations. For instance, in some cases, a given feature 104a may be a trench (single-damascene or dual-damascene), a plug cut, or other opening or recess that extends only part way through the entire thickness of

dielectric layer 104 (e.g., such that it lands over, but not on, underlying semiconductor substrate 102). In other cases, a given feature 104a may be a through-hole or other opening or recess that extends through the entire thickness of dielectric layer 104 (e.g., such that it lands on underlying semiconductor substrate 102). A given feature 104a may be formed via any suitable standard, custom, or proprietary lithography and etch technique(s), as will be apparent in light of this disclosure. In accordance with some embodiments, a given feature 104a may be formed via an etch-and-clean process, which may involve a wet etch or dry etch (or both), the etch chemistry of which may be customized based, at least in part, on the material composition of dielectric layer 104 and semiconductor substrate 102. The dimensions and geometry of a given feature 104a may be customized, as desired for a given target application or end-use. In some cases, a given feature 104a may have substantially vertical sidewalls (e.g., within about 2° of being vertically straight). In other instances, a given feature 104a may have tapered sidewalls (e.g., outside of about 2° of being vertically straight). The pitch or other spacing of neighboring features 104a may be customized. As shown in the figures, features 104a may be patterned, for instance, at a pitch of $2x$, in accordance with some embodiments. Other suitable configurations and formation techniques for feature(s) 104a will depend on a given application and will be apparent in light of this disclosure.

In accordance with some embodiments, an electrically conductive feature 106 may be disposed within a given feature 104a of dielectric layer 104. In some cases, a given electrically conductive feature 106 may be formed over semiconductor substrate 102, such that it is in contact with or otherwise disposed over an upper surface of semiconductor substrate 102. In some other cases, a given electrically conductive feature 106 may be formed at least partially within semiconductor substrate 102, such that it at least partially extends below an upper surface of semiconductor substrate 102. In some still other cases, a given electrically conductive feature 106 may be formed both over and at least partially within semiconductor substrate 102, such that it is at least partially in contact with or otherwise disposed over an upper surface of semiconductor substrate 102 and at least partially extends below the upper surface of semiconductor substrate 102. Numerous configurations and variations will be apparent in light of this disclosure.

A given conductive feature 106 may be formed from any of a wide range of electrically conductive materials. For instance, in some embodiments, a given conductive feature 106 may be formed from any one, or combination, of electrically conductive metal, such as copper (Cu), aluminum (Al), tungsten (W), nickel (Ni), cobalt (Co), silver (Ag), gold (Au), titanium (Ti), and tantalum (Ta), among others. A given conductive feature 106 may be formed via any suitable standard, custom, or proprietary technique(s), as will be apparent in light of this disclosure. In

accordance with some embodiments, a given conductive feature 106 may be formed via any one, or combination, of an electroplating process, an electroless deposition process, an atomic layer deposition (ALD) process, a PVD process, and a CVD process, among others.

The dimensions and geometry of a given conductive feature 106 may be customized, as desired for a given target application or end-use, and in some cases may depend at least in part on the dimensions and geometry of a given host feature 104a. In some cases, a given conductive feature 106 may be of generally rectangular or square cross-sectional geometry. In some other cases, a given conductive feature 106 may be of generally trapezoidal cross-sectional geometry. In some instances, a given conductive feature 106 may have one or more curvilinear surfaces (top, sidewalls, or other). In some instances, a given conductive feature 106 may have angled or tapered sidewalls, whereas in some other instances, a given conductive feature 106 may have substantially straight, vertical sidewalls. The pitch (P_1) or other spacing of neighboring conductive features 106 may be customized and may depend, at least in part on the pitch of their host features 104a. Other suitable material, formation techniques, and configurations for conductive feature(s) 106 will depend on a given application and will be apparent in light of this disclosure.

The process may continue as in Figure 2, which illustrates a cross-sectional view of the IC 100 of Figure 1 after recessing dielectric layer 104, in accordance with an embodiment of the present disclosure. Dielectric layer 104 may be recessed via any suitable standard, custom, or proprietary technique(s), as will be apparent in light of this disclosure. In some cases, recessing of dielectric layer 104 may be performed via any one, or combination, of an isotropic etch process and an anisotropic etch process. A given etch process may involve a wet etch or a dry etch (or both), and the particular etch chemistry employed by a given applied etch process may be customized, as desired for a given target application or end-use. In an example case, an air gap etch process may be utilized in recessing dielectric layer 104. The depth and degree of recessing of dielectric layer 104 can be controlled to provide a given amount of symmetry/asymmetry and isotropy/anisotropy desired.

Note that, as generally shown in Figure 2, at least one conductive feature 106 (e.g., the middle illustrated conductive feature 106) has dielectric material of dielectric layer 104 in contact with its sidewalls, whereas at least one other conductive feature 106 (e.g., the leftmost and/or rightmost illustrated conductive features 106) do not have dielectric material of dielectric layer 104 in contact with its sidewalls. This may result, at least in some cases, because any two conductive features 106 may be staggered with respect to one another over underlying semiconductor substrate 102, in accordance with some embodiments. Consider Figure 1, where at least one conductive feature 106 is at a different height with respect to semiconductor

substrate 102 than at least one other conductive feature 106. In accordance with some embodiments, the recessing of dielectric layer 104 can be optimized (or otherwise customized) for a given amount of staggering between adjacent conductive features 106. In accordance with some embodiments, dielectric layer 104 may be recessed, for example, until the bottom of a given conductive feature 106 is reached, such as is generally shown in Figure 2. In accordance with an embodiment, the recessing of dielectric layer 104 can be performed such that a given feature 104a lands on a trench stop, which may improve etch control. To that end, in some cases, dielectric layer 104 may be formed as a multi-layer structure (e.g., bi-layer, tri-layer, or other quantity of constituent layers), wherein the constituent layers are of different material composition, at least one of which is configured to serve as an etch stop layer.

The process may continue as in Figure 3, which illustrates a cross-sectional view of the IC 100 of Figure 2 after forming a barrier layer 108, in accordance with an embodiment of the present disclosure. Barrier layer 108 may be configured, in accordance with some embodiments, to serve, at least in part, as a spacer layer for IC 100 (or other host IC). To that end, the material composition of barrier layer 108 may be customized, as desired for a given target application or end-use. In some cases, barrier layer 108 may be formed from any one, or combination, of oxides, such as, for example, silicon oxide (SiO_2), aluminum oxide (Al_2O_3), and titanium oxide (TiO_2), among others. In a more general sense, and in accordance with some embodiments, barrier layer 108 may be formed, in part or in whole, from any suitable low-κ metal oxide having a dielectric constant (κ) less than or equal to about 5.0.

Barrier layer 108 may be formed via any suitable standard, custom, or proprietary technique(s), as will be apparent in light of this disclosure. In accordance with some embodiments, barrier layer 108 may be formed via any one, or combination, of a chemical vapor deposition (CVD) process, such as a plasma-enhanced CVD (PECVD) process, and an atomic layer deposition (ALD) process, among others. The dimensions and geometry of barrier layer 108 may be customized, as desired for a given target application or end-use, and may depend, at least in part, on at least one of the pitch P_1 of conductive features 106 and the dimensions of barrier layer 112 (discussed below). In some cases, barrier layer 108 may have a thickness, for example, in the range of about 0.25–0.5 times the x of pitch P_1 (e.g., about 0.25–0.375 times x, about 0.375–0.5 times x, or any other sub-range in the range of about 0.25–0.5 times x). In some instances, barrier layer 108 may have a substantially uniform thickness over the topography provided by dielectric layer 104 and conductive feature(s) 106, whereas in some other instances, barrier layer 108 may have a non-uniform or otherwise varying thickness over such topography (e.g., a first portion of barrier layer 108 may have a thickness within a first range, whereas a second portion thereof may have a thickness within a second, different range). In some

instances, barrier layer 108 may be substantially conformal to its underlying topography (e.g., over dielectric layer 104 and extending up sidewalls and over top surfaces of conductive features 106). Other suitable materials, formation techniques, and configurations for barrier layer 108 will depend on a given application and will be apparent in light of this disclosure.

The process may continue as in Figure 4, which illustrates a cross-sectional view of the IC 100 of Figure 3 after forming a hardmask layer 110, in accordance with an embodiment of the present disclosure. The material composition of hardmask layer 110 may be customized, as desired for a given target application or end-use. In some embodiments, hardmask layer 110 may be formed from any one, or combination, of titanium nitride (TiN), silicon nitride (Si_3N_4), silicon dioxide (SiO_2), silicon carbonitride (SiCN), and silicon oxynitride (SiO_xN_y), among others.

Hardmask layer 110 may be formed via any suitable standard, custom, or proprietary technique(s), as will be apparent in light of this disclosure. In accordance with some embodiments, hardmask layer 110 may be formed via any one, or combination, of non-conformal deposition processes, such as, for example, a PVD process, such as a sputter deposition process, and a CVD process, among others. As will be appreciated in light of this disclosure, use of a non-conformal process may cause the hardmask material(s) to deposit substantially (e.g., only, principally, or otherwise primarily) over the tops of conductive features 106 rather than in between them. In some cases, a given hardmask body may extend beyond (e.g., overhang) the top surface of an underlying electrically conductive feature 106 as far as the full thickness (or less than the full thickness) of an underlying barrier layer 108 (e.g., such as can be seen generally in Figures 4, 13, and 23). In some cases, a given hardmask body may extend beyond (e.g., overhang) the top surface of an underlying electrically conductive feature 106, for example, by less than about 25%, less than about 20%, less than about 15%, less than about 10%, less than about 5%, or less than about 1% of its width. In some other cases, a given hardmask body may not extend beyond (e.g., may not overhang) the top surface of an underlying electrically conductive feature 106. In forming hardmask layer 110, one or more etch-and-clean processes optionally may be employed, in accordance with some embodiments. In an example case, a wet clean process may be used to ensure that no hardmask material remains at the bottom of the space between neighboring conductive features 106.

The dimensions and geometry of hardmask layer 110 may be customized, as desired for a given target application or end-use. In some cases, hardmask layer 110 may have a thickness, for example, in the range of about 0.25–0.5 times the x of pitch P_1 (e.g., about 0.25–0.375 times x, about 0.375–0.5 times x, or any other sub-range in the range of about 0.25–0.5 times x). In some example cases, hardmask layer 110 may have a thickness, for instance, in the range of

about 5–20 nm (e.g., about 5–10 nm, about 10–15 nm, about 15–20 nm, or any other sub-range in the range of about 5–20 nm). In some instances, hardmask layer 110 may have a substantially uniform thickness over its underlying topography, whereas in some other instances, hardmask layer 110 may have a non-uniform or otherwise varying thickness over such topography (e.g., a first portion of hardmask layer 110 may have a thickness within a first range, whereas a second portion thereof may have a thickness within a second, different range). As can be seen from Figure 4, in accordance with some embodiments, hardmask layer 110 may be formed in a manner such that it comprises one or more constituent hardmask bodies. In some cases, a given hardmask body may be configured as a generally helmet-like (or otherwise cap-like) portion disposed over the topography provided by underlying portion(s) of barrier layer 108 and conductive feature(s) 106. In some cases, a given constituent hardmask body of hardmask layer 110 may be of generally rectangular or square cross-sectional geometry. In some other cases, a given constituent hardmask body of hardmask layer 110 may be of generally trapezoidal cross-sectional geometry. In some instances, a given constituent hardmask body of hardmask layer 110 may have one or more curvilinear surfaces (top, sidewalls, or other). In some instances, a given constituent hardmask body of hardmask layer 110 may have angled or tapered sidewalls, whereas in some other instances, a given constituent hardmask body of hardmask layer 110 may have substantially straight, vertical sidewalls.

In some cases, the constituent hardmask bodies (e.g., helmet-like hardmask bodies) of hardmask layer 110 may be formed in a manner that allows them to be electrically leaky. In other cases, however, such hardmask bodies may be formed in a manner such that they are not (or are otherwise only negligibly) electrically leaky. Other suitable materials, formation techniques, and configurations for hardmask layer 110 will depend on a given application and will be apparent in light of this disclosure.

The process may continue as in Figure 5, which illustrates a cross-sectional view of the IC 100 of Figure 4 after forming a barrier layer 112, in accordance with an embodiment of the present disclosure. Barrier layer 112 may be configured, in accordance with some embodiments, to serve, at least in part, as a spacer layer for IC 100 (or other host IC). As will be appreciated in light of this disclosure, barrier layer 112 may be formed with any of the example materials, techniques, and configurations discussed above, for instance, with respect to barrier layer 108. In some embodiments, barrier layer 112 may be of different material composition than barrier layer 108. In some embodiments, barrier layer 112 may have a thickness, for example, in the range of about 0.1–0.25 times the x of pitch P_1 (e.g., about 0.1–0.2 times x, about 0.15–0.25 times x, or any other sub-range in the range of about 0.1–0.25 times x). In some instances, barrier layer 112 may have a substantially uniform thickness over the topography provided by

hardmask layer 110 and barrier layer 108, whereas in some other instances, barrier layer 112 may have a non-uniform or otherwise varying thickness over such topography (e.g., a first portion of barrier layer 112 may have a thickness within a first range, whereas a second portion thereof may have a thickness within a second, different range). In some instances, barrier layer 112 may be substantially conformal to its underlying topography.

In forming barrier layer 112, it may be desirable to remove portions that deposit over hardmask layer 110, to ensure that the upper surfaces of the constituent hardmask bodies of hardmask layer 110 remain exposed. Also, it may be desirable to remove portions of barrier layer 112 that deposit over portions of barrier layer 108 between neighboring conductive features 106. To these ends, partial removal of barrier layer 112 may be performed via any suitable standard, custom, or proprietary directional etch technique(s), as will be apparent in light of this disclosure.

As can be seen from Figure 5, for example, barrier layer 112 may be formed, in accordance with some embodiments, so as to extend from barrier layer 108, along sidewalls of conductive features 106, and along sidewalls of the constituent hardmask bodies of hardmask layer 110. In some instances, barrier layer 112 may extend up the full height of barrier layer 108 and hardmask layer 110, whereas in some other instances, barrier layer 112 may extend up less than a full height thereof. As can be seen further from Figure 5, a feature 114a may exist between neighboring conductive features 106 as a result of the particular interfacing of barrier layers 112 and 108 between such conductive features 106. Other suitable materials, formation techniques, and configurations for barrier layer 112 will depend on a given application and will be apparent in light of this disclosure.

The process may continue as in Figure 6, which illustrates a cross-sectional view of the IC 100 of Figure 5 after forming a feature 114b from a given feature 114a, in accordance with an embodiment of the present disclosure. As can be seen, a given feature 114a may undergo additional patterning, for example, to provide a feature 114b. In some cases, a plurality of features 114b may be formed, for provision of a second set of conductive features 106 (e.g., the first set being formed as discussed above with reference to Figure 1). To these ends, a given feature 114b may be formed with any of the example techniques and configurations discussed above, for instance, with respect to features 104a, in accordance with some embodiments. In some cases, a given feature 114b may be formed so as to extend all the way down to a top surface of underlying semiconductor substrate 102, passing through the full local thickness of each of barrier layer 108 and dielectric layer 104, for example. A given feature 114b may be formed as, for example, a trench, through-hole, plug cut, via, or any other feature, as desired for a given target application or end-use. In accordance with some embodiments, features 114b (and

114a, discussed above) may be patterned on alternate trenches, such that the pitch P_1 of IC 100 is about halved (e.g., as generally discussed below with reference to Figure 7). The dimensions and geometry of a given feature 114b (and 114a) may depend, at least in part, on the dimensions of barrier layers 112 and 108, which may define the dimensional confines for such features 114b (and 114a). For instance, a first portion of barrier layer 112 adjacent a sidewall of a first conductive feature 106 and a second portion of barrier layer 112 adjacent a sidewall of a neighboring conductive feature 106 may serve to protect those portions of IC 100, while providing for directional formation of a given feature 114b (or 114a) over IC 100.

At this point in the process flow, there are a wide range of options for how to proceed with fabrication. For instance, consider Figure 7, which illustrates a cross-sectional view of an IC 101 configured in accordance with an embodiment of the present disclosure. As can be seen here, all (or some sub-set) of the features 114a and 114b of IC 100 may be filled with an electrically conductive material, in accordance with some embodiments. In so doing, the resultant IC 101 may have conductive features 106 of pitch P_2, which may be a fraction of the original pitch P_1 of IC 100. In an example case, pitch P_2 may be about one-half of pitch P_1 (e.g., if $P_1 = 2x$, then $P_2 = x$). In some cases, the newly formed conductive features 106 may be of the same material composition as the original conductive features 106 previously formed. In other cases, different electrically conductive materials may be employed, such that IC 101 hosts one or more conductive features 106 of a first material composition and one or more conductive features 106 of a second, different material composition.

In some cases, after filling all (or some sub-set) of features 114a and 114b, IC 101 optionally may undergo any one, or combination, of a chemical-mechanical planarization (CMP) process and an etch-and-clean process, for example, to remove any undesired portion(s) of barrier layer 112, hardmask layer 110, and barrier layer 108, as well as any excess (e.g., overburden) of conductive features 106 that may be present. In other cases, however, hardmask layer 110 may be allowed to remain over IC 101.

In other cases, after filling all (or some sub-set) of features 114a and 114b, IC 101 optionally may undergo a recessing process in which conductive feature(s) 106 are recessed to below the height of barrier layer 112 and hardmask layer 110. For instance, consider Figure 8, which illustrates a cross-sectional view of an IC 102 configured in accordance with an embodiment of the present disclosure. Recessing of conductive feature(s) 106 may be performed via any suitable standard, custom, or proprietary etch-and-clean technique(s), as will be apparent in light of this disclosure.

In some cases, after recessing conductive features 106 as in Figure 8, IC 102 optionally may undergo one or more additional fabrication processes. For instance, consider Figure 9,

which illustrates a cross-sectional view of an IC 102 after forming a hardmask layer 116, in accordance with an embodiment of the present disclosure. As can be seen, hardmask layer 116 may be formed within any one or more desired features 114a and 114b, over conductive features 106, in accordance with some embodiments. As will be appreciated in light of this disclosure, hardmask layer 116 may be formed with any of the example materials, techniques, and configurations discussed above, for instance, with respect to hardmask layer 110, in accordance with some embodiments. In some cases, hardmask layer 116 and hardmask layer 110 may differ in material composition, providing for etch selectivity with respect to one another.

In accordance with some embodiments, after forming hardmask layer 116, IC 102 may undergo formation of a dielectric layer 118, selective removal of a portion of either (or both) of its hardmask layers 110 and 116, and further formation of a given conductive feature 106. For instance, consider Figure 10, which illustrates a cross-sectional view of an IC 102 configured in accordance with an embodiment of the present disclosure. As will be appreciated in light of this disclosure, dielectric layer 118 may be formed with any of the example materials, techniques, and configurations discussed above, for instance, with respect to dielectric layer 104, in accordance with some embodiments. As can be seen here in Figure 10, dielectric layer 118 may be patterned with one or more features 118a, the dimensions and geometry of which may be customized, as desired for a given target application or end-use. In some cases, a given feature 118a may be formed so as to land, at least in part, over a portion of hardmask layer 116 and underlying conductive feature 106. After patterning such a feature 118a, a portion of the underlying hardmask layer 116 may be selectively removed (e.g., selectively etched away), exposing the underlying conductive feature 106 hosted, for instance, by a feature 114b. In accordance with an embodiment, additional conductive material may be deposited over the newly exposed conductive feature 106, allowing the resultant conductive feature 106a to extend up through the patterned feature 118a in dielectric layer 118. In an example case, a via (or other conductive feature) of a next overlying layer may be landed, in part or in whole, over the conductive feature 106, resulting in a conductive feature 106a that spans both IC layers.

Figure 11 illustrates a cross-sectional view of an IC 102 configured in accordance with another embodiment of the present disclosure. Figure 11′ illustrates a cross-sectional view of an IC 102 configured in accordance with another embodiment of the present disclosure. As will be appreciated in light of this disclosure, Figure 11′ provides a rendition of an IC 100 that is representative of some more real-world structural features and configurations, and the description provided herein with respect to Figure 11 is equally applicable to Figure 11′. As can be seen from these figures, dielectric layer 118 additionally (or alternatively) may be patterned with one or more features 118b, the dimensions and geometry of which may be customized, as

desired for a given target application or end-use. In some cases, a given feature 118b may be formed so as to land, at least in part, over a portion of hardmask layer 110 and underlying conductive feature 106. After patterning such a feature 118b, a portion of the underlying hardmask layer 110 may be selectively removed (e.g., selectively etched away), exposing the underlying conductive feature 106 hosted, for instance, by a feature 114a. In accordance with an embodiment, additional conductive material may be deposited over the newly exposed conductive feature 106, allowing the resultant conductive feature 106b to extend up through the patterned feature 118b in dielectric layer 118. In an example case, a via (or other conductive feature) of a next overlying layer may be landed, in part or in whole, over the conductive feature 106, resulting in a conductive feature 106b that spans both IC layers. As illustrated in each of Figures 11 and 11', a conductive feature 106a optionally may be present in IC 102, as well, though IC 102 is not required to have such a configuration.

As generally can be seen from Figures 10–11', in some cases, use of the disclosed techniques may allow for improved etch placement error (EPE) margin, in accordance with some embodiments. As can be seen further from Figures 10–11', hardmask layer 110 (e.g., the helmet-like hardmask bodies) and hardmask layer 116 may exhibit etch selectivity, in accordance with some embodiments.

Figures 1–2 and 12–17 illustrate a process flow of fabricating an IC 104 in accordance with another embodiment of the present disclosure. The process may begin as in Figures 1 and 2, discussed above. The process may continue as in Figure 12, which illustrates a cross-sectional view of an IC 104 configured in accordance with another embodiment of the present disclosure. As can be seen here, IC 104 includes a barrier layer 108 that extends over the sidewalls, but not top surfaces, of conductive features 106 (e.g., barrier layer 108 extends over portions of the sidewalls that are above dielectric layer 104). Consequently, the upper surfaces of conductive features 106 remain exposed. Compare this with the barrier layer 108 in Figure 3, discussed above, which instead conforms to the top surfaces of conductive features 106, as well as the sidewalls thereof.

The process may continue as in Figure 13, which illustrates a cross-sectional view of the IC 104 of Figure 12 after forming a hardmask layer 110, in accordance with an embodiment of the present disclosure. As can be seen here, hardmask layer 110 (e.g., one or more hardmask bodies, discussed above) may be disposed over and in direct contact with the top surfaces of conductive features 106, as well as the ends of portions of barrier layer 108 alongside conductive features 106, in accordance with an embodiment. Compare this with the hardmask layer 110 in Figure 4, discussed above, which instead resides over and in direct contact with portions of

barrier layer 108 conformal to the top surfaces of conductive features 106, in accordance with an embodiment.

The process may continue as in Figure 14, which illustrates a cross-sectional view of the IC 104 of Figure 13 after forming a barrier layer 112, in accordance with an embodiment of the present disclosure. As can be seen here, barrier layer 112 may be disposed over portions of barrier layer 108 and hardmask layer 110, along sidewalls of conductive features 106. In forming barrier layer 112, it may be desirable to remove portions that deposit over hardmask layer 110, to ensure that the upper surfaces of the constituent hardmask bodies of hardmask layer 110 remain exposed. Also, it may be desirable to remove portions of barrier layer 112 that deposit over portions of barrier layer 108 between neighboring conductive features 106. To these ends, partial removal of barrier layer 112 may be performed via any suitable standard, custom, or proprietary directional etch technique(s), as will be apparent in light of this disclosure.

As can be seen from Figure 14, for example, barrier layer 112 may be formed, in accordance with some embodiments, so as to extend from dielectric layer 104, along barrier layer 108 over sidewalls of conductive features 106, and along sidewalls of the constituent hardmask bodies of hardmask layer 110. In some instances, barrier layer 112 may extend up the full height of barrier layer 108 and hardmask layer 110, whereas in some other instances, barrier layer 112 may extend up less than a full height thereof. As can be seen further from Figure 4, a feature 114a may exist between neighboring conductive features 106 as a result of the particular interfacing of barrier layers 112 and 108 between such conductive features 106.

The process may continue as in Figure 15, which illustrates a cross-sectional view of the IC 104 of Figure 14 after forming a feature 114b from a given feature 114a, in accordance with an embodiment of the present disclosure. As can be seen, a given feature 114a may undergo additional patterning, for example, to provide a feature 114b. In some cases, a plurality of features 114b may be formed, for provision of a second set of conductive features 106 (e.g., the first set being formed as discussed above with reference to Figure 1). To these ends, a given feature 114b may be formed with any of the example techniques and configurations discussed above, for instance, with respect to feature(s) 114b in the context of Figure 6. As with the discussion of Figure 6 provided above, features 114b (and 114a, discussed above) here in Figure 15 may be patterned on alternate trenches, such that the pitch P_1 of IC 104 is about halved.

At this point in the process flow, there are a wide range of options for how to proceed with fabrication. For instance, all (or some sub-set) of the features 114a and 114b of IC 104 may be filled with an electrically conductive material, in accordance with some embodiments. In so doing, the resultant IC 104 may have conductive features 106 of pitch P_2, which may be a

fraction of the original pitch P_1 of IC 104. In an example case, pitch P_2 may be about one-half of pitch P_1 (e.g., if $P_1 = 2x$, then $P_2 = x$). In some cases, the newly formed conductive features 106 may be of the same material composition as the original conductive features 106 previously formed. In other cases, different electrically conductive materials may be employed, such that IC 104 hosts one or more conductive features 106 of a first material composition and one or more conductive features 106 of a second, different material composition.

In some cases, after filling all (or some sub-set) of features 114a and 114b, IC 104 optionally may undergo any one, or combination, of a CMP process and an etch-and-clean process, for example, to remove any undesired portion(s) of barrier layer 112, hardmask layer 110, and barrier layer 108, as well as any excess (e.g., overburden) of conductive features 106 that may be present. In other cases, however, hardmask layer 110 may be allowed to remain over IC 104.

In other cases, after filling all (or some sub-set) of features 114a and 114b, IC 104 optionally may undergo a recessing process in which conductive feature(s) 106 are recessed to below the height of barrier layer 112 and hardmask layer 110. For instance, consider Figure 16, which illustrates a cross-sectional view of an IC 104 configured in accordance with an embodiment of the present disclosure. Recessing of conductive feature(s) 106 may be performed via any suitable standard, custom, or proprietary etch-and-clean technique(s), as will be apparent in light of this disclosure.

In some cases, after recessing conductive features 106 as in Figure 16, IC 104 optionally may undergo one or more additional fabrication processes. For instance, consider Figure 17, which illustrates a cross-sectional view of an IC 104 after forming a hardmask layer 116, in accordance with an embodiment of the present disclosure. As can be seen, hardmask layer 116 may be formed within any one or more desired features 114a and 114b, over conductive features 106, in accordance with some embodiments. As will be appreciated in light of this disclosure, hardmask layer 116 may be formed with any of the example materials, techniques, and configurations discussed above, for instance, with respect to hardmask layer 110, in accordance with some embodiments. In some cases, hardmask layer 116 and hardmask layer 110 may differ in material composition, providing for etch selectivity with respect to one another.

In accordance with some embodiments, after forming hardmask layer 116, IC 104 may undergo formation of a dielectric layer 118, selective removal of at least a portion of either (or both) of its hardmask layers 110 and 116, and further formation of a given conductive feature 106. For instance, consider Figure 18, which illustrates a cross-sectional view of an IC 104 configured in accordance with an embodiment of the present disclosure. As can be seen here in Figure 18, dielectric layer 118 may be patterned with one or more features 118a, the dimensions

and geometry of which may be customized, as desired for a given target application or end-use. In some cases, a given feature 118a may be formed so as to land, at least in part, over a portion of hardmask layer 116 and underlying conductive feature 106. After patterning such a feature 118a, a portion of the underlying hardmask layer 116 may be selectively removed (e.g., selectively etched away), exposing the underlying conductive feature 106 hosted, for instance, by a feature 114b. In accordance with an embodiment, additional conductive material may be deposited over the newly exposed conductive feature 106, allowing the resultant conductive feature 106a to extend up through the patterned feature 118a in dielectric layer 118. In an example case, a via (or other conductive feature) of a next overlying layer may be landed, in part or in whole, over the conductive feature 106, resulting in a conductive feature 106a that spans both IC layers.

Figure 19 illustrates a cross-sectional view of an IC 104 configured in accordance with another embodiment of the present disclosure. As can be seen here in Figure 11, dielectric layer 118 additionally (or alternatively) may be patterned with one or more features 118b, the dimensions and geometry of which may be customized, as desired for a given target application or end-use. In some cases, a given feature 118b may be formed so as to land, at least in part, over a portion of hardmask layer 110 and underlying conductive feature 106. After patterning such a feature 118b, a portion of the underlying hardmask layer 110 may be selectively removed (e.g., selectively etched away), exposing the underlying conductive feature 106 hosted, for instance, by a feature 114a. In accordance with an embodiment, additional conductive material may be deposited over the newly exposed conductive feature 106, allowing the resultant conductive feature 106a to extend up through the patterned feature 118b in dielectric layer 118. In an example case, a via (or other conductive feature) of a next overlying layer may be landed, in part or in whole, over the conductive feature 106, resulting in a conductive feature 106b that spans both IC layers. As illustrated in Figure 19, a conductive feature 106a optionally may be present in IC 104, as well, though IC 104 is not required to have such a configuration.

As generally can be seen from Figures 18–19, in some cases, use of the disclosed techniques may allow for improved EPE margin, in accordance with some embodiments. As can be seen further from Figures 18–19, hardmask layer 110 (e.g., the helmet-like hardmask bodies) and hardmask layer 116 may exhibit etch selectivity, in accordance with some embodiments.

Subtractive Patterning Techniques and Structures:

Figures 20–28 illustrate a process flow of fabricating an IC 105 in accordance with another embodiment of the present disclosure. The process flow may begin as in Figure 20, which illustrates a cross-sectional view of an IC 105 configured in accordance with an

embodiment of the present disclosure. As can be seen here, IC 105 includes a semiconductor substrate 102 and a conductive layer 106 disposed there over, each discussed above.

The process flow may continue as in Figure 21, which illustrates a cross-sectional view of the IC 105 of Figure 20 after patterning conductive layer 106 into one or more conductive features 106, in accordance with an embodiment of the present disclosure. Patterning of conductive layer 106 may be performed via any suitable standard, custom, or proprietary lithography, etch, and clean (or other subtractive patterning) technique(s), as will be apparent in light of this disclosure. In some cases, conductive features 106 may be formed from conductive layer 106 via any one, or combination, of etch processes. A given etch process may be, for example, an anisotropic etch process that involves a wet etch or a dry etch (or both), and the particular etch chemistry employed by a given applied etch process may be customized, as desired for a given target application or end-use. The patterning of conductive layer 106 can be controlled to provide a given amount of symmetry/asymmetry and isotropy/anisotropy desired. In accordance with some embodiments, patterning of conductive layer 106 may be performed until the upper surface of underlying semiconductor substrate 102 is reached, such as is generally shown in Figure 21.

The process flow may continue as in Figure 22, which illustrates a cross-sectional view of the IC 105 of Figure 21 after forming a barrier layer 108, in accordance with an embodiment of the present disclosure. As can be seen here, IC 105 includes a barrier layer 108 that extends over the sidewalls, but not top surfaces, of conductive features 106. Consequently, the upper surfaces of conductive features 106 remain exposed. Compare this with the barrier layer 108 in Figure 3, discussed above, which instead conforms to the top surfaces of conductive features 106, as well as the sidewalls thereof.

The process may continue as in Figure 23, which illustrates a cross-sectional view of the IC 105 of Figure 22 after forming a hardmask layer 110, in accordance with an embodiment of the present disclosure. As can be seen here, hardmask layer 110 (e.g., one or more hardmask bodies, discussed above) may be disposed over and in direct contact with the top surfaces of conductive features 106, as well as the ends of portions of barrier layer 108 alongside conductive features 106, in accordance with an embodiment. Compare this with the hardmask layer 110 in Figure 4, discussed above, which instead resides over and in direct contact with portions of barrier layer 108 conformal to the top surfaces of conductive features 106, in accordance with an embodiment.

The process may continue as in Figure 24, which illustrates a cross-sectional view of the IC 105 of Figure 23 after forming a barrier layer 112, in accordance with an embodiment of the present disclosure. As can be seen here, barrier layer 112 may be disposed over portions of

barrier layer 108 and hardmask layer 110, along sidewalls of conductive features 106. As previously discussed, in forming barrier layer 112, it may be desirable to remove portions that deposit over hardmask layer 110, to ensure that the upper surfaces of the constituent hardmask bodies of hardmask layer 110 remain exposed. Also, it may be desirable to remove portions of barrier layer 112 that deposit over portions of barrier layer 108 between neighboring conductive features 106.

As can be seen from Figure 24, for example, barrier layer 112 may be formed, in accordance with some embodiments, so as to extend from semiconductor substrate 102, along barrier layer 108 over sidewalls of conductive features 106, and along sidewalls of the constituent hardmask bodies of hardmask layer 110. In some instances, barrier layer 112 may extend up the full height of barrier layer 108 and hardmask layer 110, whereas in some other instances, barrier layer 112 may extend up less than a full height thereof. As can be seen further from Figure 24, a feature 114a may exist between neighboring conductive features 106 as a result of the particular interfacing of barrier layers 112 and 108 between such conductive features 106.

At this point in the process flow, there are a wide range of options for how to proceed with fabrication. For instance, all (or some sub-set) of the features 114a of IC 105 may be filled with an electrically conductive material, in accordance with some embodiments. In so doing, the resultant IC 105 may have conductive features 106 of pitch P_2, which may be a fraction of the original pitch P_1 of IC 105. In an example case, pitch P_2 may be about one-half of pitch P_1 (e.g., if $P_1 = 2x$, then $P_2 = x$). In some cases, the newly formed conductive features 106 may be of the same material composition as the original conductive features 106 previously formed. In other cases, different electrically conductive materials may be employed, such that IC 105 hosts one or more conductive features 106 of a first material composition and one or more conductive features 106 of a second, different material composition.

In some cases, after filling all (or some sub-set) of features 114a, IC 105 optionally may undergo any one, or combination, of a CMP process and an etch-and-clean process, for example, to remove any undesired portion(s) of barrier layer 112, hardmask layer 110, and barrier layer 108, as well as any excess (e.g., overburden) of conductive features 106 that may be present. In other cases, however, hardmask layer 110 may be allowed to remain over IC 105.

In other cases, after filling all (or some sub-set) of features 114a, IC 105 optionally may undergo a recessing process in which conductive feature(s) 106 are recessed to below the height of barrier layer 112 and hardmask layer 110. For instance, consider Figure 25, which illustrates a cross-sectional view of an IC 105 configured in accordance with an embodiment of the present

disclosure. Recessing of conductive feature(s) 106 may be performed via any suitable standard, custom, or proprietary etch-and-clean technique(s), as will be apparent in light of this disclosure.

In some cases, after recessing conductive features 106 as in Figure 25, IC 105 optionally may undergo one or more additional fabrication processes. For instance, consider Figure 26, which illustrates a cross-sectional view of an IC 105 after forming a hardmask layer 116, in accordance with an embodiment of the present disclosure. As can be seen, hardmask layer 116 may be formed within any one or more desired features 114a, over conductive features 106, in accordance with some embodiments. In some cases, hardmask layer 116 and hardmask layer 110 may differ in material composition, providing for etch selectivity with respect to one another.

In accordance with some embodiments, after forming hardmask layer 116, IC 105 may undergo formation of a dielectric layer 118, selective removal of at least a portion of either (or both) of its hardmask layers 110 and 116, and further formation of a given conductive feature 106. For instance, consider Figure 27, which illustrates a cross-sectional view of an IC 105 configured in accordance with an embodiment of the present disclosure. As can be seen here in Figure 27, dielectric layer 118 may be patterned with one or more features 118a, the dimensions and geometry of which may be customized, as desired for a given target application or end-use. In some cases, a given feature 118a may be formed so as to land, at least in part, over a portion of hardmask layer 116 and underlying conductive feature 106. After patterning such a feature 118a, a portion of the underlying hardmask layer 116 may be selectively removed (e.g., selectively etched away), exposing the underlying conductive feature 106 hosted, for instance, by a feature 114a. In accordance with an embodiment, additional conductive material may be deposited over the newly exposed conductive feature 106, allowing the resultant conductive feature 106a to extend up through the patterned feature 118a in dielectric layer 118. In an example case, a via (or other conductive feature) of a next overlying layer may be landed, in part or in whole, over the conductive feature 106, resulting in a conductive feature 106a that spans both IC layers.

Figure 28 illustrates a cross-sectional view of an IC 105 configured in accordance with another embodiment of the present disclosure. As can be seen here in Figure 28, dielectric layer 118 additionally (or alternatively) may be patterned with one or more features 118b, the dimensions and geometry of which may be customized, as desired for a given target application or end-use. In some cases, a given feature 118b may be formed so as to land, at least in part, over a portion of hardmask layer 110 and underlying conductive feature 106. After patterning such a feature 118b, a portion of the underlying hardmask layer 110 may be selectively removed (e.g., selectively etched away), exposing the underlying conductive feature 106 hosted, for

instance, by a feature 114a. In accordance with an embodiment, additional metal may be deposited over the newly exposed conductive feature 106, allowing the resultant conductive feature 106b to extend up through the patterned feature 118b in dielectric layer 118. In an example case, a via (or other conductive feature) of a next overlying layer may be landed, in part or in whole, over the conductive feature 106, resulting in a conductive feature 106b that spans both IC layers. As illustrated in Figure 28, a conductive feature 106a optionally may be present in IC 105, as well, though IC 105 is not required to have such a configuration.

As generally can be seen from Figures 27–28, in some cases, use of the disclosed techniques may allow for improved EPE margin, in accordance with some embodiments. As can be seen further from Figures 27–28, hardmask layer 110 (e.g., the helmet-like hardmask bodies) and hardmask layer 116 may exhibit etch selectivity, in accordance with some embodiments.

As will be appreciated in light of this disclosure, the process flows of Figures 1–19 may be considered, in a general sense, damascene-based patterning processes with dielectric (e.g., ILD) recessing, in accordance with some embodiments. The process flow of Figures 20–28, however, may be considered, in a general sense, a subtractive conductive material (e.g., metal) patterning process, in accordance with some embodiments. Numerous suitable uses of the disclosed techniques will be apparent in light of this disclosure.

Example System

Figure 29 illustrates a computing system 1000 implemented with integrated circuit structures or devices formed using the disclosed techniques in accordance with an example embodiment. As can be seen, the computing system 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including, but not limited to, a processor 1004 and at least one communication chip 1006, each of which can be physically and electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board, a daughterboard mounted on a main board, or the only board of system 1000, etc. Depending on its applications, computing system 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

Any of the components included in computing system 1000 may include one or more integrated circuit structures or devices formed using the disclosed techniques in accordance with an example embodiment. In some embodiments, multiple functions can be integrated into one or more chips (e.g., for instance, note that the communication chip 1006 can be part of or otherwise integrated into the processor 1004).

The communication chip 1006 enables wireless communications for the transfer of data to and from the computing system 1000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including, but not limited to, Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing system 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 1004 of the computing system 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments, the integrated circuit die of the processor includes onboard circuitry that is implemented with one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein. The term "processor" may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 1006 also may include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more integrated circuit structures or devices formed using the disclosed techniques as described herein. As will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into the processor 1004 (e.g., where functionality of any chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any number of

processor 1004 and/or communication chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra-mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, a digital video recorder, or any other electronic device that processes data or employs one or more integrated circuit structures or devices formed using the disclosed techniques, as variously described herein.

Further Example Embodiments

The following examples pertain to further embodiments, from which numerous permutations and configurations will be apparent.

Example 1 is an integrated circuit including: a substrate; first and second electrically conductive features disposed over the substrate; a first barrier layer disposed over the substrate, wherein the first barrier layer extends along sidewalls of each of the first and second electrically conductive features; a first hardmask layer disposed over the substrate, wherein the first hardmask layer includes at least first and second hardmask bodies disposed substantially over top surfaces of the first and second electrically conductive features, respectively; and a second barrier layer disposed over the substrate, wherein the second barrier layer extends along the first barrier layer, over sidewalls of each of the first and second electrically conductive features, and along sidewalls of the first and second hardmask bodies.

Example 2 includes the subject matter of any of Examples 1 and 3–15 and further includes a third electrically conductive feature disposed over the substrate, between the first and second electrically conductive features.

Example 3 includes the subject matter of Example 2, wherein a pitch of the first and second electrically conductive features is about one-half of a pitch of the first and third electrically conductive features.

Example 4 includes the subject matter of Example 2, wherein the first, second, and third electrically conductive features are of substantially the same height.

Example 5 includes the subject matter of Example 2, wherein at least one of the first, second, and third electrically conductive features includes at least one of copper (Cu), aluminum (Al), tungsten (W), nickel (Ni), cobalt (Co), silver (Ag), gold (Au), titanium (Ti), and tantalum (Ta).

Example 6 includes the subject matter of Example 2, wherein the third electrically conductive feature is of different material composition than the first and second electrically conductive features.

Example 7 includes the subject matter of Example 2 and further includes a second hardmask layer disposed over a top surface of the third electrically conductive feature, wherein the first and second hardmask layers are physically separated by the second barrier layer.

Example 8 includes the subject matter of Example 7, wherein the first and second hardmask layers are of different material composition, such that they exhibit etch selectivity with respect to one another.

Example 9 includes the subject matter of Example 7 and further includes a dielectric layer disposed over a topography provided at least by the first and second hardmask layers and the second barrier layer.

Example 10 includes the subject matter of Example 9, wherein at least one of the first, second, and third electrically conductive features extends into the dielectric layer.

Example 11 includes the subject matter of any of Examples 1–10 and 12–15, wherein: the first hardmask layer includes at least one of titanium nitride (TiN), silicon nitride (Si_3N_4), silicon dioxide (SiO_2), silicon carbonitride (SiCN), and silicon oxynitride (SiO_xN_y); and at least one of the first and second hardmask bodies has a thickness in the range of about 5–20 nm.

Example 12 includes the subject matter of any of Examples 1–11 and 13–15, wherein at least one of the first and second hardmask bodies is configured to prevent electrical leakage therethrough.

Example 13 includes the subject matter of any of Examples 1–12 and 14–15, wherein at least one of the first and second barrier layers includes at least one of silicon oxide (SiO_2), aluminum oxide (Al_2O_3), and titanium oxide (TiO_2).

Example 14 includes the subject matter of any of Examples 1–13 and 15, wherein the substrate includes at least one of silicon (Si), germanium (Ge), and silicon germanium (SiGe).

Example 15 includes the subject matter of any of Examples 1–14, wherein the substrate is configured as at least one of a bulk semiconductor substrate, a semiconductor-on-insulator structure, a semiconductor wafer, and a multi-layered structure.

Example 16 is a method of fabricating an integrated circuit, the method including: forming first and second electrically conductive features over a substrate; forming a first barrier layer over the substrate, wherein the first barrier layer extends along sidewalls of each of the first and second electrically conductive features; forming a first hardmask layer over the substrate, wherein the first hardmask layer includes at least first and second hardmask bodies disposed substantially over top surfaces of the first and second electrically conductive features,

respectively; and forming a second barrier layer over the substrate, wherein the second barrier layer extends along the first barrier layer, over sidewalls of each of the first and second electrically conductive features, and along sidewalls of the first and second hardmask bodies.

Example 17 includes the subject matter of any of Examples 16 and 18–30, wherein forming the first hardmask layer involves at least one of a physical vapor deposition (PVD) process and a chemical vapor deposition (CVD) process.

Example 18 includes the subject matter of any of Examples 16–17 and 19–30 and further includes forming a third electrically conductive feature over the substrate, between the first and second electrically conductive features.

Example 19 includes the subject matter of Example 18, wherein a pitch of the first and second electrically conductive features is about one-half of a pitch of the first and third electrically conductive features.

Example 20 includes the subject matter of Example 18, wherein the first, second, and third electrically conductive features are of substantially the same height.

Example 21 includes the subject matter of Example 18, wherein the third electrically conductive feature is of different material composition than the first and second electrically conductive features.

Example 22 includes the subject matter of Example 18 and further includes forming a second hardmask layer over a top surface of the third electrically conductive feature, wherein the first and second hardmask layers are physically separated by the second barrier layer.

Example 23 includes the subject matter of Example 22, wherein the first and second hardmask layers are of different material composition, such that they exhibit etch selectivity with respect to one another.

Example 24 includes the subject matter of Example 22 and further includes forming a dielectric layer over a topography provided at least by the first and second hardmask layers and the second barrier layer.

Example 25 includes the subject matter of Example 24 and further includes: etching through a portion of the dielectric layer; selectively removing at least one of the first and second hardmask bodies, revealing the top surface of at least one of the first and second electrically conductive features; and further forming the at least one of the first and second electrically conductive features, such that the at least one of the first and second electrically conductive features extends into the dielectric layer.

Example 26 includes the subject matter of Example 24 and further includes: etching through a portion of the dielectric layer; selectively removing the second hardmask layer from the third electrically conductive feature, revealing the top surface of the third electrically

conductive feature; and further forming the third electrically conductive feature, such that the third electrically conductive feature extends into the dielectric layer.

Example 27 includes the subject matter of any of Examples 16–26 and 28–30, wherein the first hardmask layer includes at least one of titanium nitride (TiN), silicon nitride (Si_3N_4), silicon dioxide (SiO_2), silicon carbonitride (SiCN), and silicon oxynitride (SiO_xN_y); and at least one of the first and second hardmask bodies has a thickness in the range of about 5–20 nm.

Example 28 includes the subject matter of any of Examples 16–27 and 29–30, wherein at least one of the first and second hardmask bodies is configured to prevent electrical leakage therethrough.

Example 29 includes the subject matter of any of Examples 16–28 and 30, wherein the substrate includes at least one of silicon (Si), germanium (Ge), and silicon germanium (SiGe).

Example 30 includes the subject matter of any of Examples 16–29, wherein the substrate is configured as at least one of a bulk semiconductor substrate, a semiconductor-on-insulator structure, a semiconductor wafer, and a multi-layered structure.

Example 31 is an integrated circuit including: a substrate; a first plurality of electrically conductive features disposed over the substrate; a second plurality of electrically conductive features disposed over the substrate, wherein a pitch of a constituent electrically conductive feature of the second plurality and a constituent electrically conductive feature of the first plurality is about one-half of a pitch of two consecutive constituent electrically conductive features of the first plurality; a first barrier layer disposed over the substrate, wherein the first barrier layer extends along sidewalls of at least one constituent electrically conductive feature of the first plurality; a first hardmask layer including at least one hardmask body disposed over at least an entire top surface of the at least one constituent electrically conductive feature of the first plurality; and a second barrier layer disposed over the substrate, wherein the second barrier layer extends along the first barrier layer, over sidewalls of the at least one constituent electrically conductive feature of the first plurality, and along sidewalls of the at least one hardmask body of the first hardmask layer.

Example 32 includes the subject matter of any of Examples 31 and 33–43, wherein at least one constituent electrically conductive feature of the first plurality and at least one constituent electrically conductive feature of the second plurality are of substantially the same height.

Example 33 includes the subject matter of any of Examples 31–32 and 34–43, wherein at least one constituent electrically conductive feature of the first plurality is of different material composition than at least one constituent electrically conductive feature of the second plurality.

Example 34 includes the subject matter of any of Examples 31–33 and 35–43 and further includes a second hardmask layer including at least one hardmask body disposed over at least an entire top surface of at least one constituent electrically conductive feature of the second plurality, wherein the at least one hardmask body of the second hardmask layer and the at least one hardmask body of the first hardmask layer are physically separated by the second barrier layer.

Example 35 includes the subject matter of Example 34, wherein the first and second hardmask layers are of different material composition, such that they exhibit etch selectivity with respect to one another.

Example 36 includes the subject matter of Example 34 and further includes a dielectric layer disposed over a topography provided at least by the first and second hardmask layers and the second barrier layer.

Example 37 includes the subject matter of Example 36, wherein at least one constituent electrically conductive feature of at least one of the first plurality and the second plurality extends into the dielectric layer.

Example 38 includes the subject matter of any of Examples 31–37 and 39–43, wherein the first barrier layer is further disposed between the at least one constituent electrically conductive feature of the first plurality and the at least one hardmask body of the first hardmask layer disposed there over.

Example 39 includes the subject matter of any of Examples 31–38 and 40–43, wherein: the first hardmask layer includes at least one of titanium nitride (TiN), silicon nitride (Si_3N_4), silicon dioxide (SiO_2), silicon carbonitride (SiCN), and silicon oxynitride (SiO_xN_y); and the at least one hardmask body of the first hardmask layer has a thickness in the range of about 5–20 nm.

Example 40 includes the subject matter of any of Examples 31–39 and 41–43, wherein the at least one hardmask body of the first hardmask layer is configured to prevent electrical leakage therethrough.

Example 41 includes the subject matter of any of Examples 31–40 and 42–43, wherein at least one of the first and second barrier layers includes at least one of silicon oxide (SiO_2), aluminum oxide (Al_2O_3), and titanium oxide (TiO_2).

Example 42 includes the subject matter of any of Examples 31–41 and 43, wherein the substrate includes at least one of silicon (Si), germanium (Ge), and silicon germanium (SiGe).

Example 43 includes the subject matter of any of Examples 31–42, wherein the substrate is configured as at least one of a bulk semiconductor substrate, a semiconductor-on-insulator structure, a semiconductor wafer, and a multi-layered structure.

The foregoing description of example embodiments has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the present disclosure to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of the present disclosure be limited not by this detailed description, but rather by the claims appended hereto. Future-filed applications claiming priority to this application may claim the disclosed subject matter in a different manner and generally may include any set of one or more limitations as variously disclosed or otherwise demonstrated herein.

CLAIMS

What is claimed is:

1. An integrated circuit comprising:

a substrate;

first and second electrically conductive features disposed over the substrate;

a first barrier layer disposed over the substrate, wherein the first barrier layer extends along sidewalls of each of the first and second electrically conductive features;

a first hardmask layer disposed over the substrate, wherein the first hardmask layer comprises at least first and second hardmask bodies disposed substantially over top surfaces of the first and second electrically conductive features, respectively; and

a second barrier layer disposed over the substrate, wherein the second barrier layer extends along the first barrier layer, over sidewalls of each of the first and second electrically conductive features, and along sidewalls of the first and second hardmask bodies.

2. The integrated circuit of claim 1 further comprising a third electrically conductive feature disposed over the substrate, between the first and second electrically conductive features.

3. The integrated circuit of claim 2, wherein a pitch of the first and second electrically conductive features is about one-half of a pitch of the first and third electrically conductive features.

4. The integrated circuit of claim 2, wherein the first, second, and third electrically conductive features are of substantially the same height.

5. The integrated circuit of claim 2 further comprising a second hardmask layer disposed over a top surface of the third electrically conductive feature, wherein the first and second hardmask layers are physically separated by the second barrier layer.

6. The integrated circuit of claim 5, wherein the first and second hardmask layers are of different material composition, such that they exhibit etch selectivity with respect to one another.

7. The integrated circuit of claim 1, wherein:

the first hardmask layer comprises at least one of titanium nitride (TiN), silicon nitride (Si_3N_4), silicon dioxide (SiO_2), silicon carbonitride (SiCN), and silicon oxynitride (SiO_xN_y); and

at least one of the first and second hardmask bodies has a thickness in the range of about 5–20 nm.

8. The integrated circuit of claim 1, wherein at least one of the first and second hardmask bodies is configured to prevent electrical leakage therethrough.

9. A method of fabricating an integrated circuit, the method comprising:

forming first and second electrically conductive features over a substrate;

forming a first barrier layer over the substrate, wherein the first barrier layer extends along sidewalls of each of the first and second electrically conductive features;

forming a first hardmask layer over the substrate, wherein the first hardmask layer comprises at least first and second hardmask bodies disposed substantially over top surfaces of the first and second electrically conductive features, respectively; and

forming a second barrier layer over the substrate, wherein the second barrier layer extends along the first barrier layer, over sidewalls of each of the first and second electrically conductive features, and along sidewalls of the first and second hardmask bodies.

10. The method of claim 9, wherein forming the first hardmask layer involves at least one of a physical vapor deposition (PVD) process and a chemical vapor deposition (CVD) process.

11. The method of claim 9 further comprising:

forming a third electrically conductive feature over the substrate, between the first and second electrically conductive features.

12. The method of claim 11, wherein a pitch of the first and second electrically conductive features is about one-half of a pitch of the first and third electrically conductive features.

13. The method of claim 11, wherein the first, second, and third electrically conductive features are of substantially the same height.

14. The method of claim 11, wherein the third electrically conductive feature is of different material composition than the first and second electrically conductive features.

15. The method of claim 11 further comprising:

forming a second hardmask layer over a top surface of the third electrically conductive feature, wherein the first and second hardmask layers are physically separated by the second barrier layer.

16. The method of claim 15, wherein the first and second hardmask layers are of different material composition, such that they exhibit etch selectivity with respect to one another.

17. The method of claim 15 further comprising:

forming a dielectric layer over a topography provided at least by the first and second hardmask layers and the second barrier layer.

18. The method of claim 17 further comprising:

etching through a portion of the dielectric layer;

selectively removing at least one of the first and second hardmask bodies, revealing the top surface of at least one of the first and second electrically conductive features; and

further forming the at least one of the first and second electrically conductive features, such that the at least one of the first and second electrically conductive features extends into the dielectric layer.

19. The method of claim 17 further comprising:

etching through a portion of the dielectric layer;

selectively removing the second hardmask layer from the third electrically conductive feature, revealing the top surface of the third electrically conductive feature; and

further forming the third electrically conductive feature, such that the third electrically conductive feature extends into the dielectric layer.

20. The method of claim 9, wherein:

the first hardmask layer comprises at least one of titanium nitride (TiN), silicon nitride (Si_3N_4), silicon dioxide (SiO_2), silicon carbonitride (SiCN), and silicon oxynitride (SiO_xN_y); and

at least one of the first and second hardmask bodies has a thickness in the range of about 5–20 nm.

21. An integrated circuit comprising:

a substrate;

a first plurality of electrically conductive features disposed over the substrate;

a second plurality of electrically conductive features disposed over the substrate, wherein a pitch of a constituent electrically conductive feature of the second plurality and a constituent electrically conductive feature of the first plurality is about one-half of a pitch of two consecutive constituent electrically conductive features of the first plurality;

a first barrier layer disposed over the substrate, wherein the first barrier layer extends along sidewalls of at least one constituent electrically conductive feature of the first plurality;

a first hardmask layer comprising at least one hardmask body disposed over at least an entire top surface of the at least one constituent electrically conductive feature of the first plurality; and

a second barrier layer disposed over the substrate, wherein the second barrier layer extends along the first barrier layer, over sidewalls of the at least one constituent electrically conductive feature of the first plurality, and along sidewalls of the at least one hardmask body of the first hardmask layer.

22. The integrated circuit of claim 21, wherein at least one constituent electrically conductive feature of the first plurality and at least one constituent electrically conductive feature of the second plurality are of substantially the same height.

23. The integrated circuit of claim 21 further comprising a second hardmask layer comprising at least one hardmask body disposed over at least an entire top surface of at least one constituent electrically conductive feature of the second plurality, wherein the at least one hardmask body of the second hardmask layer and the at least one hardmask body of the first hardmask layer are physically separated by the second barrier layer.

24. The integrated circuit of claim 23, wherein the first and second hardmask layers are of different material composition, such that they exhibit etch selectivity with respect to one another.

25. The integrated circuit of claim 21, wherein the first barrier layer is further disposed between the at least one constituent electrically conductive feature of the first plurality and the at least one hardmask body of the first hardmask layer disposed there over.

26. The integrated circuit of claim 21, wherein:

the first hardmask layer comprises at least one of titanium nitride (TiN), silicon nitride (Si_3N_4), silicon dioxide (SiO_2), silicon carbonitride (SiCN), and silicon oxynitride (SiO_xN_y); and

the at least one hardmask body of the first hardmask layer has a thickness in the range of about 5–20 nm.

Figure 1

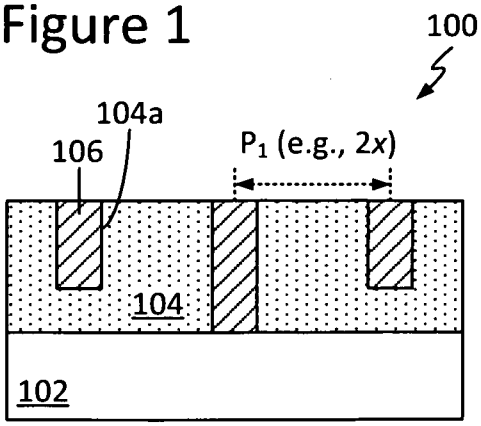


Figure 2

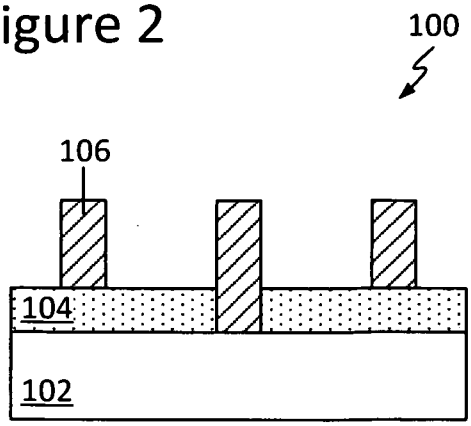


Figure 3

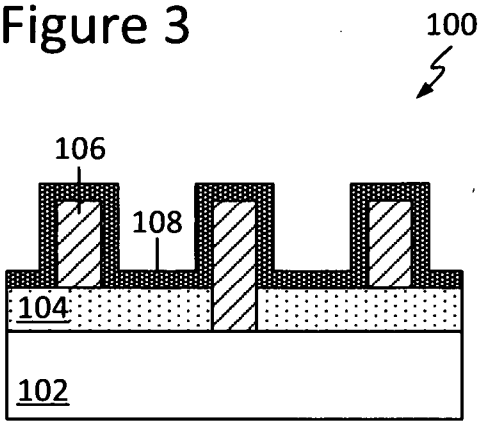


Figure 4

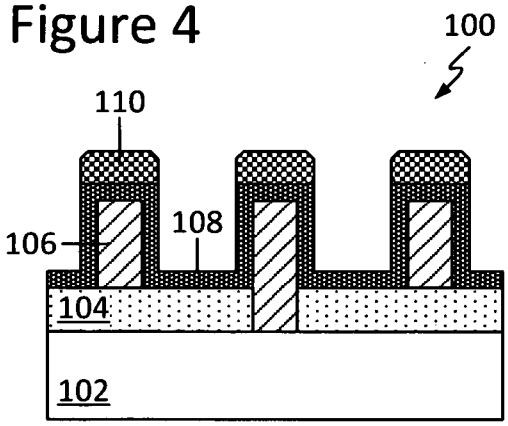


Figure 5

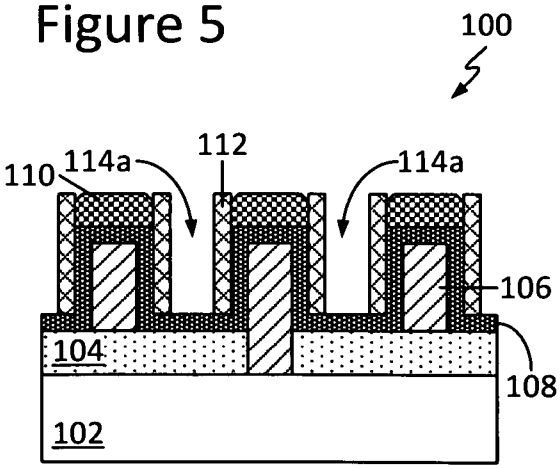


Figure 6

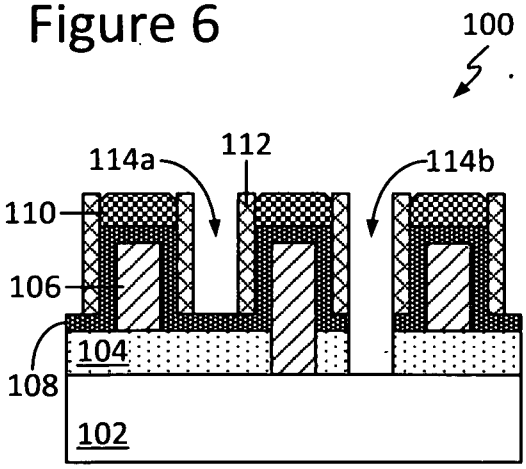


Figure 7

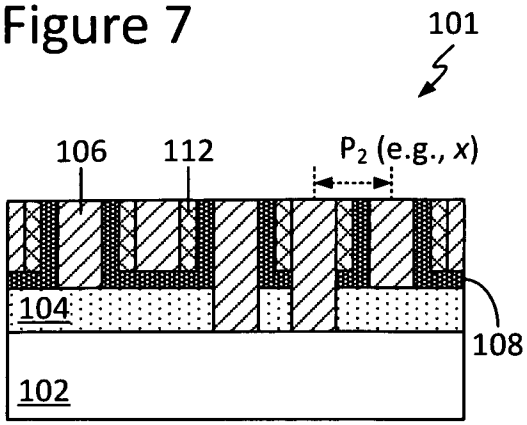


Figure 8

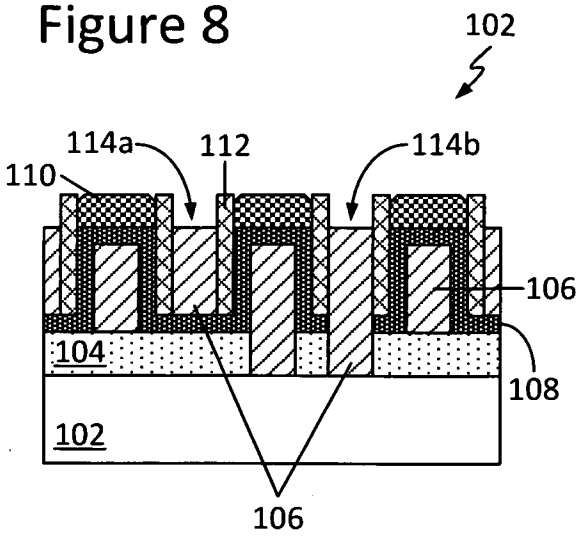


Figure 9

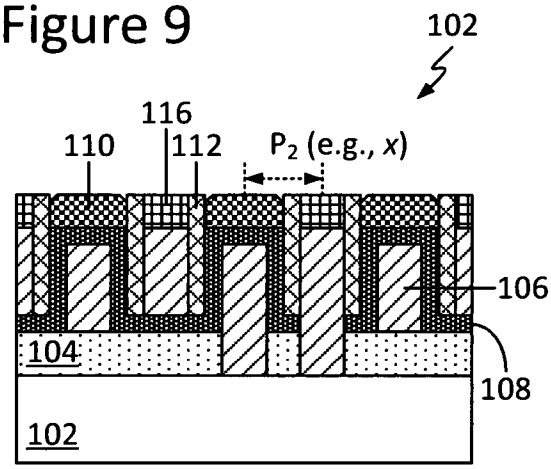


Figure 10

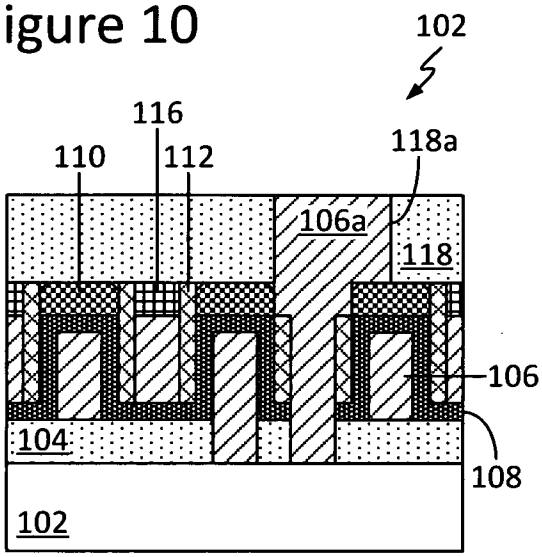


Figure 11

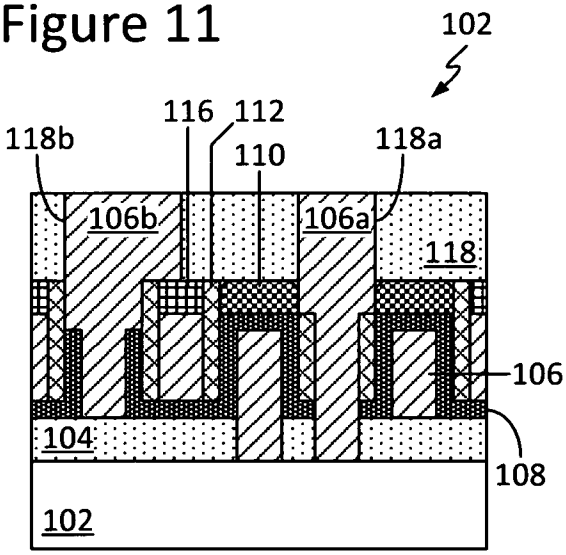


Figure 11'

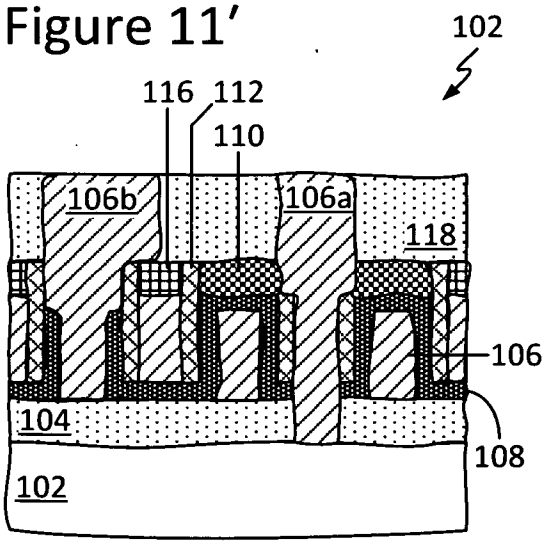


Figure 12

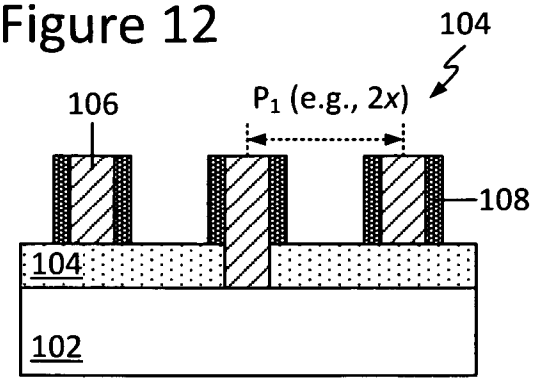


Figure 13

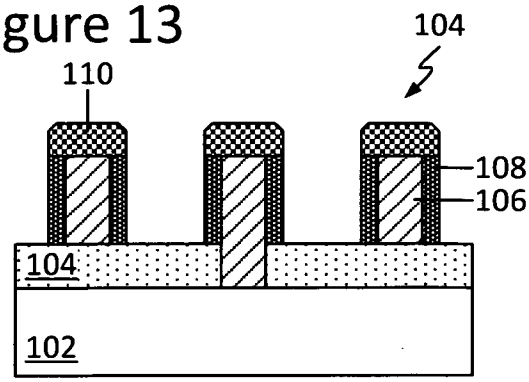


Figure 14

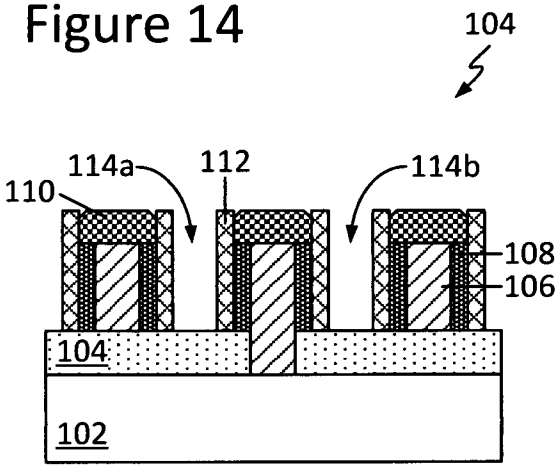


Figure 15

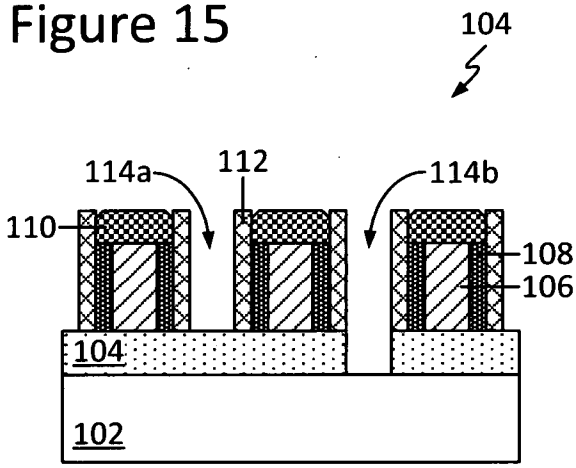


Figure 16

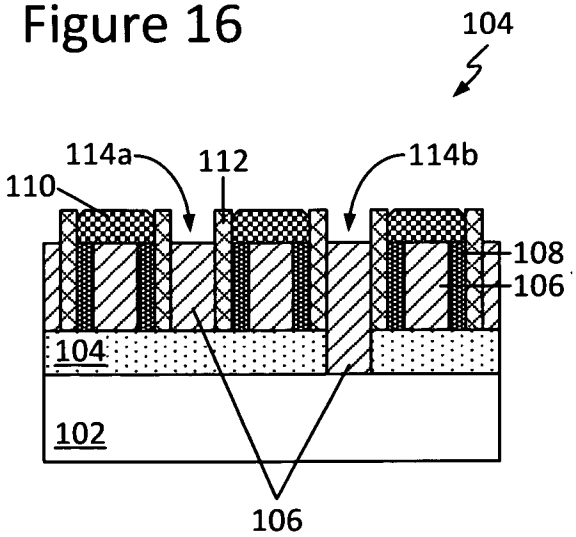


Figure 17

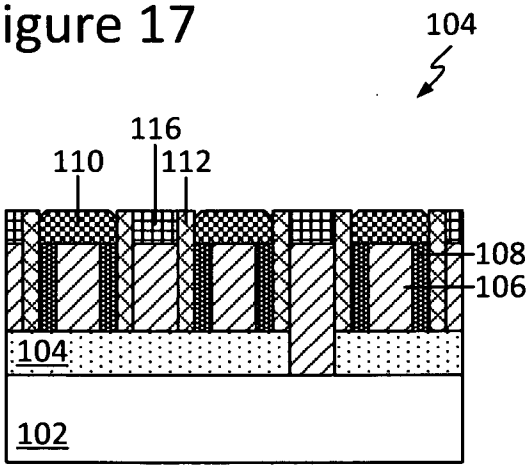


Figure 18

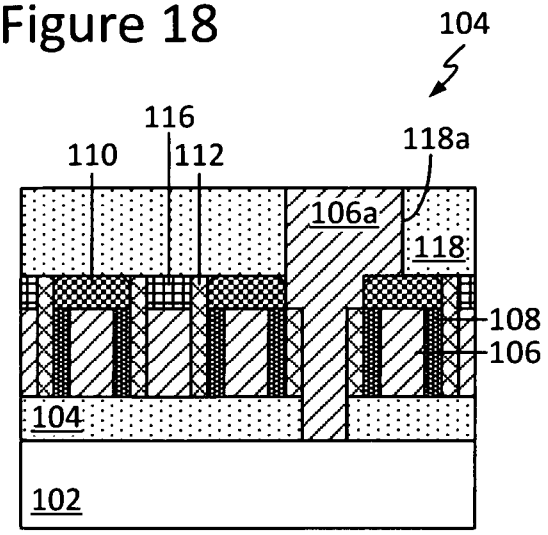


Figure 19

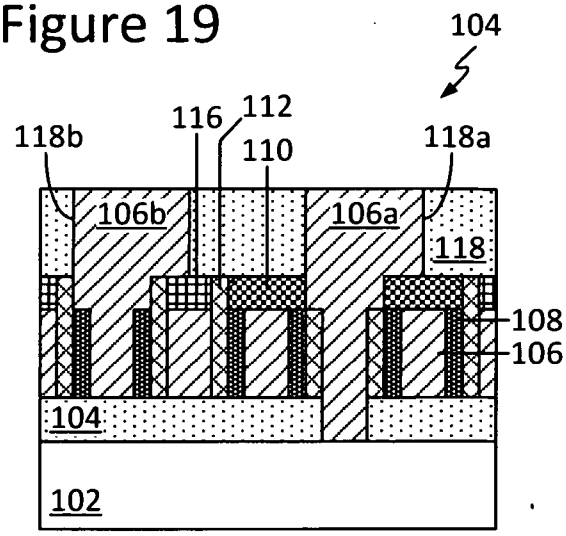


Figure 20

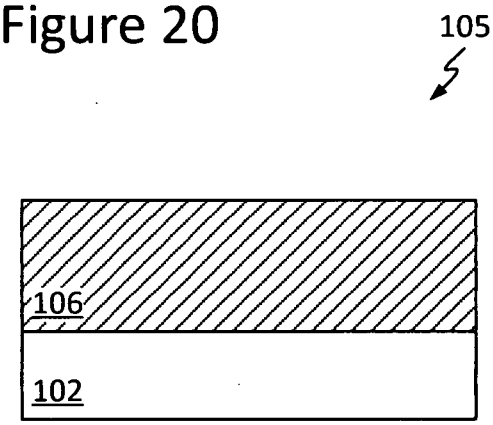


Figure 21

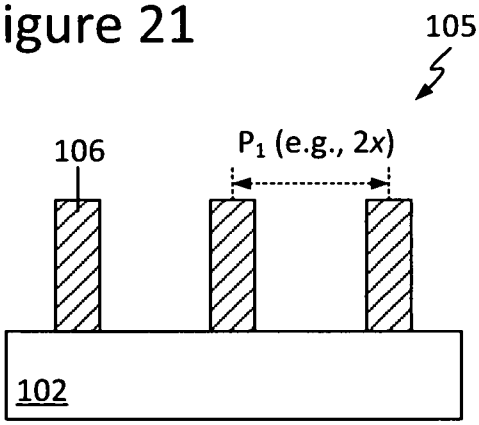


Figure 22

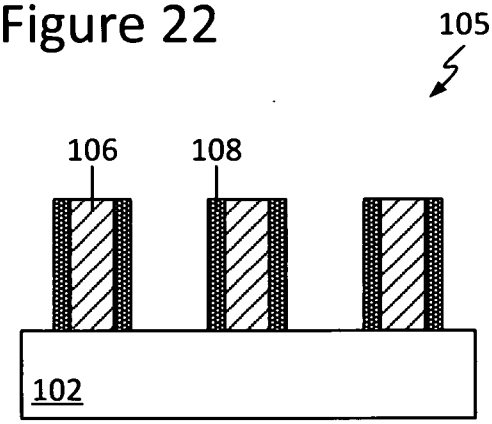


Figure 23

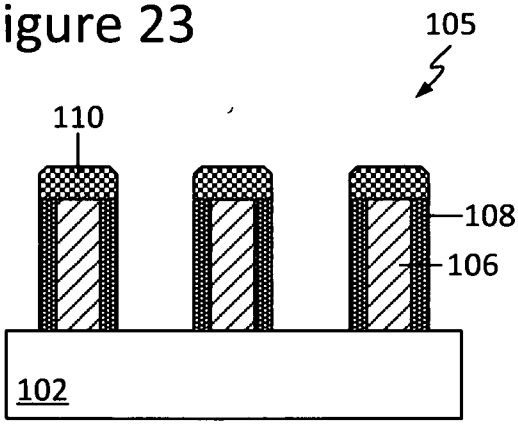


Figure 24

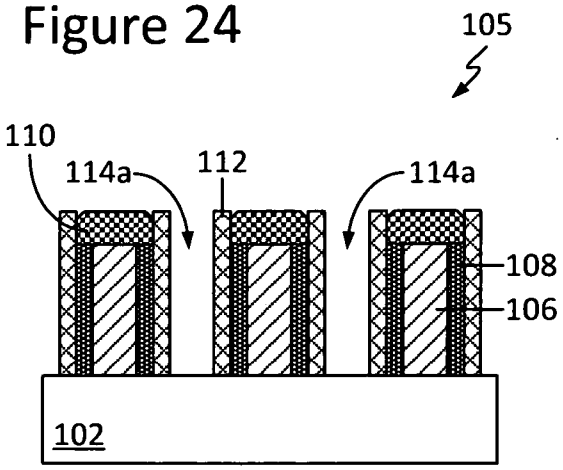


Figure 25

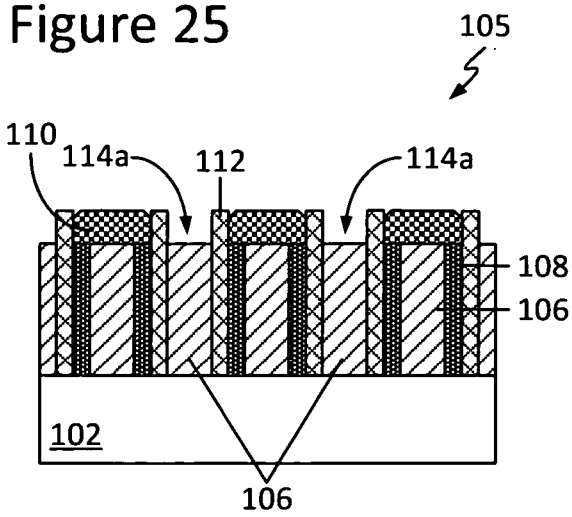


Figure 26

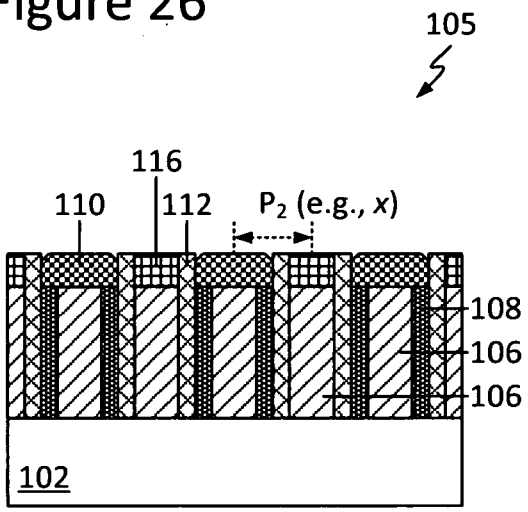


Figure 27

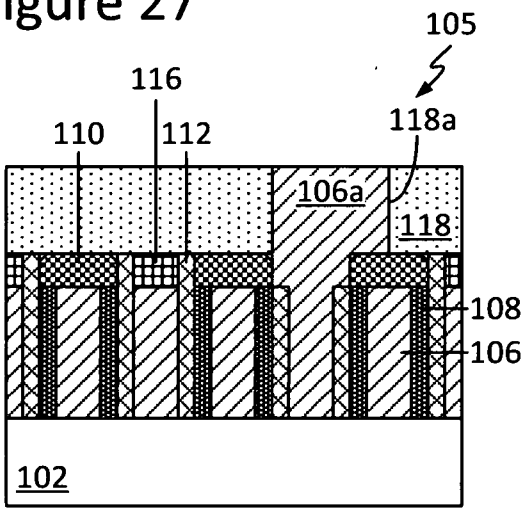


Figure 28

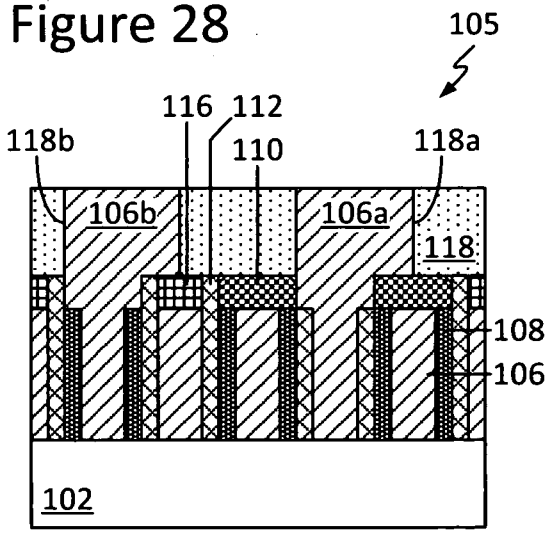
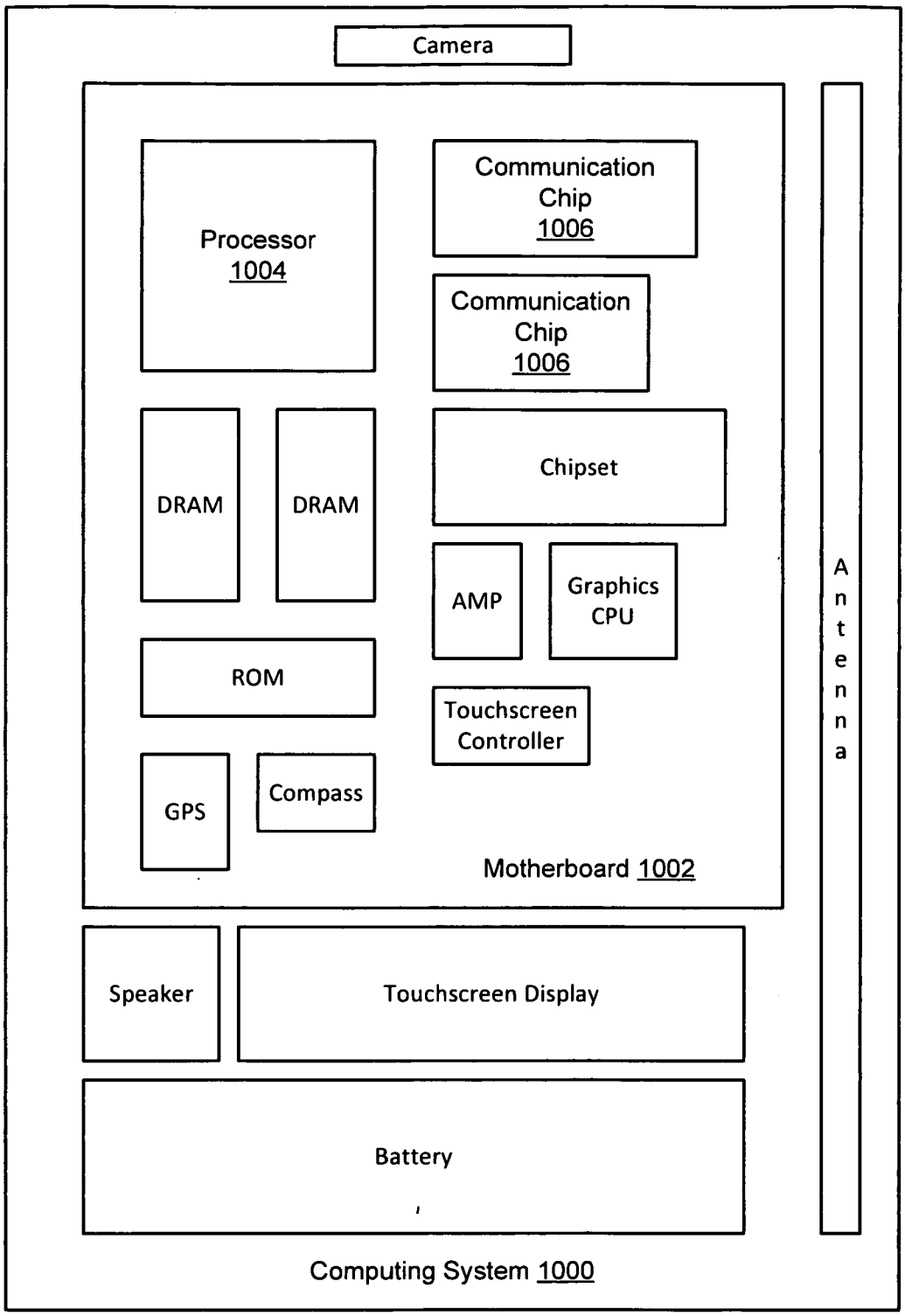


Figure 29


Camera
Processor 1004
Communication Chip 1006
Communication Chip 1006
DRAM
DRAM
Chipset
AMP
Graphics CPU
ROM
Touchscreen Controller
GPS
Compass
Motherboard 1002
Antenna
Speaker
Touchscreen Display
Battery
Computing System 1000

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/000341

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/768(2006.01)i, H01L 21/60(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/768; H01L 21/4763; H01L 21/28; H01L 23/48; H01L 29/40; H01L 29/66; H01L 21/44; H01L 23/525; H01L 21/60

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & keywords: substrate, conduct, metal, hardmask, barrier

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005-0077627 A1 (CHEN-HUA YU et al.) 14 April 2005 See abstract, paragraphs [0014]-[0020] and figures 1-5.	1-26
A	US 2006-0234497 A1 (CHIH-CHAO YANG et al.) 19 October 2006 See abstract, paragraphs [0019]-[0036] and figures 1A-3E.	1-26
A	US 2015-0263131 A1 (TOKYO ELECTRON LIMITED) 17 September 2015 See abstract, paragraphs [0027]-[0031] and figures 1A-1G.	1-26
A	US 2009-0017616 A1 (STEPHAN GRUNOW et al.) 15 January 2009 See abstract, paragraphs [0009]-[0016] and figures 1-8.	1-26
A	US 2013-0043556 A1 (DAVID V. HORAK et al.) 21 February 2013 See abstract, paragraphs [0020]-[0044] and figures 1A-5B.	1-26

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 September 2016 (22.09.2016)	**22 September 2016 (22.09.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/000341

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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