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(54) Title: MULTI-LEVEL/MULTI-LAYERED HYBRID PACKAGE

(57) Abstract

An integrated circuit module that includes a plurality of layers (14, 26), each layer having one or more active components (10, 12) disposed thereon and an interconnect structure (34). The interconnect structure is supported by a substrate (30) with the active components either on the substrate or on the interconnect structure itself. The substrates (30) and their associated interconnect structure and active components are disposed in a stack with a low pressure epoxy resin (24). The epoxy resin layers act as both an adhesive and encapsulate and also as an isolation layer. An interconnect structure is also provided on the opposite side of the substrate from the active component and provides an intermediate layer to which the epoxy resin is bonded. The epoxy resin layer is amenable to the active components. Plated-through holes (44) are provided between the interconnect structures on both sides of the substrates and also between various adjacent substrates.
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MULTI-LEVEL/MULTI-LAYERED HYBRID PACKAGE

TECHNICAL FIELD OF THE INVENTION

The present invention pertains in general to packages and, more particularly, to a hybrid microelectronic package using multiple layers and multiple levels.
BACKGROUND OF THE INVENTION

Integrated circuits have seen a significant increase in density due to advances in technology. However, interconnection of the chip to supporting circuitry is still required regardless of how dense the chip is. When multiple chips are utilized in a system, this interconnection can be achieved in a planar manner or in a three-dimensional manner. Present technology that exists for building three-dimensional packages or "modules" involves disposing separate chips on single layers and laminating the layers together with various separating or insulating layers disposed therebetween. However, the manner in which the layers are put together determines the resultant packaging configuration, and also the interconnection scheme.

One example of an interconnection scheme in a multi-layer package is illustrated in U.S. Patent No. 4,288,841, issued to Gogal, et. al. on September 18, 1981. The Gogal device utilizes a plurality of layers with some layers having a chip associated therewith and some layers functioning as interconnects. Plated-through holes are utilized to interconnect the various layers and form the overall circuit structure. The layers are fabricated from ceramics, which have patterns formed thereon.

In another multi-layered package technique, that disclosed in U.S. Patent No. 4,064,552, issued to Angelucci, et. al. on September 20, 1977, a flexible multi-layered system is disclosed. This flexible system consists of a flexible tape layer having a conductor pattern formed thereon which can be disposed over another flexible tape having another pattern formed thereon. Various interconnect schemes are provided for connecting the two layers. The Angelucci device is devised primarily as a flexible printed circuit carrier that functions to support
active circuit components and form an overall electronic module. The basic interconnect scheme utilizes apertures formed in each of the layers through which connections are made.
SUMMARY OF THE INVENTION

The present invention disclosed and claimed herein comprises a method and apparatus for forming a multi-level integrated circuit package. The package includes a plurality of substrates having upper and lower surfaces. Each of the substrates has formed on the upper surface thereof an interconnection layer for providing interconnects to carry signals thereon. The interconnects are formed by patterning the interconnect layer. At least one active component is disposed proximate to the upper surface of one of the plurality of substrates and interfaced with the associated interconnect layer. The substrates are then configured to substantially overly each other and a spacing layer of encapsulant material disposed between the substrates to hold the substrates together and space them apart at a predetermined distance.

In another aspect of the present invention, an intermediate attachment layer is disposed on the lower sides of each of the substrates to provide an intermediate surface that has adherence properties that differ from the surface of the substrate. The encapsulate material that is disposed between the substrates is such that it will adhere better to the intermediate layer. Further, the intermediate layer can be fabricated from a conductive layer for carrying signals and patterned to form a second interconnect layer. The intermediate layer is disposed on the substrate prior to disposing the active component proximate thereto.

In yet another aspect of the present invention, the intermediate layer on the lower side of the substrate and the interconnect layer on the upper side of the substrate are formed on the substrate with a high pressure lamination process. The encapsulate material utilizes a low pressure encapsulant material. Therefore, the high pressure lamination process is performed prior to mounting the active
components on the surface of the substrate, whereas the low pressure encapsulate is utilized to encapsulate the entire active component and interconnect structure on the substrates in a single module.

In a still yet further aspect of the present invention, the active component includes optical elements disposed on the active surface thereof for carrying optical signals. An optical conductor is provided on the upper surface of each of the substrates having associated therewith an active component with active elements on the surface thereof, and abutted with the optical elements on the active component. Further, the active surface of the active component is disposed in substantially the same plane as the upper surface of the substrate.
BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying Drawings in which:

FIGURE 1 illustrates a perspective cut-away view of the multi-layered module of the present invention illustrating two active components and two separate and distinct layers;

FIGURE 2 illustrates an exploded view of a multi-layered module in accordance with the present invention;

FIGURE 3 illustrates a cross-sectional view of two layers of a multi-layered module in accordance with the present invention;

FIGURE 4 illustrates a cross-sectional view of a plated-through hole that has one end buried in the module;

FIGURE 5 illustrates an alternate embodiment of the present invention illustrating the use of optical fibers formed on one of the layers; and

FIGURE 6 illustrates a cross-sectional view of the optical fiber interface of FIGURE 5.
DETAILED DESCRIPTION OF THE INVENTION

Referring now to FIGURE 1, there is illustrated a perspective view of a multi-layered/multi-level module fabricated in accordance with the present invention, illustrating two active component layers. Although only two layers are illustrated, it should be understood that any number of layers can be incorporated. In general, a first active component 10 is illustrated in one layer with a second active component 12 disposed in a second and higher layer. In the first layer, the active component 10 is disposed in substantially the same plane as a layer of Kapton 14. The layer of Kapton 14 has an opening 16 disposed therein for receiving the active component 10. The active component 10 has a plurality of bonding pads 18 disposed on the active surface thereof for interfacing with tabs 20 that extend outward from the surface of the layer of Kapton 14 into the opening 16. This operation will be described in more detail hereinbelow. Although the active component 10 is illustrated as being disposed in the opening 16, it should be understood that the active component 10 could be disposed above the surface of the Kapton layer 14 with the active surface thereof directed downward, the active component 10 mounted in a "flip chip" configuration with no opening required.

Although Kapton is described as the material utilized for the substrates, it should be understood that an epoxy material or other thermal set plastic material could be utilized.

The layer of Kapton 14 has an interconnect pattern disposed on the upper side thereof from which the tabs 20 extend. The tabs 20 are a part of the interconnect pattern. The interconnect pattern is essentially fabricated by laminating a layer of copper onto the surface of the Kapton 14, utilizing a high
pressure adhesive in a high pressure laminating process. The interconnect layer on the upper surface of Kapton layer 14 is then patterned and etched to form the interconnect pattern as illustrated in FIGURE 1. Therefore, the high pressure laminating process results in a metallization layer that has very good adhesion for all temperatures. As will be described hereinbelow, one problem with Kapton is the adhesion of low pressure insulating layers, etc., thereto for forming multilayered systems.

One aspect of the present invention that will be described in more detail hereinbelow is the use of a second layer of metalization or an interconnect pattern disposed on the opposite side of the Kapton 14 from the side on which the tabs 20 extend from. The side on which the tabs 20 extend will be referred to as the mounting surface of the Kapton layer 14, whereas the other side thereof will be referred to as the interconnect surface. On the interconnect surface, the interconnect layer is formed in the same way as that on the mounting side; that is, a conductive copper layer is first laminated onto the surface of the Kapton layer 14 with a high pressure laminating process prior to mounting of the active component 10 and then patterned and etched. The interconnect layer on the interconnect side of the Kapton layer 14 is illustrated by a single metal "run" 22 that extends outward from a cut-away portion.

The interconnect side of the Kapton layer 14 is disposed adjacent a layer of low pressure epoxy 24. As will be described hereinbelow, the low pressure epoxy 24 is applied after mounting of the component 10 in the opening 16, this layer forming a good adhesion with the interconnect side of the Kapton layer 14. An important aspect of the present invention is the utilization of a low-temperature, low-pressure layer adjacent to the surface of the Kapton layer 14 to provide an adhesion between multiple levels of the resultant module. Although conventional high pressure adhesives can be utilized, the high pressure nature
results in damage to the relatively fragile active components 10. Therefore, use of the low-pressure, low-temperature epoxy layer 24 provides an adhesive between two adjacent layers which can be formed therebetween with relatively low pressure. Also, as will be described hereinbelow, the pattern on the interconnect side and on the mounting side of the Kapton layer 14 assists in adhesion, since some epoxy materials have poor adhesion with the surface of the Kapton 14. However, it is the use of the low-pressure adhesive material that provides important aspects of the present invention in conjunction with both active components and associated substrates and interconnect layers.

The active component 12 is disposed in the same plane as a Kapton layer 26. The active component 12 is disposed within an opening 28 within a Kapton layer 26 and separated from the edges thereof. The active component 12 has bonding pads 18 disposed thereon with tabs 20 extending from the mounting surface of the Kapton layer 26 across the gap between the opening 28 and the edge of the active component 12 to interface with the bonding pads 18. The tabs 20 are part of an interconnect pattern on the mounting side of the Kapton layer 26. A layer of epoxy 30 is disposed between the mounting surface of the Kapton layer 14 and the interconnect side of the Kapton layer 26. The interconnect side of the Kapton layer 26 has an interconnect pattern disposed thereon, which is illustrated with two runs 34 and 36, illustrated in a cut-away view. These are similar to the run 22 on the interconnect side of the Kapton layer 14. A layer of epoxy 38 is disposed on the mounting side of the Kapton layer 26, it being understood that additional layers can be disposed above the Kapton layer 26.

The interconnect patterns on both the mounting side and the interconnect side of both of the Kapton layers 14 and 26 can be interconnected through various plated-through holes. For example, the run 22 has a plated-through hole 39 disposed therethrough and, adjacent thereto, another metal run 40 is illustrated as
interfacing with a plated-through hole 44 through the Kapton layer 14. The run 40 extends back under the interconnect side of the Kapton layer 14. A run 42 on the mounting side of the Kapton layer 14 interfaces through the plated-through hole 44 that extends through the Kapton layer 14 interconnecting both the run 42 and the run 40.

The plated-through holes can extend between multiple layers. This is illustrated with a plated-through hole 46 that extends from a run 48 on the mounting surface of the layer of Kapton 14 to a run 50 that is disposed on the interconnect surface side of the Kapton layer 26. This plated-through hole 46 can extend upward to multiple layers. As will be described hereinbelow, this plated-through hole can be either completely filled or just hollow with the sides thereof conductive.

Referring now to FIGURE 2, there is illustrated an exploded view of the module of the present invention illustrating one of the Kapton layers and the overlying and underlying epoxy layers. The general module is referred to by a reference numeral 60. An upper Kapton layer 62 is illustrated as having an opening 64 disposed therein for receiving an active component. The active component is referred to by a reference numeral 66. The Kapton layer 62 has a mounting side and an interconnect side, as described above. On the mounting side, an interconnect pattern of runs 68 are provided, some of which terminate in tabs 20 that extend into the opening 64 for interface with the bonding pads 18 on the active surface of the active component 66. The layer of Kapton 62 further has a plurality of holes 70 disposed therethrough, which interface with portions of the run 68, for example, a portion 72, to provide for plated-through holes, as described hereinabove.
The interconnect side of the Kapton layer 62 has an interconnect pattern disposed thereon, which interconnect pattern is formed with a plurality of runs 74. The runs 74 are similar to the runs 68 with the exception that they do not have tabs 20 disposed on terminating ends thereof. The runs 68 and 74 are fabricated by first high pressure laminating a layer of copper to the respective surfaces of the Kapton layer 62 and then patterning and etching the copper layers, all prior to mounting of the active component 66.

A layer of epoxy 76 is formed on the mounting surface of the Kapton layer 62 above the run 68 after mounting of the active component 66. The epoxy layer 76 is formed with low pressure epoxy materials. Further, an epoxy layer 78 is disposed on the opposite side of the Kapton layer 62 from the epoxy layer 76 on the interconnect side thereof. This epoxy layer 78 contacts on the other side thereof another Kapton layer 80, which also may contain active components.

The epoxy layer 78 has disposed therethrough plated-through holes 82 that extend upward through the Kapton layer 62 and the holes 70. The plated-through holes 82 form a wall that extends down through the epoxy layer 78 into underlying Kapton layers 80 and the various runs disposed on either the mounting side or the interconnect sides thereof. For example, the runs 74 have two end portions 84 and 86 for interfacing with the plated-through holes 82 and the metal disposed therein.

Referring now to FIGURE 3, there is illustrated a detailed cross-sectional diagram of the structure of FIGURE 1, illustrating the interface between the active components 10 and 12 and the Kapton layers 14 and 26, respectively. In the cross-sectional diagram, each of the Kapton layers is illustrated as having a conductor disposed on the mounting side and on the interconnect side. Also, these are patterned to form various runs. The Kapton layer 26, for example, has
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a run 88 disposed on one side thereof and attached to the mounting side of the Kapton layer 26 with a layer of high-pressure adhesive 90. On the interconnect side thereof, a run 92 is disposed and attached thereto with a layer of high pressure adhesive 94. Although described as a run, the run 92 could be an entire shielding layer of copper.

The Kapton layer 14 also has metal runs disposed on the mounting and interconnect sides thereof. On the mounting side thereof, a run 96 is illustrated that is attached thereto by a layer of high pressure adhesive 98. On the interconnect side thereof, a run 100 is disposed thereon and attached with a layer of high pressure adhesive 102. Each of the runs 88 and 96 have disposed thereon the tabs 20 that extend over the openings 16 and 28, respectively.

From a dimensional standpoint, the Kapton substrates 14 and 26 have a thickness of approximately 5 mils. The runs 88, 92, 96 and 100, have a thickness of approximately 1.5 mils. The adhesive layers 90, 94, 98 and 102, have a thickness of approximately 1 mil. The active components 10 and 12 have a thickness of approximately 20 mils. The distance between the bottom of the active component 12 and the uppermost portion of the underlying layer, i.e., the upper surface of the runs 88 or 96, is on the order of 1-2 mils. Therefore, each layer would have a thickness of approximately 22-25 mils, this being determined primarily by the thickness of the active components 10 and 12. With respect to co-efficient of expansion, the active components 10 and 12, when fabricated from a semi-conductor material, have a co-efficient of around four. By comparison, the Kapton layers 14 and 26 have a co-efficient of expansion of around thirty and the epoxy layers 24 and 30 have a co-efficient of expansion of around twenty.

The epoxy is disposed such that it will fill virtually all voids between the layers.
In fabrication, the Kapton substrate is first formed by using a high pressure lamination procedure wherein layers of copper or similar metal are disposed on either side of the Kapton layer. These are then patterned and etched to form the various interconnect patterns and the tabs 20. The opening is pre-formed in the Kapton substrate for disposing the active component. Typically, the Kapton substrate is on a "tape" which is a series of interconnect patterns. The substrate is then turned upside down and an active component then disposed in the opening and aligned with the tabs. Typically, a raised "bump" is disposed on the chip or active component during fabrication, which requires only heat processing to form the bond between the bonding pad 18 and the tab 20. This is conventional technique. However, any automated bonding technique that allows the bonding pad 18 to be adhered to the tab 20 could be utilized. For example, wire bonding could be utilized from the tab 20 onto the bonding pad 18, wherein the tab would not extend past the edge of the opening 28, or would only extend a very short distance.

After the Kapton substrate has been formed, the pattern is defined thereon and the active components disposed in the openings and bonded to the tabs 20, the layers then assembled. This is facilitated by utilizing a low temperature epoxy, which, in the preferred embodiment, is a low stress glob top semiconductor encapsulate FP4401, manufactured under the trademark HYSOL by Dexter Electronics Materials Division. The specifications are described in a Bulletin No. E3-434B, which is incorporated herein by reference. In general, the encapsulate is a thixotropic, high-purity epoxy encapsulate. This material has a high-glass transition temperature and low co-efficient of thermal expansion. It has a
viscosity between 73-77, with a co-efficient of linear thermal expansion of 22 x $10^4$ IN/IN°C. The glass transition is approximately 160°C with a hardness of 90 Shore D. The thermal conductivity is 16 x $10^{-14}$ CAL/SEC x CM x °C. The specific gravity is 1.78-1.82 with a flammability of 94HB. In general, the product is cured for approximately three hours at 170°C or six hours at 160°C.

When the epoxy is applied, it is only necessary to sandwich the multiple layers together with the epoxy and move them in a lateral motion to ensure that the epoxy has filled all voids. Thereafter, the epoxy is cured to form the layers 24 and 30.

With use of the present material, sufficient adhesion is obtained between the layers 24 and 30 and the upper and lower surfaces of the Kapton layers 14 and 26. For example, the layer 30 adheres to the mounting surface of the Kapton layer 14 and the run 96 disposed thereon, and also to the interconnect side of the Kapton layer 26 and the run 92 disposed thereon. Due to the use of the particular epoxy for the layer 30 and the layer 24, the run 92 is needed for two reasons. First, it provides an interconnect layer and second, it provides an adhesive surface for the epoxy 30. However, it should be understood that other materials may be utilized that will provide good adhesion with the surface of the Kapton layer 26. Although the specific material utilized in the present invention may adhere to the Kapton layer 26, the use of the run 92 and the remaining portions of the interconnect layer provide better adhesion. The important aspect of the present invention is the use of a low temperature low pressure thermal set plastic material for the adhesion layer or insulating layer between the various active layers.

Referring now to FIGURE 4, there is illustrated a cross-sectional view of a plated-through hole, illustrating a buried termination therefor. Three Kapton layers 106, 108 and 110 are illustrated with layer 106 separated from layer 108
by an epoxy layer 112, and layer 108 separated from layer 110 by an epoxy layer 114. An epoxy layer 116 is disposed on the opposite side of layer 110 from the epoxy layer 114. Each of the Kapton layers 106, 108 and 110 have conductive layers disposed on either side thereof. Kapton layer 106 has a conductive layer 118 disposed on the upper side thereof and a conductive layer 120 disposed on the lower side thereof. Similarly, the Kapton layer 108 has a conductive layer 122 disposed on the upper side thereof and a conductive layer 124 disposed on the lower side thereof. Kapton layer 110 has a conductive layer 126 disposed on the upper side thereof and a conductive layer 128 disposed on the lower side thereof.

A hole is formed through the layers 106-110 and the epoxy layers 112 and 114 without penetrating layer 116. The hole is referred to by the reference numeral 130. The sides of the hole are lined with a conductive material 132 with conventional plating processes. Although illustrated as a lining, it should be understood that this also could be a plug wherein the entire hollow cavity 130 is filled. The lining 132 contacts all of the conductive layers 118-128, such that they conduct therewith. As this is a cross-sectional diagram, each of the conductor layers 126-128 could represent a thin run and it is not necessary that each run terminate at the lining 132. Therefore, one of the conductive layers 118 could conduct with the conductive layer 128 without conducting with the intermediate conductive layers 120-126.

In order to form the hole 130, the layers 106-110 are first formed and then a hole drilled therethrough with a conventional drilling mechanism. If it is to be a buried layer, the module is assembled in multiple steps with only a few layers assembled, the hole drilled, the hole plated through and then subsequent layers disposed on the upper end thereof. This can be done multiple times to achieve the entire effect. It is only necessary that when the hole is drilled, the edge of the conductive layer that terminates at the hole be exposed. This is the reason
that the portion at the end of each of the runs that terminates at the plated-through hole has an expanded area. By drilling through the expanded area, metal that is a portion of the run will be adjacent to and surround the potential plated-through hole. When the plating material is disposed within the hole, a conductive path is formed.

Referring now to FIGURE 5, there is illustrated an alternate embodiment of the present invention. A Kapton layer 134 is illustrated that is separated from another Kapton layer 136 by an epoxy layer 138. An active component 140 is disposed in an opening 142 in the Kapton layer 134. In a similar manner, an active component 144 is disposed in an opening 146 on the Kapton layer 136. The active component 140 has a plurality of optical waveguides 148, disposed on the upper surface thereof, in addition to the bonding pads 18. Tabs 20 extend from an interconnect pattern formed with metal runs 150 disposed on the mounting surface of the Kapton layer 134. Additionally, optical fibers 152 are provided on the mounting surface of the Kapton layer 134 that are butted up against an optical junction on the optical waveguides 148. This optical junction is typically an optical diode that makes the conversion from an optical waveguide to an optical fiber. This is conventional in fabricating optical semiconductor devices. One of the primary disadvantages to forming optical semiconductor devices is the alignment of the optical fibers 152 and the optical waveguides 148 on the surface of the chip. The reason that this is difficult, is that typically the surface of the chip is higher than the mounting surface on which it is disposed. With the present invention, the surface of the chip is disposed in approximately the same plane as the mounting surface of the Kapton layer 134 on which the optical fibers are disposed. Therefore, the optical fibers 152 can be disposed on
the mounting surface of the Kapton layer 134 after the active component 140 has been mounted thereon with the tabs 20 interfaced with the mounting pads 18. The optical fibers 152 then can be laminated to the mounting surface of the Kapton layer 134 with an appropriate adhesive.

The optical device 144 also has associated therewith optical devices such as waveguides. An optical fiber 154 is disposed on the mounting surface of the Kapton layer 136 that interfaces with the upper surface of the active component 144 and extends over to an optical coupler 156. The optical coupler 156 can be laminated onto the surface of the Kapton layer 136.

Referring now to FIGURE 6, there is illustrated a cross-sectional view of the Kapton layer 134 and the epoxy layer 138. The active component 140 is illustrated as having a surface that is essentially co-planar with the upper surface of the Kapton layer 134, but slightly disposed therebeneath. The optical fiber 152 is adhered to the surface of the Kapton layer 134 and the mounting side thereof, with an adhesive layer 159. The end of the optical fiber is then aligned with respect to the optical waveguide 144, or similar optical component on the active surface of active component 140, and then a glass epoxy adhesive applied thereto. An interface device 160 is provided for this purpose, which interface device 160 could be a diode.

In summary, there has been provided a multi-layered, multi-level hybrid package utilizing two substrates having an interconnect layer and active components disposed on one surface thereof. The combined active components and interconnect layers and associated substrate are disposed adjacent to similar structures to form a multi-layer module with active components imbedded in the middle of the modules. The layers are adhered together with a low pressure epoxy rosin.
Although the preferred embodiment has been described in detail, it should be understood that various changes, substitutions and alterations can be made therein without departing from the spirit and scope of the invention as defined by the appended claims.
WHAT IS CLAIMED IS:

1. A method for forming a multi-level package, comprising:
   providing first and second substrates having upper and lower surfaces;
   forming on at least one of the surfaces of both the first and second
   substrates an interconnection layer of interconnects for carrying signals;
   disposing at least one active component proximate to the surface of one of
   the first and second substrates and interfaced with at least one interconnection
   layers;
   disposing the first and second substrates in a substantially overlying
   configuration; and
   forming a spacing layer of a encapsulant material between the first and
   second substrates with the at least one active component disposed thereon to hold
   the first and second substrates together and space them apart in a predetermined
   distance.

2. The method of Claim 1 wherein the first and second substrates are
   flexible.

3. The method of Claim 1 wherein the first and second substrates are
   comprised of a polyimide material.

3.5 The method of Claim 1 wherein the first and second substrates are
   comprised of a thermal set plastic material.

4. The method of Claim 1 wherein the encapsulant material is
   comprised of a low pressure thermal set plastic.
5. The method of Claim 4 wherein the thermal set material is a thixotropic material.

6. The method of Claim 1 and further comprising forming an intermediate attachment layer on the opposite surface of the first and second substrates from the surface on which the interconnection layer is formed, an intermediate attachment layer formed prior to disposing the at least one semiconductor component on the surface of one of the first and second substrates, the intermediate attachment layer providing surface properties different from the properties of the first and second substrates to which the encapsulant layer adheres.

7. The method of Claim 6 wherein the encapsulant material is a low pressure epoxy resin material.

8. The method of Claim 7 wherein the intermediate attachment layer is fabricated from copper.

9. The method of Claim 8 wherein the step of forming the intermediate attachment layer on the first and second substrates comprises adhering the copper layer to the surface of the first and second substrates by a high pressure lamination process.

10. The method of Claim 6 wherein the step of forming the intermediate attachment layer comprises patterning the intermediate attachment layer to form an interconnection network.
11. The method of Claim 1 wherein the at least one active component is disposed on the surface of the one of the first and second substrates that is substantially beneath the other of the first and second substrates.

12. The method of Claim 1 and further comprising disposing a plurality of active components on the surface of the first and second substrates and interfaced with the respective interconnection layers.

13. The method of Claim 1 wherein the at least one active component has the active surface thereof disposed in substantially the same plane as the surface of the one of the first and second substrates to which it is proximate to.

14. The method of Claim 13 and further comprising: forming an opening in the one of the first and second substrates on which the at least one active component is disposed proximate to; and disposing the active component in the opening and interfaced with the interconnect layer on the associated one of the first and second substrates.

15. The method of Claim 1 wherein the first and second substrates are disposed in an overlying configuration such that one of the first and second substrates overlies the first and second substrates and wherein the step of forming the spacing layer of encapsulant material comprises forming the layer of encapsulant material such that it fills all voids between the first and second substrates in the overlying configuration.

16. The method of Claim 1 wherein the spacing of encapsulant material provides electrical insulation.
17. The method of Claim 1 wherein the active component includes optical elements disposed thereon for carrying optical signals and further comprising:

   disposing an optical conductor on the interconnection layer and interfaced with the at least one active component; and

   interfacing the optical conductor with the optical elements on the at least one active component associated therewith.
18. A method for forming a multi-level package, comprising:
    providing a plurality of planar substrates having upper and lower surfaces;
    forming an interconnection layer on the upper surface of each of the
    plurality of substrates;
    forming an interconnect pattern in select ones of the interconnection layers;
    disposing a plurality of active components proximate to the surface of
    select ones of the substrates having interconnect patterns formed thereon, each of
    the active components having an active surface that is interfaced with the
    associated interconnect pattern;
    disposing the plurality of substrates in a layered configuration such that
    each of the plurality of substrates substantially overly each other; and
    forming a spacing layer of encapsulant material between a plurality of
    substrates to hold adjacent ones of the plurality of substrates together and space
    them apart at a predetermined distance.

19. The method of Claim 18 wherein the substrates are comprised of
    a flexible material.

20. The method of Claim 19 wherein the substrates are comprised of
    a polyimide material.

20.5 The method of Claim 19 wherein the substrates are comprised of
    a thermal set plastic material.

21. The method of Claim 18 wherein the encapsulant material is
    comprised of a low pressure epoxy resin material.
22. The method of Claim 21 wherein the step of forming the interconnect layer comprises laminating a layer of conducting material on the upper surface of the plurality of substrates under high pressure conditions with a high pressure adhesive.

23. The method of Claim 22 and further comprising laminating a layer of material on the lower surfaces of each of the plurality of substrates, the material having adherence characteristics that are different from the adherence characteristics of the lower surfaces of the plurality of substrates and allows the low pressure epoxy resin to adhere thereto.

24. The method of Claim 23 wherein select ones of the layers of material laminated to the lower surfaces of the substrates are conductive and further comprising patterning the conductive ones of the layers of material on the lower surfaces of the plurality of substrates to form an interconnect layer thereon.

25. The method of Claim 24 and further comprising interconnecting select ones of the interconnect patterns on the upper surfaces of the plurality of substrates and select ones of the interconnect patterns on the lower surfaces of the plurality of substrates to each other in a predetermined interconnect pattern.

26. The method of Claim 18 and further comprising interconnecting select ones of the interconnection patterns on the surfaces of the plurality of substrates to each other with conductive members.

27. The method of Claim 26 wherein the step of interconnecting ones of the interconnect patterns between the plurality of substrates comprises:

forming a via through the substrates and spacing layers between the upper surfaces of the plurality of substrates; and
plating the sides of the via with material for carrying signals between select portions of the interconnect patterns on the surfaces of select ones of the plurality of substrates that the via interfaces with.

28. The method of Claim 18 wherein select ones of the active components have optical elements on the active surfaces thereof for carrying optical signals and further comprising:

forming an optical conductor as part of the interconnect pattern on the associated ones of the substrates that are associated with the active components having optical elements disposed on the active surface thereof; and

interfacing the optical conductor on the associated upper surface of the plurality of substrates.

29. The method of Claim 28 wherein the active surface of the ones of the active components having optical elements associated therewith is substantially planar with the upper surface of the associated substrate.
30. A multi-level/multi-layer integrated circuit module, comprising:
   a plurality of planar substrates having upper and lower surfaces and
   disposed in a substantially overlying configuration;
   an interconnect layer disposed on the upper surfaces of select ones of the
   plurality of substrates, each of the interconnect layers having an interconnect
   pattern formed therein;
   a plurality of active components disposed proximate to the upper surfaces
   of select ones of the plurality of substrates and the associated interconnect pattern
   thereon and interfaced with the associated interconnect pattern; and
   a spacing layer of encapsulant material disposed between adjacent ones of
   the substrates.

31. The module of Claim 30 and further comprising an interconnect
   layer disposed on the lower surfaces of select ones of said plurality of substrates
   and having interconnect patterns formed therein.

32. The module of Claim 31 and further comprising a plurality of
   vertical interconnects that interconnect select portions of the interconnect patterns
   on the upper surfaces and lower surfaces of the plurality of substrates with other
   interconnect patterns on other of said plurality of substrates.

33. The module of Claim 32 wherein the plurality of interconnects
   comprise:
   a plurality of vias disposed between the upper and lower surfaces of select
   ones of said substrates and passed through all adjacent ones of said substrates; and
   a plating material for being disposed within said vias for allowing signals
   to pass between ones of said interconnect patterns that are interfaced with said via
   through said interconnect patterns.
34. The module of Claim 30 wherein said encapsulant material is an epoxy resin material.

35. The module of Claim 30 wherein said substrates are flexible.

36. The module of Claim 30 wherein said substrates are comprised of a Kapton material.

36.5 The module of Claim 30 wherein said substrates are comprised of a thermal set plastic material.

37. The module of Claim 30 wherein select ones of said active components have associated therewith active elements for carrying optical signals on the active surface of the associated active component and further comprising:

an optical conductor for carrying optical signals, said optical conductor disposed on the upper surface of the associated one of said plurality of substrates; and

means for interfacing said optical conductor with active elements on said active component.

38. The module of Claim 37 wherein the active surface of said active components having the active elements disposed thereon is substantially planar with respect to the upper surface of the associated one of said plurality of substrates.

39. The module of claim 30 wherein said active components are disposed such that the active surface thereof is substantially in the same plane as the upper surface of said associated substrates.
40. The module of Claim 29 wherein select ones of said substrates have holes disposed therein for receiving said associated active components, said active components mounted such that the active surface thereof is in substantially the same plane as the upper surface of said associated substrates.
INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/02295

A. CLASSIFICATION OF SUBJECT MATTER
   IPC(5) : H05K 7/06
   US CL : 361/396
   According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
   Minimum documentation searched (classification system followed by classification symbols)
   U.S. : 361/396; 156/239; 174/52.2, 251, 253, 254, 155, 256;357/74, 80; 361/393, 395, 396, 398, 414

   Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

   Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

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<tr>
<th>Category*</th>
<th>Citation of document, with indication, where appropriate, of the relevant passages</th>
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Further documents are listed in the continuation of Box C. See patent family annex.

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Date of mailing of the international search report: 26 AUG 1992

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### INTERNATIONAL SEARCH REPORT

**C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT**

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