CIRCUIT CONFIGURATION FOR SWITCHING OVER A RECEIVER CIRCUIT IN PARTICULAR IN DRAM MEMORIES AND DRAM MEMORY HAVING THE CIRCUIT CONFIGURATION

Inventors: Eckhard Brass, Unterhaching (DE); Thoai-Thai Le, Munchen (DE); Jurgen Lindolf, Friedberg (DE); Joachim Schnabel, Munchen (DE)

Correspondence Address:
LERNER AND GREENBERG, PA.
POST OFFICE BOX 2480
HOLLYWOOD, FL 33022-2480 (US)

Publication Classification

Int. Cl. G06G 7/12
U.S. Cl. 327/563

ABSTRACT

A circuit configuration for switching over a receiver circuit, in particular in DRAM memories, between a standby mode and an operating mode, includes a differential amplifier functioning as a receiver receiving a control voltage derived from a reference current and generated or fed in for setting a correct operating point of said differential amplifier. A line feeds a current for generating the control voltage. The switching elements are disposed in said line for each receiver. The switching elements are permanently closed in the operating mode by an enable signal present at said switching elements for continuously supplying the current for generating the control voltage. The switching elements are closed at discrete times or periodically in the standby mode by feeding a refresh signal for discontinuously refreshing the control voltage. A DRAM memory having the circuit configuration is also provided.
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BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] The invention relates to a circuit configuration for switching over a receiver circuit, in particular in DRAM memories, between a standby mode and an operating mode. A differential amplifier functions as a receiver. A control voltage derived from a reference current and serving for setting a correct operating point of the differential amplifier is generated or fed in for each differential amplifier. The invention also relates to a DRAM memory having the circuit configuration.

[0002] In the case of laptop or notebook applications, in particular, it is necessary for memory modules, in particular DRAM memory modules, which are contained therein, to also have a low current consumption in a power-down or standby mode. In the memory module, differential amplifiers function as receivers, which need a control voltage for setting the correct operating point thereof. In existing DRAM memory modules, the control voltage is generated from a reference current which is distributed through current mirrors. Whereas the receivers can be switched off in the power-down or standby mode, the distributed currents must not be switched off, in order to ensure that the receivers are immediately available again, i.e. as far as possible in one clock cycle, in the event of reactivation of the memory chip in the operating mode.

[0003] Therefore, a standby current continuously flows through the known memory chips while they are in the standby mode. The standby current is not negligible and, when a laptop or notebook is battery-operated, is a constant load on the battery. The current paths distributed through current mirrors could be switched off in the standby mode by a respective switching transistor located in the individual lines feeding the current to the receivers. However, as already mentioned above, the control voltage of the receivers must not be switched off in the standby mode, since otherwise the receivers might possibly not be able to be reactivated quickly enough in the event of switching over to the operating mode.

[0004] U.S. Pat. No. 5,557,221 (columns 1 to 16, figure sheets 1 to 8) describes and shows, in particular in FIG. 8, a circuit configuration for switching over a receiver circuit, in which switching over between a first operating mode and a second, current-saving mode is effected in a manner dependent on a frequency or amplitude present at an input.

[0005] U.S. Pat. No. 5,920,208 discloses a switch-over device for a sense amplifier with which an end of a read operation is detected through the use of a data comparison, and a switch-over to a power-down mode is performed.

SUMMARY OF THE INVENTION

[0006] It is accordingly an object of the invention to provide a circuit configuration for switching over a receiver circuit, in particular in DRAM memories, and a DRAM memory having the circuit configuration, which avoid the hereinafore-mentioned disadvantages of the heretofore-known switch-over configurations between standby or power-down mode and operating mode and which maintain a control voltage of receivers even in the standby or power-down mode with reduced standby current, in such a way that the receivers can be activated sufficiently quickly, e.g. within a few nanoseconds, in the event of a transition to the operating mode.

[0007] With the foregoing and other objects in view there is provided, in accordance with the invention, a circuit configuration for switching over a receiver circuit between a standby mode and an operating mode. The configuration comprises differential amplifiers each functioning as a receiver receiving a control voltage derived from a reference current and fed in or generated, for setting a correct operating point of the differential amplifier. A line feeds a current for generating the control voltage. Switching elements are disposed in the line for each receiver. The switching elements are permanently closed in the operating mode by an enable signal present at the switching elements for continuously supplying the current for generating the control voltage. The switching elements are closed at discrete times or periodically in the standby mode by feeding a refresh signal for discontinuously refreshing the control voltage.

[0008] Consequently, with the present circuit configuration according to the invention, the control voltage for the differential amplifiers functioning as a receiver circuit is refreshed discontinuously or periodically. In this way, the standby current for the receivers is considerably reduced. In DRAM memories, in particular, a separate generator for a periodic refresh signal for switching on the switching elements can be omitted if, as is preferred, the self-refresh signal of the DRAM memory is used. It goes without saying, however, that it is also possible to use a switch-on signal for the switching elements which is derived from the self-refresh signal and has a period that is a multiple of the self-refresh period.

[0009] In order to stabilize the control voltage fed discontinuously or periodically to the receivers, backup capacitors assigned to each receiver can be used for prolonging the refresh time.

[0010] Other features which are considered as characteristic for the invention are set forth in the appended claims.

[0011] Although the invention is illustrated and described herein as embodied in a circuit configuration for switching over a receiver circuit, in particular in DRAM memories, and a DRAM memory having the circuit configuration, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

[0012] The construction and method of operation of the invention, together with additional objects and advantages thereof will be best understood from the following description of specific embodiments when read in connection with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The figure of the drawing is a schematic and block diagram of one possible realization of a circuit configuration according to the invention.
DESCRIPTION OF THE PREFERRED EMOIDMENTS

[0014] Referring now in detail to the single figure of the drawing, there is seen a differential amplifier 6, 7 which forms a receiver for a load 5 having an operating point defined by a control voltage that is generated from a current flowing from a current mirror transistor 2 through an enable transistor 3. The enable transistor 3 is closed by an enable signal (EN) 16 in an operating mode. An intensity of the current flowing from the current source 2 is determined by a reference voltage $V_{IRAS}$ which is determined by a charge of a backup capacitor 14 in a standby mode. In standby, in a manner described below, the backup capacitor 14 having a capacitance C is charged periodically or discontinuously by a current Idis_n flowing through a lead 13. This current Idis originates from a current mirror circuit including current mirror transistors 4, 4, . . ., 4, a transistor 8 and a reference current source 9 through which a reference current IREF flows.

[0015] In order to ensure that the receivers are available again within a few nanoseconds in the event of reactivation of the chip in the operating mode, as mentioned, in the standby mode the control voltage for the differential amplifier 6, 7 is taken from the charge of the backup capacitor 14.

[0016] According to the invention, switching elements 10, 11, 12 are provided in the lead 13 for generating the reference voltage $V_{IRAS}$. The switching elements 10 and 11 are preferably MOS transistors, and the switching element 12 forms an OR element which receives a periodic or discontinuous refresh signal SRF 15 in the standby mode and receives the enable signal (EN) 16 in the operating mode.

[0017] Furthermore, the backup capacitor 14 is constructed in such a way that it can stabilize the reference voltage $V_{IRAS}$ and thus prolong the refresh time.

[0018] During “power-down”, i.e., in the standby mode (EN=0), the MOS transistors 10, 11 are activated only in a refresh cycle (SRF periodically or discontinuously equal to 1) and switch the current fed through the line 13 to the transistor 1.

[0019] In the case of a DRAM memory, the refresh signal 15 may be the periodic self-refresh signal that is present anyway in the memory. A generator for generating the refresh signal 15 can thus be omitted.

[0020] It goes without saying that the refresh period may also be a multiple of the self-refresh period.

[0021] In other applications, the refresh signal 15 may also be non-periodic as long as the capacitance of the backup capacitor 14 is large enough to bridge the longest time duration between two successive refresh signals.

[0022] With the above-described embodiment of a circuit configuration according to the invention, as illustrated in the figure, the standby current in the power-down or standby mode can be significantly reduced and the receivers can nevertheless be reactivated very quickly in the event of switch-over to the operating mode.

[0023] It goes without saying that the circuit configuration according to the invention can be used not only in DRAM memories but also in other configurations in which a reduction of the standby current flowing through receivers in the standby mode is desirable.

We claim:

1. A circuit configuration for switching over a receiver circuit between a standby mode and an operating mode, comprising:

a differential amplifier functioning as a receiver receiving a control voltage derived from a reference current, for setting a correct operating point of said differential amplifier;

a line feeding a current for generating the control voltage;

and

switching elements disposed in said line for said receiver, said switching elements permanently closed in the operating mode by an enable signal present at said switching elements for continuously supplying the current for generating the control voltage, and said switching elements closed at discrete times or periodically in the standby mode by feeding a refresh signal for discontinuously refreshing the control voltage.

2. The circuit configuration according to claim 1, wherein the control voltage is generated for said differential amplifier.

3. The circuit configuration according to claim 1, wherein the control voltage is fed in to said differential amplifier.

4. The circuit configuration according to claim 1, wherein said switching elements are MOS switching transistors.

5. The circuit configuration according to claim 1, wherein the refresh signal is a memory self-refresh signal of a DRAM memory.

6. The circuit configuration according to claim 1, wherein the refresh signal is a signal having a period duration being a multiple of a period of a memory self-refresh signal of a DRAM memory.

7. The circuit configuration according to claim 1, including at least one backup capacitor for said receiver, said at least one backup capacitor having a capacitance sufficient for storing a charge due to the current supplied by said switching elements over a time duration exceeding a longest period duration of the refresh signal.

8. A DRAM memory, comprising a circuit configuration for switching over a receiver circuit between a standby mode and an operating mode, said circuit configuration including:

a differential amplifier functioning as a receiver receiving a control voltage derived from a reference current, for setting a correct operating point of said differential amplifier;

a line feeding a current for generating the control voltage;

and

switching elements disposed in said line for said receiver, said switching elements permanently closed in the operating mode by an enable signal present at said switching elements for continuously supplying the current for generating the control voltage, and said switching elements closed at discrete times or periodically in the standby mode by feeding a refresh signal for discontinuously refreshing the control voltage.

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