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[Continued on next page]

(54) Title: SHARED INTERRUPT CONTROLLER FOR A MULTI-THREADED PROCESSOR

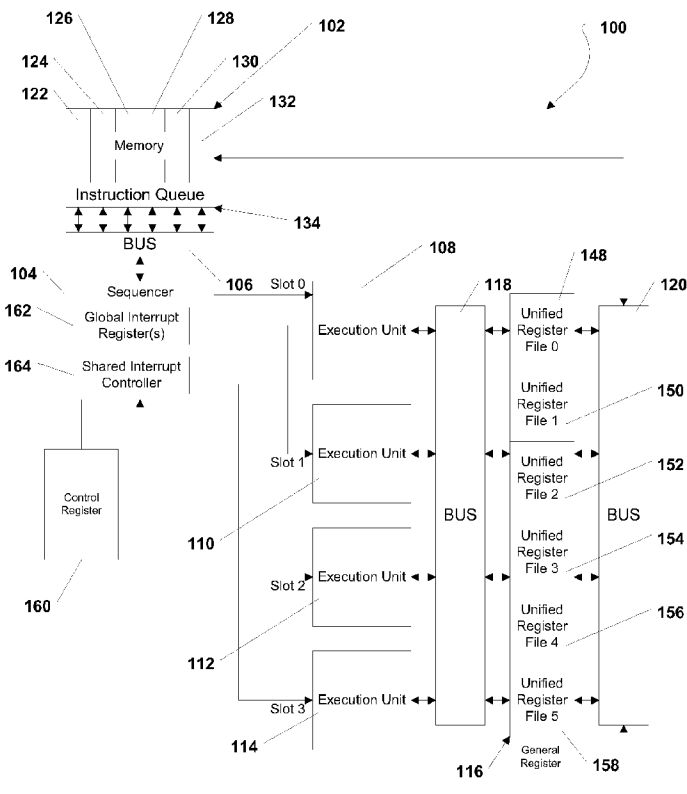


FIG. 1

(57) Abstract: A multi-threaded processor is disclosed that includes a sequencer adapted to provide instructions associated with one or more threads of a multi-threaded processor. The sequencer includes an interrupt controller adapted to receive one or more interrupts and to selectively allow a first thread of the one or more threads to service at least one interrupt. The interrupt controller includes logic to preclude a second thread of the one or more threads from responding to the at least one interrupt.

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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/088938 A1 (CODRESCU LUCIAN [US] ET AL) 19 April 2007 (2007-04-19) abstract; figures 3,4 paragraphs [0008] - [0010], [0027], [0030], [0033]	1-31
A	US 6 163 829 A (GREIM MICHAEL C [US] ET AL) 19 December 2000 (2000-12-19) column 2, lines 3-40 column 25, lines 1-12 column 25, lines 27-28	1-31

Further documents are listed in the continuation of Box C.

See patent family annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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