

[54] **CIRCUIT ARRANGEMENT FOR RHYTHMIC, INTERMITTENT OPERATION OF SEPARATE MAGNETS**

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[56]

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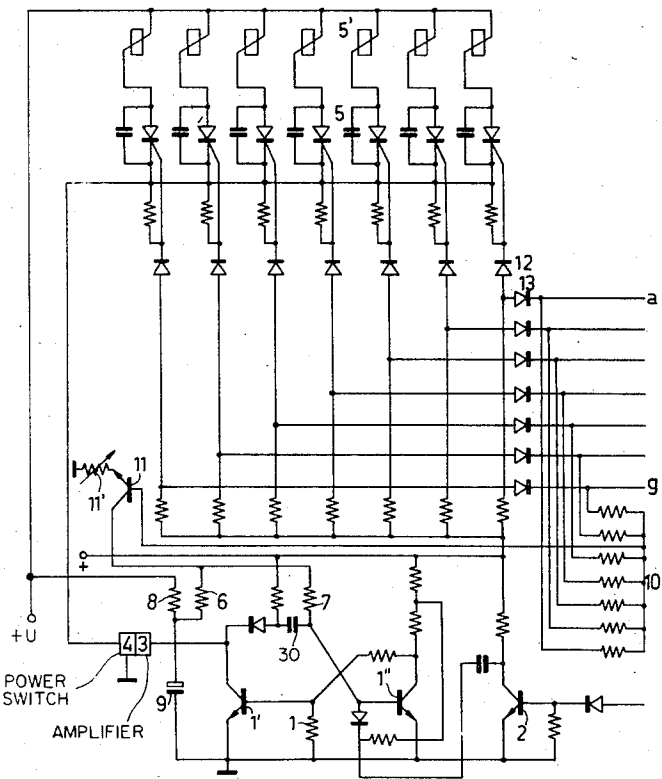
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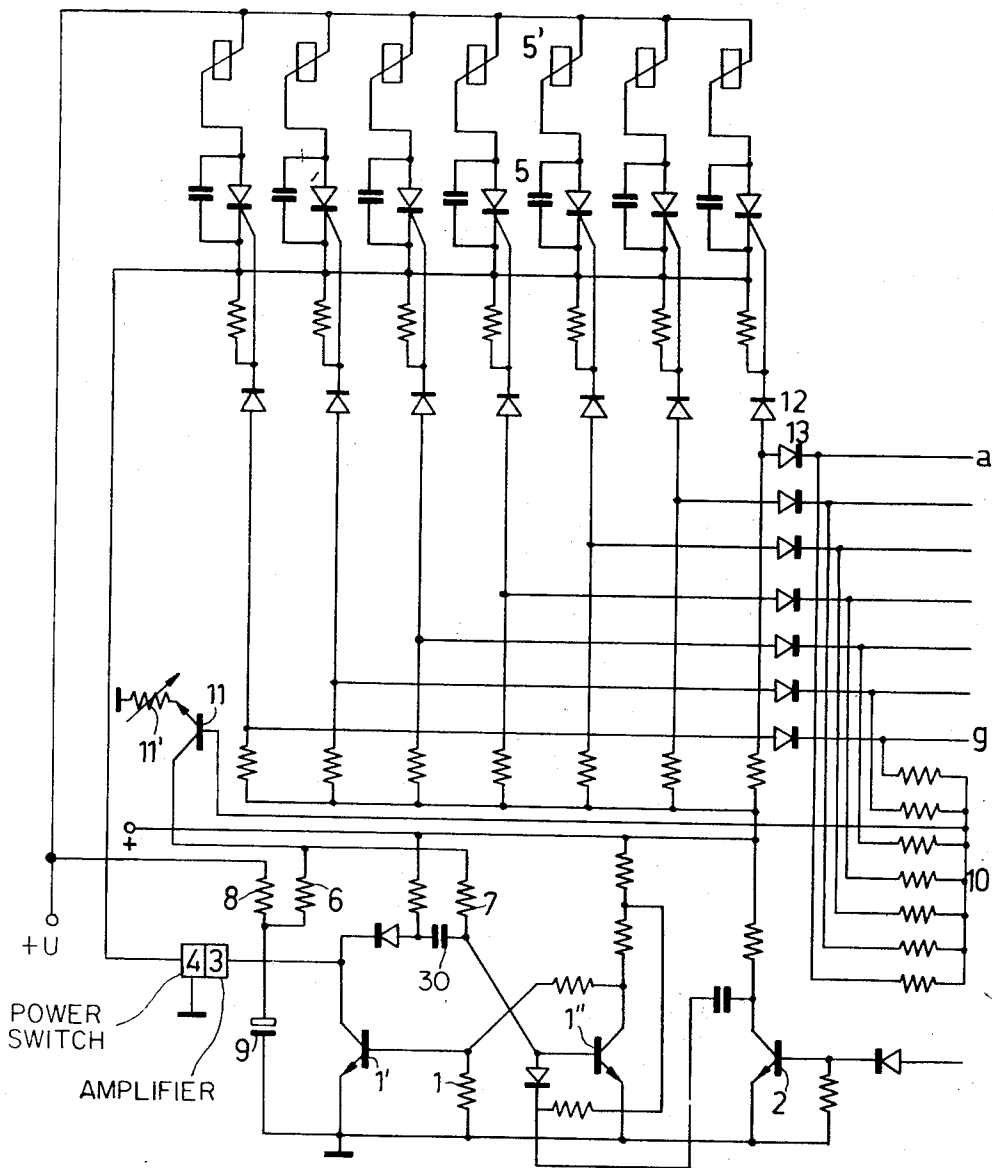
[57]

ABSTRACT

A triggering circuit for a plurality of printing solenoids that insures the uniform density of the printed matter by producing actuating pulses of a duration varying as an inverse function of the supply voltage. The natural energy integration of printing solenoids causes the solenoid to print with a uniform force in response to short-duration, high voltage energization, and long-duration, low voltage energization.

8 Claims, 1 Drawing Figure





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AGENT

CIRCUIT ARRANGEMENT FOR RHYTHMIC, INTERMITTENT OPERATION OF SEPARATE MAGNETS

This a continuation, of application Ser. No. 30,648, filed Apr. 22, 1970 now abandoned.

The invention relates to a circuit arrangement for the rhythmic, intermittent operation of separate magnets of a group, which can be selected by means of triggering semiconductor switches. Such circuit arrangements are employed, for example, for actuating mosaic printers supplying a printed image formed by points. The uniformity of the density of such an image depends primarily upon the energy supply during the time in which the needle impinges on the printing substrate.

The reaction of the printing solenoids to fluctuations in the operating voltage caused by changes from constant to intermittent operation and the fluctuations of the line voltage due to others causes would adversely affect the uniformity of the printed image. Electronic voltage stabilizers, in spite of their high capacity, would not solve this problem due to the transient load. On the other hand fluctuations of the actuating energy required depends upon the number of needles to be simultaneously actuated and are unavoidable.

The invention obviates these disadvantages and is characterized in that a monostable trigger switched into operation by clock pulses is provided for triggering the semiconductor switches and in that the timing capacitor of the trigger circuit is connected through an RC-member and a series resistor to the unstabilized operational voltage of the separate magnets.

The invention can not only be applied to mosaic printers, but also anywhere if the uniform load of solenoids is concerned, for example, punches and the like.

The sole FIGURE of the drawing shows one embodiment.

The monostable trigger circuit comprising the two transistors 1' and 1'' is triggered via the transistor stage 2 with a repetition frequency of about 1,000 Hz and supplies pulses of a duration t_p of about 400 μ sec. Via amplifying stages 3 a power switch 4 is actuated. Switch 4 connects one end of the thyristor to ground thereby energizing the main conduction path of thyristors 5 used as semiconductor switches. Selection conductors a to g enable or interrupt the current through the thyristors 5 in accordance with the desired sign to be printed by the solenoids so that the intermittently operating solenoid magnets 5' are selectively energized or de-energized.

This conventional monostable multivibrator circuit arrangement has the following features:

The load resistor 6, 7 of the monostable trigger circuit 1 is connected via only a preliminary filter consisting of a resistor 8 and a capacitor 9 to the uncontrolled operational voltage, which is also used for actuating the thrust magnets 5'. It is thus ensured that at a decreasing voltage the current through the resistors 6 and 7 also decreases so that the charging time of the trigger circuit capacitor 30 is prolonged. A suitable choice of the resistor combination results in that the current decrease due to the decrease of the supply voltage at the thrust magnets 5' is compensated for by a current pulse of longer duration so that the energy content, which is $(1/2)U \cdot i_{max} \cdot t_p$ owing to the current increase which is approximately linear in this example, remains constant where U is the average voltage across the sole-

noid. At an increasing voltage the inverse effect is obtained.

For producing perpendicular signs all seven thrust magnets 5' have to be actuated simultaneously. For producing horizontal lines, however, only one has to be actuated. The resultant peak current differences bring about different voltage drops when using seven needles in the ratio 7 : 1. By the use of semiconductors as power switches, printing paths, junction resistors, energizing connections and so on these voltage drops attain an order of magnitude which results in an appreciable decrease in printing energy. Even a high complicated, electronically controlled supply voltage apparatus could not eliminate non-uniform printing in this case. Also in this case the pulse duration may be influenced additionally in accordance with the separately exited thrust magnets. The triggering supply conductors a to g of the thyristors 5 are monitored by an adder resistance network 10 and by the resultant sum voltage a load transistor 11 is controlled. Each gate circuit of the thyristors and each of the selection conductors a to g include a diode 12 and 13 respectively, the junction of which receives a fixed bias voltage which may serve in addition as a supply voltage for the transistor stages.

As more thrust magnets 5' are excited, the conductivity of the load transistor 11 increase. The collector of load transistor 11 is connected to the junction of the divided load resistors 6 and 7. An additional voltage drop across the resistor 7 has, however, the effect of a reduction of the supply voltage, as stated above, and results in an increase in pulse duration t_p . In this circuit arrangement by an appropriate choice of the amplification of the load transistor 11, which is adjustable by means of the emitter resistor 11', a completely uniform blackening of perpendicular and horizontal lines is obtained, which are produced as a grating print by the mosaic printer.

What is claimed is:

1. A circuit arrangement for rhythmic, intermittent operation of separate magnets of a group, which can be selected by means of triggered semiconductor switches, characterized in that a monostable trigger circuit controlled by the time signals is provided for triggering the semiconductor switches and in that the capacitor of the trigger circuit is connected via an RC-member and a series resistor to the uncontrolled operational voltage of the separate magnets.

2. A circuit arrangement as claimed in claim 1, characterized in that the series resistor is divided into two resistors and the junction has connected to it the collector-emitter path of a load transistor, which can be controlled in accordance with the sum of the currents required for triggering the semiconductor switches.

3. A circuit arrangement as claimed in claim 2, characterized in that the thyristors are used as semiconductor switches and the gates thereof are each connected to a diode summation circuit, the resistors of which are connected to the base of the adjustable load transistor.

4. A circuit arrangement as claimed in claim 3, characterized in that for each gate of the thyristors a fixed bias voltage is provided and the selection conductor is connected via a diode to the bias voltage supply conductor and a diode connected in opposite sense relative to the diode of the selection conductor is provided in front of the gate.

5. A circuit arrangement for providing selected solenoids of a group of solenoids with electrical pulses hav-

ing a uniform energy content from an unstabilized source of voltage, comprising a plurality of semiconductor switches, each of said semiconductor switches having a control input for receiving solenoid selection signals and having a main conduction path selectively switchable from a normally high impedance to a lower impedance in response to a corresponding solenoid selection signal on the control input thereof, means connecting the main conduction path of each semiconductor switch in series with a separate solenoid, a monostable multivibrator means triggered by clock pulses and comprising a timing network including a capacitor connected to the unstabilized source of voltage for providing an output pulse having a duration varying as an inverse function of the magnitude of the unstabilized source of voltage, filter means comprising an R-C network connecting the timing network of the monostable multivibrator means to the unstabilized voltage source for providing a signal voltage to the timing network of the multivibrator that increases the pulse width of the multivibrator means as an inverse function of the unstabilized voltage, and sensing means connected to the control inputs of the semiconductor switches for providing a sensing signal to the timing network of the monostable multivibrator that increases the pulse width of the multivibrator as a direct function of the number of solenoid selection signals applied to the semiconductor switches, and energizing switch means connected to the multivibrator means for connecting all the series connected solenoids and semiconductor switches in parallel with the unstabilized source of voltage in re-

sponse to the output pulse of the multivibrator.

6. A circuit arrangement as claimed in claim 5 wherein the timing network in the monostable multivibrator comprises two series connected resistors, the sensing means further comprising a transistor having a collector-emitter path connecting the junction of the two series connected resistors to a reference potential, the sensing means further comprising a summing circuit for adding the total number of solenoid selection signals on the control input of the semiconductor switches, and means for connecting the summing circuit to the transistor for controlling the conductivity of the transistor, whereby the duration of the multivibrator output pulse is controllable by the number of solenoid selection signals applied to the semiconductor switches.

7. A circuit arrangement as claimed in claim 6, wherein the semiconductor switches comprise thyristors, wherein the control inputs of the semiconductor switches comprise the gates of the thyristors, wherein the summing circuit comprises a diode summation network comprising diodes and resistors, and wherein the resistors of the diode summation network and connected to the base of the transistor.

8. A circuit arrangement as claimed in claim 7, wherein the gate of each thyristor is provided with a fixed bias voltage through a circuit diode polarized oppositely to an associated diode in the diode summation network.

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CERTIFICATE OF CORRECTION

Patent No. 3,789,272 Dated January 29, 1974

Inventor(s) DIETRICH VOLLHARDT

It is certified that error appears in the above-identified patent
and that said Letters Patent are hereby corrected as shown below:

ON THE TITLE PAGE

"[30] Foreign Application Priority Data

May 6, 1969 Germany.....1923037
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should read:

--[30] Foreign Application Priority Data

May 6, 1969 Germany P.1923037.6
May 3, 1969 Germany.....P.1922752.2--.

Signed and sealed this 10th day of September 1974.

(SEAL)
Attest:

McCOY M. GIBSON, JR.
Attesting Officer

C. MARSHALL DANN
Commissioner of Patents

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