US011481669B2

(12) **United States Patent**
Rolfe et al.

(10) **Patent No.: US 11,481,669 B2**
(45) **Date of Patent: Oct. 25, 2022**

(54) **SYSTEMS, METHODS AND APPARATUS FOR SAMPLING FROM A SAMPLING SERVER**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 753 days.

(21) Appl. No.: **16/336,625**

(22) PCT Filed: **Sep. 26, 2017**

(86) PCT No.: **PCT/US2017/053303**
§ 371 (c)(1),
(2) Date: **Mar. 26, 2019**

(87) PCT Pub. No.: **WO2018/058061**
PCT Pub. Date: **Mar. 29, 2018**

(65) **Prior Publication Data**

US 2021/0289020 A1 Sep. 16, 2021

Related U.S. Application Data

(60) Provisional application No. 62/399,683, filed on Sep. 26, 2016.

(51) **Int. Cl.**
G06N 20/00 (2019.01)
G06N 10/00 (2022.01)
(Continued)

(52) **U.S. Cl.**
CPC ***G06N 20/00*** (2019.01); ***G06F 9/30*** (2013.01); ***G06F 15/173*** (2013.01); ***G06N 7/005*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC H04L 67/10; G06F 15/173; G06F 9/30; G06N 7/08; G06N 7/005; G06N 3/0445; G06N 3/0472; G06N 20/00; G06N 10/00
See application file for complete search history.

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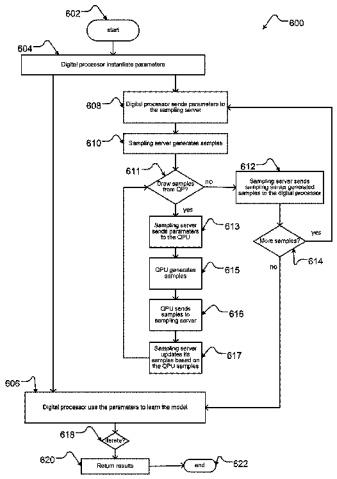
(57) **ABSTRACT**

A digital processor runs a machine learning algorithm in parallel with a sampling server. The sampling sever may continuously or intermittently draw samples for the machine learning algorithm during execution of the machine learning algorithm, for example on a given problem. The sampling server may run in parallel (e.g., concurrently, overlapping, simultaneously) with a quantum processor to draw samples from the quantum processor.

18 Claims, 7 Drawing Sheets



(51) **Int. Cl.**

G06F 15/173	(2006.01)
G06N 7/08	(2006.01)
H04L 67/10	(2022.01)
G06N 7/00	(2006.01)
G06F 9/30	(2018.01)

(52) **U.S. Cl.**

CPC ***G06N 7/08*** (2013.01); ***G06N 10/00*** (2019.01); ***H04L 67/10*** (2013.01)

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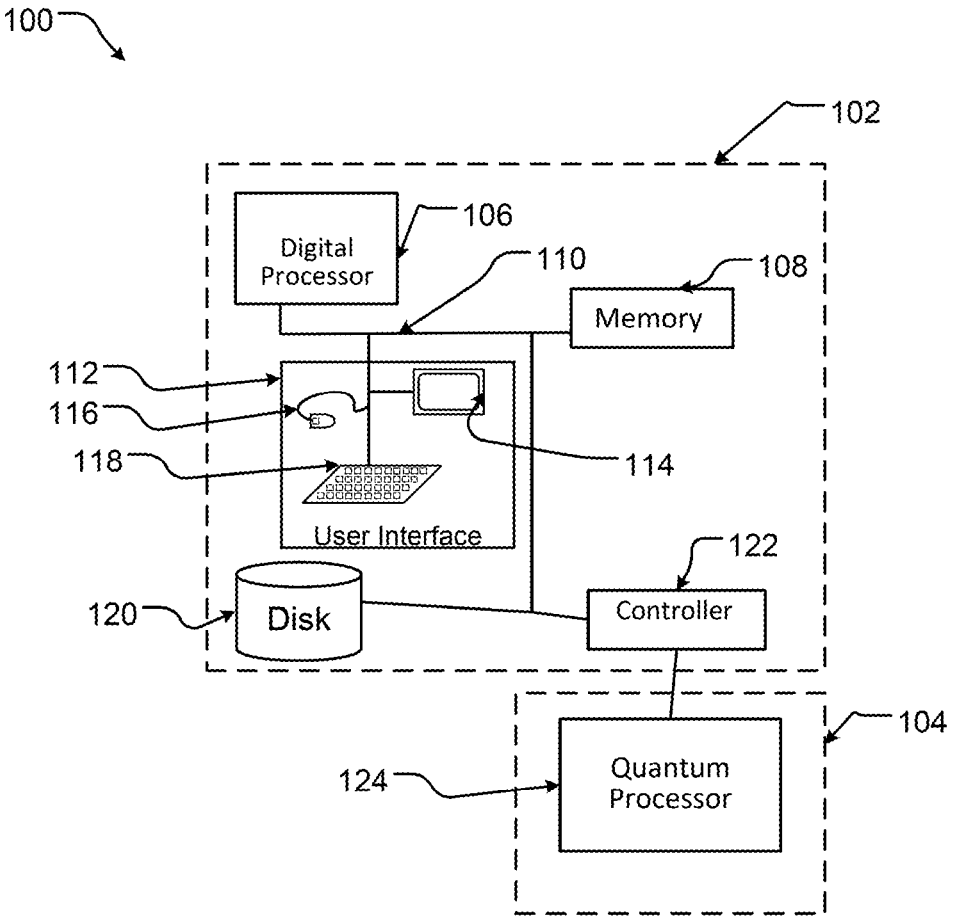
100
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Digital Processor
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108
Memory
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116
118
114
User Interface
122
120
Disk
Controller
104
124
Quantum Processor

Fig. 1

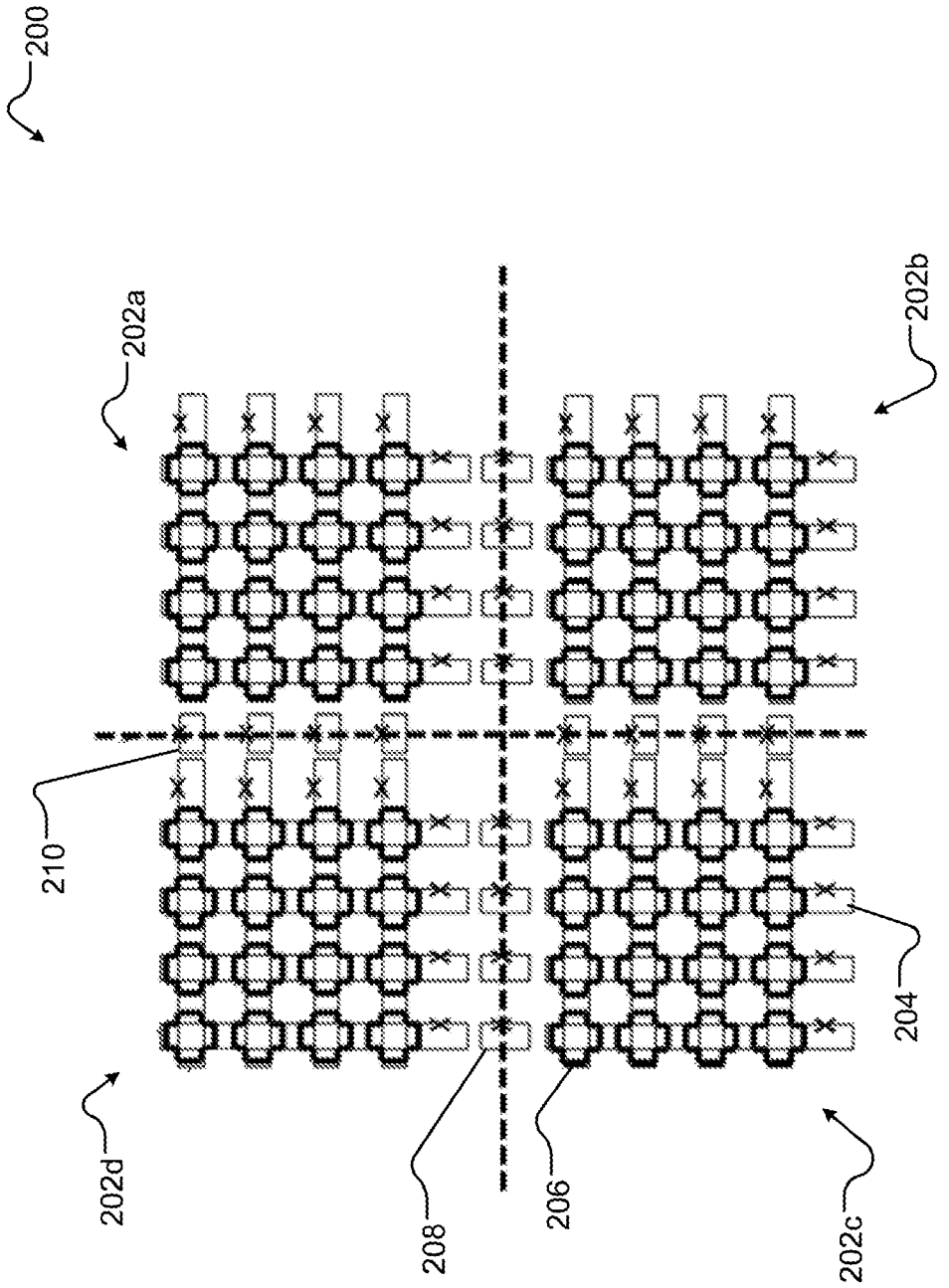

Fig. 2

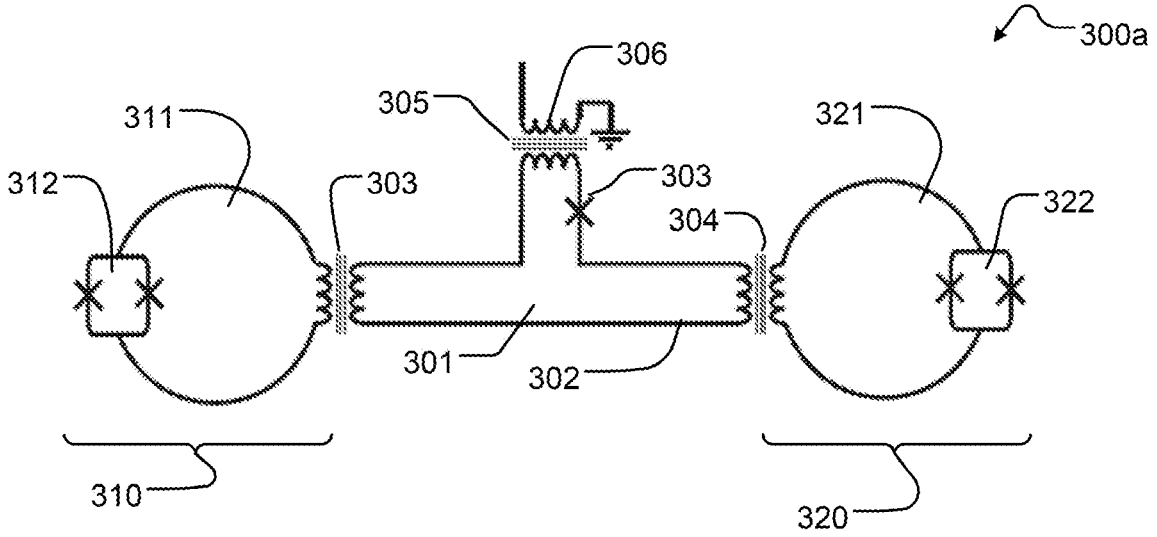
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Fig. 3A

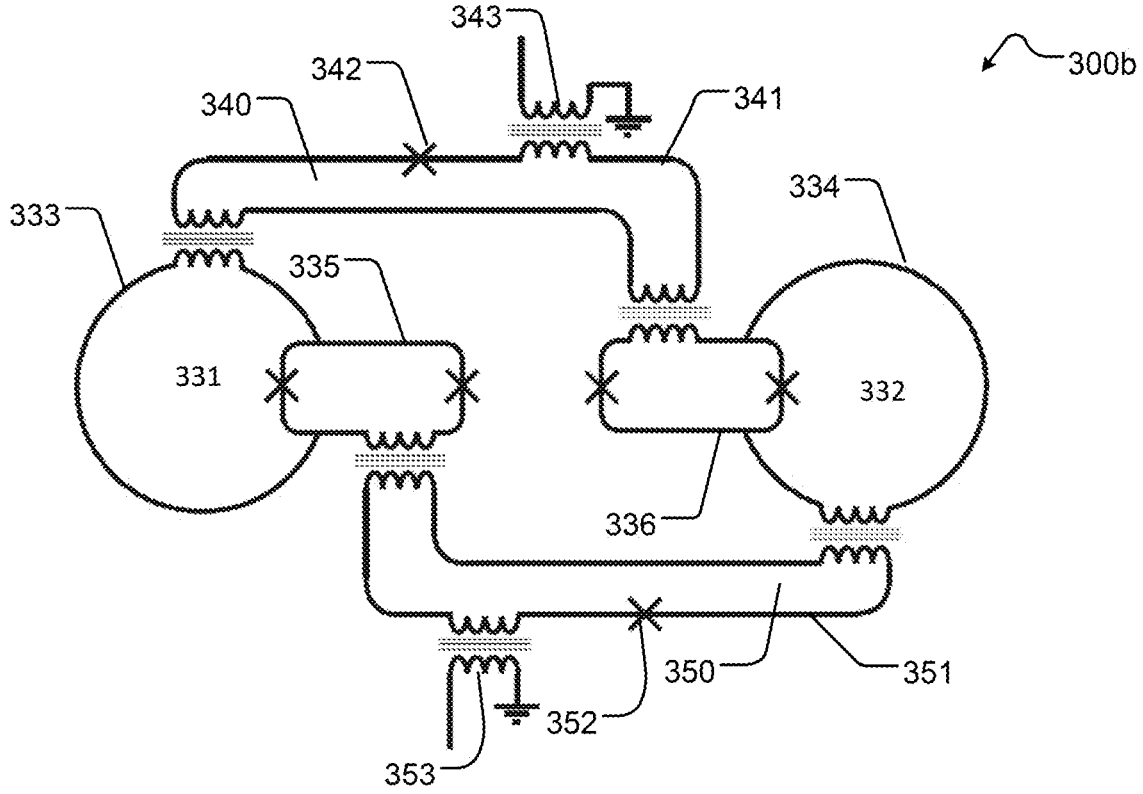
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Fig. 3B

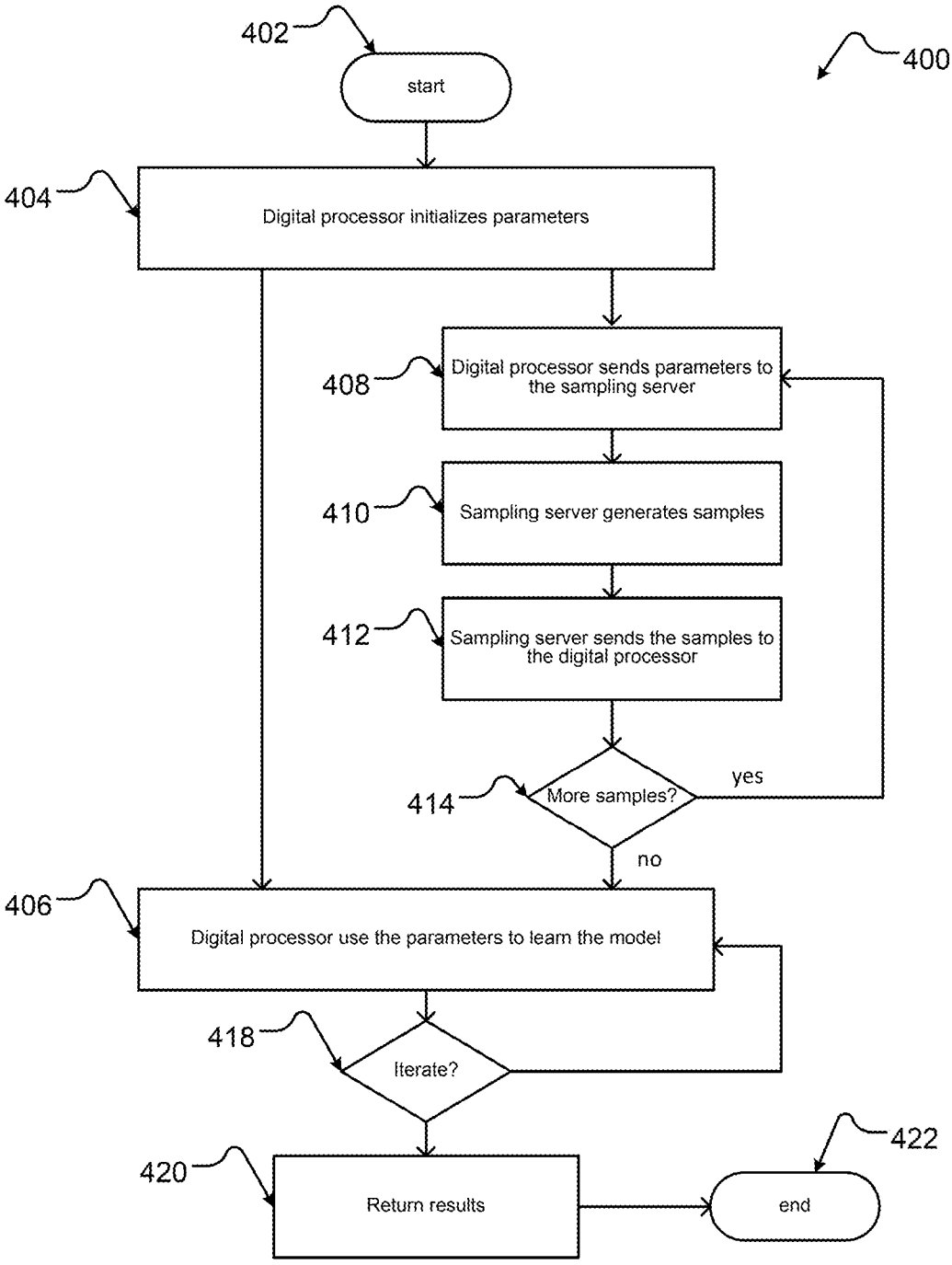
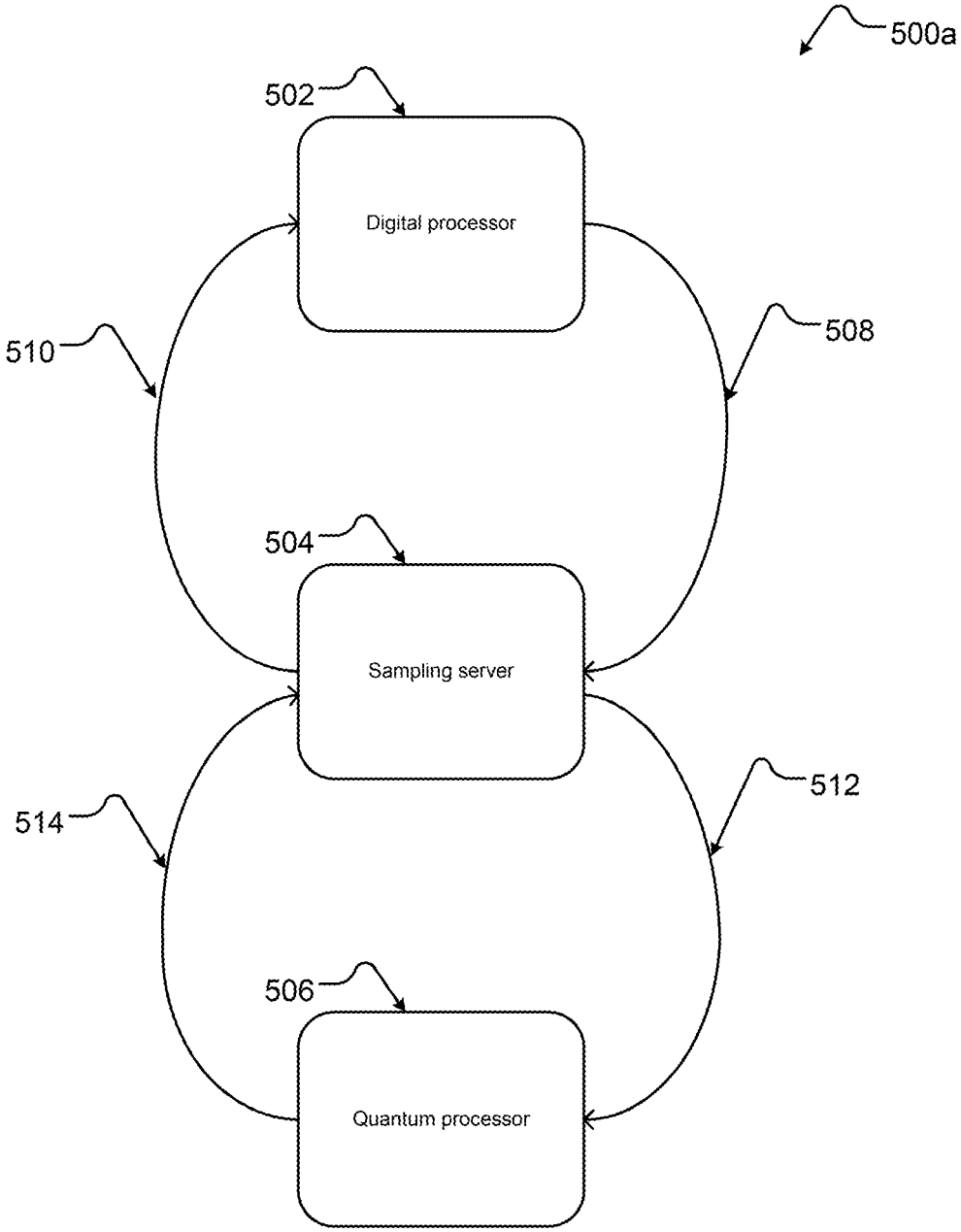

402
start
400
404
Digital processor initializes parameters
408
Digital processor sends parameters to the sampling server
410
Sampling server generates samples
412
Sampling server sends the samples to the digital processor
414
More samples?
yes
no
406
Digital processor use the parameters to learn the model
418
Iterate?
420
Return results
422
end

Fig. 4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Digital processor
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Sampling server
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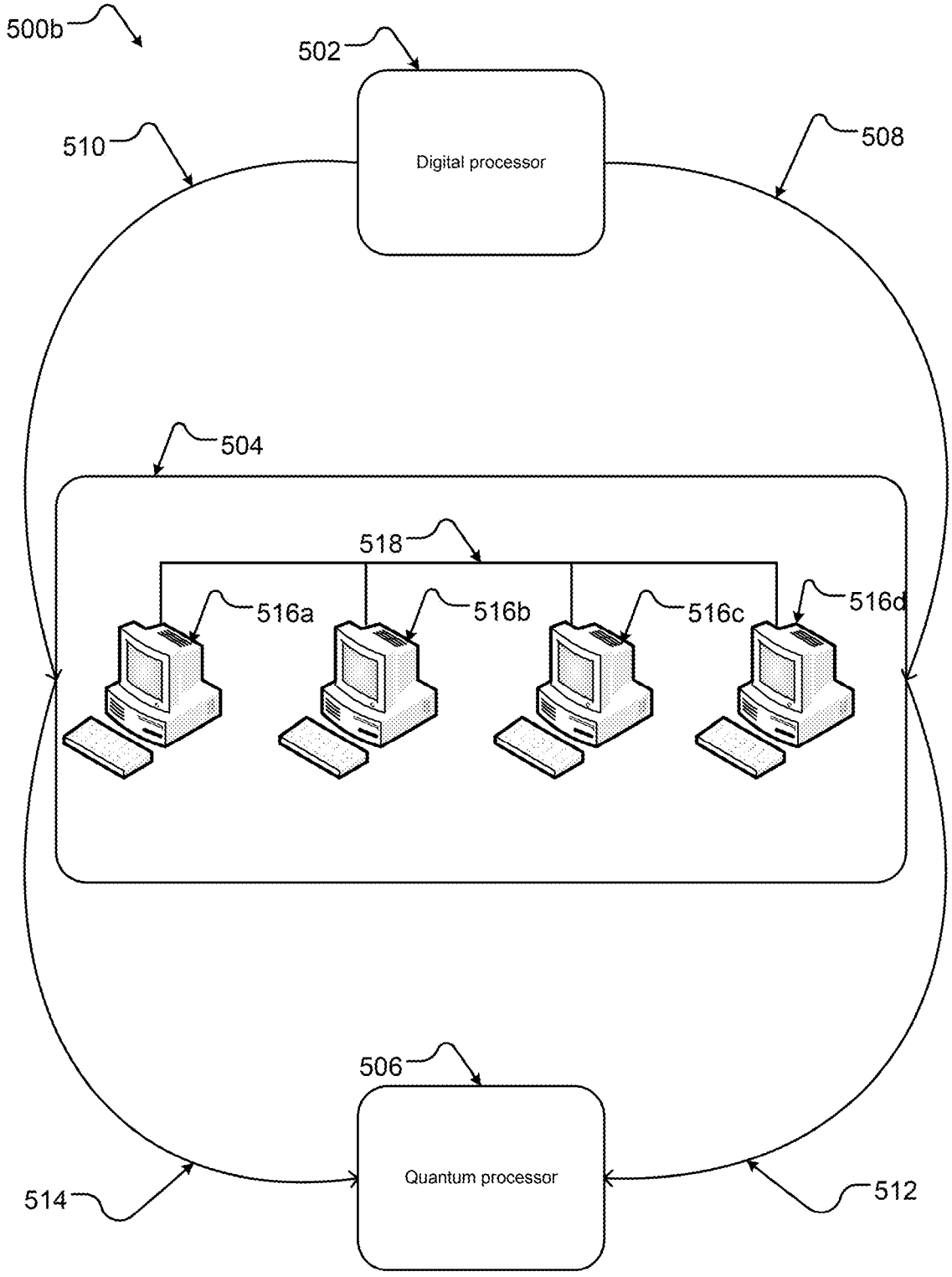
506
Quantum processor

Fig. 5A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Digital processor
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516a
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516c
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Quantum processor
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Fig. 5B

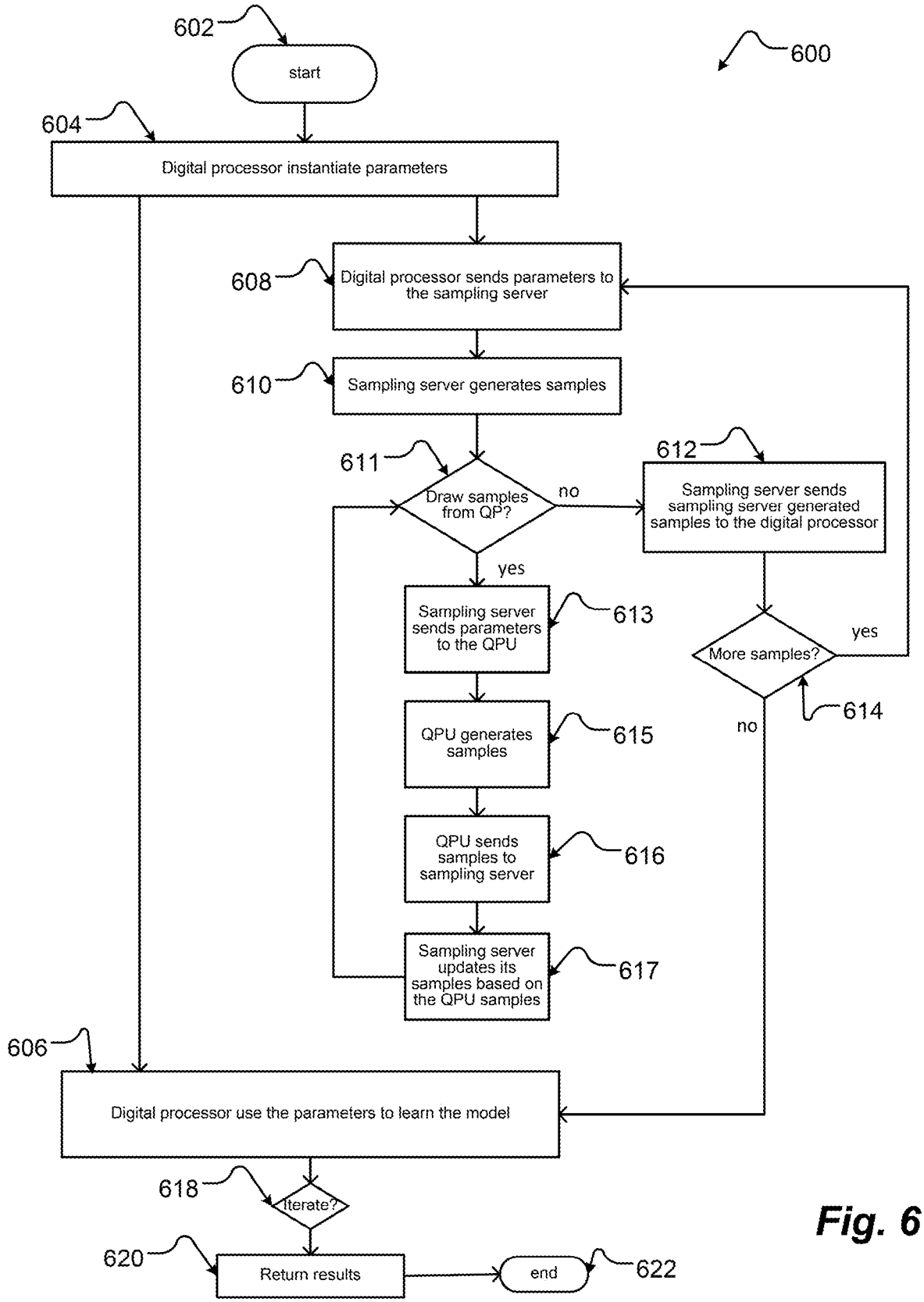
602
start
600
604
Digital processor instantiate parameters
608
Digital processor sends parameters to the sampling server
610
Sampling server generates samples
611
Draw samples from QP?
no
612
Sampling server sends sampling server generated samples to the digital processor
yes
Sampling server sends parameters to the QPU
613
More samples?
yes
614
no
QPU generates samples
615
QPU sends samples to sampling server
616
Sampling server updates its samples based on the QPU samples
617
606
Digital processor use the parameters to learn the model
618
Iterate?
620
Return results
end
622

Fig. 6

SYSTEMS, METHODS AND APPARATUS FOR SAMPLING FROM A SAMPLING SERVER

FIELD

This disclosure generally relates to machine learning systems employing a sampling server.

BACKGROUND

Machine Learning

Machine learning relates to methods and circuitry that can learn from data and make predictions based on data. In contrast to methods or circuitry that follow static program instructions, machine learning methods and circuitry can include deriving a model from example inputs (such as a training set) and then making data-driven predictions.

Machine learning is related to optimization. Some problems can be expressed in terms of minimizing a loss function on a training set, where the loss function describes the disparity between the predictions of the model being trained and observable data.

Machine learning tasks can include unsupervised learning, supervised learning, and reinforcement learning. Approaches to machine learning include, but are not limited to, decision trees, linear and quadratic classifiers, case-based reasoning, Bayesian statistics, and artificial neural networks.

Machine learning can be used in situations where explicit approaches are considered infeasible. Example application areas include optical character recognition, search engine optimization, and computer vision.

Quantum Processor

A quantum processor is a computing device that can harness quantum physical phenomena (such as superposition, entanglement, and quantum tunneling) unavailable to non-quantum devices. A quantum processor may take the form of a superconducting quantum processor. A superconducting quantum processor may include a number of qubits and associated local bias devices, for instance two or more superconducting qubits. An example of a qubit is a flux qubit. A superconducting quantum processor may also employ coupling devices (i.e., "couplers") providing communicative coupling between qubits. Further details and embodiments of exemplary quantum processors that may be used in conjunction with the present systems and devices are described in, for example, U.S. Pat. Nos. 7,533,068; 8,008,942; 8,195,596; 8,190,548; and 8,421,053.

Adiabatic Quantum Computation

Adiabatic quantum computation typically involves evolving a system from a known initial Hamiltonian (the Hamiltonian being an operator whose eigenvalues are the allowed energies of the system) to a final Hamiltonian by gradually changing the Hamiltonian. A simple example of an adiabatic evolution is a linear interpolation between initial Hamiltonian and final Hamiltonian. An example is given by:

$$H_e=(1-s)H_i+sH_f$$

where H_i is the initial Hamiltonian, H_f is the final Hamiltonian, H_e is the evolution or instantaneous Hamiltonian, and s is an evolution coefficient which controls the rate of evolution (i.e., the rate at which the Hamiltonian changes).

As the system evolves, the evolution coefficient s goes from 0 to 1 such that at the beginning (i.e., s=0) the evolution Hamiltonian H_e is equal to the initial Hamiltonian H_i and at the end (i.e., s=1) the evolution Hamiltonian H_e is equal to the final Hamiltonian H_f. Before the evolution begins, the system is typically initialized in a ground state of the initial Hamiltonian H_i and the goal is to evolve the system in such a way that the system ends up in a ground state of the final Hamiltonian H_f at the end of the evolution. If the evolution is too fast, then the system can transition to a higher energy state, such as the first excited state. As used herein an "adiabatic" evolution is an evolution that satisfies the adiabatic condition:

$$\dot{s}\left|\left\langle 1\left|dH_e/ds\right|0\right\rangle\right|=\delta g^2(s)$$

where $\dot{s}$ is the time derivative of s, g(s) is the difference in energy between the ground state and first excited state of the system (also referred to herein as the "gap size") as a function of s, and δ is a coefficient much less than 1.

If the evolution is slow enough that the system is always in the instantaneous ground state of the evolution Hamiltonian, then transitions at anti-crossings (when the gap size is smallest) are avoided. Other evolution schedules, besides the linear evolution described above, are possible including non-linear evolution, parametric evolution, and the like. Further details on adiabatic quantum computing systems, methods, and apparatus are described in, for example, U.S. Pat. Nos. 7,135,701; and 7,418,283.

Quantum Annealing

Quantum annealing is a computation method that may be used to find a low-energy state, typically preferably the ground state, of a system. Similar in concept to classical simulated annealing, the method relies on the underlying principle that natural systems tend towards lower energy states because lower energy states are more stable. While classical annealing uses classical thermal fluctuations to guide a system to a low-energy state and ideally its global energy minimum, quantum annealing may use quantum effects, such as quantum tunneling, as a source of disordering to reach a global energy minimum more accurately and/or more quickly than classical annealing. In quantum annealing thermal effects and other noise may be present to annealing. The final low-energy state may not be the global energy minimum. Adiabatic quantum computation may be considered a special case of quantum annealing for which the system, ideally, begins and remains in its ground state throughout an adiabatic evolution. Thus, those of skill in the art will appreciate that quantum annealing systems and methods may generally be implemented on an adiabatic quantum computer. Throughout this specification and the appended claims, any reference to quantum annealing is intended to encompass adiabatic quantum computation unless the context requires otherwise.

Quantum annealing uses quantum mechanics as a source of disorder during the annealing process. An objective function, such as an optimization problem, is encoded in a Hamiltonian H_P, and the algorithm introduces quantum effects by adding a disordering Hamiltonian H_D that does not commute with H_P. An example case is:

$$H_E\propto A(t)H_D+B(t)H_P,$$

where A(t) and B(t) are time dependent envelope functions. For example, A(t) can change from a large value to substantially zero during the evolution and H_E can be thought of as an evolution Hamiltonian similar to H_e described in the context of adiabatic quantum computation above. The disorder is slowly removed by removing H_D (i.e., by reducing A(t)).

Thus, quantum annealing is similar to adiabatic quantum computation in that the system starts with an initial Hamiltonian and evolves through an evolution Hamiltonian to a final "problem" Hamiltonian H_P whose ground state encodes

a solution to the problem. If the evolution is slow enough, the system may settle in the global minimum (i.e., the exact solution), or in a local minimum close in energy to the exact solution. The performance of the computation may be assessed via the residual energy (difference from exact solution using the objective function) versus evolution time. The computation time is the time required to generate a residual energy below some acceptable threshold value. In quantum annealing, H_P may encode an optimization problem and therefore H_P may be diagonal in the subspace of the qubits that encode the solution, but the system does not necessarily stay in the ground state at all times. The energy landscape of H_P may be crafted so that its global minimum is the answer to the problem to be solved, and low-lying local minima are good approximations.

The gradual reduction of disordering Hamiltonian H_D (i.e., reducing A(t)) in quantum annealing may follow a defined schedule known as an annealing schedule. Unlike adiabatic quantum computation where the system begins and remains in its ground state throughout the evolution, in quantum annealing the system may not remain in its ground state throughout the entire annealing schedule. As such, quantum annealing may be implemented as a heuristic technique, where low-energy states with energy near that of the ground state may provide approximate solutions to the problem.

The foregoing examples of the related art and limitations related thereto are intended to be illustrative and not exclusive. Other limitations of the related art will become apparent to those of skill in the art upon a reading of the specification and a study of the drawings.

BRIEF SUMMARY

There exists a need to be able to process at least some problems having size and/or connectivity greater than (and/or at least not fully provided by) the working graph of an analog processor. Computational systems and methods are described which, at least in some implementations, allow for the computation of at least some problem graphs which have representations which do not fit within the working graph of an analog processor (e.g. because the problem graphs require more computation devices and/or more/other couplers than the processor provides).

A computational system for use in machine learning may be summarized as including at least one digital processor core; and at least one nontransitory processor-readable medium communicatively coupleable to the at least one digital processor core and that stores at least one of processor-executable instructions or data which, when executed by the at least one digital processor core, causes the at least one digital processor core to implement a sampling server that: receives an initial set of parameters for an iteration of a machine learning process that is executing in parallel with the sampling server on a separate at least one digital processor core from the at least one digital processor core on which the sampling server is implemented; generates a first set of samples based on the initial set of parameters temporarily in parallel with execution of the machine learning process; and provide the first set of samples generated by sampling server as implemented by the at least one digital processor core for use in a further iteration of the machine learning process. The sampling server executes concurrently or even simultaneously, with the machine learning process, overlapping at least a portion thereof.

The at least one digital processor core that implements the sampling server can provide a first set of functions along with the first set of samples generated by sampling server to one or more other processor cores that are executing the machine learning algorithm, for instance on an given problem. The first set of functions can include first- and second-order statistics.

The at least one digital processor core that implements the sampling server can draw samples from a Boltzmann distribution, for instance from a Chimera structured Boltzmann distribution. The at least one digital processor core that implements the sampling server can draw samples via at least one of Markov Chain of single temperature Gibbs sampling, simulated tempering, parallel tempering, population annealing, and annealed importance sampling.

The at least one digital processor core that implements the sampling server can provide a current set of parameters from the sampling server; and receive a set of quantum processor generated samples from the at least one quantum processor. The at least one digital processor core that implements the sampling server can perform post processing on the samples received from the quantum processor.

The sampling server may, for example, send samples, functions of samples and an approximation to a log partition function to the at least one separate digital processor core on which the machine learning process executes.

The sampling server may, for example, iteratively receive additional sets of parameters for each of a number of iterations of the machine learning process that is executing in parallel with the sampling server on the separate at least one digital processor core from the at least one digital processor core on which the sampling server is implemented; iteratively generate an additional sets of samples based on respective ones of the additional sets of parameters temporarily in parallel with execution of the machine learning process; and iteratively provide the additional sets of samples generated by sampling server as implemented by the at least one digital processor core for use in the iterations of the machine learning process.

The computational system for use in machine learning may be summarized as further including at least one digital processor core that executes the machine learning process, for example on the given problem. The machine learning process may, for example, maximize a log-likelihood of a generative model.

The at least one digital processor core on which the sampling server is implemented can be a first processor core of a graphical processor unit with a memory space, and the separate at least one digital processor core that executes the machine learning process can be a second processor core of the graphical processor unit and shares the memory space with the first processor core of the graphical processor unit. The at least one digital processor core on which the sampling server is implemented can be a processor core of a first graphical processor unit and the separate at least one digital processor core that executes the machine learning process can be a processor core of a second graphical processor unit, the second graphical processor unit separate and distinct from the first graphical processor unit. The first graphical processing unit can be part of a first computer and the second graphical processing unit can be part of a second computer, the second computer separate and distinct from the first computer. The at least one digital processor core on which the sampling server is implemented can include a plurality of digital processor cores of a plurality of processors that are separate and distinct from one another, and the plurality of processors can be components of a plurality of computers, the computers which can from a cluster of machines communicatively coupled via a network infrastructure.

The computational system for use in machine learning may be summarized as further including one or more quantum processors that draw samples from a distribution based at least in part on the current set of parameters provided by the sampling server. The quantum processor(s) may perform chain embedding before drawing samples.

A computational system for use in machine learning may include a first digital processor core or set of cores (i.e., hardware processor circuitry executing software or firmware instructions stored on nontransitory computer- or processor-readable media) and a sampling server (i.e., hardware processor circuitry executing software or firmware instructions stored on nontransitory computer- or processor-readable media) implemented on a second digital processor core or set of cores. The digital processor core(s) that executes the machine learning algorithm maximizes the log-likelihood of a generative model. The sampling server is communicatively coupled to the first digital processor core(s) that execute the machine learning algorithm and receives an initial set of parameters from the first digital processor core(s), draws samples from a distribution based on the initial set of parameters and sends the samples and functions of the samples to the first digital processor core(s). The functions of the samples may be first- and second-order statistics. The sampling server may draw samples from a Boltzmann distribution. The Boltzmann distribution may be Chimera structured. The sampling server may draw samples via any one or more of Markov Chain of single temperature Gibbs sampling, simulated tempering, parallel tempering, population annealing, annealed importance sampling. The computational system may further comprise a quantum processor in communicative coupling with the sampling server. The quantum processor periodically receives a current set of parameters from the sampling server, draws samples from a distribution and sends the samples to the sampling server, and the sampling server performs post processing on the samples received from the quantum processor before sending the samples to the first digital processor core or set of cores. The quantum processor may perform chain embedding before drawing samples. The sampling server may share memory space with the digital processor on a GPU. The sampling server may be on a different GPU. The sampling server may be on a different machine. The sampling server may be on a cluster of machines over a network.

A method for machine learning employing a first digital processor core or set of cores and a sampling server implemented on a second digital processor core or set of cores includes the first digital processor core or set of cores (i.e., hardware processor circuitry executing software or firmware instructions stored on nontransitory computer- or processor-readable media) initializing an initial set of parameters, the first digital processor core(s) sending the initial set of parameters to the sampling server, the first digital processor core(s) maximizing the log-likelihood of a generative model in parallel with the sampling server drawing samples from a distribution based on the initial set of parameters and calculating functions of the samples, the sampling server sending the samples to the first digital processor core(s), and the first digital processor core(s) using the samples to learn the distribution by maximizing the log-likelihood of the generative model. The functions of the samples may be first- and second-order statistics. The distribution may be a Boltzmann distribution. The sampling server may draw samples via any one or more of Markov Chain of single temperature Gibbs sampling, simulated tempering, parallel tempering, population annealing, annealed importance sampling. The method of claim may further comprise a quantum processor in communicative coupling with the sampling server. The digital processor sends a set of initial parameters corresponding to the distribution to be learned to the sampling server, the sampling server uses the initial parameters to draws a first set of samples from the distribution, thereby producing updated parameters, the sampling server sending the first set of samples and functions of the samples to the first digital processor core(s), periodically or intermittently the sampling server sends the updated parameters to the quantum processor, the quantum processor uses quantum hardware to draw a second set of samples corresponding to the updated parameters, the quantum processor returns the second set of samples to the sampling server, the sampling server uses the second set of samples to update the first set of samples to produce a third set of samples corresponding to the updated parameters and the second set of samples, the sampling server returns the third set of samples to the first digital processor core or set of cores, and the first digital processor core(s) uses the third set of samples to maximize the log-likelihood of a generative model. The functions of the samples may be first- and second-order statistics. The method may further comprise the quantum processor performing chain embedding before drawing samples.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S)

In the drawings, identical reference numbers identify similar elements or acts. The sizes and relative positions of elements in the drawings are not necessarily drawn to scale. For example, the shapes of various elements and angles are not necessarily drawn to scale, and some of these elements may be arbitrarily enlarged and positioned to improve drawing legibility. Further, the particular shapes of the elements as drawn, are not necessarily intended to convey any information regarding the actual shape of the particular elements, and may have been solely selected for ease of recognition in the drawings.

FIG. **1** is a schematic diagram that illustrates an exemplary hybrid computer including a digital processor and an analog processor in accordance with the present systems, devices, methods, and articles.

FIG. **2** is a schematic diagram that illustrates a portion of an exemplary topology, suitable for implementing the analog computer of FIG. **1**, for example via quantum annealing in accordance with the present systems, devices, articles, and methods.

FIG. **3**A shows a schematic diagram of a controllable ZZ-coupler, suitable for implementing the topology of FIG. **2**.

FIG. **3**B is a schematic diagram of an embodiment of a system that includes two superconducting qubits and both a ZX-coupler and an XZ-coupler, each of which is operable to communicably couple information between the two qubits, suitable for implementing the topology of FIG. **2**.

FIG. **4** is a flow diagram that shows a method for performing machine learning by sampling from a sampling server in accordance with the present systems, devices, articles, and methods.

FIG. **5**A is a schematic diagram that illustrates an exemplary hybrid system including a digital processor, a sampling server and a quantum processor and communications therebetween in accordance with the present systems, methods and apparatus.

FIG. **5**B is a schematic diagram that illustrates an exemplary hybrid system including a digital processor, a sampling

server implemented as a cluster of processors and a quantum processor and communications therebetween in accordance with the present systems, methods and apparatus.

FIG. **6** is a flow diagram that shows a method for performing machine learning by sampling from a sampling server and a quantum processor.

DETAILED DESCRIPTION

In the following description, certain specific details are set forth in order to provide a thorough understanding of various disclosed implementations. However, one skilled in the relevant art will recognize that implementations may be practiced without one or more of these specific details, or with other methods, components, materials, etc. In other instances, well-known structures associated with computer systems, server computers, and/or communications networks and associated hardware components or circuitry have not been shown or described in detail to avoid unnecessarily obscuring descriptions of the implementations.

Unless the context requires otherwise, throughout the specification and claims that follow, the word "comprising" is synonymous with "including," and is inclusive or open-ended (i.e., does not exclude additional, unrecited elements or method acts).

Reference throughout this specification to "one implementation" or "an implementation" means that a particular feature, structure or characteristic described in connection with the implementation is included in at least one implementation. Thus, the appearances of the phrases "in one implementation" or "in an implementation" in various places throughout this specification are not necessarily all referring to the same implementation. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more implementations.

As used in this specification and the appended claims, the singular forms "a," "an," and "the" include plural referents unless the context clearly dictates otherwise. It should also be noted that the term "or" is generally employed in its sense including "and/or" unless the context clearly dictates otherwise.

The headings and Abstract of the Disclosure provided herein are for convenience only and do not interpret the scope or meaning of the implementations.

FIG. **1** illustrates a hybrid computing system **100** including a digital computer **102** coupled to an analog computer **104**. In some implementations the analog computer **104** is a quantum computer. The exemplary digital computer **102** includes a digital processor **106** that may be used to perform classical digital processing tasks.

Digital computer **102** may include at least one digital processor **106** with one or more cores, at least one system memory **108**, and at least one system bus **110** that couples various system components, including system memory **108** to digital processor **106**.

The digital processor **106** may be any circuitry that forms a logic processing unit, such as one or more central processing units ("CPUs"), graphics processing units ("GPUs"), digital signal processors ("DSPs"), application-specific integrated circuits ("ASICs"), programmable gate arrays ("FPGAs"), programmable logic controllers (PLCs), etc.

Digital computer **102** may include a user input/output subsystem **112**. In some implementations, the user input/output subsystem includes one or more user input/output components such as a display **114**, mouse **116**, and/or keyboard **118**.

System bus **110** can employ any known bus structures or architectures, including a memory bus with a memory controller, a peripheral bus, and a local bus. System memory **108** may include non-volatile memory, such as read-only memory ("ROM"), static random access memory ("SRAM"), Flash NAND; and volatile memory such as random access memory ("RAM") (not shown).

Digital computer **102** may also include other non-transitory computer- or processor-readable storage media or non-volatile memory **120**. Non-volatile memory **120** may take a variety of forms, including: spinning media for instance a hard disk drive (HDD) for reading from and writing to a magnetic hard disk and/or an optical disk drive for reading from and writing to removable optical disks, and/or non-spinning media for instance a solid state drive (SSD) for reading from and writing to solid state memory. The optical disk can be a CD-ROM or DVD, while the magnetic disk can be a magnetic floppy disk or diskette or one or more magnetic disc platters. Non-volatile memory **120** may communicate with digital processor via system bus **110** and may include appropriate interfaces or controllers **122** coupled to system bus **110**. Non-volatile memory **120** may serve as long-term storage for processor- or computer-readable instructions, data structures, or other data (sometimes called program modules) for digital computer **102**.

Although digital computer **102** has been described as employing hard disks, optical disks and/or magnetic disks, those skilled in the relevant art will appreciate that other types of non-volatile computer-readable media may be employed, such magnetic cassettes, flash memory cards, Flash, ROMs, smart cards, etc. Those skilled in the relevant art will appreciate that some computer architectures employ volatile memory and non-volatile memory. For example, data in volatile memory can be cached to non-volatile memory or in a solid-state drive that employs integrated circuits to provide non-volatile memory.

Various processor- or computer-readable instructions, data structures, or other data can be stored in system memory **108**. For example, system memory **108** may store instruction for communicating with remote clients and scheduling use of resources including resources on the digital computer **102** and analog computer **104**.

In some implementations system memory **108** may store processor- or computer-readable calculation instructions to perform pre-processing, co-processing, and post-processing to analog computer **104**. System memory **108** may store at set of analog computer interface instructions to interact with the analog computer **104**.

Analog computer **104** may include an analog processor such as quantum processor **124**. The analog computer **104** can be provided in an isolated environment, for example, in an isolated environment that shields the internal elements of the quantum computer from heat, magnetic field, and other external noise (not shown) and/or which cools the analog processor to temperatures (i.e., critical temperature) at or below which the circuitry of the analog processor becomes superconductive. In contrast, the digital computer **102** will typically operate at much higher temperatures (e.g., room temperature) at which superconductivity does not occur and/or may employ materials that do not superconduct even at or below the critical temperature.

FIG. **2** shows an exemplary topology **200** for a quantum processor, in accordance with the presently described systems, devices, articles, and methods. Topology **200** may be

used to implement quantum processor **124** of FIG. **1**, however other topologies can also be used for the systems and methods of the present disclosure. Topology **200** comprises a grid of 2×2 cells such as cells **202***a*, **202***b*, **202***c* and **202***d* (collectively **202**), each cell comprised of 8 qubits such as qubit **204** (only one called out in FIG. **2**).

Within each cell **202**, there are eight qubits **204**, the qubits **204** in each cell **202** arranged four rows (extending horizontally in drawing sheet) and four columns (extending vertically in drawing sheet). Pairs of qubits **204** from the rows and columns can be communicatively coupled to one another by a respective coupler such as coupler **206** (illustrated by bold cross shapes, only one called out in FIG. **2**). A respective coupler **206** is positioned and operable to communicatively couple the qubit in each column (vertically-oriented qubit in drawing sheet) in each cell to the qubits in each row (horizontally-oriented qubit in drawing sheet) in the same cell. Additionally, a respective coupler, such as coupler **208** (only one called out in FIG. **2**), is positioned and operable to communicatively couple the qubit in each column (vertically-oriented qubit in drawing sheet) in each cell with a corresponding qubit in each column (vertically-oriented qubit in drawing sheet) in a nearest neighboring cell in a same direction as the orientation of the columns. Similarly, a respective coupler, such as coupler **210** (only one called out in FIG. **2**), is positioned and operable to communicatively couple the qubit in each row (horizontally-oriented qubit in drawing sheet) in each cell with a corresponding qubit in each row (horizontally-oriented qubit in drawing sheet) in each nearest neighboring cell in a same direction as the orientation of the rows. While couplers **206** are illustrated by bold cross shapes, such is not intended to be limiting, and couplers **206** can have any of a variety of other shapes.

FIG. **3**A shows a schematic diagram of an exemplary implementation of a system **300***a* comprising a controllable ZZ-coupler **301**. Controllable ZZ-coupler **301** includes a loop of superconducting material **302** interrupted by a Josephson junction **303** and is used to couple a first qubit **310** and a second qubit **320**. First qubit **310** is comprised of a loop of superconducting material (or "qubit loop") **311** interrupted by a compound Josephson junction ("CJJ") **312** and is coupled to controllable ZZ-coupler **301** through the exchange of flux **303** between controllable ZZ-coupler **301** and first qubit **310**. Second qubit **320** is comprised of a loop of superconducting material (or "qubit loop") **321** interrupted by a CJJ **322** and is coupled to controllable ZZ-coupler **301** through the exchange of flux **304** between controllable ZZ-coupler **301** and second qubit **320**. Loop of superconducting material **302** is threaded by flux **305** created by electrical current flowing through a magnetic flux inductor **306**. Controllable ZZ-coupler **301** may be used in in topology **200** to provide communicative coupling between qubits and thus be used in a quantum processor, in accordance with the presently described systems, devices, articles, and methods.

Variations and, for some applications, improvements to the ZZ-coupler design shown in FIG. **3**A are presented in U.S. Pat. Nos. 7,898,282, and 7,800,395.

FIG. **3**B is a schematic diagram of an exemplary implementation of a system **300***b* that includes two superconducting qubits **331**, **332** and both a ZX-coupler **340** and an XZ-coupler **350**, each of which is configured to communicably couple information between qubits **331** and **332**. Each of qubits **331** and **332** includes a qubit loop **333**, **334**, respectively, formed by a closed superconducting current path that is interrupted by a CJJ **335**, **336**, respectively.

ZX-coupler **340** includes a closed superconducting current path **341** that is inductively coupled to both the qubit loop **333** of qubit **331** and the CJJ **336** of qubit **332**. Thus, ZX-coupler **340** provides coupling between the Z-degree of freedom in qubit **331** and the X-degree of freedom in qubit **332** by inductively coupling the persistent current in the qubit loop **333** of qubit **331** into the CJJ **336** of qubit **332**.

In the case of ZX-coupler **340**, tunability is realized by two tuning elements: closed superconducting current path **341** is interrupted by at least one Josephson junction **342** and closed superconducting current path **341** is inductively coupled to a programming interface **343**.

Similarly, XZ-coupler **350** includes a closed superconducting current path **351** that is inductively coupled to both the qubit loop **334** of qubit **332** and the CJJ **335** of qubit **331**. Thus, XZ-coupler **350** provides coupling between the X-degree of freedom in qubit **331** and the Z-degree of freedom in qubit **332** by inductively coupling the persistent current in the qubit loop **334** of qubit **332** into the CJJ **335** of qubit **331**.

Both XZ-coupler **350** and ZX-coupler **340** may also be made tunable by the combination of two tuning elements: closed superconducting current path **351** is interrupted by at least one Josephson junction **352** and inductively coupled to a programming interface **353**, while closed superconducting current path **341** is interrupted by at least one Josephson Junction **342** and inductively coupled to a programming interface **343**.

System **300***b* may be used in topology **200** to provide communicative coupling between qubits and thus be used in a quantum processor, in accordance with the presently described systems, devices, articles, and methods.

The present disclosure describes systems, methods and apparatus for performing machine learning by sampling from a sampling server.

Many machine learning algorithms depend on upon samples from computationally intractable distributions. An example of such an algorithm is gradient descent on the expected negative log-likelihood of a Restricted Boltzmann Machine (RBM). Other algorithms calculate the gradient descent on the expected negative log-likelihood to train deep Boltzmann machines or deep Boltzmann Machines networks. For all the above mentioned algorithms good samples may lead to successful learning.

However, sampling from RBMs and their progeny is #P-hard, and difficult to approximate in polynomial time. Heuristic approximations can be used in place of accurate samples. Algorithms such as contrastive divergence (CD) and persistent contrastive divergence (PCD) make use of heuristic approximations. CD and PCD are based on single Markov chains of single-temperature Gibbs sampling. CD and PCD may be run for a specified number of iterations to obtain samples with the desired accuracy. Other algorithms, such as simulated tempering and parallel tempering (including population annealing) use multiple temperatures. All of the methods may use multiple chains. Annealed importance sampling is another approach to approximation to evaluate expectations from computationally intractable distributions. A description of annealed importance sampling and applications using this method can be found in US Patent Application Publication No 2015-0269124. Annealed importance sampling obtains importance-weighted samples, but may suffer from large computation times on problems for which good proposal distributions are unknown. There is thus a general desire for systems and methods that produce better samples from computationally intractable distributions.

Algorithms such as CD and PCD integrate the sampling operation into the machine learning algorithm, seeding the Markov chains either from the approximation to the posterior distribution over the latent variables given the training data or from the end of the last set of Markov chains. Applicant believe that in all these algorithms, the sampling operation is performed on the same machine as the main machine learning algorithm. In addition, the sampling operation is generally implemented so as not to consume orders of magnitude more processing power than other components of the machine learning algorithm. However, obtaining accurate samples is resource intensive and can take exponentially more time to produce than other computations of the machine learning algorithm (e.g., calculating the gradient of the expected negative log-likelihood).

In response to the difficulty of obtaining accurate samples from computationally intractable distribution, modern generative learning algorithms are based on directed graphical models and use prior distributions for which sampling is computationally tractable by construction. An example of such a generative learning algorithms is variational auto encoders.

Given the difficulty in obtaining accurate samples from computationally intractable distribution, the performance of machine learning algorithms is limited by the computational time and resources needed to produce samples.

The following systems, methods and apparatus describe an approach which may significantly improve the performance of machine learning algorithms, and hence machine learning systems, by detaching the sampling operations from the other computations of the machine learning algorithms.

The distributions from which machine learning algorithms require samples change slowly over the course of the training. As a result, samples from a distribution at iteration n are a good approximation to samples from the distribution at iteration n+1. Therefore, work done on previous iterations can be used to bootstrap sampling from the current iteration. PCD also leverages this phenomenon.

In order to do as much work as possible during iteration n in preparation for iteration n+1, the sampling operation may be offloaded onto a distinct server. A distinct server, or sampling server, may do the sampling work in the background, while the machine learning algorithm performs other operations, for example calculates the gradient descent. The sampling server can devote all its resources to increase the quality of the samples without impacting the running time of the machine learning algorithm. The sampling server may run on a cluster of machines, in which case the sampling work can be parallelized over the number of machines in the cluster of machines.

In one implementation, the sampling server receives a stream of slowly changing parameters (h, j) of a Boltzmann distribution from a machine learning algorithm and returns functions of the samples from the current distribution. An example of functions of the samples are first- and second-order statistics (i.e., average spin and spin-spin correlations). The machine learning algorithm can then maximize the log-likelihood of a generative model based on a Boltzmann machine.

Upon receiving parameters (h, j), the sampling server uses parameter (h, j) to construct an RBM from which to generate samples using Gibbs sampling, parallel tempering, population annealing or other algorithms, with chains seeded from the last call to the sampling server. As long as the parameters (h, j) change slowly between calls to the sampling server, the seed can produce useful samples. A successive call to the sampling server is accompanied by the most recent set of parameters (h', j'), so that the sampling server constructs a new RBM based on the received parameters (h', j') each time it is called.

In addition to the samples and the statistics, the sampling server may return to the machine learning algorithm other metrics. An examples of metrics that can be calculated by the sampling server are: an approximation to the log-partition function, the auto correlation time of the current distribution, other measures of sampling difficulty. These additional metrics may be requested and returned infrequently, e.g., once every 3000 requests for samples.

In the case of a Boltzmann distribution, the distribution may be Chimera-structured, full-bipartite or fully connected. In certain cases, e.g. graph of low tree-width, specialized algorithms may be used.

The sampling server may run on the sample GPU or CPU as the machine learning algorithm, in which case memory is shared between the sampling sever and the machine learning algorithm. In a different implementation, the sampling server may run the same machine as the machine learning algorithm but on a different GPU or CPU.

In alternative, the sampling server may run on a different machine than the machine learning algorithm and be in communication with the machine learning algorithm over a network. In the latter case, the request for samples and the transfer of parameters and samples happens over the network. The sampling server may be spread over a cluster of machines over a network.

If the sampling server is not on the same GPU or CPU as the machine learning algorithm, the sampling server may use the available time between requests for samples to improve the quality of the samples under the current set of parameters. These high quality samples may be used by the sampling server to seed sampling when the machine learning algorithm requests samples with a new, slightly different, set of parameters.

The sampling server may be used with variational auto encoders to produce samples from the Boltzmann machine in its prior. The use of a sampling server would facilitate the use of fully-connected Boltzmann machines, from which it is difficult to samples efficiently using conventional methods, such as TensorFlow, given that the sampling operation can be parallelized over multiple units in the Boltzmann machine. A description of a variational auto encoder can be found in International Patent Application No PCT/US2016/047627.

FIG. **4** shows a method **400** for performing machine learning by drawing samples from a sampling server in accordance with the present systems, devices, articles, and methods. Execution of the method **400** by one or more processor-based devices may occur in accordance with the present system, devices, articles, and methods. Method **400**, like other methods herein, may be implemented by a series or set of processor-readable instructions executed by one or more processors (i.e., hardware circuitry). Method **400** may, for example, be executed on two or more cores of a single processor (e.g., graphics processor unit or GPU), each of the cores separate and distinct from the other processor cores. Method **400** may be executed on two or more cores of two or more processor units, each of the processor units separate and distinct from the other processor units. The method **400** may be executed on two or more cores of two or more processor units, which belong to two or more computers or machines, each computer or machine separate and distinct from the other computers or machines. The computers or machines may, for example, form one or more clusters,

communicatively coupled by a network infrastructure, for instance a packet switch network with various packet switches and/or routers.

Method **400** starts at **402**, for example in response to a call or invocation from another routine.

At **404**, a first digital processor core or set of cores starts or start running a machine learning algorithm by initializing parameters of a distribution to be learned. An example of a distribution is the Boltzmann distribution with parameters (h, j).

Method **400** executes acts **406** and **408** in parallel or concurrently or even simultaneously.

At **406**, the first digital processor core or set of cores that executes or execute the machine learning algorithm uses the parameters of the distribution to run a machine learning algorithm to learn said distribution with samples received from the sampling server. For example, the first digital processor core or set of cores may use the samples to calculate the gradient of the log-likelihood of a generative model based on a Boltzmann machine, with the aim of maximizing the log-likelihood of the generative model.

At **408**, the first digital processor core or set of cores that executes or execute the machine learning algorithm sends a current set of parameters to the sampling server. At the first iteration, the first digital processor core or set of cores sends or send the parameters initialized at **404**. At successive iterations, the first digital processor core or set of cores sends the sampling server a set of parameters from the most recent iteration of the machine learning algorithm running at **406**.

At **410**, a second digital processor core or set of cores that implements or implement the sampling server uses the parameters received at **408** to generate samples to be used in the machine learning algorithm running at **406**. The sampling server can use the received parameters to construct an RBM from which to draw samples. The sampling server may use techniques such as Gibbs sampling, parallel tempering or other algorithms to draw samples.

At **412**, the sampling server provides the samples to the first digital processor core or set of cores that executes or execute the machine learning algorithm. As previously noted, the first digital processor core or set of cores at **406** uses the samples for running the machine learning algorithm. Where the sampling server is implemented on a different machine from the machine learning, the samples are returned over a communications network, for example a packet switched network of packet switches and routers.

At **414**, the first digital processor core or set of cores that executes or execute the machine learning algorithm determines whether more samples are needed. A decision to draw more samples may be based upon the completion of a number of iterations or based on a calculated performance factor. In the latter case, when a performance factor lacks improvement or starts to degrade is an indication to interrupt the sampling operation.

If a decision is made to draw more samples, control passes to **408** and the first digital processor core or set of cores that executes or execute the machine learning algorithm sends an updated set of parameters to the sampling server. Otherwise, control passes to **406** and the first digital processor core or set of cores runs the machine learning algorithm.

At **418**, the first digital processor core or set of cores that executes or execute the machine learning algorithm tests to check whether stopping criterion has been met. A stopping criterion can be, for example, related to the number of iterations or measurement of a performance criterion between successive iterations. A performance criterion may be assessed, for example, via the difference between the output of an iteration of the machine learning algorithm and a training dataset. In the latter case, when a performance criterion starts to degrade or lack improvement between successive iteration is an indication that the machine learning algorithm should stop and control passes to **420**. Otherwise control passes to **406** and the machine learning algorithm keeps running.

At **420**, the first digital processor core or set of cores that executes or execute the machine learning algorithm returns the result of the machine learning algorithm.

At **422**, method **400** terminates, for example until invoked again.

The sampling server may be used in conjunction with a quantum processor where the sampling server works as an interface between a machine learning algorithm and the quantum processor.

FIG. **5**A shows a hybrid system **500***a* comprising a digital processor core **502**, a sampling server computer **504** and a quantum processor **506**.

One or more processor cores **502** run the machine learning algorithm while sampling server computer **504** implemented by a different processor core or set of cores provides the samples as described above with reference to method **400** of FIG. **4**. Sampling server computer **504** may be implemented on the same GPU or CPU as the machine learning algorithm, for instance on a separate core or separate set of cores. Alternatively, the sampling server computer **504** may be implemented on a separate GPU/CPU or separate set of GPUs/CPUs on the same machine or set of machines that executes or execute the machine learning algorithm. Additionally or alternatively, the sampling server computer **504** may be implemented on a separate machine or separate set of machines from a machine or set of machines that executes or execute the machine learning algorithm. The machine(s) that implements or implement the sampling server in communication with the digital processor(s) that execute the machine learning algorithm via one or more networks, for example packet switched networks. Quantum processor **506** may be a superconducting quantum processor and may be constructed with topology **200** of FIG. **2**.

Methods for operating a quantum processor as a sample generator are described in U.S. Pat. No. 9,218,567 and US Patent Publication No US20160042294A1.

Sampling server **504** may request samples from quantum processor **506** and use such samples to reseed persistent Markov chains at the appropriate temperature. When requesting samples from quantum processor **506**, sampling server **504** may perform parameter scaling before sending the parameters to quantum processor **506** to ensure that the distribution sampled by quantum processor **506** corresponds to the desired logical temperature. Sampling server **504** may select chain strengths and perform spin reversal transformation on the chains.

Sampling server **504** may request samples from quantum processor **506** at a slower rate than that at which parameters are received from and samples returned to the machine learning algorithm, or for every set of samples.

Sampling server **504** may ensure that the samples generated by the quantum processor are post-processed as needed before being sent to the machine learning algorithm. Sampling server **504** may use post processing techniques such as MCMC and importance sampling; however other post processing algorithms may also be used. Methods and techniques for post processing the output of a quantum processor can be found in U.S. Pat. Nos. 7,307,275, and 8,244,650.

In addition to reseeding the its Markov chains using the samples from quantum processor **506** that correspond

directly to the desired distribution, sampling server **504** may use the samples provided by quantum processor **506** in a different way. For example, quantum processor **506** may be used to improve the quality of the samples in an indirect way. As an example, quantum processor **506** may be used to discover new valleys in the energy landscape of the distribution, therefore improving the quality of samples to be used by digital processor **502** to run a machine learning algorithm.

Digital processor **502** in hybrid system **500***a* sends a set of parameters (i.e., h, j of a Boltzmann distribution) to sampling server **504** (arrow **508** in FIG. **5**A). Sampling server **504** may generate samples and send them to the digital processor (arrow **510** in FIG. **5**A) or send the parameters (e.g., h, j) to quantum processor **506** (arrow **512** in FIG. **5**A). Quantum processor **506** generates samples and sends them to sampling server **504** (arrow **514** in FIG. **5**A). Upon receiving samples from quantum processor **506**, sampling server **504** uses them samples to reseeds its Markov chains and sends updated samples to digital processor **502** (arrow **510** in FIG. **5**A).

FIG. **5**B shows a hybrid system **500***b* comprising a digital processor **502**, a quantum processor **506** and a sampling server **504** implemented as a cluster of machines **516***a*-**516***d* (collectively **516**) in communicative coupling over a network **518**. Network **518** may be implemented as a bus network, a ring network or other types of network structure. While in FIG. **5**B sampling server **504** is illustrated as implemented as a cluster of four machines **516***a*-**516***d* the number of machine is for illustration purposes only and cluster of machines **516** may have a smaller or larger number of distinct machines.

Digital processor **502** runs the machine learning algorithm while sampling server **504** provides the samples as described above with reference to method **400** of FIG. **4** and hybrid system **500***a*. Quantum processor **506** may be a superconducting quantum processor and may be constructed with topology **200** of FIG. **2**.

Sampling server **504** may request samples from quantum processor **506** and use such samples to reseed persistent Markov chains at the appropriate temperature as described above with reference to hybrid system **5001**.

Sampling server **504** may request samples from quantum processor **506** at a slower rate than a rate at which parameters are received from and samples returned to the machine learning algorithm, or for every set of samples.

Sampling server **504** may ensure that the samples generated by the quantum processor are post-processed as needed before being sent to the machine learning algorithm. In some implementations, the sampling server **504** employs the post-processed samples generated by the quantum processor to improve the generation of samples by the sampling server **504**.

In addition to reseeding the its Markov chains using the samples from quantum processor **506** that correspond directly to the desired distribution, sampling server **504** may use the samples provided by quantum processor **506** in a different way. For example, quantum processor **506** may be used to improve the quality of the samples in an indirect way as described above with reference to hybrid system **500***a*.

Digital processor **502** in hybrid system **500***b* sends a set of parameters (i.e., h, j of a Boltzmann distribution) to sampling server **504** (arrow **508** in FIG. **5**B). Sampling server **504** may generate samples and send them to the digital processor (arrow **510** in FIG. **5**B) or send the parameters (e.g., h, j) to quantum processor **506** (arrow **512** in FIG. **5**B). Quantum processor **506** generates samples and sends them to sampling server **504** (arrow **514** in FIG. **5**B). Upon receiving samples from quantum processor **506**, sampling server **504** uses them samples to reseeds its Markov chains and sends updated samples to digital processor **502** (arrow **510** in FIG. **5**B).

FIG. **6** shows a method **600** for performing machine learning by drawing samples from a sampling server and a quantum processor. Method **600** may be implemented using hybrid system **500***a* or **500***b*. Execution of the method **600** by one or more processor-based devices may occur in accordance with the present system, devices, articles, and methods. Method **600**, like other methods herein, may be implemented by a series or set of processor-readable instructions executed by one or more processors (i.e., hardware circuitry). Method **600** may, for example, be executed on two or more cores of a single processor (e.g., graphics processor unit or GPU), each of the cores separate and distinct from the other processor cores. Method **600** may be executed on two or more cores of two or more processor units, each of the processor units separate and distinct from the other processor units. The method **600** may be executed on two or more cores of two or more processor units, which belong to two or more computers or machines, each computer or machine separate and distinct from the other computers or machines. The computers or machines may, for example, form one or more clusters, communicatively coupled by a network infrastructure, for instance a packet switch network with various packet switches and/or routers.

Method **600** starts at **602**, for example in response to a call from another routine.

At **604**, a first digital processor core or set of cores starts running a machine learning algorithm by initializing parameters of a distribution to be learned, as described with reference to **404** of method **400**.

Method **600** executes acts **606** and **608** in parallel or concurrently or even simultaneously.

At **606**, the first digital processor core or set of cores that executes or execute the machine learning algorithm uses the parameters of the distribution to run a machine learning algorithm to learn said distribution with samples received from the sampling server, as describe with reference to **406** of method **400**.

At **608**, the first digital processor core or set of cores that executes or execute the machine learning algorithm sends the current set of parameters to the sampling server, as described above with reference to **408** of method **400**.

At **610**, a second digital processor core or set of cores that implement the sampling server uses the parameters received at **608** to generate samples to be used in the machine learning algorithm running at **606**, as described with reference to **410** of method **400**.

At **611**, the sampling server determines whether to request samples from the quantum processor. The sampling server may determine whether to request samples from the quantum processor based on a number of factors, including availability or scheduling ability of the quantum processor, recent requests for sample to the quantum processor or other factors. If the sampling server determines not to request samples from the quantum processor control passes to **612**, otherwise to **613**.

At **612**, the sampling server returns the samples to the first digital processor core or set of cores that executes or execute the machine learning algorithm, as described with reference to **412** of method **400**.

At **614**, the first digital processor core or set of cores that executes or execute the machine learning algorithm determines or determine whether more samples are needed, as

described with reference to **414** of method **400**. If the first digital processor core or set of cores determines or determine that more samples are needed, control passes to **608**, otherwise to **606**.

At **613**, the sampling server sends the most recent set of parameters to the quantum processor. The most recent set of parameters are the parameters last received from the digital processor. The sampling server may perform parameter scaling as described above before sending the parameters to the quantum processor.

At **615**, the quantum processor uses the received set of parameters to construct a distribution corresponding to the parameters and draw samples from said distribution.

At **616**, the quantum processor sends the samples to the sampling server. The transmission of the samples may happen over a network.

At **617**, the sampling server may perform post-processing on the received samples from the quantum processor before using the samples to reseed it Markov chains, thus producing updated samples based on the results from the quantum processor. Control then passes to **611**.

At **618**, method **600** tests to check whether stopping criterion has been met, as described with reference to **428** of method **400**.

At **620**, the first digital processor or set of cores that executes or execute the machine learning algorithm returns or return the result of the machine learning algorithm.

At **622**, method **600** terminates until invoked again. Alternatively, the method **600** may automatically repeat.

The above described method(s), process(es), or technique (s) could be implemented by a series of processor readable instructions stored on one or more nontransitory processor-readable media. Some examples of the above described method(s), process(es), or technique(s) method are performed in part by a specialized device such as an adiabatic quantum computer or a quantum annealer or a system to program or otherwise control operation of an adiabatic quantum computer or a quantum annealer, for instance a computer that includes at least one digital processor. The above described method(s), process(es), or technique(s) may include various acts, though those of skill in the art will appreciate that in alternative examples certain acts may be omitted and/or additional acts may be added. Those of skill in the art will appreciate that the illustrated order of the acts is shown for exemplary purposes only and may change in alternative examples. Some of the exemplary acts or operations of the above described method(s), process(es), or technique(s) are performed iteratively. Some acts of the above described method(s), process(es), or technique(s) can be performed during each iteration, after a plurality of iterations, or at the end of all the iterations.

The above description of illustrated implementations, including what is described in the Abstract, is not intended to be exhaustive or to limit the implementations to the precise forms disclosed. Although specific implementations of and examples are described herein for illustrative purposes, various equivalent modifications can be made without departing from the spirit and scope of the disclosure, as will be recognized by those skilled in the relevant art. The teachings provided herein of the various implementations can be applied to other methods of quantum computation, not necessarily the exemplary methods for quantum computation generally described above.

The various implementations described above can be combined to provide further implementations. To the extent that they are not inconsistent with the specific teachings and definitions herein, all of the US patent application publications, US patent applications, US patents, International patent applications, foreign patents, and foreign patent applications referred to in this specification and/or listed in the Application Data Sheet that are commonly owned by D-Wave Systems Inc. are incorporated herein by reference, in their entirety, including but not limited to: U.S. Pat. Nos. 7,898,282; 7,800,395; 8,670,807; U.S. patent application Ser. No. 14/676,605; International Patent Application No. PCT/US2016/047627; U.S. Pat. No. 9,218,567; US Patent Publication No. US20160042294A1; and U.S. provisional patent application Ser. No. 62/399,764, file Sep. 26, 2016 and entitled "Systems and Methods for Degeneracy Mitigation in a Quantum Processor" and U.S. provisional patent application Ser. No. 62/399,683, file Sep. 26, 2016 and entitled "Systems, Methods and Apparatus for Sampling from a Sampling Server".

These and other changes can be made to the implementations in light of the above-detailed description. In general, in the following claims, the terms used should not be construed to limit the claims to the specific implementations disclosed in the specification and the claims, but should be construed to include all possible implementations along with the full scope of equivalents to which such claims are entitled. Accordingly, the claims are not limited by the disclosure.

The invention claimed is:

1. A computational system for use in machine learning, the computational system comprising:

at least one digital processor core; and

at least one nontransitory processor-readable medium communicatively coupleable to the at least one digital processor core and that stores at least one of processor-executable instructions or data which, when executed by the at least one digital processor core, causes the at least one digital processor core to implement a sampling server that:

receives an initial set of parameters for an iteration of a machine learning process that is executing in parallel with the sampling server on a separate at least one digital processor core from the at least one digital processor core on which the sampling server is implemented;

generates a first set of samples based on the initial set of parameters temporarily in parallel with execution of the machine learning process; and

provide the first set of samples generated by sampling server as implemented by the at least one digital processor core for use in a further iteration of the machine learning process,

wherein the at least one digital processor core on which the sampling server is implemented is further communicatively coupleable to at least one quantum processor, and execution of the processor-executable instructions or data cause the at least one digital processor core on which the sampling server is implemented further to:

provide a current set of parameters from the sampling server to the at least one quantum processor; and

receive a set of quantum processor generated samples from the at least one quantum processor, wherein the quantum processor draws samples from a distribution based at least in part on the current set of parameters provided by the sampling server.

2. The computational system of claim **1** wherein execution of the processor-executable instructions or data cause the at least one digital processor core to provide a first set of functions along with the first set of samples generated by sampling server, wherein the first set of functions include are

first- and second-order statistics; and causes the sampling server to send samples, functions of samples and an approximation to a log partition function to the at least one separate digital processor core on which the machine learning process executes.

3. The computational system of claim **1** wherein execution of the processor-executable instructions or data cause the at least one digital processor core to draw samples via at least one of Markov Chain of single temperature Gibbs sampling, simulated tempering, parallel tempering, population annealing, annealed importance sampling, and from a Boltzmann distribution.

4. The computational system of claim **1** wherein the machine learning process maximizes a log-likelihood of a generative model.

5. The computational system of claim **1** wherein execution of the processor-executable instructions or data cause the at least one digital processor core on which the sampling server is implemented further to:

perform post processing on the samples received from the quantum processor.

6. The computational system of claim **1** wherein the quantum processor performs chain embedding before drawing samples.

7. The computational system of claim **1** wherein the at least one digital processor core on which the sampling server is implemented is a first processor core of a graphical processor unit with a memory space, the separate at least one digital processor core that executes the machine learning process is a second processor core of the graphical processor unit and shares the memory space with the first processor core of the graphical processor unit.

8. The computational system of claim **1** wherein the at least one digital processor core on which the sampling server is implemented is a processor core of a first graphical processor unit and the separate at least one digital processor core that executes the machine learning process is a processor core of a second graphical processor unit, the second graphical processor unit separate and distinct from the first graphical processor unit.

9. The computational system of claim **8** wherein the at least one digital processor core on which the sampling server is implemented includes a plurality of digital processor cores of a plurality of processors that are separate and distinct from one another, and the plurality of processors are components of a plurality of computers, the computers which from a cluster of machines communicatively coupled via a network infrastructure.

10. The computational system of claim **1** wherein execution of the processor-executable instructions or data cause the at least one digital processor core further to:

iteratively receive additional sets of parameters for each of a number of iterations of the machine learning process that is executing in parallel with the sampling server on the separate at least one digital processor core from the at least one digital processor core on which the sampling server is implemented;

iteratively generate an additional set of samples based on respective ones of the additional sets of parameters temporarily in parallel with execution of the machine learning process; and

iteratively provide the additional sets of samples generated by sampling server as implemented by the at least one digital processor core for use in the iterations of the machine learning process.

11. The computational system of claim **1** wherein the sampling server executes concurrently with the machine learning process, overlapping at least a portion thereof.

12. A method of operation of a computational system for use in machine learning, the method comprising:

receiving, by at least one digital processor core that implements a sampling server, an initial set of parameters for an iteration of a machine learning process that is executing in parallel with the sampling server on a separate at least one digital processor core from the at least one digital processor core on which the sampling server is implemented;

generating, by at least one digital processor core that implements a sampling server, a first set of samples based on the initial set of parameters temporarily in parallel with execution of the machine learning process;

providing, by at least one digital processor core that implements a sampling server, the first set of samples generated by sampling server as implemented by the at least one digital processor core for use in a further iteration of the machine learning process;

providing a current set of parameters from the sampling server to at least one quantum processor; and

receiving, by the sampling server, a second set of quantum processor generated samples from the at least one quantum processor based at least in part on the current set of parameters provided by the sampling server.

13. The method of claim **12**, further comprising:

providing, by at least one digital processor core that implements a sampling server, a first set of functions along with the first set of samples generated by sampling server, wherein the first set of functions include are first- and second-order statistics; and

sending functions of samples and an approximation to a log partition function by the sampling server to the at least one separate digital processor core on which the machine learning process executes.

14. The method of claim **12**, further comprising:

drawing samples via at least one of Markov Chain of single temperature Gibbs sampling, simulated tempering, parallel tempering, population annealing, annealed importance sampling, and from a Boltzmann distribution by the separate at least one digital processor core that executes the machine learning process.

15. The method of claim **12**, further comprising:

performing post processing, by the sampling server, on the second set of samples before updating the current set of samples to produce a third set of samples based at least in part on the second set of samples.

16. The method of claim **12**, further comprising:

performing a chain embedding, by the quantum processor, before drawing samples by the quantum processor.

17. The method of claim **12**, further comprising:

iteratively receiving additional sets of parameters for each of a number of iterations of the machine learning process that is executing in parallel with the sampling server on the separate at least one digital processor core from the at least one digital processor core on which the sampling server is implemented;

iteratively generating an additional sets of samples based on respective ones of the additional sets of parameters temporarily in parallel with execution of the machine learning process; and

iteratively providing the additional sets of samples generated by sampling server as implemented by the at

least one digital processor core for use in the iterations of the machine learning process.

18. The method of claim **12** wherein the sampling server executes concurrently with the machine learning process, overlapping at least a portion thereof.

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